

**Please note that Cypress is an Infineon Technologies Company.**

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

**Continuity of document content**

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

**Continuity of ordering part numbers**

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

# 4-Mbit (256K words × 16 bit) Static RAM

## Features

- High speed
  - $t_{AA}/t_{ACE} = 9 \text{ ns}^{[1]}$
- Low active and standby currents
  - Active current:  $I_{CC} = 38\text{-mA}$  typical
  - Standby current:  $I_{SB2} = 6\text{-mA}$  typical
- Operating voltage range: 2.2 V to 3.6 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Pb-free 48-ball VFBGA package

## Functional Description

CG9108AT is high-performance CMOS fast static RAM, organized as 256K words by 16-bits.

Data writes are performed by asserting the Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW, while providing the data on I/O<sub>0</sub>

through I/O<sub>15</sub> and address on A<sub>0</sub> through A<sub>17</sub> pins. The Byte High Enable ( $\overline{BHE}$ ) and Byte Low Enable ( $\overline{BLE}$ ) inputs control write operations to the upper and lower bytes of the specified memory location.  $\overline{BHE}$  controls I/O<sub>8</sub> through I/O<sub>15</sub> and  $\overline{BLE}$  controls I/O<sub>0</sub> through I/O<sub>7</sub>.

Data reads are performed by asserting the Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) inputs LOW and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O<sub>0</sub> through I/O<sub>15</sub>). Byte accesses can be performed by asserting the required byte enable signal ( $\overline{BHE}$  or  $\overline{BLE}$ ) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state during the following events:

- The device is deselected ( $\overline{CE}$  HIGH)
- The control signals ( $\overline{OE}$ ,  $\overline{BLE}$ ,  $\overline{BHE}$ ) are de-asserted

The logic block diagram is on page 2.

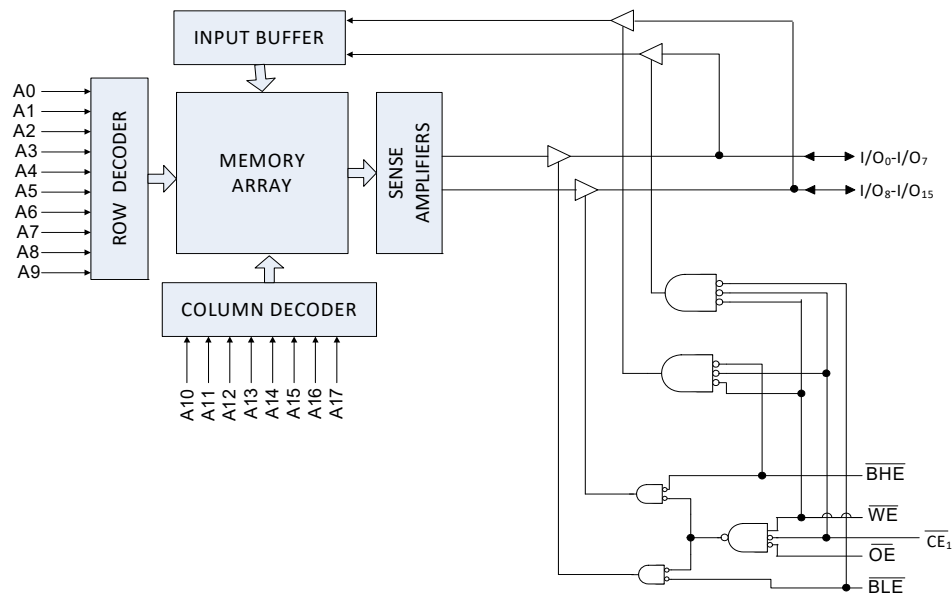
## Product Portfolio

Product	Range	V <sub>CC</sub> Range (V)	Speed (ns)  10	Power Dissipation			
				Operating I <sub>CC</sub> , (mA)		Standby, I <sub>SB2</sub> (mA)	
				f = f <sub>max</sub>			
				Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max
CG9108AT	Industrial	2.2 V–3.6 V	10	38	45	6	8

### Notes

1. These parameters are guaranteed by Test only.
2. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 3 V (for a V<sub>CC</sub> range of 2.2 V–3.6 V) T<sub>A</sub> = 25 °C.

## Logic Block Diagram – CG9108AT

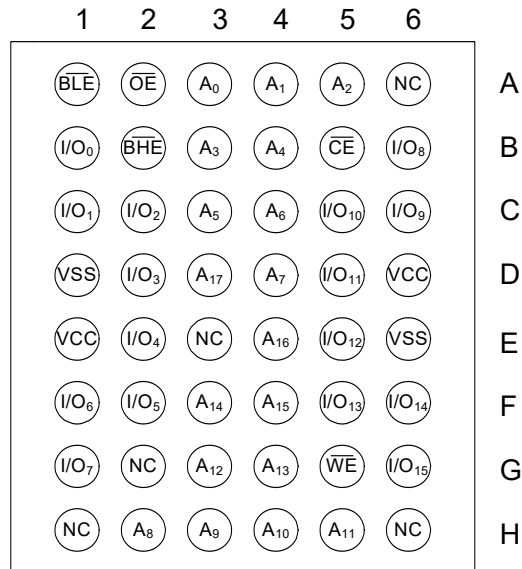


## Contents

<b>Pin Configurations .....</b>	<b>4</b>	<b>Package Diagrams.....</b>	<b>14</b>
<b>Maximum Ratings.....</b>	<b>5</b>	<b>Acronyms .....</b>	<b>15</b>
<b>Operating Range.....</b>	<b>5</b>	<b>Document Conventions .....</b>	<b>15</b>
<b>DC Electrical Characteristics .....</b>	<b>5</b>	Units of Measure .....	15
<b>Capacitance .....</b>	<b>6</b>	<b>Document History Page .....</b>	<b>16</b>
<b>Thermal Resistance.....</b>	<b>6</b>	<b>Sales, Solutions, and Legal Information .....</b>	<b>17</b>
<b>AC Test Loads and Waveforms.....</b>	<b>6</b>	Worldwide Sales and Design Support.....	17
<b>Data Retention Characteristics .....</b>	<b>7</b>	Products .....	17
<b>Data Retention Waveform .....</b>	<b>7</b>	PSoC® Solutions .....	17
<b>AC Switching Characteristics .....</b>	<b>8</b>	Cypress Developer Community.....	17
<b>Switching Waveforms .....</b>	<b>9</b>	Technical Support .....	17
<b>Truth Table .....</b>	<b>12</b>		
<b>Ordering Information.....</b>	<b>13</b>		
Ordering Code Definitions .....	13		

## Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout, Package/Grade ID: BVXI<sup>[3]</sup>



### Note

3. NC pins are not connected internally to the die.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature  
with power applied ..... –55 °C to +125 °C

Supply voltage  
on  $V_{CC}$  relative to GND<sup>[4]</sup> ..... –0.5 V to  $V_{CC} + 0.5$  V

DC voltage applied to outputs  
in HI-Z State<sup>[4]</sup> ..... –0.5 V to  $V_{CC} + 0.5$  V

DC input voltage<sup>[4]</sup> ..... –0.5 V to  $V_{CC} + 0.5$  V

Current into outputs (in LOW state) ..... 20 mA

Static discharge voltage  
(MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 140 mA

## Operating Range

Grade	Ambient Temperature	$V_{CC}$
Industrial	–40 °C to +85 °C	2.2 V to 3.6 V

## DC Electrical Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description	Test Conditions	10 ns			Unit
			Min	Typ <sup>[5]</sup>	Max	
$V_{OH}$	Output HIGH voltage	2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OH} = -1.0$ mA	2	–	–	V
		2.7 V to 3.0 V $V_{CC} = \text{Min}, I_{OH} = -4.0$ mA	2.2	–	–	
		3.0 V to 3.6 V $V_{CC} = \text{Min}, I_{OH} = -4.0$ mA	2.4	–	–	
$V_{OL}$	Output LOW voltage	2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OL} = 2$ mA	–	–	0.4	V
		2.7 V to 3.6 V $V_{CC} = \text{Min}, I_{OL} = 8$ mA	–	–	0.4	
$V_{IH}$	Input HIGH voltage	2.2 V to 2.7 V –	2	–	$V_{CC} + 0.3^{[4]}$	V
		2.7 V to 3.6 V –	2	–	$V_{CC} + 0.3^{[4]}$	
$V_{IL}$	Input LOW voltage	2.2 V to 2.7 V –	–0.3 <sup>[4]</sup>	–	0.6	V
		2.7 V to 3.6 V –	–0.3 <sup>[4]</sup>	–	0.8	
$I_{IX}$	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$	–1	–	+1	μA
$I_{OZ}$	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$ , Output disabled	–1	–	+1	μA
$I_{CC}$	Operating supply current	Max $V_{CC}$ , $I_{OUT} = 0$ mA, CMOS levels f = 100 MHz	–	38	45	mA
		f = 66.7 MHz	–	–	40	
$I_{SB1}$	Automatic CE power-down current – TTL inputs	Max $V_{CC}$ , $\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , f = f <sub>MAX</sub>	–	–	15	mA
$I_{SB2}$	Automatic CE power-down current – CMOS inputs	Max $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0	–	6	8	mA

### Notes

4.  $V_{IL(\text{min})} = -2.0$  V and  $V_{IH(\text{max})} = V_{CC} + 2$  V for pulse durations of less than 20 ns.

5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 3$  V (for  $V_{CC}$  range of 2.2 V–3.6 V)  $T_A = 25$  °C.

## Capacitance

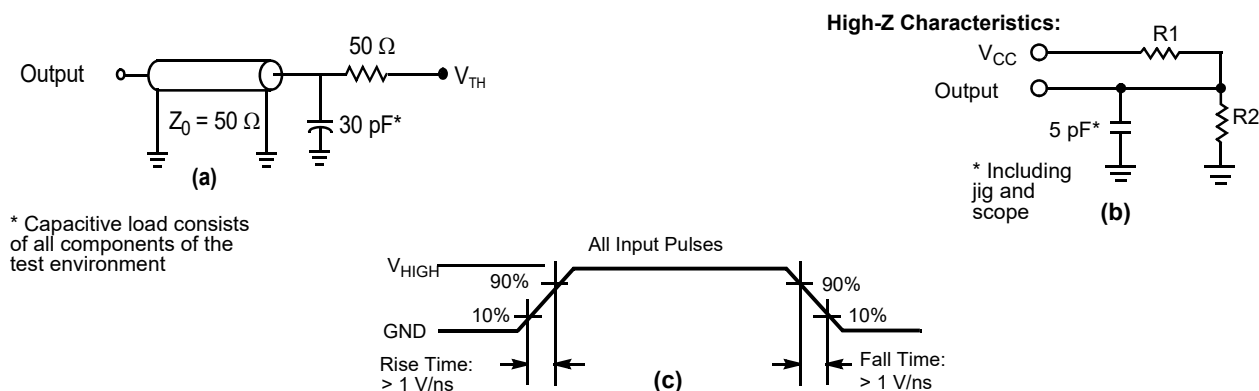
Parameter <sup>[6]</sup>	Description	Test Conditions	48-ball VFBGA	Unit
$C_{IN}$	Input capacitance	$T_A = 25\text{ }^{\circ}\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = V_{CC(typ)}$	10	pF
$C_{OUT}$	I/O capacitance		10	pF

## Thermal Resistance

Parameter <sup>[6]</sup>	Description	Test Conditions	48-ball VFBGA	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still air, soldered on a $3 \times 4.5$ inch, four-layer printed circuit board	31.35	$^{\circ}\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		14.74	$^{\circ}\text{C/W}$

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms<sup>[7]</sup>



Parameters	3.0 V	Unit
R1	317	$\Omega$
R2	351	$\Omega$
$V_{TH}$	1.5	V
$V_{HIGH}$	3	V

### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Full-device AC operation assumes a  $100\text{-}\mu\text{s}$  ramp time from 0 to  $V_{CC(min)}$  and a  $100\text{-}\mu\text{s}$  wait time after  $V_{CC}$  stabilization.

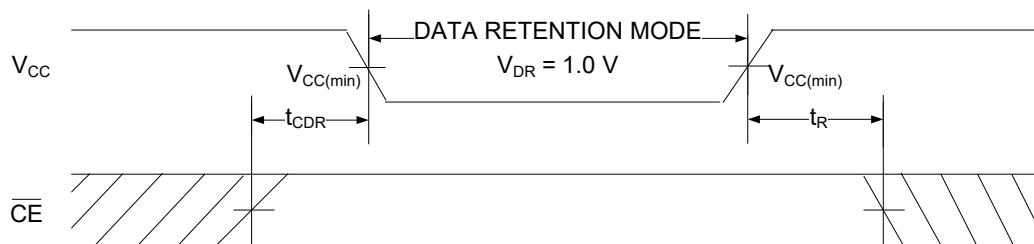
## Data Retention Characteristics

Over the operating range of  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = 1.2\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.2\text{ V}^{[8]}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ , or $V_{IN} \leq 0.2\text{ V}$	–	8	mA
$t_{CDR}^{[9]}$	Chip deselect to data retention time		0	–	ns
$t_R^{[8, 9]}$	Operation recovery time	$V_{CC} \geq 2.2\text{ V}$	10	–	ns

## Data Retention Waveform

**Figure 3. Data Retention Waveform<sup>[8]</sup>**



### Notes

8. Full-device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ .
9. These parameters are guaranteed by design.



## AC Switching Characteristics

Over the operating range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

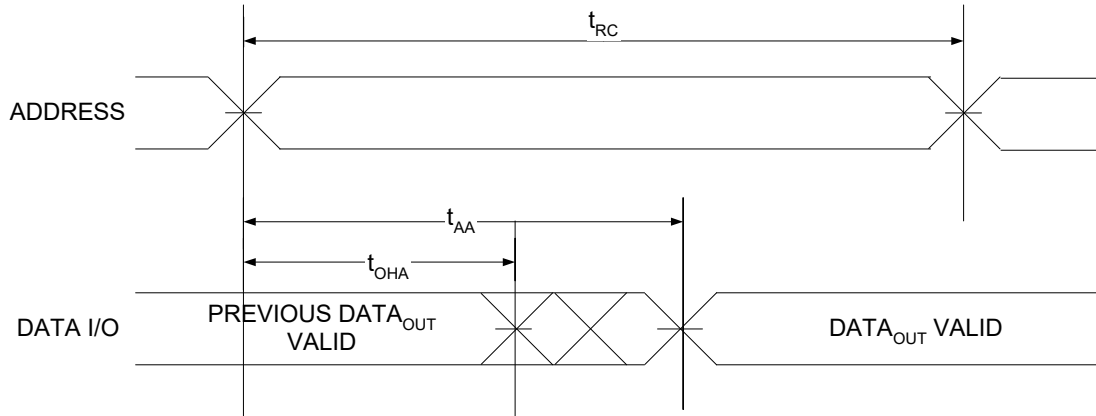
Parameter <sup>[10]</sup>	Description	10 ns		Unit
		Min	Max	
Read Cycle				
t <sub>RC</sub>	Read cycle time	10	–	ns
t <sub>AA</sub> <sup>[11]</sup>	Address to data	–	9	ns
t <sub>OHA</sub>	Data hold from address change	3	–	ns
t <sub>ACE</sub> <sup>[11]</sup>	$\overline{CE}$ LOW to data <sup>[12]</sup>	–	9	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to data	–	4.5	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to low impedance <sup>[13, 14]</sup>	0	–	ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to HI-Z <sup>[13, 14]</sup>	–	5	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to low impedance <sup>[12, 13, 14]</sup>	3	–	ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to HI-Z <sup>[12, 13, 14]</sup>	–	5	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to power-up <sup>[12, 14, 15]</sup>	0	–	ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to power-down <sup>[12, 14, 15]</sup>	–	10	ns
t <sub>DBE</sub>	Byte enable to data valid	–	4.5	ns
t <sub>LZBE</sub>	Byte enable to low impedance <sup>[14]</sup>	0	–	ns
t <sub>HZBE</sub>	Byte disable to HI-Z <sup>[14]</sup>	–	6	ns
Write Cycle <sup>[15, 16]</sup>				
t <sub>WC</sub>	Write cycle time	10	–	ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to write end <sup>[12]</sup>	7	–	ns
t <sub>AW</sub>	Address setup to write end	7	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	ns
t <sub>SA</sub>	Address setup to write start	0	–	ns
t <sub>PWE</sub>	$\overline{WE}$ pulse width	7	–	ns
t <sub>SD</sub>	Data setup to write end	5	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to low impedance <sup>[13, 14]</sup>	3	–	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to HI-Z <sup>[13, 14]</sup>	–	5	ns
t <sub>BW</sub>	Byte Enable to write end	7	–	ns

### Notes

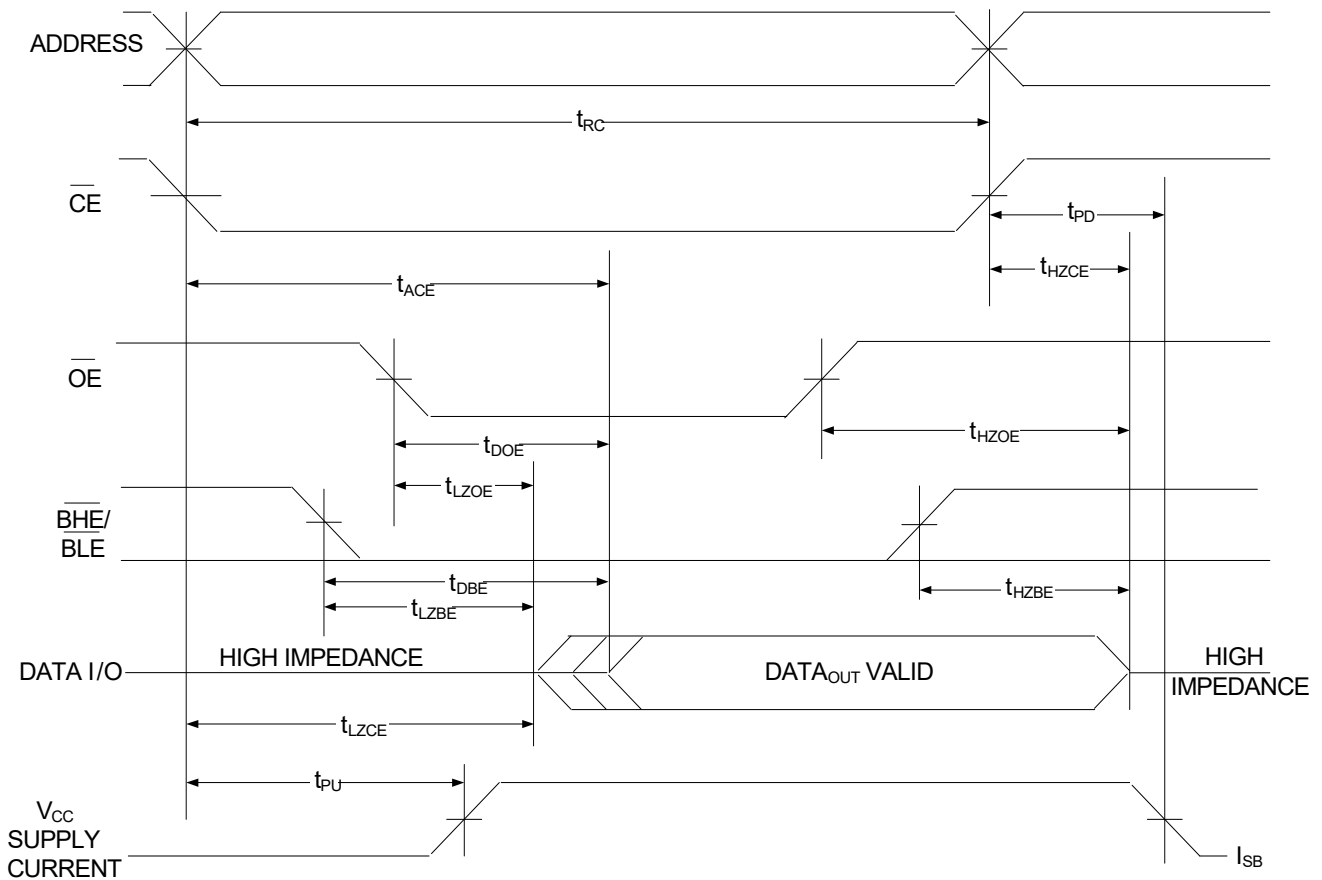
- Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for  $V_{CC} \geq 3\text{ V}$ ) and  $V_{CC}/2$  (for  $V_{CC} < 3\text{ V}$ ), and input pulse levels of 0 to 3 V (for  $V_{CC} \geq 3\text{ V}$ ) and 0 to  $V_{CC}$  (for  $V_{CC} < 3\text{ V}$ ). Test conditions for the read cycle use output loading, as shown in part (a) of Figure 2 on page 6, unless specified otherwise.
- These parameters are guaranteed by Test only.
- For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ ,  $t_{LZOE}$ ,  $t_{LZCE}$ ,  $t_{LZWE}$ , and  $t_{LZBE}$  are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 2 on page 6. Transition is measured  $\pm 200\text{ mV}$  from steady state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ , and  $\overline{BHE}$  or  $\overline{BLE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- The minimum write cycle pulse width in Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be equal to sum of  $t_{SD}$  and  $t_{HZWE}$ .

## Switching Waveforms

**Figure 4. Read Cycle No. 1 (Address Transition Controlled)**<sup>[17, 18]</sup>



**Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled)**<sup>[18, 19]</sup>

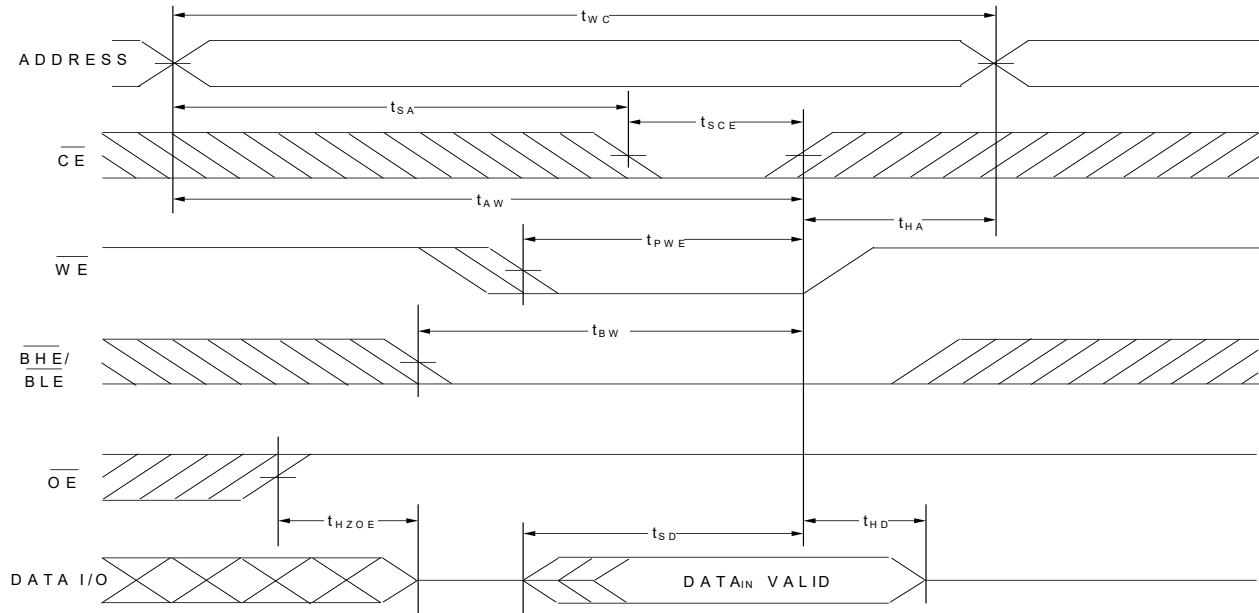
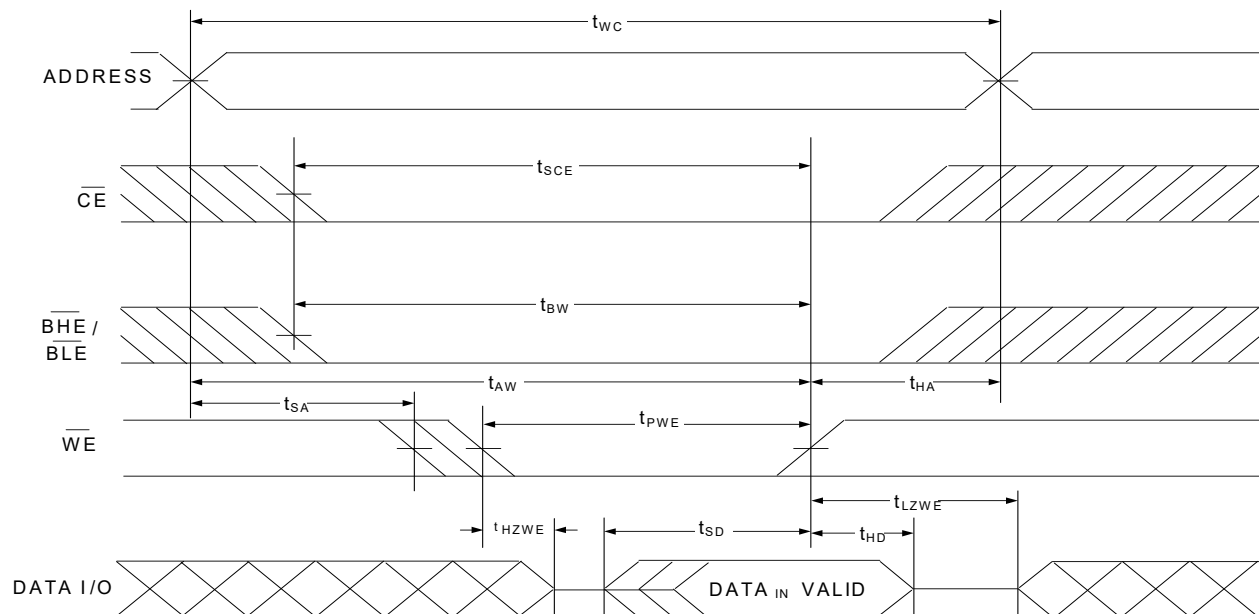


### Notes

17. The device is continuously selected,  $\overline{OE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$  or both =  $V_{IL}$ .

18.  $\overline{WE}$  is HIGH for the read cycle.

19. Address valid prior to or coincident with  $\overline{CE}$  LOW transition.

**Switching Waveforms (continued)**
**Figure 6. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[20, 21]</sup>**

**Figure 7. Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[20, 21, 22]</sup>**

**Notes**

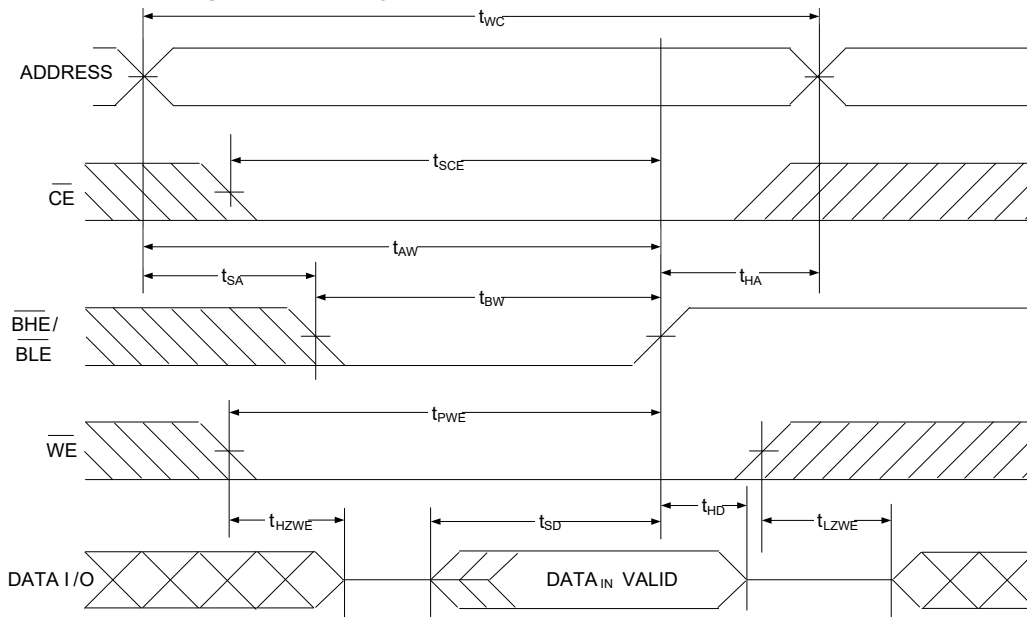
20. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{IL}$ ,  $\overline{\text{CE}} = V_{IL}$ , and  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

21. Data I/O is in HI-Z state if  $\overline{\text{CE}} = V_{IH}$ , or  $\overline{\text{OE}} = V_{IH}$ , or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{IH}$ .

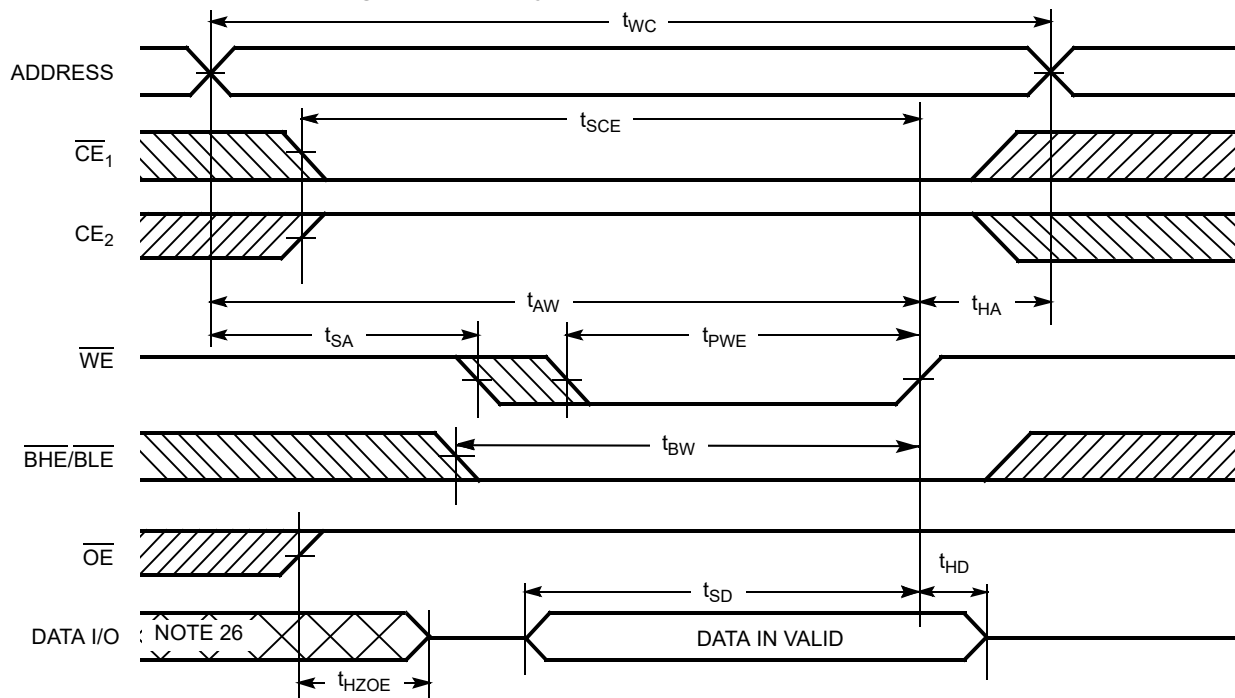
22. The minimum write cycle pulse width should be equal to sum of  $t_{SD}$  and  $t_{HZWE}$ .

## Switching Waveforms (continued)

**Figure 8. Write Cycle No. 3 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**<sup>[23, 24]</sup>



**Figure 9. Write Cycle No. 4 ( $\overline{\text{WE}}$  Controlled)**<sup>[23, 24, 25]</sup>



### Notes

23. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{IL}$ ,  $\overline{\text{CE}} = V_{IL}$ , and  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

24. Data I/O is in HI-Z state if  $\overline{\text{CE}} = V_{IH}$ , or  $\overline{\text{OE}} = V_{IH}$ , or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{IH}$ .

25. Data I/O is high impedance if  $\overline{\text{OE}} = V_{IH}$ .

26. During this period the I/Os are in output state. Do not apply input signals.

## Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
H	X <sup>[27]</sup>	X <sup>[27]</sup>	X <sup>[27]</sup>	X <sup>[27]</sup>	HI-Z	HI-Z	Power down	Standby (I <sub>SB</sub> )
L	L	H	L	L	Data out	Data out	Read all bits	Active (I <sub>CC</sub> )
L	L	H	L	H	Data out	HI-Z	Read lower bits only	Active (I <sub>CC</sub> )
L	L	H	H	L	HI-Z	Data out	Read upper bits only	Active (I <sub>CC</sub> )
L	X	L	L	L	Data in	Data in	Write all bits	Active (I <sub>CC</sub> )
L	X	L	L	H	Data in	HI-Z	Write lower bits only	Active (I <sub>CC</sub> )
L	X	L	H	L	HI-Z	Data in	Write upper bits only	Active (I <sub>CC</sub> )
L	H	H	X	X	HI-Z	HI-Z	Selected, outputs disabled	Active (I <sub>CC</sub> )

### Note

27. The input voltage levels on these pins should be either at V<sub>IH</sub> or V<sub>IL</sub>.

## Ordering Information

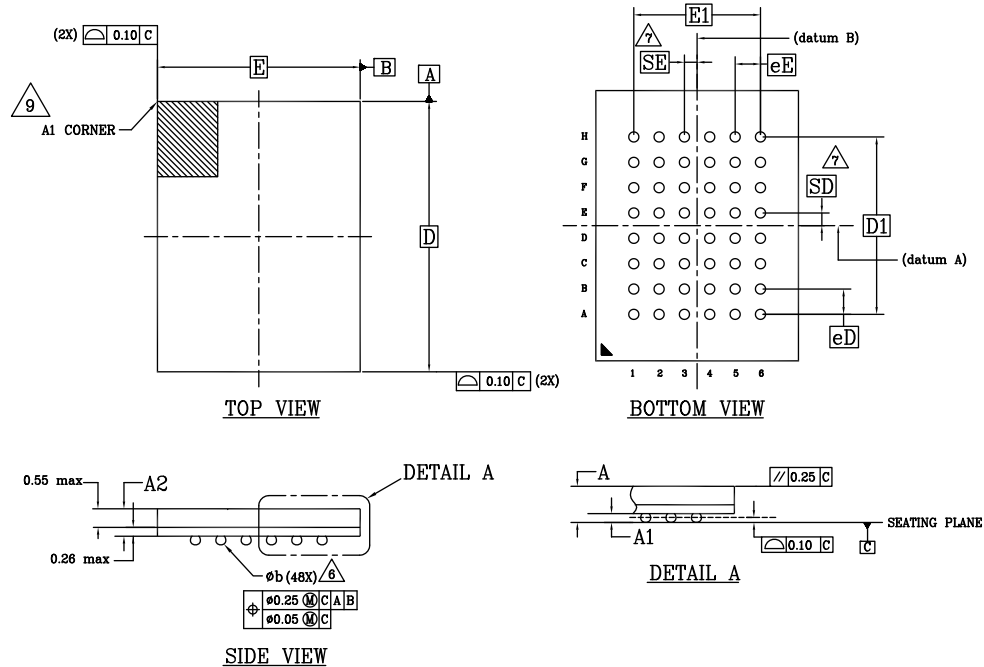
Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Operating Range
10	2.2 V–3.6 V	CG9108AT	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm)	Industrial

## Ordering Code Definitions

Code	Definition
CG	Customer generic
9108AT	Async SRAM

## Package Diagram

Figure 10. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1,00
A1	0,16	-	-
A2	-	-	0,81
D	8,00 BSC		
E	6,00 BSC		
D1	5,25 BSC		
E1	3,75 BSC		
MD	8		
ME	6		
n	48		
Ø b	0,25	0,30	0,35
eE	0,75 BSC		
eD	0,75 BSC		
SD	0,375 BSC		
SE	0,375 BSC		

### NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14,5M-2009.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
- SE REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.  
n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.  
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW  
"SD" OR "SE" = 0.  
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW,  
"SD" = eD/2 AND "SE" = eE/2.
- \*" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.

51-85150 \*I

## Acronyms

Acronym	Description
$\overline{\text{BHE}}$	byte high enable
$\overline{\text{BLE}}$	byte low enable
$\overline{\text{CE}}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{\text{OE}}$	output enable
SRAM	static random-access memory
TSOP	thin small outline package
TTL	transistor-transistor logic
VFBGA	very fine-pitch ball grid array
$\overline{\text{WE}}$	write enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	Degrees Celsius
MHz	megahertz
μA	microamperes
μs	microseconds
mA	milliamperes
mm	millimeters
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts



## Document History Page

Document Title: CG9108AT, 4-Mbit (256K words × 16 bit) Static RAM  
Document Number: 002-27969

Rev.	ECN No.	Submission Date	Description of Change
**	6631437	07/25/2019	New datasheet.
*A	6958213	09/01/2020	Changed datasheet status to Final.

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

### Products

Arm® Cortex® Microcontrollers	<a href="http://cypress.com/arm">cypress.com/arm</a>
Automotive	<a href="http://cypress.com/automotive">cypress.com/automotive</a>
Clocks & Buffers	<a href="http://cypress.com/clocks">cypress.com/clocks</a>
Interface	<a href="http://cypress.com/interface">cypress.com/interface</a>
Internet of Things	<a href="http://cypress.com/iot">cypress.com/iot</a>
Memory	<a href="http://cypress.com/memory">cypress.com/memory</a>
Microcontrollers	<a href="http://cypress.com/mcu">cypress.com/mcu</a>
PSoC	<a href="http://cypress.com/psoc">cypress.com/psoc</a>
Power Management ICs	<a href="http://cypress.com/pmic">cypress.com/pmic</a>
Touch Sensing	<a href="http://cypress.com/touch">cypress.com/touch</a>
USB Controllers	<a href="http://cypress.com/usb">cypress.com/usb</a>
Wireless Connectivity	<a href="http://cypress.com/wireless">cypress.com/wireless</a>

### PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

### Cypress Developer Community

[Community](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

### Technical Support

[cypress.com/support](http://cypress.com/support)

© Cypress Semiconductor Corporation, 2019-2020. This document is the property of Cypress Semiconductor Corporation and its subsidiaries ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, its directors, officers, employees, agents, affiliates, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit [cypress.com](http://cypress.com). Other names and brands may be claimed as property of their respective owners.