CG7772AA (CY7C1470BV33-167AXI with NiPdAu Lead Finish)

72-Mbit (2M × 36) Pipelined SRAM with NoBL™ Architecture

Features

- Pin-compatible and functionally equivalent to ZBT™
- Supports 167 MHz bus operations with zero wait states
- Internally self timed output buffer control to eliminate the need to use asynchronous $\overline{OE}$
- Fully registered (inputs and outputs) for pipelined operation
- Byte Write capability
- Single 3.3 V power supply
- 3.3 V/2.5 V I/O power supply
- Fast clock-to-output time
  - 3.4 ns (for 167 MHz device)
- Clock Enable ($\overline{CEN}$) pin to suspend operation
- Synchronous self timed writes
- CG7772AA available in JEDEC-standard Pb-free 100-pin TQFP
- Burst capability – linear or interleaved burst order
- "ZZ" Sleep Mode option and Stop Clock option

Functional Description

The CG7772AA is 3.3 V, 2M × 36 Synchronous pipelined burst SRAMs with No Bus Latency™ (NoBL™) logic, respectively. They are designed to support unlimited true back-to-back read or write operations with no wait states. The CG7772AA is equipped with the advanced (NoBL) logic required to enable consecutive read or write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data in systems that require frequent read or write transitions.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable ($\overline{CEN}$) signal, which when deasserted suspends operation and extends the previous clock cycle.

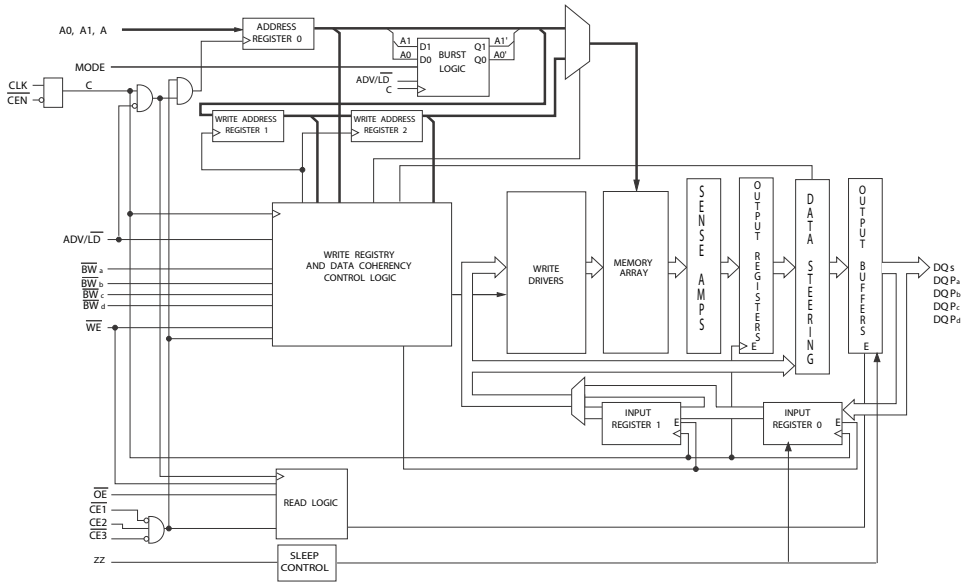
Write operations are controlled by the Byte Write Selects ($\overline{BW_a}$–$\overline{BW_d}$ for CG7772AA) and a Write Enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self timed write circuitry.

Three synchronous Chip Enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. To avoid bus contention, the output drivers are synchronously tri-stated during the data portion of a write sequence.

Selection Guide

Description	167 MHz	Unit
Maximum Access Time	3.4	ns
Maximum Operating Current	450	mA
Maximum CMOS Standby Current	120	mA

Logic Block Diagram – CG7772AA



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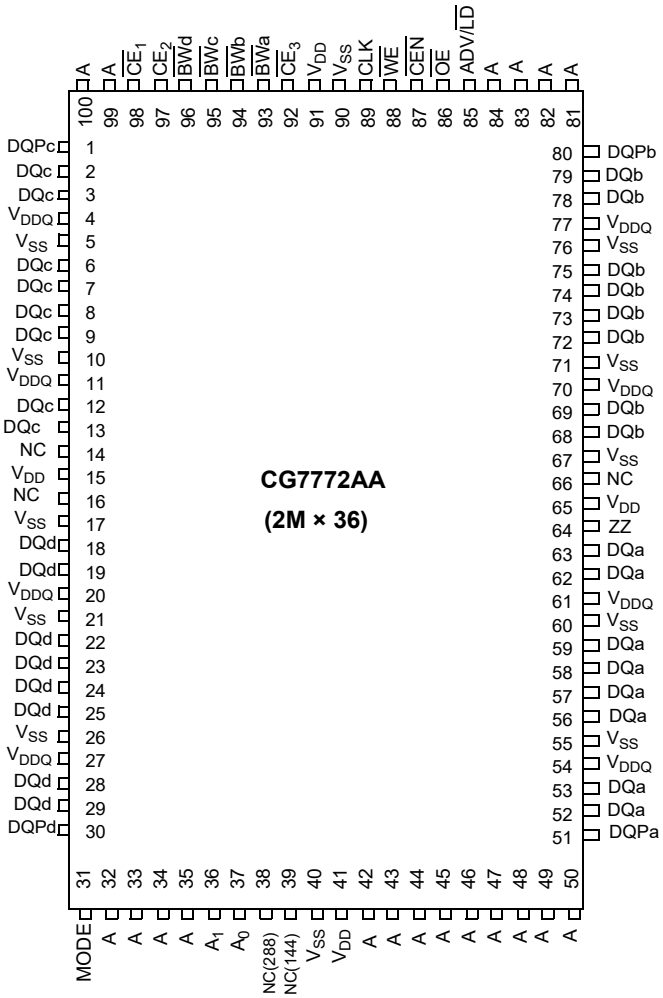
Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) Pinout



Pin Definitions

Pin Name	I/O Type	Pin Description
A_0, A_1, A	Input-Synchronous	**Address Inputs Used to Select One of the Address Locations**. Sampled at the rising edge of the CLK.
$\overline{BW}_a$, $\overline{BW}_b$, $\overline{BW}_c$, $\overline{BW}_d$	Input-Synchronous	**Byte Write Select Inputs, Active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK. $\overline{BW}_a$ controls DQ_a and DQP_a, $\overline{BW}_b$ controls DQ_b and DQP_b, $\overline{BW}_c$ controls DQ_c and DQP_c, $\overline{BW}_d$ controls DQ_d and DQP_d,
$\overline{WE}$	Input-Synchronous	**Write Enable Input, Active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	Input-Synchronous	**Advance/Load Input Used to Advance the On-chip Address Counter or Load a New Address**. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ must be driven LOW to load a new address.
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE}_1$	Input-Synchronous	**Chip Enable 1 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select or deselect the device.
CE_2	Input-Synchronous	**Chip Enable 2 Input, Active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select or deselect the device.
$\overline{CE}_3$	Input-Synchronous	**Chip Enable 3 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select or deselect the device.
$\overline{OE}$	Input-Asynchronous	**Output Enable, Active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are enabled to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state and when the device has been deselected.
$\overline{CEN}$	Input-Synchronous	**Clock Enable Input, Active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
DQ_S	I/O-Synchronous	**Bidirectional Data I/O Lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by address A during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, DQ_a–DQ_d are placed in a tri-state condition. The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_X	I/O-Synchronous	**Bidirectional Data Parity I/O Lines**. Functionally, these signals are identical to DQ_X. During write sequences, DQP_a is controlled by $\overline{BW}_a$, DQP_b is controlled by $\overline{BW}_b$, DQP_c is controlled by $\overline{BW}_c$, and DQP_d is controlled by $\overline{BW}_d$,
MODE	Input Strap Pin	**Mode Input**. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE must not change states during operation. When left floating MODE defaults HIGH, to an interleaved burst order.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{DDQ}	I/O Power Supply	**Power Supply for the I/O Circuitry**.
V_{SS}	Ground	**Ground for the Device**. Should be connected to ground of the system.
NC	–	**No Connects**. This pin is not connected to the die.

Pin Definitions (continued)

Pin Name	I/O Type	Pin Description
NC(144M, 288M, 576M, 1G)	–	**These Pins are Not Connected**. They are used for expansion to the 144M, 288M, 576M, and 1G densities.
ZZ	Input-Asynchronous	**ZZ "Sleep" Input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved. During normal operation, this pin must be LOW or left floating. ZZ pin has an internal pull-down.

Functional Overview

The CG7772AA is synchronous-pipelined Burst NoBL SRAM designed specifically to eliminate wait states during read or write transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal ($\overline{CEN}$). If $\overline{CEN}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{CEN}$. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 3.4 ns (167 MHz device).

Accesses can be initiated by asserting all three Chip Enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) active at the rising edge of the clock. If $\overline{CEN}$ is active LOW and ADV/$\overline{LD}$ is asserted LOW, the address presented to the device is latched. The access can either be a read or write operation, depending on the status of the Write Enable ($\overline{WE}$). $\overline{BW_{[x]}}$ can be used to conduct Byte Write operations.

Write operations are qualified by the Write Enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous Chip Enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous Output Enable ($\overline{OE}$) simplify depth expansion. All operations (reads, writes, and deselects) are pipelined. ADV/$\overline{LD}$ must be driven LOW after the device has been deselected to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are ALL asserted active, (3) the input signal $\overline{WE}$ is deasserted HIGH, and (4) ADV/$\overline{LD}$ is asserted LOW. The address presented to the address inputs is latched into the Address Register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus within 3.4 ns (167 MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the read access the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW to drive out the requested data. During the second clock, a subsequent operation (read, write, or deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output tri-states following the next clock rise.

Burst Read Accesses

The CG7772AA has an on-chip burst counter that enables the user to supply a single address and conduct up to four reads without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW to load a new address into the SRAM, as described in the section Single Read Accesses. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and wraps around when incremented sufficiently. A HIGH input on ADV/$\overline{LD}$ increments the internal burst counter regardless of the state of chip enables inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

Single Write Accesses

Write accesses are initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are all asserted active, and (3) the signal $\overline{WE}$ is asserted LOW. The address presented to the address inputs is loaded into the Address Register. The write signals are latched into the Control Logic block.

On the subsequent clock rise the data lines are automatically tri-stated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CG7772AA. In addition, the address for the subsequent access (read, write, or deselect) is latched into the Address Register (provided the appropriate control signals are asserted).

On the next clock rise the data presented to DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CG7772AA) (or a subset for byte write operations, see Partial Write Cycle Description on page 9 for details) inputs is latched into the device and the write is complete.

The data written during the Write operation is controlled by $\overline{BW}$ ($\overline{BW_{a,b,c,d}}$ for CG7772AA) signals. The CG7772AA provides Byte Write capability that is described in Partial Write Cycle Description on page 9. Asserting the Write Enable input ($\overline{WE}$) with the selected $\overline{BW}$ input selectively writes to only the desired bytes. Bytes not selected during a Byte Write operation remain unaltered. A synchronous self timed write mechanism has been provided to simplify the write operations. Byte Write capability has been included to greatly simplify read, modify, or write sequences, which can be reduced to simple Byte Write operations.

Because the CG7772AA is common I/O devices, data must not be driven into the device while the outputs are active. The OE can be deasserted HIGH before presenting data to the DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CG7772AA) inputs. Doing so tri-states the output drivers. As a safety precaution, DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CG7772AA) are automatically tri-stated during the data portion of a write cycle, regardless of the state of OE.

Burst Write Accesses

The CG7772AA has an on-chip burst counter that enables the user to supply a single address and conduct up to four write operations without reasserting the address inputs. ADV/LD must be driven LOW to load the initial address, as described in the section Single Write Accesses on page 6. When ADV/LD is driven HIGH on the subsequent clock rise, the Chip Enables (CE_1, CE_2, and CE_3) and WE inputs are ignored and the burst counter is incremented. The correct BW ($BW_{a,b,c,d}$ for CG7772AA) inputs must be driven in each cycle of the burst write to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected before entering the “sleep” mode. CE_1, CE_2, and CE_3, must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ ≥ V_{DD} – 0.2 V	–	120	mA
t_{ZZS}	Device operation to ZZ	ZZ ≥ V_{DD} – 0.2 V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ ≤ 0.2 V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

Truth Table

The truth table for CG7772AA follows[1, 2, 3, 4, 5, 6, 7].

Operation	Address Used	$\overline{CE}$	ZZ	ADV/$\overline{LD}$	$\overline{WE}$	$\overline{BW_X}$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect Cycle	None	H	L	L	X	X	X	L	L–H	Tri-State
Continue Deselect Cycle	None	X	L	H	X	X	X	L	L–H	Tri-State
Read Cycle (Begin Burst)	External	L	L	L	H	X	L	L	L–H	Data Out (Q)
Read Cycle (Continue Burst)	Next	X	L	H	X	X	L	L	L–H	Data Out (Q)
NOP/Dummy Read (Begin Burst)	External	L	L	L	H	X	H	L	L–H	Tri-State
Dummy Read (Continue Burst)	Next	X	L	H	X	X	H	L	L–H	Tri-State
Write Cycle (Begin Burst)	External	L	L	L	L	L	X	L	L–H	Data In (D)
Write Cycle (Continue Burst)	Next	X	L	H	X	L	X	L	L–H	Data In (D)
NOP/Write Abort (Begin Burst)	None	L	L	L	L	H	X	L	L–H	Tri-State
Write Abort (Continue Burst)	Next	X	L	H	X	H	X	L	L–H	Tri-State
Ignore Clock Edge (Stall)	Current	X	L	X	X	X	X	H	L–H	-
Sleep Mode	None	X	H	X	X	X	X	X	X	Tri-State

Notes

1. X = “Don't Care”, H = Logic HIGH, L = Logic LOW, $\overline{CE}$ stands for ALL Chip Enables active. $\overline{BW}$x = 0 signifies at least one Byte Write Select is active, $\overline{BW}$x = Valid signifies that the desired byte write selects are asserted, see Truth Table for details.
2. Write is defined by $\overline{WE}$ and $\overline{BW}_{[a:d]}$. See Partial Write Cycle Description on page 9 for details.
3. When a write cycle is detected, all IOs are tri-stated, even during Byte Writes.
4. The DQ and DQP pins are controlled by the current cycle and the $\overline{OE}$ signal.
5. $\overline{CEN}$ = H inserts wait states.
6. Device powers up deselected with the IOs in a tri-state condition, regardless of $\overline{OE}$.
7. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during Write cycles. During a read cycle DQ_s and $DQP_{[a:d]}$ = tri-state when $\overline{OE}$ is inactive or when the device is deselected, and DQ_s= data when $\overline{OE}$ is active.

Partial Write Cycle Description

The partial write cycle description for CG7772AA follows[8, 9, 10, 11].

Function (CG7772AA)	$\overline{WE}$	$\overline{BW}_d$	$\overline{BW}_c$	$\overline{BW}_b$	$\overline{BW}_a$
Read	H	X	X	X	X
Write – No bytes written	L	H	H	H	H
Write Byte a – (DQ_a and DQP_a)	L	H	H	H	L
Write Byte b – (DQ_b and DQP_b)	L	H	H	L	H
Write Bytes b, a	L	H	H	L	L
Write Byte c – (DQ_c and DQP_c)	L	H	L	H	H
Write Bytes c, a	L	H	L	H	L
Write Bytes c, b	L	H	L	L	H
Write Bytes c, b, a	L	H	L	L	L
Write Byte d – (DQ_d and DQP_d)	L	L	H	H	H
Write Bytes d, a	L	L	H	H	L
Write Bytes d, b	L	L	H	L	H
Write Bytes d, b, a	L	L	H	L	L
Write Bytes d, c	L	L	L	H	H
Write Bytes d, c, a	L	L	L	H	L
Write Bytes d, c, b	L	L	L	L	H
Write All Bytes	L	L	L	L	L

Notes

8. X = “Don't Care”, H = Logic HIGH, L = Logic LOW, $\overline{CE}$ stands for ALL Chip Enables active. $\overline{BW}$x = 0 signifies at least one Byte Write Select is active, $\overline{BW}$x = Valid signifies that the desired byte write selects are asserted, see Truth Table on page 8 for details.
9. Write is defined by $\overline{WE}$ and $\overline{BW}_{[a:d]}$. See Partial Write Cycle Description on page 9 for details.
10. When a write cycle is detected, all IOs are tri-stated, even during Byte Writes.
11. Table lists only a partial listing of the Byte Write combinations. Any combination of $\overline{BW}_{[a:d]}$ is valid. Appropriate Write is based on which Byte Write is active.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND .....–0.5 V to +4.6 V

Supply Voltage on V_{DDQ} Relative to GND .... –0.5 V to +V_{DD}

DC to Outputs in Tri-State .....–0.5 V to V_{DDQ} + 0.5 V

DC Input Voltage ..... –0.5 V to V_{DD} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... > 2001V

Latch Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Industrial	–40 °C to +85 °C	3.3 V – 5% / +10%	2.5 V – 5% to V_{DD}

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical Single Bit Upsets	25 °C	361	394	FIT/Mb
LMBU	Logical Multi Bit Upsets	25 °C	0	0.01	FIT/Mb
SEL	Single Event Latch up	85 °C	0	0.1	FIT/Dev

* *No LMBU or SEL events occurred during testing*; this column represents a statistical χ^2, 95% confidence limit calculation. For more details refer to Application Note AN54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates".

Electrical Characteristics

Over the Operating Range

Parameter[12, 13]	Description	Test Conditions	Min	Max	Unit
V_{DD}	Power supply voltage		3.135	3.6	V
V_{DDQ}	I/O supply voltage	For 3.3 V I/O	3.135	V_{DD}	V
		For 2.5 V I/O	2.375	2.625	V
V_{OH}	Output HIGH voltage	For 3.3 V I/O, I_{OH} = –4.0 mA	2.4	–	V
		For 2.5 V I/O, I_{OH}= –1.0 mA	2.0	–	V
V_{OL}	Output LOW voltage	For 3.3 V I/O, I_{OL}= 8.0 mA	–	0.4	V
		For 2.5 V I/O, I_{OL}= 1.0 mA	–	0.4	V
V_{IH}	Input HIGH voltage [12]	For 3.3 V I/O	2.0	V_{DD} + 0.3	V
		For 2.5 V I/O	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage [12]	For 3.3 V I/O	–0.3	0.8	V
		For 2.5 V I/O	–0.3	0.7	V
I_X	Input leakage current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}	–5	5	µA
	Input current of MODE	Input = V_{SS}	–30	–	µA
		Input = V_{DD}	–	5	µA
	Input current of ZZ	Input = V_{SS}	–5	–	µA
		Input = V_{DD}	–	30	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{DDQ}, output disabled	–5	5	µA

Notes

12. Overshoot: $V_{IH(AC)}$ < V_{DD} + 1.5 V (pulse width less than $t_{CYC}/2$). Undershoot: $V_{IL(AC)}$ > –2 V (pulse width less than $t_{CYC}/2$).
13. $T_{power\ up}$: assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

Electrical Characteristics (continued)

Over the Operating Range

Parameter[12, 13]	Description	Test Conditions		Min	Max	Unit
I_{DD} [14]	V_{DD} Operating Supply	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	6.0-ns cycle, 167 MHz	–	450	mA
I_{SB1}	Automatic CE power-down current – TTL Inputs	Max V_{DD}, Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX} = $1/t_{CYC}$	6.0-ns cycle, 167 MHz	–	245	mA
I_{SB2}	Automatic CE power-down current – CMOS Inputs	Max V_{DD}, Device Deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V, f = 0	6.0-ns cycle, 167 MHz	–	120	mA
I_{SB3}	Automatic CE power-down current – CMOS Inputs	Max V_{DD}, Device Deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V, f = f_{MAX} = $1/t_{CYC}$	6.0-ns cycle, 167 MHz	–	245	mA
I_{SB4}	Automatic CE Power Down Current – TTL Inputs	Max V_{DD}, Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0	6.0-ns cycle, 167 MHz	–	135	mA

Note
14. The operation current is calculated with 50% read cycle and 50% write cycle.

Capacitance

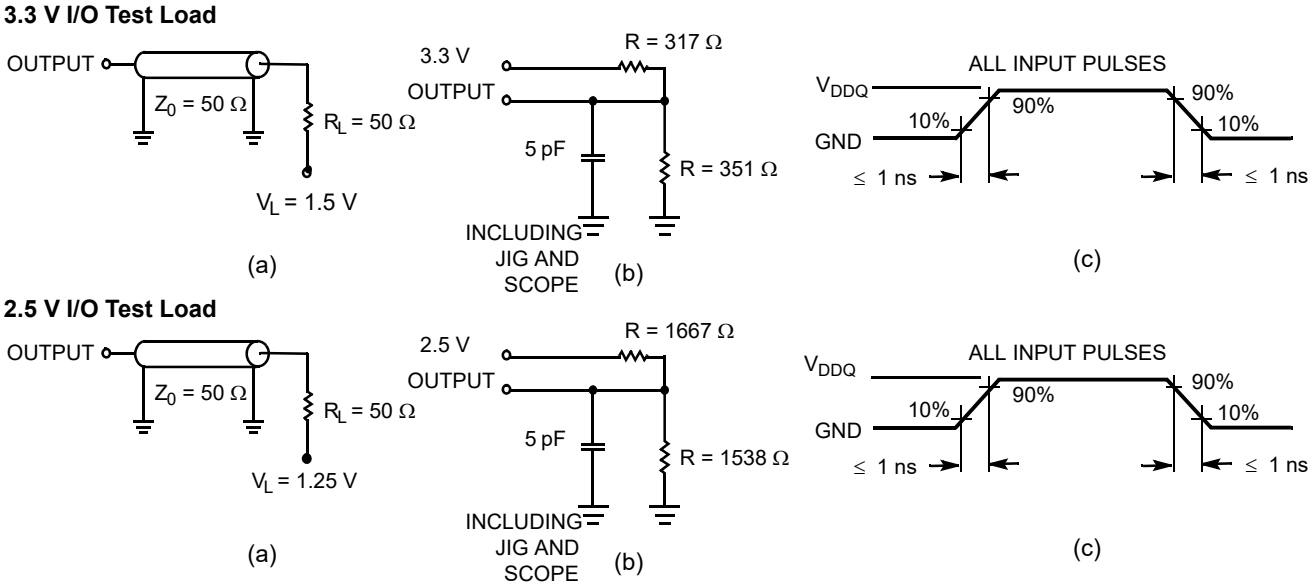
Parameter[15]	Description	Test Conditions	100-pin TQFP Max	Unit
$C_{ADDRESS}$	Address input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V	6	pF
C_{DATA}	Data input capacitance		5	pF
C_{CTRL}	Control input capacitance		8	pF
C_{CLK}	Clock input capacitance		6	pF
C_{IO}	I/O capacitance		5	pF

Thermal Resistance

Parameter[15]	Description	Test Conditions	100-pin TQFP Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	24.63	°C/W
Θ_{JC}	Thermal resistance (junction to case)		2.28	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Note
15. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics

Over the Operating Range

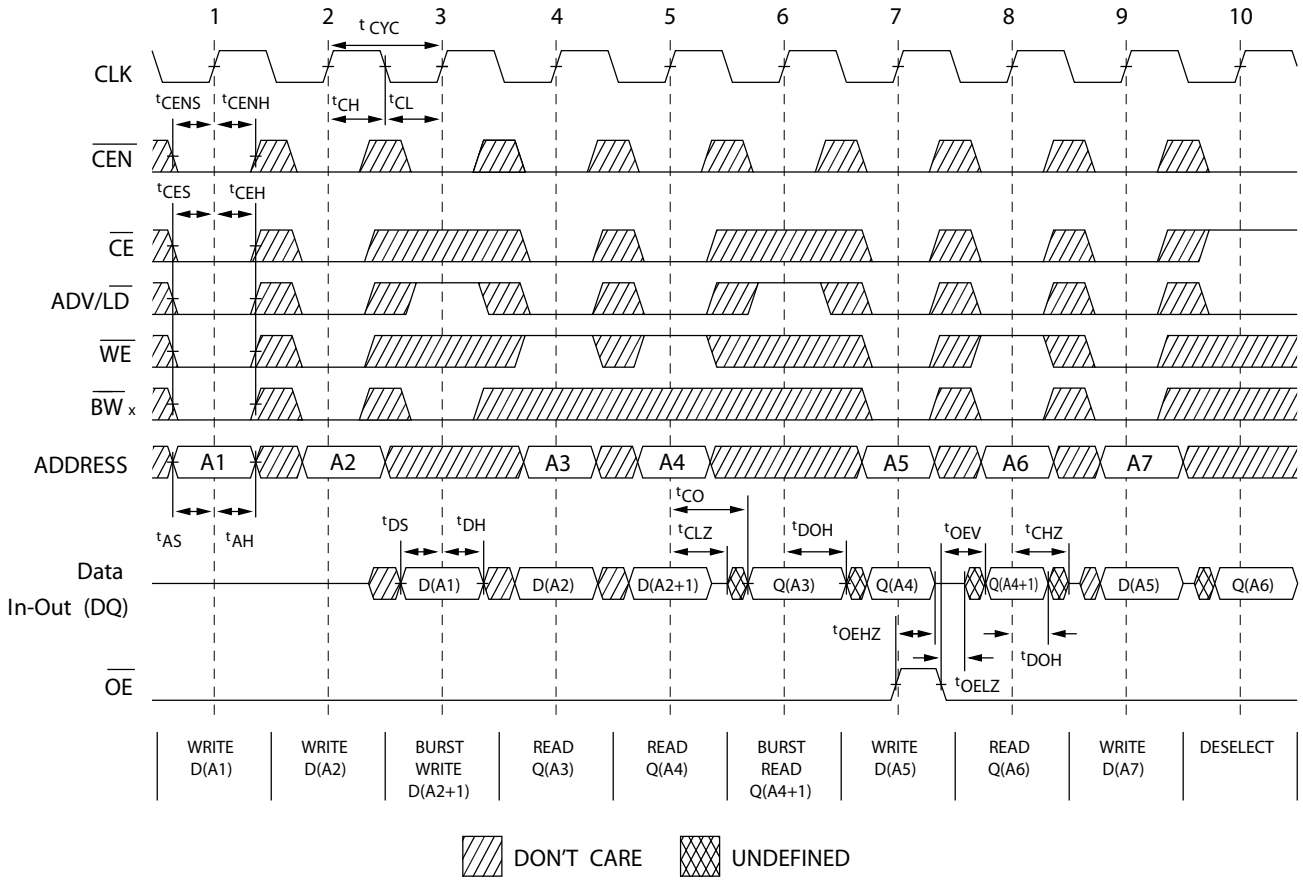
Parameter[16, 17]	Description	-167		Unit
		Min	Max	
t_{Power}[18]	V_{CC}(typical) to the first access read or write	1	–	ms
Clock				
t_{CYC}	Clock cycle time	6.0	–	ns
F_{MAX}	Maximum operating frequency	–	167	MHz
t_{CH}	Clock HIGH	2.2	–	ns
t_{CL}	Clock LOW	2.2	–	ns
Output Times				
t_{CO}	Data output valid after CLK rise	–	3.4	ns
t_{OEV}	$\overline{OE}$ LOW to output valid	–	3.4	ns
t_{DOH}	Data output hold after CLK rise	1.5	–	ns
t_{CHZ}	Clock to high Z[19, 20, 21]	–	3.4	ns
t_{CLZ}	Clock to low Z[19, 20, 21]	1.5	–	ns
t_{EOHZ}	$\overline{OE}$ HIGH to output high Z[19, 20, 21]	–	3.4	ns
t_{EOLZ}	$\overline{OE}$ LOW to output low Z[19, 20, 21]	0	–	ns
Setup Times				
t_{AS}	Address setup before CLK rise	1.5	–	ns
t_{DS}	Data input setup before CLK rise	1.5	–	ns
t_{CENS}	$\overline{CEN}$ setup before CLK rise	1.5	–	ns
t_{WES}	$\overline{WE}$, $\overline{BW}_x$ setup before CLK rise	1.5	–	ns
t_{ALS}	ADV/$\overline{LD}$ setup before CLK rise	1.5	–	ns
t_{CES}	Chip select setup	1.5	–	ns
Hold Times				
t_{AH}	Address hold after CLK rise	0.5	–	ns
t_{DH}	Data input hold after CLK rise	0.5	–	ns
t_{CENH}	$\overline{CEN}$ hold after CLK rise	0.5	–	ns
t_{WEH}	$\overline{WE}$, $\overline{BW}_x$ hold after CLK rise	0.5	–	ns
t_{ALH}	ADV/$\overline{LD}$ hold after CLK rise	0.5	–	ns
t_{CEH}	Chip select hold after CLK rise	0.5	–	ns

Notes

16. Timing reference is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
17. Test conditions shown in (a) of Figure 2 on page 12 unless otherwise noted.
18. This part has an internal voltage regulator; t_{power} is the time power is supplied above V_{DD} minimum initially, before a read or write operation can be initiated.
19. t_{CHZ}, t_{CLZ}, t_{EOLZ}, and t_{EOHZ} are specified with AC test conditions shown in (b) of Figure 2 on page 12. Transition is measured ±200 mV from steady-state voltage.
20. At any voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z before Low Z under the same system conditions.
21. This parameter is sampled and not 100% tested.

Switching Waveforms

Figure 3. Read/Write Timing[22, 23, 24]



Notes
22. For this waveform ZZ is tied LOW.
23. When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH, and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH, CE_2 is LOW or $\overline{CE}_3$ is HIGH.
24. Order of the Burst sequence is determined by the status of the MODE (0 = Linear, 1= Interleaved). Burst operations are optional.

Switching Waveforms (continued)

Figure 4. NOP, STALL and DESELECT Cycles[25, 26, 27]

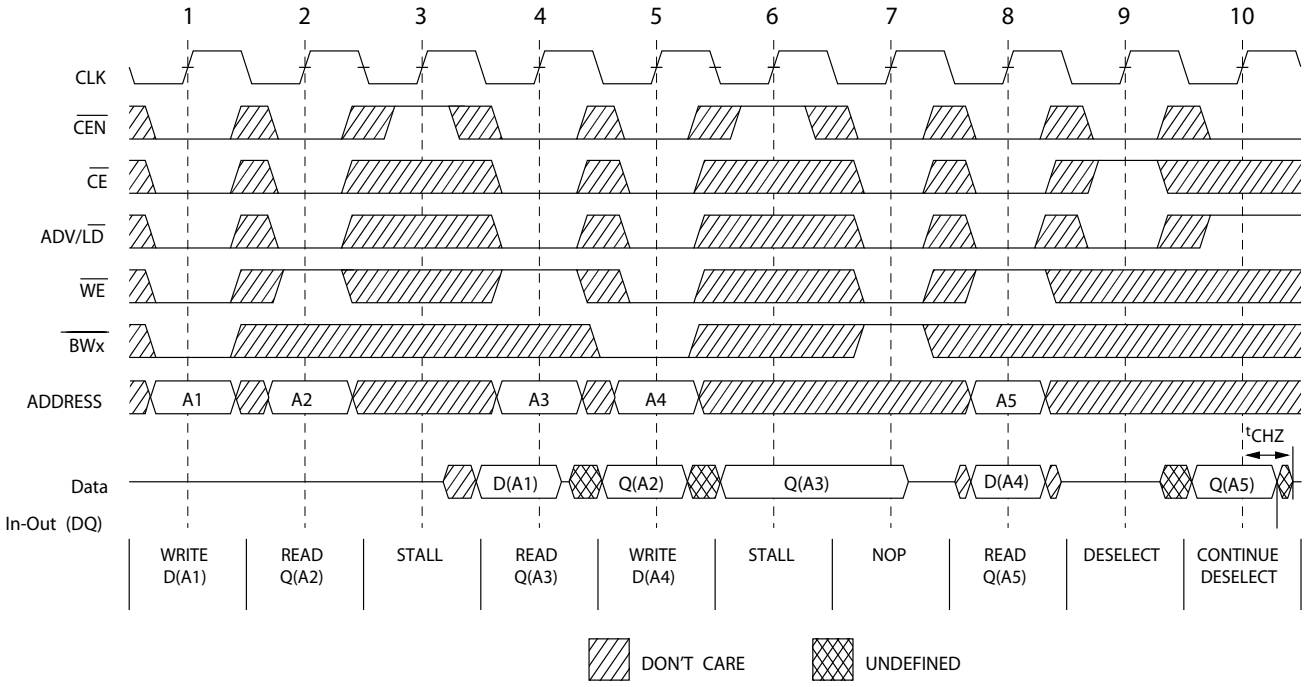
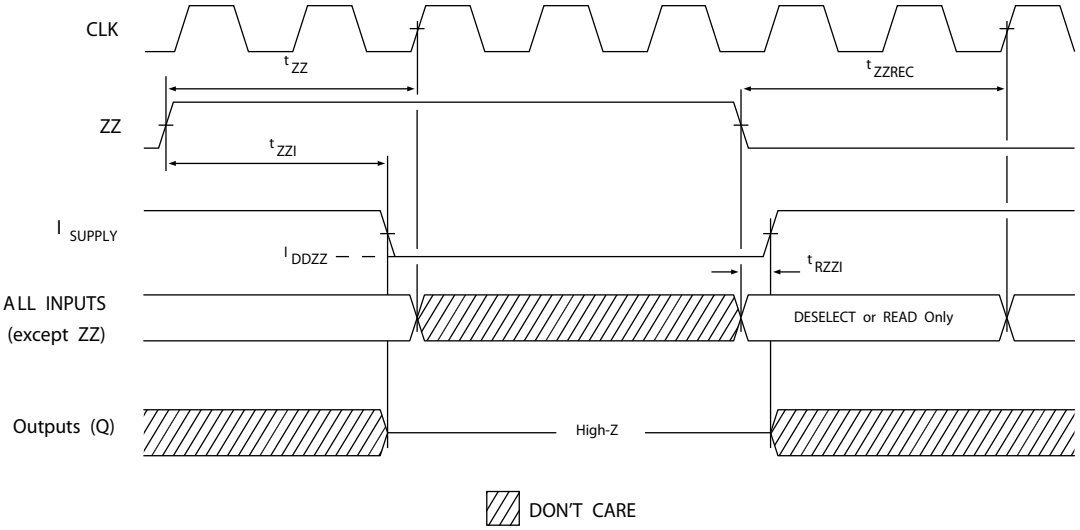


Figure 5. ZZ Mode Timing[28, 29]



Notes
25. For this waveform ZZ is tied LOW.
26. When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH, and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH, CE_2 is LOW or $\overline{CE}_3$ is HIGH.
27. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrated $\overline{CEN}$ being used to create a pause. A Write is not performed during this cycle.
28. Device must be deselected when entering ZZ mode. See Truth Table on page 8 for all possible signal conditions to deselect the device.
29. IOs are in High Z when exiting ZZ sleep mode.

Ordering Information

The table below contains only the parts that are currently available. If you don't see what you are looking for, please contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

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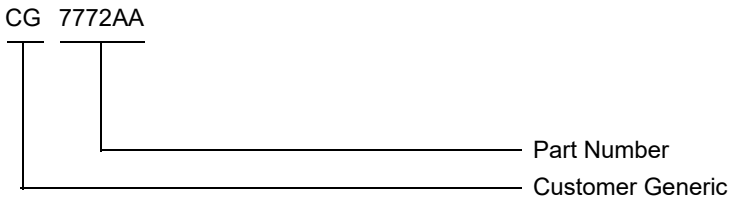
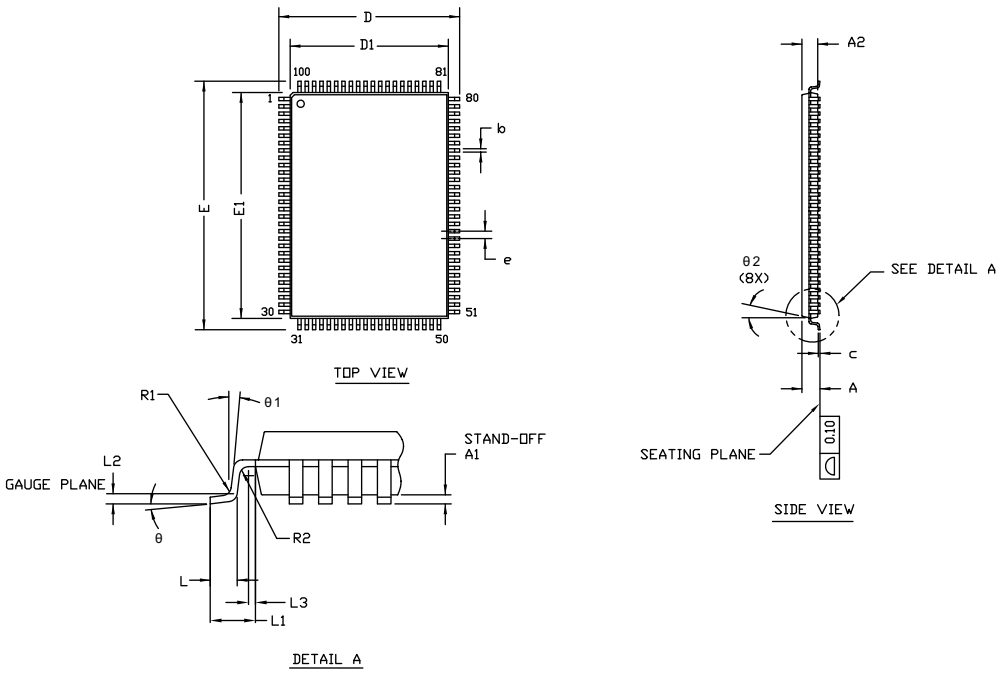
Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
167	CG7772AA	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Industrial

Ordering Code Definitions



Package Diagrams

Figure 6. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
R1	0.08	—	0.20
R2	0.08	—	0.20
θ	0°	—	7°
θ1	0°	—	—
θ2	11°	12°	13°
c	—	—	0.20
b	0.22	0.30	0.38
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
L3	0.20	—	—
e	0.65 TYP		

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH. MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE. BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
3. JEDEC SPECIFICATION NO. REF: MS-026.

51-85050 *G

Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
EIA	Electronic Industries Alliance
I/O	Input/Output
LSB	Least Significant Bit
LMBU	Logical Multi Bit Upsets
LSBU	Logical Single Bit Upsets
MSB	Most Significant Bit
$\overline{OE}$	Output Enable
SEL	Single Event Latch-up
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CG7772AA (CY7C1470BV33-167AXI with NiPdAu Lead Finish), 72-Mbit (2M × 36) Pipelined SRAM with NoBL™ Architecture Document Number: 001-86589				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*B	5440770	PRIT	09/20/2016	Changed status from Preliminary to Final.
*C	6067844	CNX	02/12/2018	Updated Package Diagrams: spec 51-85050 – Changed revision from *F to *G. Updated to new template. Completing Sunset Review.

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