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CG7480AT

8-Mbit (512 K × 16) Static RAM

Features

- Temperature ranges
  - –40 °C to 125 °C
- High speed
  - t_{AA} = 15 ns
- Low active power
  - I_{CC} = 120 mA at 67 MHz
- Low CMOS standby power
  - I_{SB2} = 20 mA
- 2.0-V data retention
- Automatic power-down when deselected
- Transistor-transistor logic (TTL)-compatible inputs and outputs
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Available in Pb-free 44-pin thin small outline package (TSOP) II.

Functional Description

The CG7480AT is a high performance CMOS Static RAM organized as 512 K words by 16 bits.

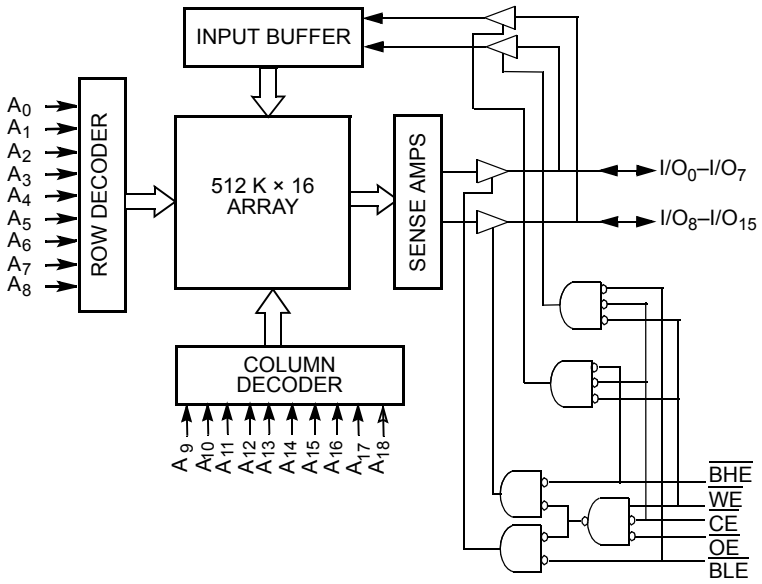
To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte LOW Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0–I/O_7), is written into the location specified on the address pins (A_0–A_{18}). If Byte HIGH Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8–I/O_{15}) is written into the location specified on the address pins (A_0–A_{18}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte LOW Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0–I/O_7. If Byte HIGH Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 11 for a complete description of read and write modes.

The input/output pins (I/O_0–I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW) is in progress.

The CG7480AT is available in a 44-pin TSOP II package with center power and ground (revolutionary) pinout.

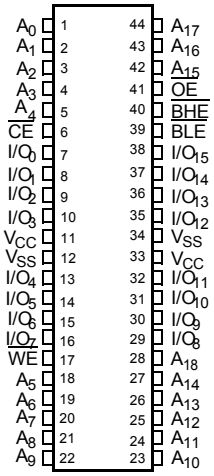
Logic Block Diagram



Contents

Pin Configuration

Figure 1. 44-pin TSOP II pinout (Top View) [1]



Selection Guide

Description	-15	Unit
Maximum access time	15	ns
Maximum operating current	120	mA
Maximum CMOS standby current	20	mA

Note
1. NC pins are not connected on the die.

Maximum Ratings

Exceeding the maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} to relative GND [2] .....–0.5 V to +4.6 V

DC voltage applied to outputs in high-Z state [2] ..... –0.3 V to V_{CC} + 0.3 V

DC input voltage [2] ..... –0.3 V to V_{CC} + 0.3 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) .....>2001 V

Latch-up current .....>200 mA

Operating Range

Device	Ambient Temperature	V_{CC}	Speed
CG7480AT	–40 °C to +125 °C	3.3 V ± 0.3 V	15 ns

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-15		Unit
			Min	Max	
V_{OH}	Output HIGH voltage	Min V_{CC}, I_{OH} = –4.0 mA	2.4	–	V
V_{OL}	Output LOW voltage	Min V_{CC}, I_{OL} = 8.0 mA	–	0.4	V
V_{IH}[2]	Input HIGH voltage		2.0	V_{CC} + 0.3	V
V_{IL}[2]	Input LOW voltage		–0.3	0.8	V
I_{IX}	Input leakage current	GND ≤ V_{IN} ≤ V_{CC}	–5	+5	µA
I_{OZ}	Output leakage current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled	–5	+5	µA
I_{CC}	V_{CC} operating supply current	Max V_{CC}, f = f_{MAX} = $1/t_{RC}$	–	120	mA
I_{SB1}	Automatic CE power down current – TTL inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	–	60	mA
I_{SB2}	Automatic CE Power Down Current – CMOS Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V or V_{IN} ≤ 0.3 V, f = 0	–	20	mA

Note
2. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2.0 V for pulse durations of less than 20 ns.

Capacitance

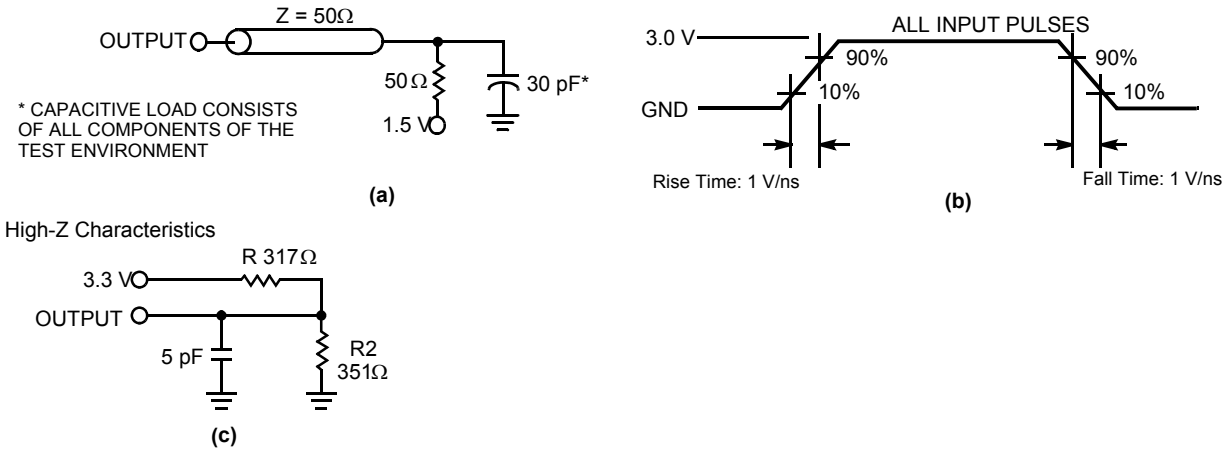
Parameter [3]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	12	pF
C_{OUT}	I/O capacitance		12	pF

Thermal Resistance

Parameter [3]	Description	Test Conditions	TSOP II Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	51.43	°C/W
Θ_{JC}	Thermal resistance (junction to case)		15.8	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms [4]



Notes
3. Tested initially and after any design or process changes that may affect these parameters.
4. AC characteristics (except High-Z) are tested using the load conditions shown in Figure 2 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).

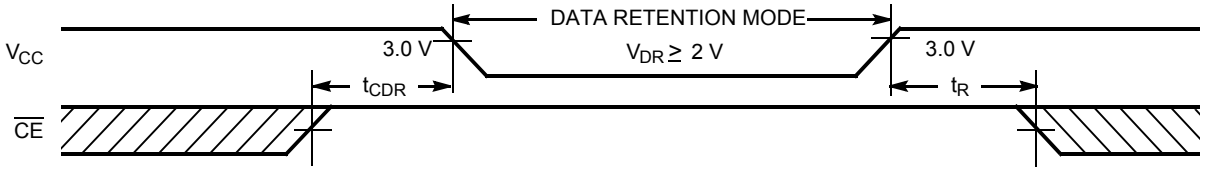
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions [5]	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention		2.0	–	V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0$ V, $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V	–	20	mA
t_{CDR}[6]	Chip Deselect to Data Retention Time		0	–	ns
t_R[6]	Operation Recovery Time		t_{RC}	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes
5. No inputs may exceed V_{CC} + 0.3 V.
6. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC}(min) ≥ 50 µs or stable at V_{CC}(min) ≥ 50 µs.

AC Switching Characteristics

Over the Operating Range

Parameter [7]	Description	-15		Unit
		Min	Max	
Read Cycle				
t_{power} [8]	V_{CC}(typical) to the First Access	100	–	µs
t_{RC}	Read Cycle Time	15	–	ns
t_{AA}	Address to Data Valid	–	15	ns
t_{OHA}	Data Hold from Address Change	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid	–	15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	–	7	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z [9, 10]	–	7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z [10]	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z [9, 10]	–	6	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to Power Down	–	15	ns
t_{DBE}	Byte Enable to Data Valid	–	7	ns
t_{LZBE}	Byte Enable to Low-Z	0	–	ns
t_{HZBE}	Byte Disable to High-Z	–	7	ns
Write Cycle [11, 12]				
t_{WC}	Write Cycle Time	15	–	ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10	–	ns
t_{AW}	Address Setup to Write End	10	–	ns
t_{HA}	Address Hold from Write End	0	–	ns
t_{SA}	Address Setup to Write Start	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	10	–	ns
t_{SD}	Data Setup to Write End	7	–	ns
t_{HD}	Data Hold from Write End	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z [10]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z [9, 10]	–	7	ns
t_{BW}	Byte Enable to End of Write	10	–	ns

Notes

7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
8. t_{POWER} gives the minimum amount of time that the power supply must be at typical V_{CC} values until the first memory access can be performed.
9. t_{HZOE}, t_{HZCE}, t_{HZBE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of Figure 2 on page 5.Transition is measured when the outputs enter a high impedance state.
10. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, t_{HZBE} is less than t_{LZBE}, and t_{HZWE} is less than t_{LZWE} for any device.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data setup and hold timing must refer to the leading edge of the signal that terminates the write.
12. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 4. Read Cycle No. 1 [13, 14]

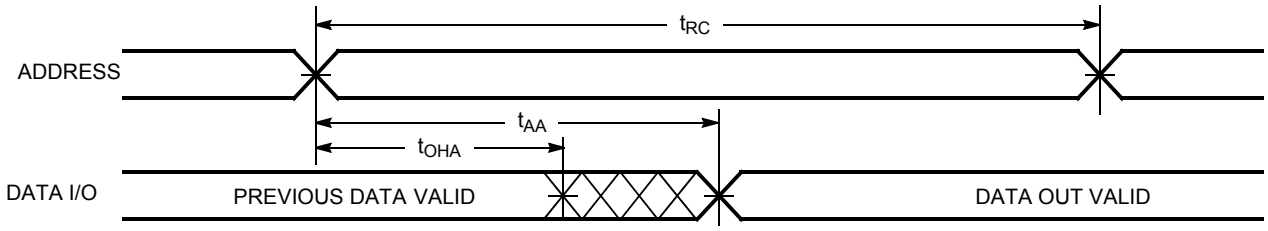
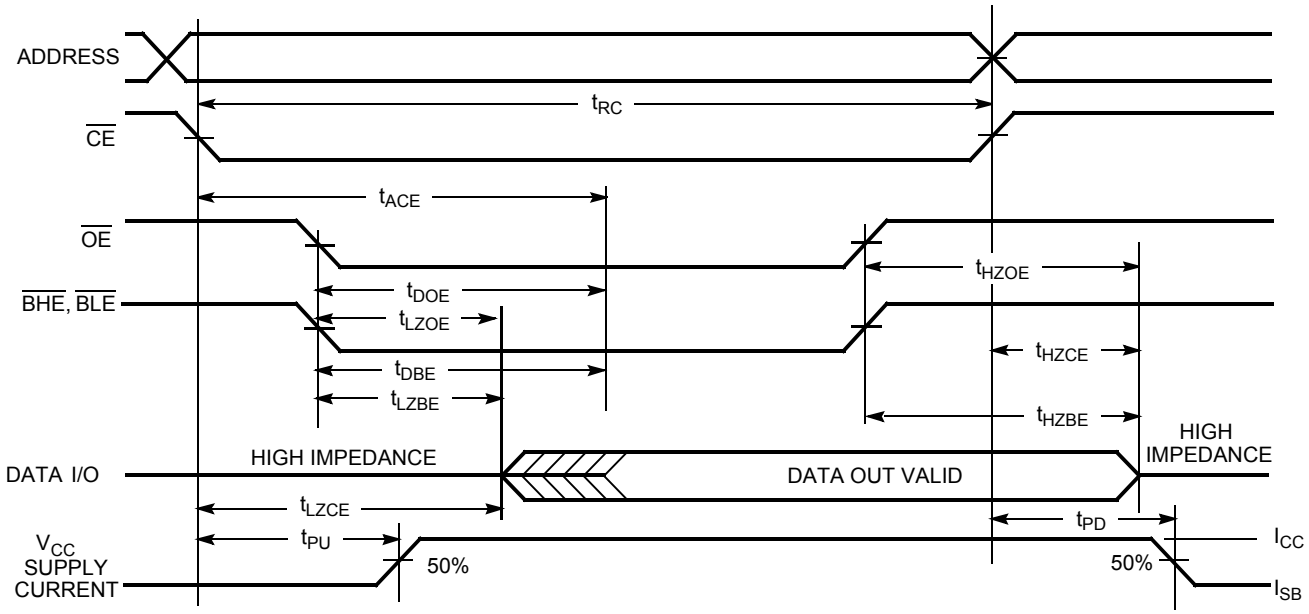


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [14, 15]



Notes
13. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$, or both = V_{IL}.
14. $\overline{WE}$ is HIGH for Read cycle.
15. Address valid before or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms(continued)

Figure 6. Write Cycle No. 1 ($\overline{CE}$ Controlled) [16, 17]

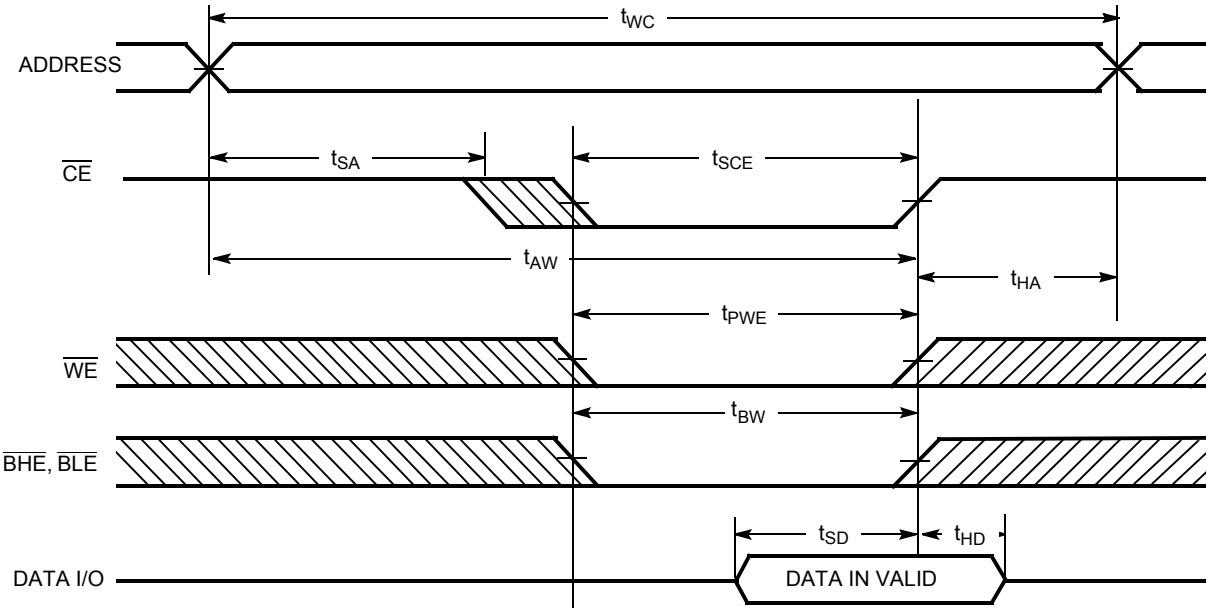
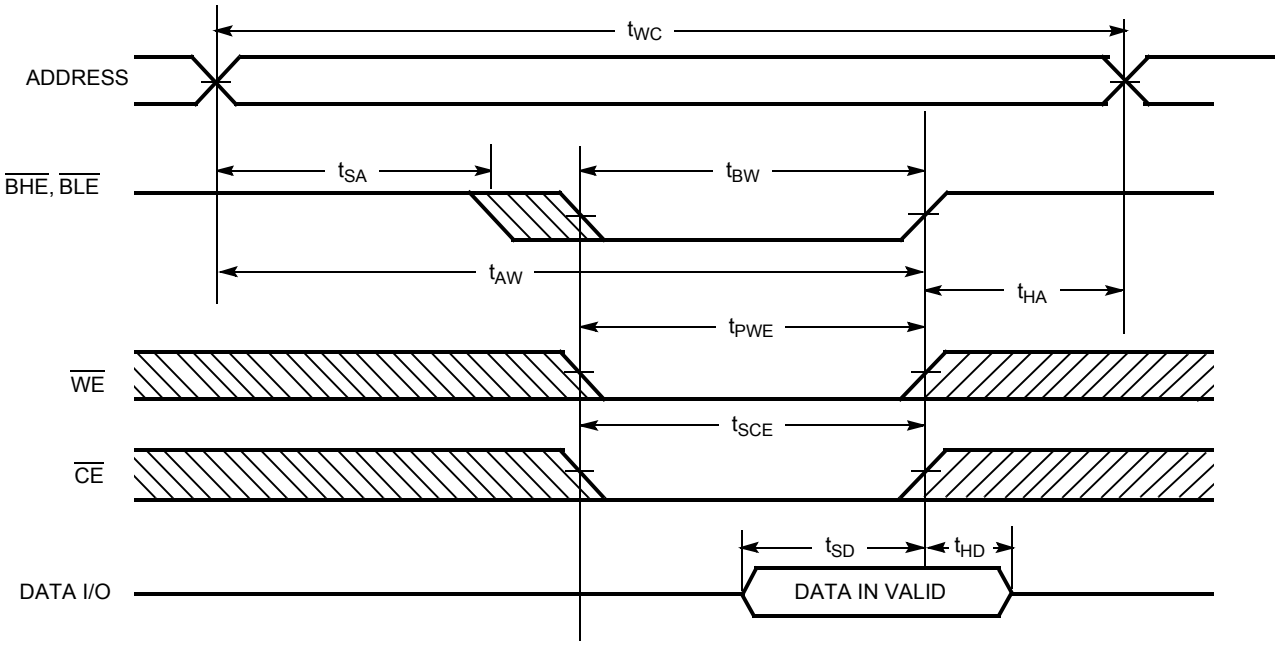


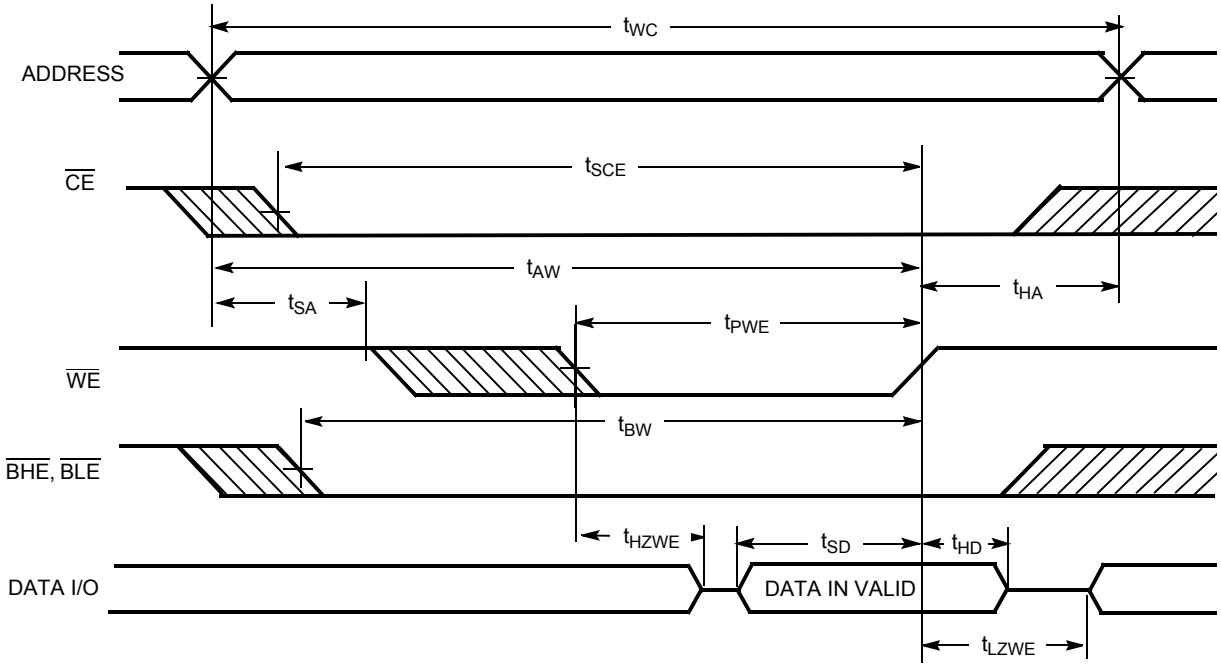
Figure 7. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Notes
16. Data I/O is high-impedance if $\overline{OE}$, or $\overline{BHE}$, $\overline{BLE}$, or both = V_{IH}.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms(continued)

Figure 8. Write Cycle No. 3 (WE Controlled, OE LOW) [18]



Note
18. The minimum pulse width for Write Cycle No. 3 (WE Controlled and OE LOW) should be sum of t_{HZWE} and t_{SD}.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0–I/O_7	I/O_8–I/O_{15}	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I_{CC})
L	L	H	L	H	Data Out	High-Z	Read Lower Bits Only	Active (I_{CC})
L	L	H	H	L	High-Z	Data Out	Read Upper Bits Only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write All Bits	Active (I_{CC})
L	X	L	L	H	Data In	High-Z	Write Lower Bits Only	Active (I_{CC})
L	X	L	H	L	High-Z	Data In	Write Upper Bits Only	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})

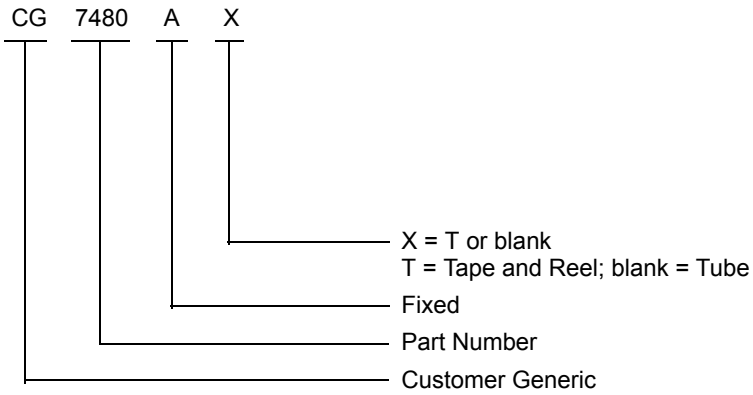
Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative. Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CG7480AT	51-85087	44-pin TSOP II (Pb-free)	Industrial

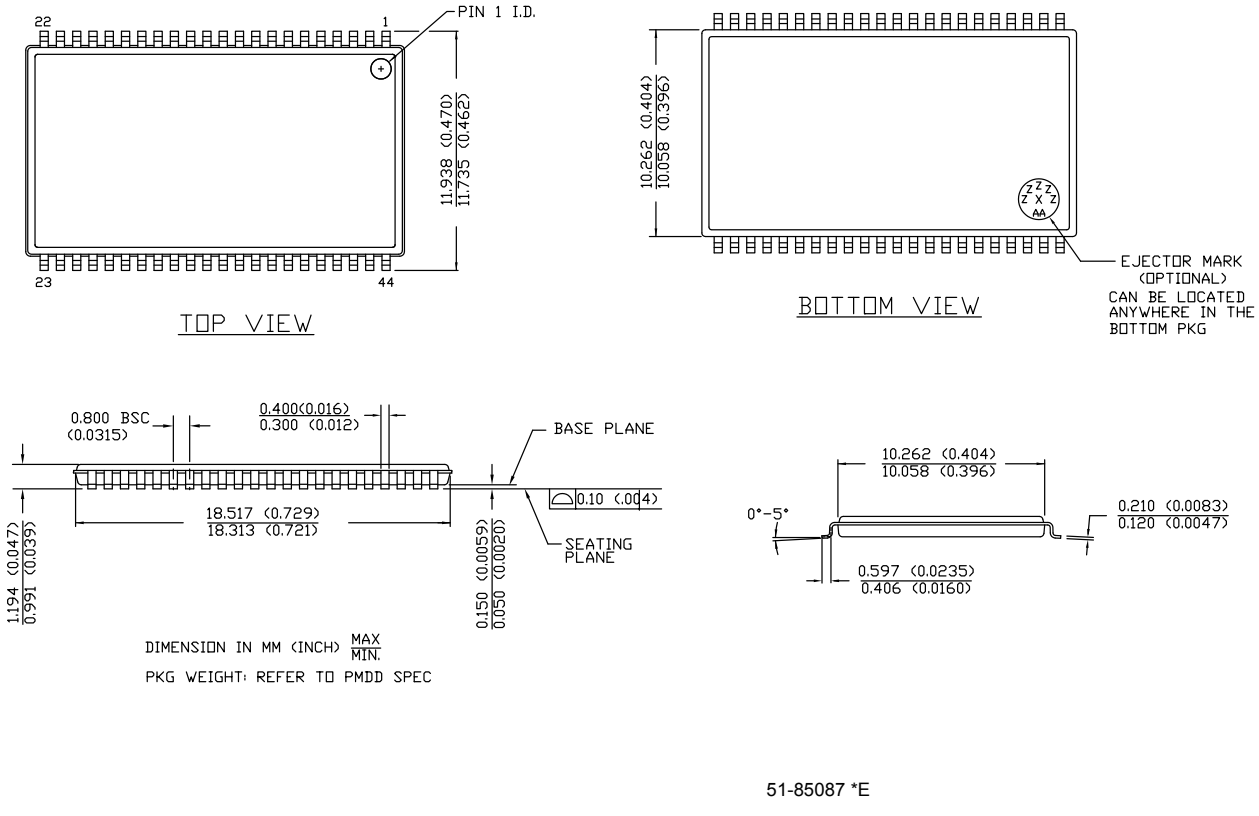
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

Figure 9. 44-pin TSOP II Package Outline, 51-85087



51-85087 *E

Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
SOJ	Small Outline J-lead
TSOP	Thin Small Outline Package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mV	millivolt
mW	milliwatt
ns	nanosecond
ppm	parts per million
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CG7480AT, 8-Mbit (512 K × 16) Static RAM Document Number: 001-73191				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3389929	TAVA	01/18/2012	New data sheet.
*A	4333695	VINI	04/04/2014	Updated Switching Waveforms: Added Note 18 and referred the same note in Figure 8. Updated Package Diagrams: spec 51-85087 – Changed revision from *D to *E. Updated in new template. Completing Sunset Review.

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