CE95387–Trim and Margin Code Example with PSoC®3/PSoC 5LP

Objective

This code example demonstrates the basic operation of the Trim and Margin Component in PSoC Creator™.

Overview

This code example shows how the Trim and Margin Component runs on PSoC® 3 and PSoC 5LP devices. It is intended for use with the CY8CKIT-030 PSoC 3 Development Kit (DVK) orCY8CKIT-050 PSoC 5LP DVK and the CY8CKIT-035 PSoC Power Supervision Expansion Board Kit (EBK). The example project consists of the Trim and Margin, Power Monitor, Status Register, Control Register, and Character LCD Components.

The Power Monitor Component is configured to monitor the output voltages of the four power converters installed on the CY8CKIT-035 board for display on the LCD. The Trim and Margin Component is used to adjust the power converter output voltages by pressing the two switches on the DVK. These switches are also used to turn off/on the power converters. The Control Register Component is used to control the power-up sequence of the power converters. The Character LCD Component displays the measured and desired voltage for the selected rail. It also displays the current duty cycle of the internal Trim and Margin Component's PWM of the selected rail.

Requirements

Tool: PSoC Creator 3.2 SP1

Programming Language: C (GCC 4.8.4 or later)

Associated Parts: All PSoC 3 and PSoC 5LP parts

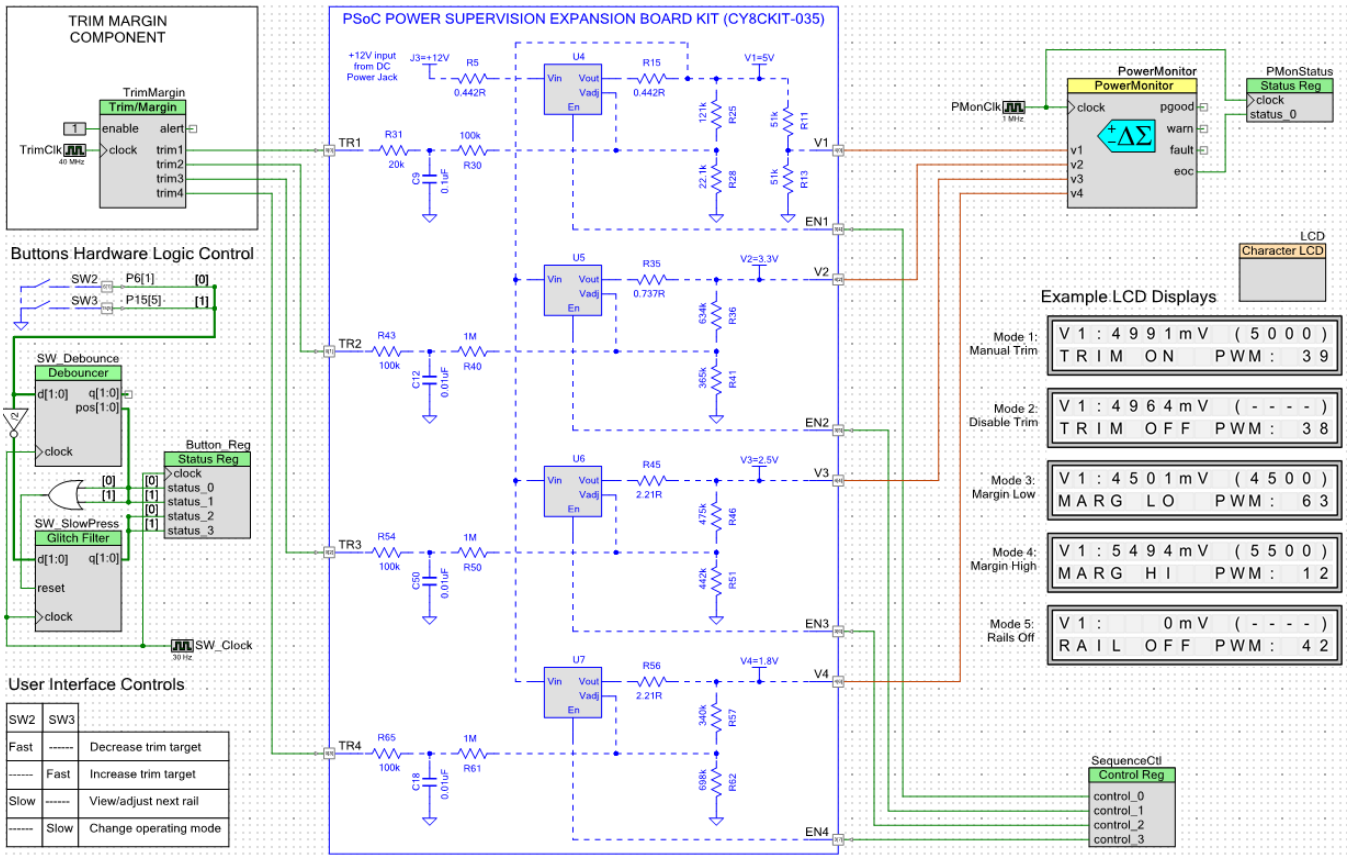
Related Hardware: CY8CKIT-030, CY8CKIT-050, CY8CKIT-035

Design

The code example consists of the Trim and Margin, Power Monitor, Control Register, Status Register, and Character LCD Components. Figure 1 shows the design schematic. The blue annotated block in the middle of the schematic shows the components that are installed on the PSoC Power Supervision EBK, most notably the power converters and the components used for trimming and margining. The Power Monitor Component and the associated Status Registers are used to measure the power converter output voltages, which are then displayed on the Character LCD. The Control Register is used to control the power-up sequence of the power converters.

The four power converter enables are mapped to PSoC GPIO pins P3[4], P3[5], P3[6], and P3[7] respectively. The four PWM pseudo-DAC outputs from the Trim and Margin Components are mapped to PSoC GPIO pins P0[0], P0[1], P0[2], and P0[3] respectively. The four power converter output voltages are mapped to PSoC GPIO pins P4[0], P4[2], P4[4], and P4[6] respectively.

Figure 1. Example Project Power Supervision Schematic



The Debouncer Component prevents mechanical noise associated with pressing a switch, avoiding false triggering of a button press. The Glitch Filter Component works as a slow-press detector. A sticky status register with four bits is used to inform the CPU when the switches are pressed and how. The first two bits represent fast presses, and the other two bits represent slow presses on each switch. Fast and slow presses perform different functions in the design as discussed in the Operation section.

Design Considerations

This design can be extended to a much larger scale system by simply adjusting the number of converters in the various Components and adding Pins Components to the design.

Hardware Setup

1. Configure the PSoC DVK to 5-V operation by setting jumpers J10 and J11 to position 2-3.
2. If using a CY8CKIT-050, remove the SAR bypass jumpers J43 and J44.
3. Connect a USB cable to J1, and connect the other end to an available USB connection on a PC. Proceed to build and program the PSoC DVK. Do not connect the PSoC Power Supervision EBK until you have programmed the PSoC with one of the example projects.
4. Disconnect the USB cable from the PSoC DVK. Ensure the LCD module included with the PSoC DVK is mounted. Connect the Power Supervision EBK to Port E.
5. On the CY8CKIT-035, insert jumper J5 in position 1-2 and populate J6, J7, J8, J9, J10, J11, J12, and J13.
6. Connect the 12-V/3-A supply to J3 and connect the MiniProg3 to white connector J2 of the CY8CKIT-035.

Software Setup

No special software setup is required to use this project.

Components

Table 1 lists the PSoC Creator Components used in this example, as well as the hardware resources used by each.

Table 1. PSoC Creator Components

Component	Hardware Resources
Trim/Margin	Universal digital blocks (UDBs) (4x Datapath Cells, 1x Macrocell, 1x Control Cell)
Power Monitor	1x PGA, 1x DelSig ADC, 1x ISR, UDBs (4x Macrocells, 2x Control Cells)
Character LCD	7x GPIOs
Debouncer	UDBs (5x Macrocells)
Glitch Filter	UDBs (2x Datapath Cells, 2x Macrocells)
Pins	GPIOs
Control Register	UDBs (1x Control Cell)
Status Register	UDB (2x Status Cells)

Parameter Settings

The Trim and Margin and Power Monitor Components are configured to support the four power converters installed on the CY8CKIT-035. Figure 2, Figure 3, and Figure 4 show the Component Configuration Tools. The Character LCD is used in its default configuration. For more information on the use of the Character LCD, Control Register, and Status Register Components, refer to the corresponding Component datasheets.

Figure 2. Trim and Margin Component Configuration

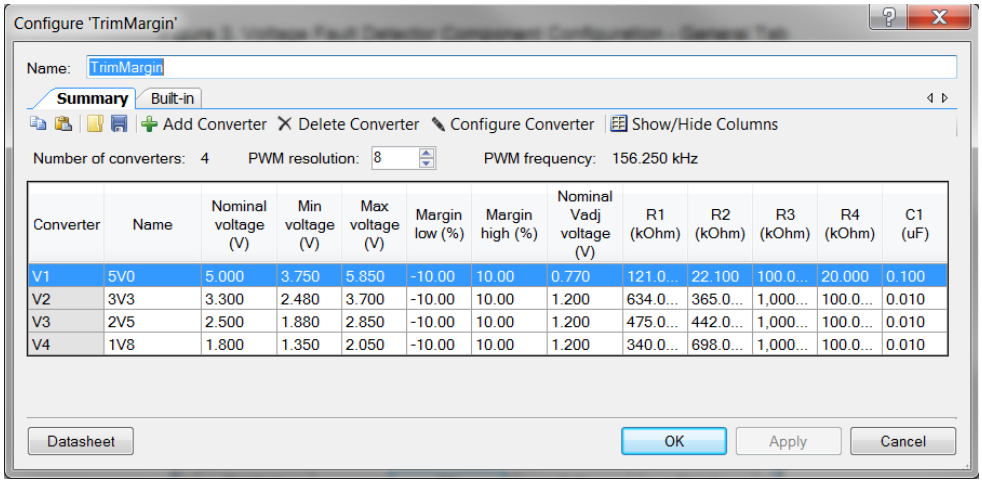


Figure 3. Power Monitor Component Configuration – General Tab

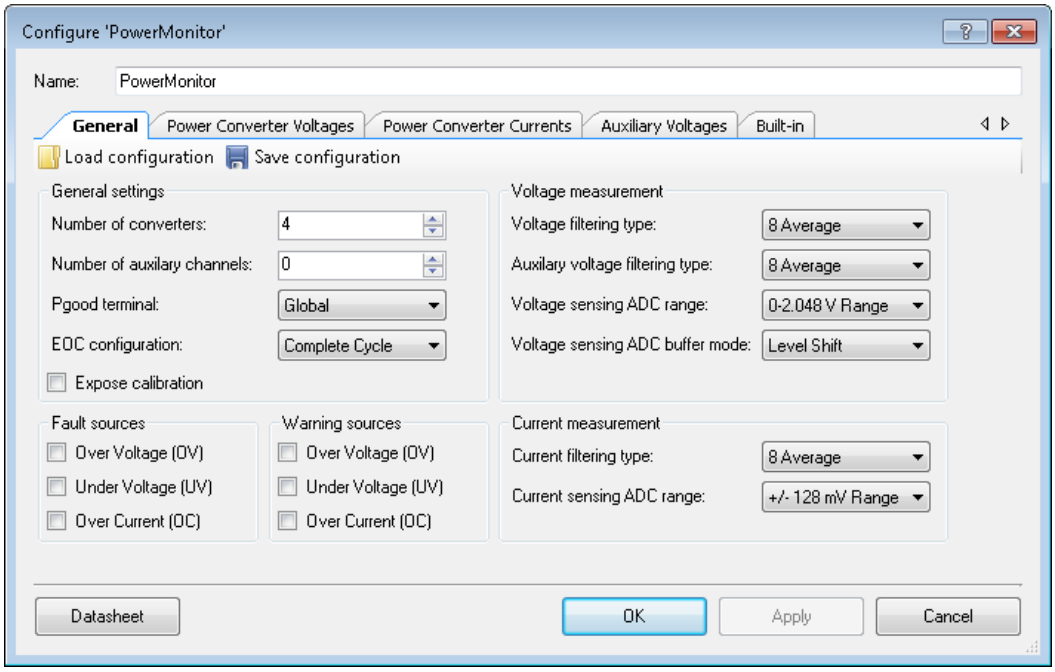
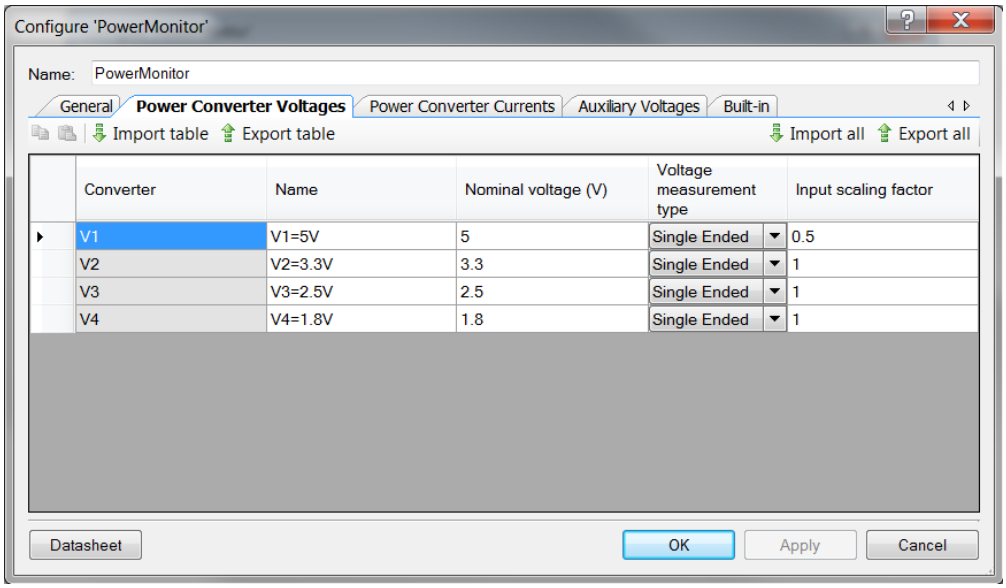


Figure 4. Power Monitor Component Configuration – Power Converter Voltages Tab



Design-Wide Resources

Figure 5 shows the pin selections for the project.

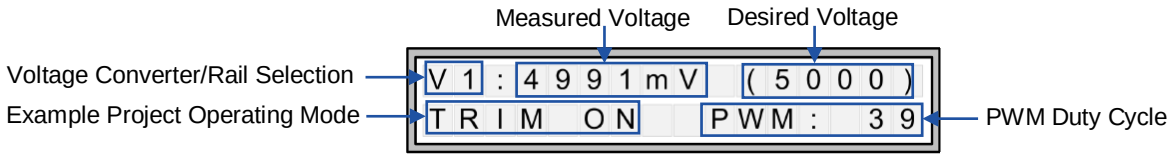
Figure 5. Pin Selections

Alias	Name	Port	Pin	Lock
	\LCD:LCDPort[6:0]\	P2[6:0]	95..99,1..2	☑
	EN1	P3[4] OpAmp1:vminus	48	☑
	EN2	P3[5] OpAmp1:vplus	49	☑
	EN3	P3[6] OpAmp1:vout	51	☑
	EN4	P3[7] OpAmp3:vout	52	☑
	SW2	P6[1]	90	☑
	SW3	P15[5]	94	☑
	TR1	P0[0] OpAmp2:vout	71	☑
	TR2	P0[1] OpAmp0:vout	72	☑
	TR3	P0[2] OpAmp0:vplus	73	☑
	TR4	P0[3] OpAmp0:vminus, DSM:ext_pin_1	74	☑
	V1	P4[0]	69	☑
	V2	P4[2]	80	☑
	V3	P4[4]	82	☑
	V4	P4[6]	84	☑

Operation

On power up, the power converters on the Power Supervision EBK are turned on, and the Trim and Margin Component assists in regulating them to their nominal voltages. As shown in Figure 6, the LCD displays the measured and desired voltages of the selected power converter. It also displays the operating mode of the example project and the duty cycle of the PWM output that adjusts the power converter output voltage.

Figure 6. Character LCD Display Configuration



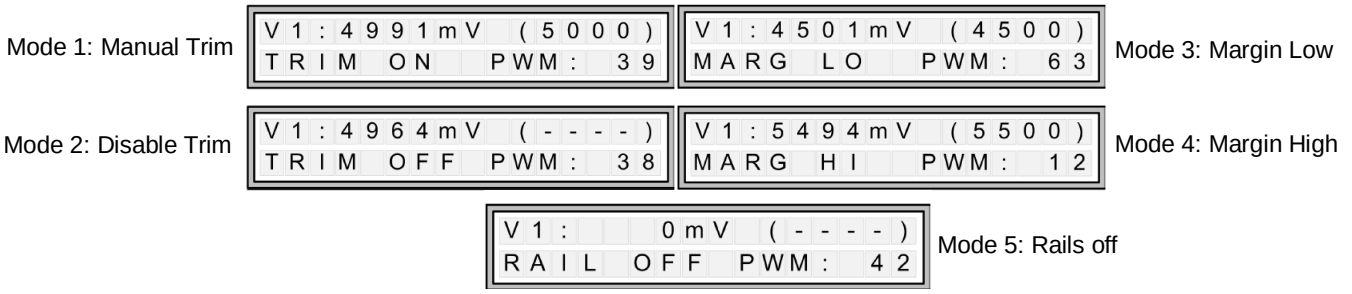
This example project has five operating modes that are intended to demonstrate all the features of the Trim and Margin Component (Manual Trimming mode is the default mode after power up or reset):

- Manual Trimming: A fast press on SW2 (<330 ms) trims converter down by 20 mV; a fast press on SW3 (<330 ms) trims up by 20 mV
- Trimming Off: Disables the trimming function
- Margin Low: Sets all converters to the Margin Low limit set in the **Configure** dialog
- Margin High: Sets all converters to the Margin High limit set in the **Configure** dialog
- Rail Off: Turns all converters off

Press and hold SW3 for more than 330 ms to change the operation modes. Press and hold SW2 for more than 330 ms to change the next power converter information displayed on the LCD.

Figure 7 shows examples of what you should see displayed on the LCD in various situations.

Figure 7. Example Character LCD Displays



Related Documents

Table 2 lists the relevant Component datasheets and application notes.

Table 2. Related Documents

Document	Title	Description
001-94248	PSoC ® Creator ™ Component Datasheet-Power Monitor 1.60	Provides details on using the Power Monitor Component.
001-89124	PSoC ® Creator ™ Component Datasheet-Trim and Margins 1.30	Provides details on using the Trim and Margin Component.
AN93529	Introduction to Power Supervision with PSoC 5LP	Demonstrates how to configure a fully featured power supervision solution using the PSoC Power Supervision Tool. Note that this application note is not posted publicly. Please contact Cypress Technical Support for information on this document.
AN89127	PSoC 5LP Custom Power Supervision	An extension of AN93529 that demonstrates how to customize and create a full-featured power supervision design. Note that this application note is not posted publicly. Please contact Cypress Technical Support for information on this document.

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4818772	RLOS	07/03/2015	New code example.

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