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## Objective

This example demonstrates the operation of multi-counter watchdog timer (MCWDT) counters and interrupts in PSoC® 6 MCU.

## Overview

This example uses two MCWDT PSoC Creator™ Components available in the PSoC 6 MCU devices to generate periodic events. These periodic events are used to drive GPIO pins.

## Requirements

**Tool:** PSoC Creator™ 4.2

**Programming Language:** C (Arm® GCC 5.4-2016-q2-update, Arm MDK 5.22)

**Associated Parts:** All PSoC 6 MCU parts

**Related Hardware:** CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit

## Design

The design shown in Figure 1 consists of two MCWDT\_PDL PSoC Creator Components namely MCWDT\_0 and MCWDT\_1. Each MCWDT block has two 16-bit counters (Counter0 and Counter1) and one 32-bit counter (Counter2). All counters are clocked by either LFCLK (nominal 32 kHz) or by a cascaded counter.

Figure 1. MCWDT Interrupts Example Schematic

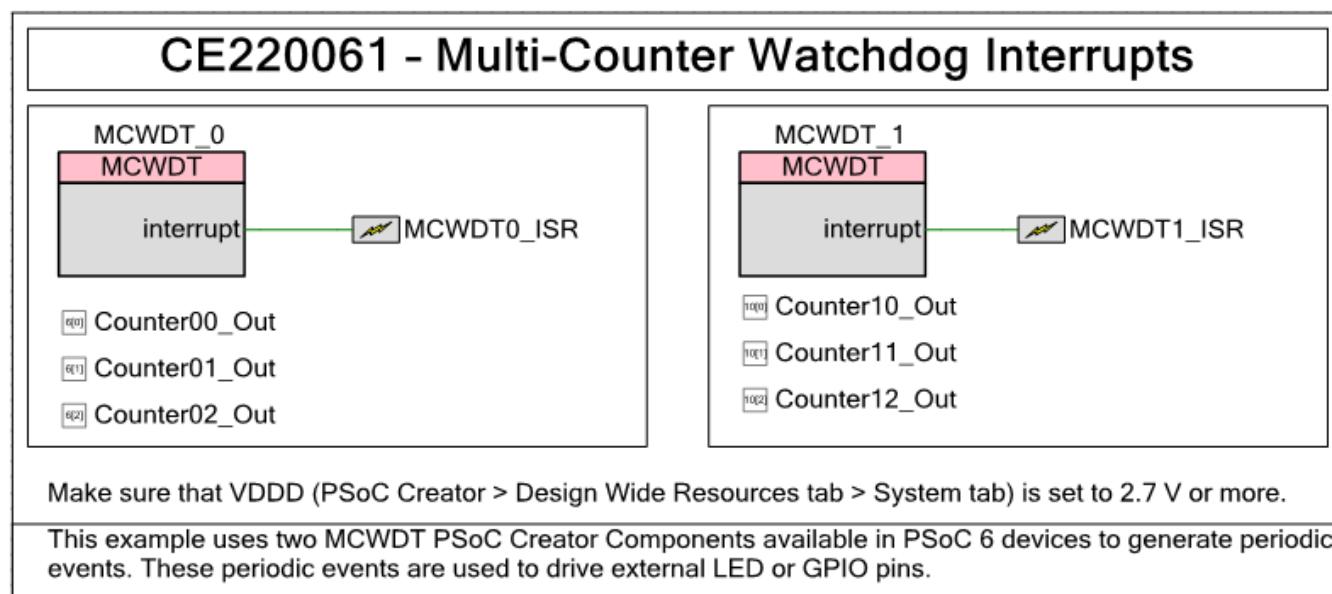


Table 1 shows the configuration of each counter in both the MCWDTs.

Table 1. MCWDT\_0 and MCWDT\_1 Configuration

	Counter0	Counter1	Counter2
<b>MCWDT_0</b>	<ul style="list-style-type: none"> <li>16-bit counter</li> <li>Clocked by LFCLK (32 kHz)</li> <li>Free-running with a period of 65,536 counts</li> <li>Interrupt mode (generates an interrupt when count reaches 65,536)</li> <li>Drives Counter00_Out</li> <li>Period of event = 2 s</li> </ul>	<ul style="list-style-type: none"> <li>16-bit counter</li> <li>Clocked by LFCLK (32 kHz)</li> <li>Clears on match with period 15,999+1</li> <li>Interrupt mode (generates an interrupt when count reaches 16,000)</li> <li>Drives Counter01_Out</li> <li>Period of event = 488 ms</li> </ul>	<ul style="list-style-type: none"> <li>32-bit counter</li> <li>Clocked by MCWDT_0 - Counter1 interrupt</li> <li>Interrupt mode (generates an interrupt when bit position 1 of counter toggles)</li> <li>Drives Counter02_Out</li> <li>Period of event = 976 ms</li> </ul>
<b>MCWDT_1</b>	<ul style="list-style-type: none"> <li>16-bit counter</li> <li>Clocked by LFCLK (32 kHz)</li> <li>Free-running with a period of 65,536 counts</li> <li>Interrupt mode (generates an interrupt when count reaches 65,536)</li> <li>Drives Counter10_Out</li> <li>Period of event = 2 s</li> </ul>	<ul style="list-style-type: none"> <li>16-bit counter</li> <li>Clocked by LFCLK (32 kHz)</li> <li>Clear on match with period 32,768+1</li> <li>Interrupt mode (generates an interrupt when count reaches 32,769)</li> <li>Drives Counter11_Out</li> <li>Period of event = 1 s</li> </ul>	<ul style="list-style-type: none"> <li>32-bit counter</li> <li>Clocked by LFCLK (32 kHz)</li> <li>Interrupt mode (generates an interrupt when bit position 15 of counter toggles)</li> <li>Drives Counter12_Out</li> <li>Period of event = 1 s</li> </ul>

Figure 2 shows the MCWDT\_0 timing diagram.

Figure 2. MCWDT\_0 Timing Diagram

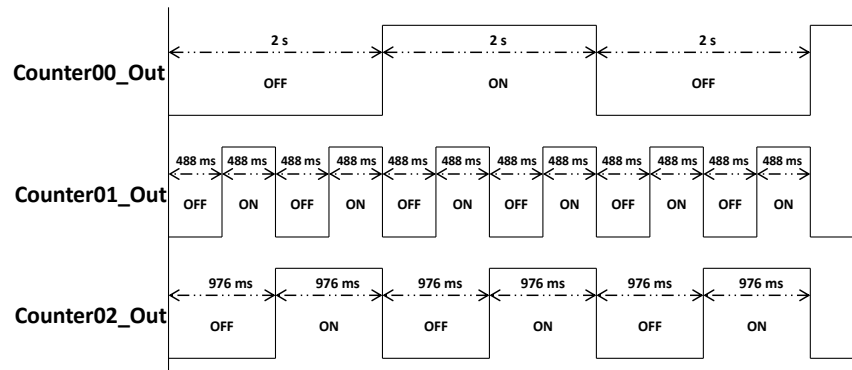
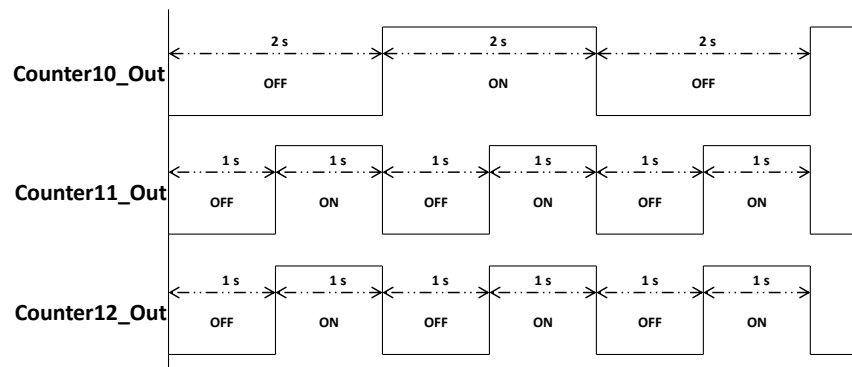


Figure 3 shows the MCWDT\_1 timing diagram.

Figure 3. MCWDT\_1 Timing Diagram



The firmware performs the following in the main function:

1. Initializes the interrupts for MCWDT\_0 and MCWDT\_1.
2. Configures the MCWDT\_0 and MCWDT\_1 Components.
3. Waits for the MCWDT\_0 or MCWDT\_1 interrupt in an infinite loop.

The firmware performs the following in the MCWDT\_0 ISR function:

1. Toggles the Counter00\_Out pin for interrupt from MCWDT\_0 Counter0.
2. Toggles the Counter01\_Out pin for interrupt from MCWDT\_0 Counter1.
3. Toggles the Counter02\_Out pin for interrupt from MCWDT\_0 Counter2.

The firmware performs the following in the MCWDT\_1 ISR function:

1. Toggles the Counter10\_Out pin for interrupt from MCWDT\_1 Counter0.
2. Toggles the Counter11\_Out pin for interrupt from MCWDT\_1 Counter1.
3. Toggles the Counter12\_Out pin for interrupt from MCWDT\_1 Counter2.

## Design Considerations

This code example is designed to run on CY8CKIT-062-BLE with the PSoC 6 MCU. To port the design to other PSoC 6 MCU and kits, you must change the target device in Device Selector, and change the pin assignments in the **cydwr** settings. For single-core PSoC 6 MCU devices, port the code from *main\_cm4.c* to *main.c* file as CM0+ CPU is not used in this code example.

This code example does not work at 1.8V (VDD) out of the box. Make sure that the switch "SW5" is set to select "3.3V" as VDD on the CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit.

## Hardware Setup

The code example works with the default settings on the CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit. If the settings are different from the default values, see the "Selection Switches" table in the [kit guide](#) to reset to the default settings.

## Operation

1. Connect CY8CKIT-062 BLE to a USB port on your PC.
2. Build and program the application into CY8CKIT-062 BLE. For more information on building a project or programming a device, see PSoC Creator Help.
3. Probe the following signals on a logic analyzer - Counter00\_Out (P6[0]), Counter01\_Out (P6[1]), Counter02\_Out (P6[2]), Counter10\_Out (P10[0]), Counter11\_Out (P10[1]), Counter12\_Out (P10[2]). Make sure that signal waveforms match the waveforms in [Figure 2](#) and [Figure 3](#).

## Components

[Table 2](#) lists the PSoC Creator Components used in this example and the hardware resources used by each Component.

Table 2. PSoC Creator Components

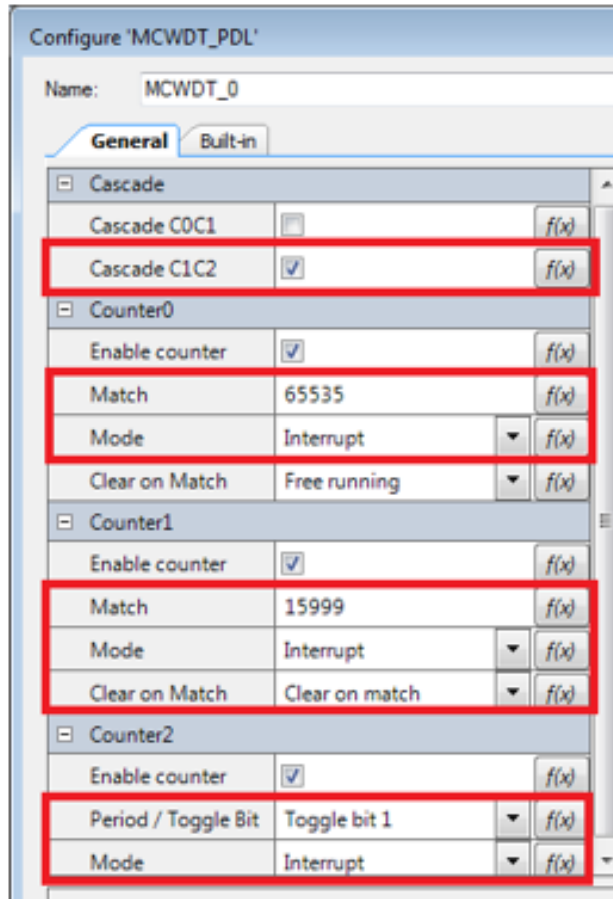
Component	Instance Name	Hardware Resources
Multi-Counter Watchdog (MCWDT_PDL)	MCWDT_0, MCWDT_1	Two MCWDT blocks of the System Resources Sub-System (SRSS)
System Interrupt (SysInt)	MCWDT0_ISR, MCWDT1_ISR	Two entries in the device interrupt vector table

## Parameter Settings

Non-default settings for each Component is outlined in red in the following figure.

MCWDT\_0 Component parameter settings are shown in [Figure 4](#).

Figure 4. MCWDT\_0 Component Parameter Settings



Configure 'MCWDT\_PDL'

Name: MCWDT\_0

**General** Built-in

**Cascade**

Cascade C0C1	<input type="checkbox"/>	f(x)
Cascade C1C2	<input checked="" type="checkbox"/>	f(x)

**Counter0**

Enable counter	<input checked="" type="checkbox"/>	f(x)
Match	65535	f(x)
Mode	Interrupt	f(x)
Clear on Match	Free running	f(x)

**Counter1**

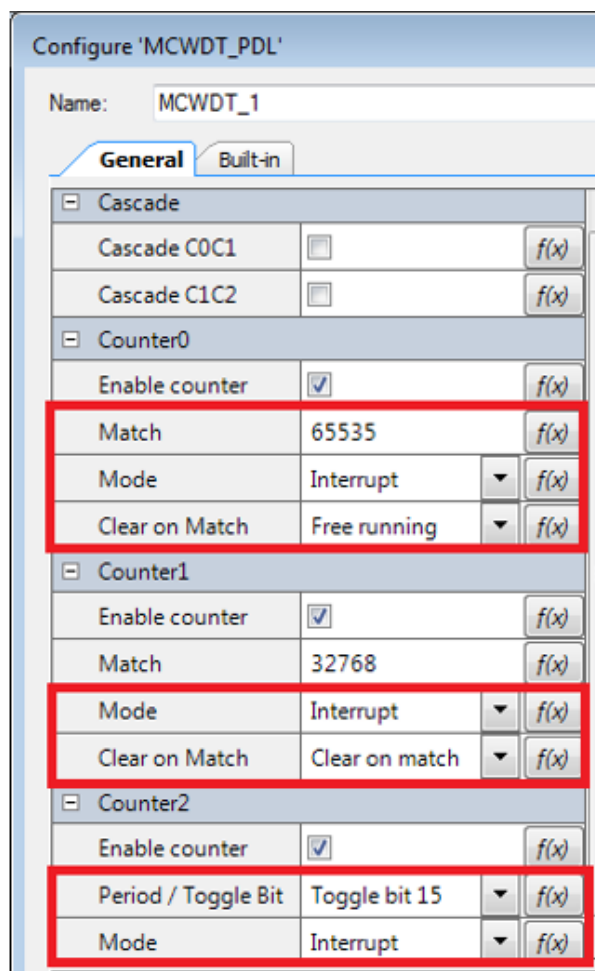
Enable counter	<input checked="" type="checkbox"/>	f(x)
Match	15999	f(x)
Mode	Interrupt	f(x)
Clear on Match	Clear on match	f(x)

**Counter2**

Enable counter	<input checked="" type="checkbox"/>	f(x)
Period / Toggle Bit	Toggle bit 1	f(x)
Mode	Interrupt	f(x)

MCWDT\_1 Component parameter settings are shown in Figure 5.

Figure 5. MCWDT\_1 Component Parameter Settings



## Design-Wide Resources

Table 3 shows the pin assignment for the code example.

Table 3. Pin Names and Location

Pin Name	Location
Counter00_Out	P6[0]
Counter01_Out	P6[1]
Counter02_Out	P6[2]
Counter10_Out	P10[0]
Counter11_Out	P10[1]
Counter12_Out	P10[2]

## Related Documents

Application Notes	
<a href="#">AN210781 – Getting Started with PSoC 6 MCU with Bluetooth Low Energy (BLE) Connectivity</a>	Describes PSoC 63 with Bluetooth Low Energy (BLE) Connectivity and how to build your first PSoC Creator project
PSoC Creator Component Datasheets	
<a href="#">MCWDT_PDL</a>	Supports Multi-Counter Watchdog with two 16-bit counters and one 32-bit counter
<a href="#">System Interrupt</a>	Interrupt vectoring and control
Device Documentation	
<a href="#">PSoC 6 MCU: PSoC 63 with BLE Datasheet</a>	<a href="#">PSoC 6 MCU: PSoC 63 with BLE Architecture Technical Reference Manual</a>
Development Kit (DVK) Documentation	
<a href="#">CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit</a>	

## Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
*A	5858250	VJYA	08/22/2017	Initial public release
*B	5918161	VJYA	11/03/2017	Updated project name
*C	6003197	VJYA	12/22/2017	Updated to latest PSoC Creator build



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