Please note that Cypress is an Infineon Technologies Company.
The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CE219506 – PSoC 6 MCU Clock Buffer with Smart IO

Objective

This example shows how to use a Smart IO Component in PSoC® 6 MCU to implement a clock buffer that can operate in chip low-power modes. The example can also be used to drive a load higher than that is rated for one GPIO by replicating the signal and driving two GPIO pins.

Overview

This code example demonstrates how the lookup tables (LUTs) in the Smart IO block can be used to buffer an external signal. It further shows how to use the buffered signal to drive a high load at the output. The PSoC 6 MCU device is put to Deep Sleep mode.

Requirements

Tool: PSoC Creator™ 4.2

Programming Language: C (Arm® GCC 5.4)

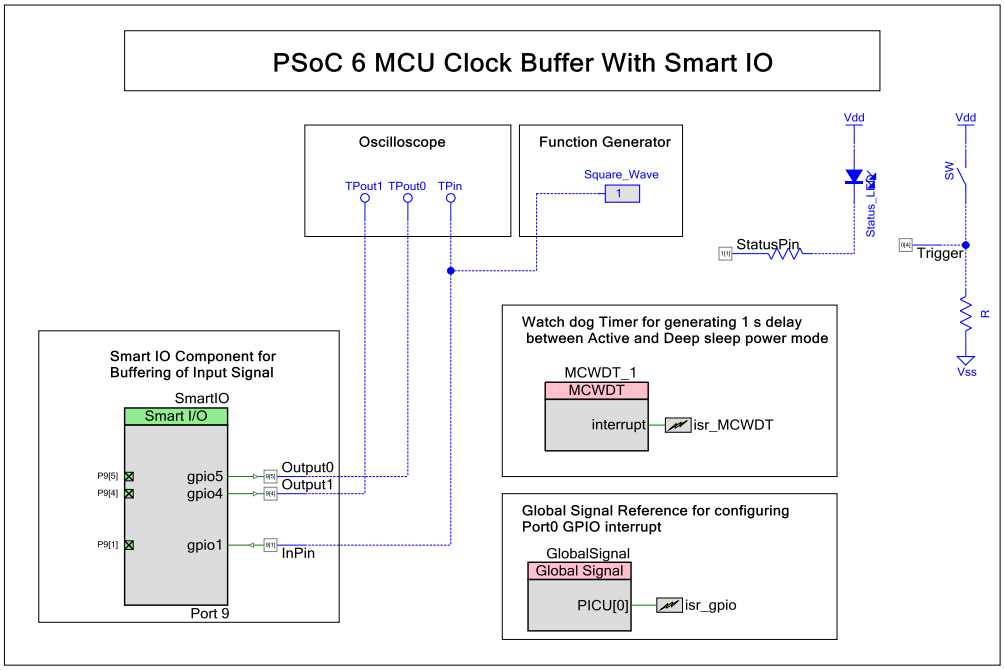
Associated Parts: PSoC 6 MCU

Related Hardware: CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit

Design

The design consists of a Smart IO Component with only input and output pins on the port. The Component does not use any peripherals or internal chip signals. The Smart IO Component performs signal replication by taking in an external signal (such as an external clock) and driving it out to two pins. This effectively implements signal buffer functionality. The two pins can then be ganged externally to the chip to drive a load that is higher than rated for a single GPIO pin. Figure 1 shows the schematic overview of the design.

Figure 1. Design Schematic



The Smart IO Component is operational during the device's Deep Sleep mode. For the clock buffer, an external signal is input through InPin, which in turn is connected to gpio1. This signal is repeated and output to gpio4 and gpio5. These are connected to Output1 and Output0, respectively. Note that when a clock signal is buffered using LUTs of the Smart IO Component, there will be a lag between the input clock signal and the output signal. In a timing-critical system design, this lag must be taken into consideration.

The Smart IO Component is operational in chip Deep Sleep mode. To demonstrate this, PSoC 6 MCU is put to Deep Sleep mode. The device wakes up on a GPIO interrupt and remains in Active mode for 1 second before going back to Deep Sleep mode again.

A GPIO interrupt is generated by a digital input pin Trigger. A Global Signal Reference Component is used to enable the Port 0 Interrupt (PICU [0]) and configure the ISR of the port interrupt. On an interrupt, the device wakes up from Deep Sleep mode, blinks an LED for 1 second, and re-enters Deep Sleep mode. A digital output pin StatusPin is used for device wakeup indication by turning an LED (green) ON for 1 second. A MCWDT Component is used to generate a 1-second timing between device wakeup and device Deep Sleep modes.

The firmware is implemented in *main_cm0p.c* and performs the following functions:

1. Starts the *isr_smartio* interrupt Component and sets up ISR function.
2. Starts the Smart IO Component.
3. The device enters Deep-Sleep mode.
4. If the interrupt is triggered, the device wakes up and drives the StatusPin LOW for 1 second.
5. Drives the StatusPin HIGH (turns OFF Status_LED) and the device re-enters Deep Sleep.

Hardware Setup

1. Connect InPin to a square wave (for example, from a signal generator) that is under 1 MHz. Also, connect the InPin to an oscilloscope.
2. Connect Output0 and Output1 to an oscilloscope.
3. The Smart IO Component is a port-wide resource;, you must define its port before using the Component. Port 8 and Port 9 are Smart IO-enabled ports in PSoC 6 MCU. In CY8CKIT-062-BLE, Port 8 of PSoC 6 is dedicated to CapSense® functionality. Therefore, only Port 9 can be used for Smart IO-based projects on CY8CKIT-062-BLE.

Operation

1. Connect the PSoC 6 BLE Pioneer kit baseboard (CY8CKIT-062-BLE) to your computer's USB port.
2. Build the project and program the PSoC 6 MCU device. For more information on device programming, see PSoC Creator Help.
3. On an oscilloscope, observe that the signal going into InPin (**P9[1]**) is replicated on Output0 (**P9[5])** and Output1 (**P9[4]**). These are operational during Deep Sleep mode, and the two signals can be externally ganged to drive a higher load.
4. Press and release the Trigger pin (**P0[4]**) to generate an interrupt. Observe that the green LED connected to StatusPin (**P1[1]**) lights up for approximately 1 second. Observe that the Output0 and Output1 continue to operate regardless of the chip power mode.

The sections that follow discuss the Components, parameter settings, and resources used to make the example.

Components

Table 1. PSoC Creator Components/Hardware Resources

Component	Hardware Resources
SmartIO	1 I/O port (PRGIO)
Output0, Output1, IntrPin, InPin, TrigPin, StatusPin	6 pins
Global Signal Reference	-
isr_gpio, isr_MCWDT	2 interrupts
MCWDT	1 Multi-counter watch

Component	Hardware Resources
	dog counter (MCWDT)

Parameter Settings

The Smart IO Component is configured in Asynchronous mode.

Figure 2. Smart IO Routing Configuration

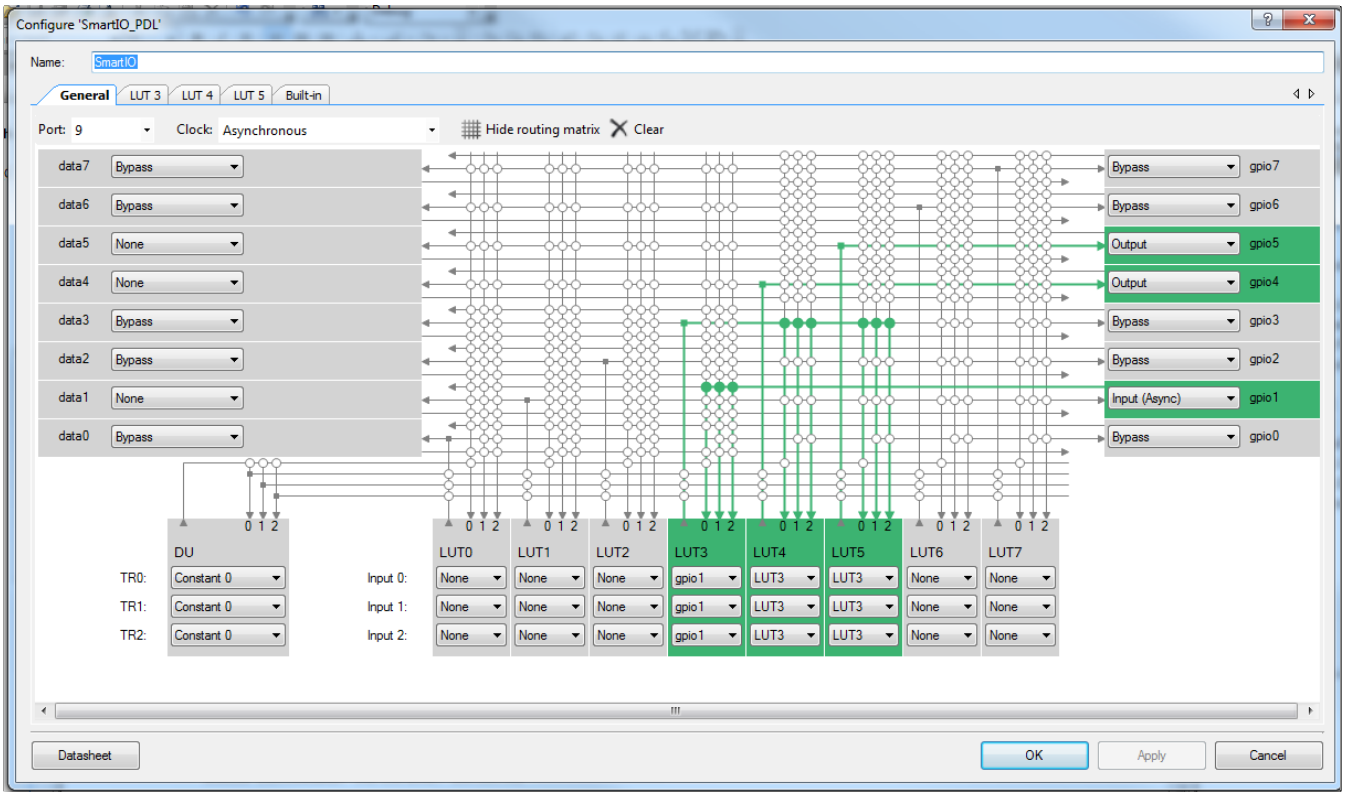


Figure 3 shows the LUT configurations. Only combinatorial elements are used and the block is operational in Deep Sleep mode.

LUT 3 accepts gpio1as input. The LUT 3 configuration performs a buffering operation on the input signal on gpio1 pin. LUT 4 and LUT 5 perform the buffering operation on the LUT 3 output. The output of LUT 4 and LUT 5 are brought out to gpio4 and gpio5 outputs, respectively.

Figure 3. Smart IO LUT Configuration

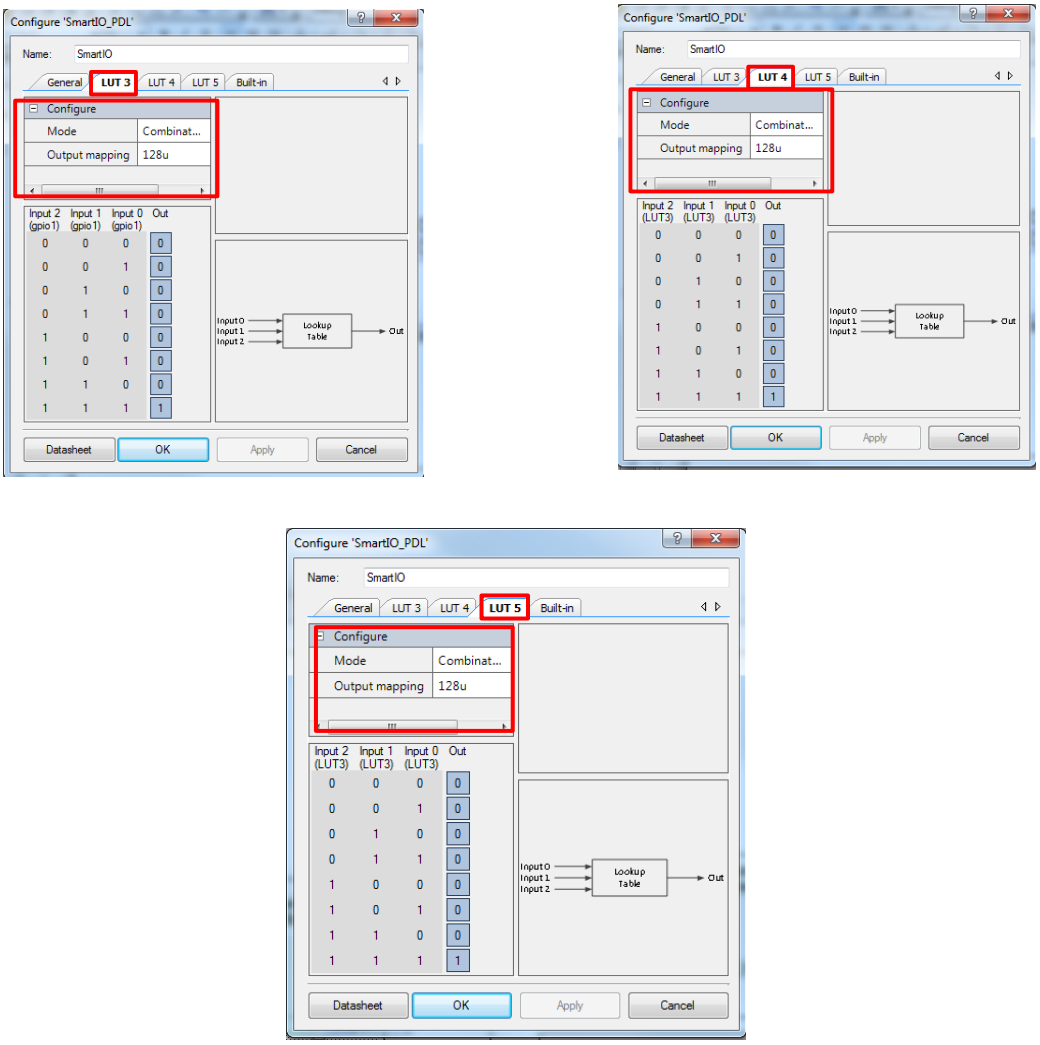


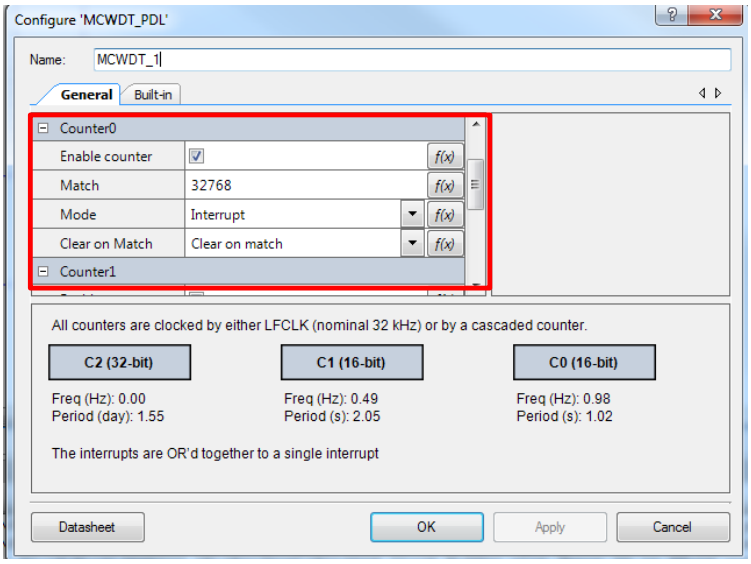
Table 2 shows the configuration settings for the device pins used in this example.

Table 2. Pin Configurations

Pin Name	Device Pin Mapping	Type	Drive Mode	Interrupt
InPin	P9[1]	Input	High Impedance Digital	None
Trigger	P0[4]	Input	Resistive Pull Up	None
Output0	P9[5]	Output	Strong Drive	-
Output1	P9[4]	Output	Strong Drive	-
StatusPin	P1[1]	Output	Strong Drive	-

Configure the MCWDT to generate an interrupt every 1 second as shown in Figure 4.

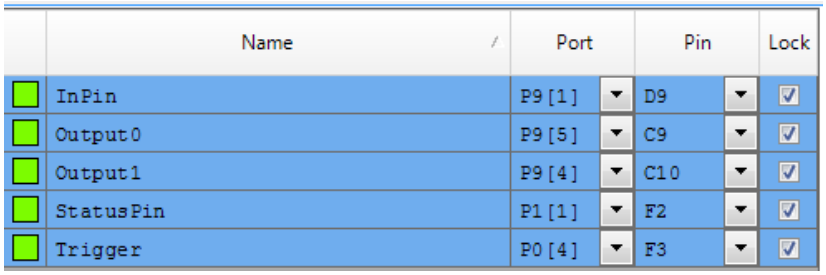
Figure 4. MCWDT Configuration



Design-Wide Resources

Figure 5 shows the pin assignments for the CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit.

Figure 5. Device Pin Assignments



Related Documents

Application Notes	
AN210781 Getting Started with PSoC 6 MCU with Bluetooth Low Energy (BLE) Connectivity	Describes the PSoC 6 MCU with BLE and how to build your first PSoC Creator Project.
PSoC Creator Component Datasheets	
Smart IO	Supports Smart IO peripheral
Pins	Supports connection of hardware resources to physical pins
Global Signal Reference	Supports global interrupt signals
Interrupt	Supports connection of interrupts to peripherals
Device Documentation	
PSoC 6 MCU: PSoC 63 with BLE Datasheet	PSoC 6 MCU: PSoC 63 with BLE Architecture Technical Reference Manual
Development Kit (DVK) Documentation	
CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit	

Document History

Document Title: CE219506 - PSoC 6 MCU Clock Buffer with Smart IO

Document Number: 002-19506

Revision	ECN	Orig. of Change	Submission Date	Description of Change
*B	5857349	VKVK	08/18/2017	Initial public release
*C	6001025	VKVK	12/22/2017	Updated for PSoC Creator 4.2

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Videos | Blogs | Training | Components

Technical Support

cypress.com/support

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709