

C164SV

16-Bit Single-Chip Microcontroller

16bit

Microcontrollers



Never stop thinking.

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16-Bit Single-Chip Microcontroller

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Previous Version: ---

Page	Subjects (major changes since last revision)

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16-Bit Single-Chip Microcontroller C166 Family

C164SV

C164SV

- High Performance 16-bit CPU with 4-Stage Pipeline
 - 80 ns Instruction Cycle Time at 25 MHz CPU Clock
 - 400 ns Multiplication (16×16 bit), 800 ns Division ($32 / 16$ bit)
 - Enhanced Boolean Bit Manipulation Facilities
 - Additional Instructions to Support HLL and Operating Systems
 - Register-Based Design with Multiple Variable Register Banks
 - Single-Cycle Context Switching Support
 - 16 Mbytes Total Linear Address Space for Code and Data
 - 1024 Bytes On-Chip Special Function Register Area
- 16-Priority-Level Interrupt System with 32 Sources, Sample-Rate down to 40 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- Clock Generation via on-chip PLL (factors 1:1.5/2/2.5/3/4/5), via prescaler or via direct clock input
- On-Chip Memory Modules
 - 1 Kbyte On-Chip Internal RAM (IRAM)
 - 16 Kbytes On-Chip Program Mask ROM
- On-Chip Peripheral Modules
 - 8-Channel 10-bit/12-bit A/D Converter with Programmable Conversion Time down to $7.8 \mu\text{s}$ (10-bit) or $10.9 \mu\text{s}$ (12-bit)
 - 12-Channel General Purpose Capture/Compare Unit (CAPCOM2)
 - Capture/Compare Unit for flexible PWM Signal Generation (CAPCOM6) (3/6 Capture/Compare Channels and 1 Compare Channel)
 - Multi-Functional General Purpose Timer Unit with 3 Timers
 - Synchronous/Asynchronous Serial Channel (ASC)
 - High-Speed Synchronous Serial Channel (SSC)
 - On-Chip Real Time Clock
- Up to 64 Kbytes External Address Space for Code and Data
 - Programmable External Bus Characteristics for Different Address Ranges
 - Multiplexed External Address/Data Bus with
 - 8-Bit Data Bus Width (2 Kbytes Address Space, A10 ... A0, Serial Interfaces)
 - 16-Bit Data Bus Width (64 Kbytes Address Space, A15 ... A0)
- Idle, Sleep, and Power Down Modes with Flexible Power Management
- Programmable Watchdog Timer and Oscillator Watchdog
- Up to 50 General Purpose I/O Lines
- Supported by a Large Range of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards

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- On-Chip Bootstrap Loader
- 64-Pin TQFP Package, 0.5 mm pitch

This document describes several derivatives of the C164 group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

Table 1 C164SV Derivative Synopsis

Derivative ¹⁾	Program Memory	CAPCOM6	CAN Interf.	Operating Frequency
SAK-C164SV-2RF SAF-C164SV-2RF	16 Kbytes ROM	Full function	---	20 MHz
SAK-C164SV-2R25F SAF-C164SV-2R25F	16 Kbytes ROM	Full function	---	25 MHz

¹⁾ This Data Sheet is valid for devices starting with and including design step AA.

For simplicity all versions are referred to by the term **C164SV** throughout this document.

Note: The C164SV is compatible (pin-compatible and function-compatible) with the C164SM with reduced memory areas.

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Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the C164SV please refer to the “**Product Catalog Microcontrollers**”, which summarizes all available microcontroller variants.

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.

Introduction

The C164SV derivatives of the Infineon C166 Family of full featured single-chip CMOS microcontrollers are especially suited for cost sensitive applications. They combine high CPU performance (up to 12.5 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. They also provide clock generation via PLL and various on-chip memory modules such as program ROM and internal RAM.

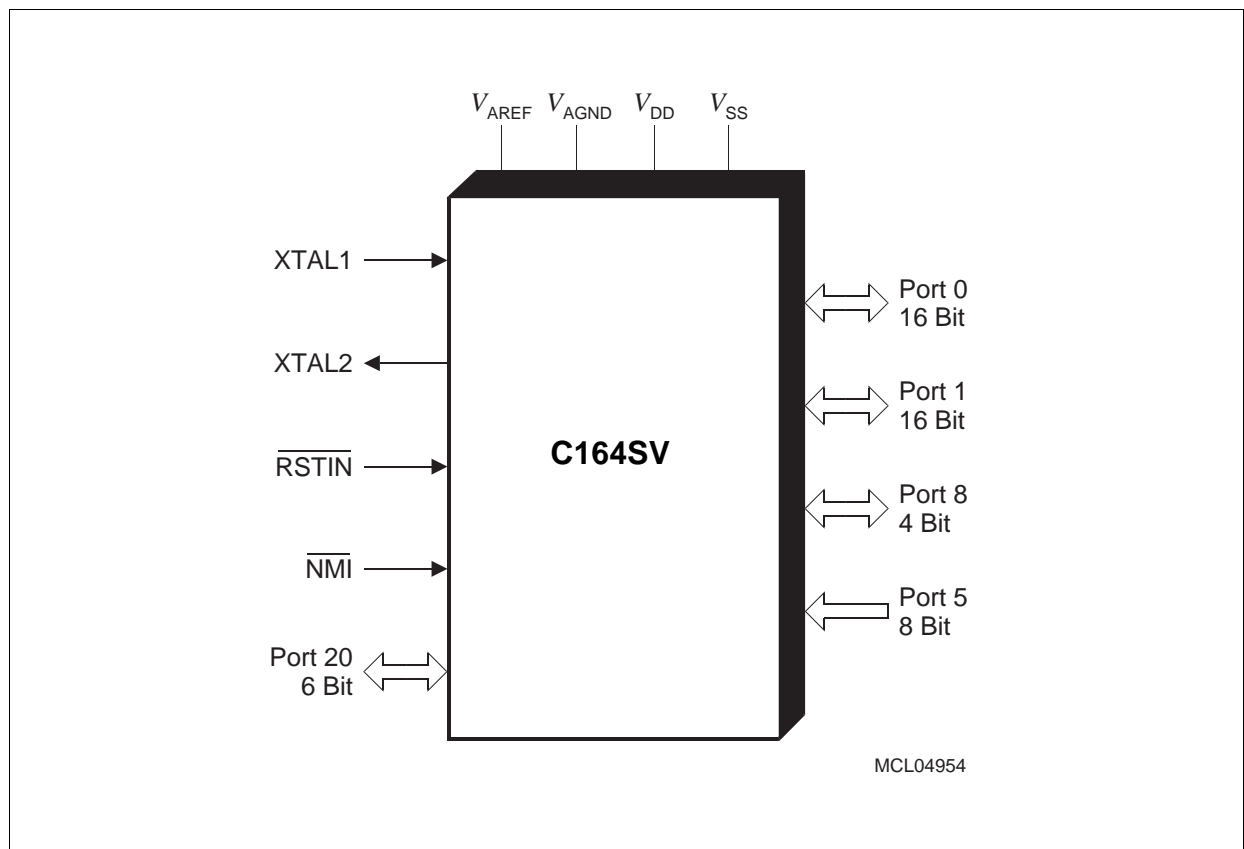


Figure 1 Logic Symbol

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Pin Configuration

(top view)

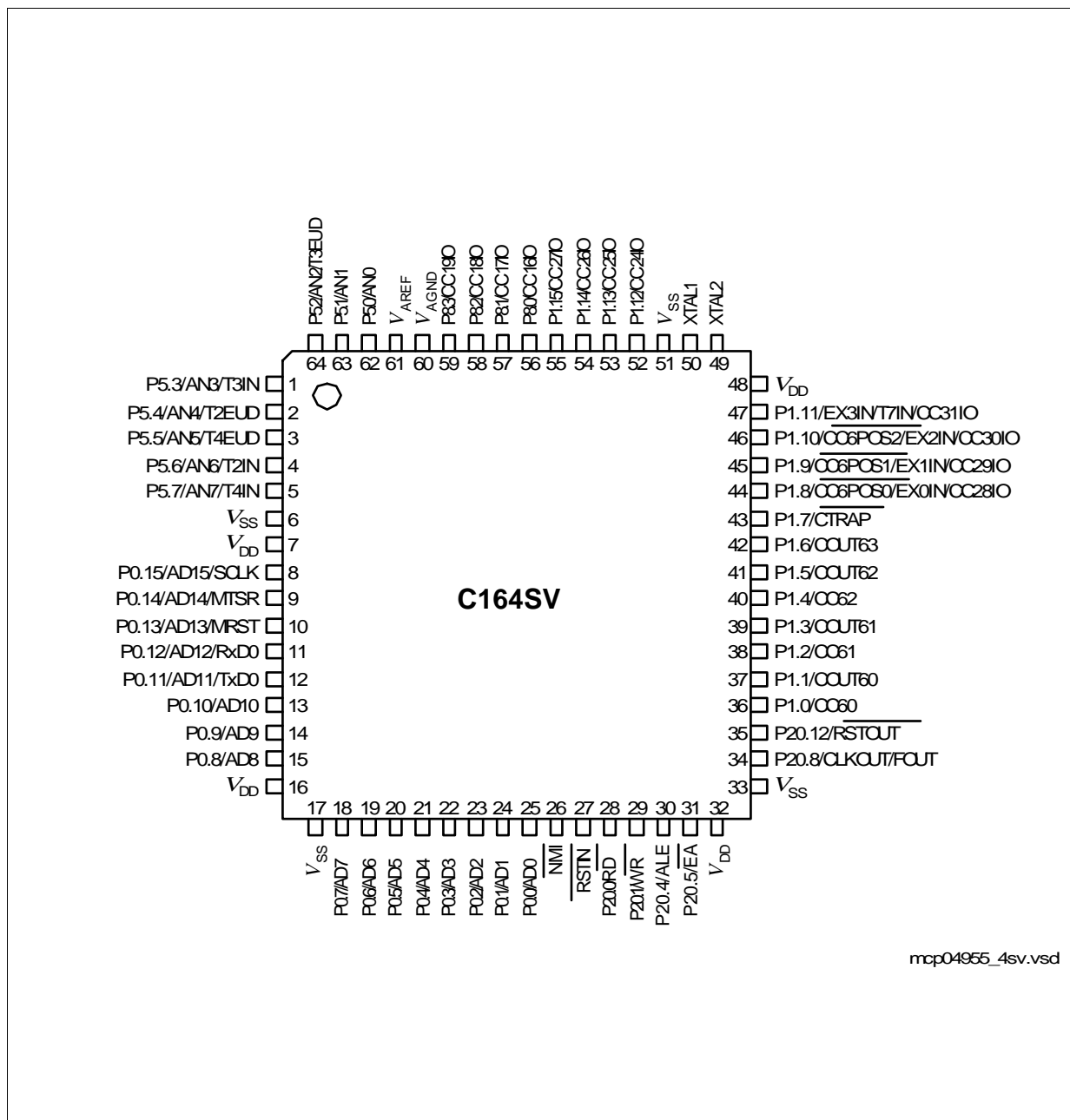


Figure 2

Table 2 on the pages below lists the possible assignments.

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Table 2 Pin Definitions and Functions

Symbol	Pin No.	Input Outp.	Function
PORT0		IO	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes.
P0H.7	8	(I)/O	A(D)15 Most Significant Address(/Data) Line
		I/O	SCLK SSC Master Clock Output / Slave Clock Input.
P0H.6	9	(I)/O	A(D)14 Address(/Data) Line
		I/O	MTRSR SSC Master-Transmit/Slave-Receive Outp./Inp.
P0H.5	10	(I)/O	A(D)13 Address(/Data) Line
		I/O	MRST SSC Master-Receive/Slave-Transmit Inp./Outp.
P0H.4	11	(I)/O	A(D)12 Address(/Data) Line
		I/O	RxD0 ASC0 Data Input (Async.) or Inp./Outp. (Sync.)
P0H.3	12	(I)/O	A(D)11 Address(/Data) Line
		O	TxD0 ASC0 Clock/Data Output (Async./Sync.)
P0H.2	13	(I)/O	A(D)10 Address(/Data) Line
P0H.1	14	(I)/O	A(D)9 Address(/Data) Line
P0H.0	15	(I)/O	A(D)8 Address(/Data) Line
P0L.7	18	I/O	AD7 Address/Data Line
P0L.6	19	I/O	AD6 Address/Data Line
P0L.5	20	I/O	AD5 Address/Data Line
P0L.4	21	I/O	AD4 Address/Data Line
P0L.3	22	I/O	AD3 Address/Data Line
P0L.2	23	I/O	AD2 Address/Data Line
P0L.1	24	I/O	AD1 Address/Data Line
P0L.0	25	I/O	AD0 Least Significant Address/Data Line
NMI	26	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the <u>NMI</u> pin must be <u>low</u> in order to force the C164SV into power down mode. If <u>NMI</u> is high, when PWRDN is executed, the part will <u>continue</u> to run in normal mode. If not used, pin <u>NMI</u> should be pulled high externally.

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Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function
$\overline{\text{RSTIN}}$	27	I/O	<p>Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the C164SV. An internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.</p> <p>A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles.</p> <p>In bidirectional reset mode (<u>enabled</u> by setting bit BDRSTEN in register SYSCON) the $\overline{\text{RSTIN}}$ line is internally pulled low for the duration of the internal reset sequence upon any reset (HW, SW, WDT). See note below this table.</p> <p><i>Note: To let the reset configuration of PORT0 settle and to let the PLL lock a reset duration of ca. 1 ms is recommended.</i></p>

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Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function
P20		IO	Port 20 is a 6-bit bidirectional I/O port (no P20.5 output driver in the OTP versions). It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state.
			The following Port 20 pins also serve for alternate functions:
P20.0	28	O	\overline{RD} External Memory Read Strobe, activated for every external instruction or data read access.
P20.1	29	O	\overline{WR} External Memory Write Strobe, activated for every external data write access.
P20.4	30	O	ALE Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
P20.5	31	I	\overline{EA} External Access Enable pin. A low level at this pin during and after Reset forces the C164SV to latch the configuration from PORT0 and pin \overline{RD} , and to begin instruction execution out of external memory. A high level forces the C164SV to latch the configuration from pins \overline{RD} , ALE, and \overline{WR} , and to begin instruction execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.
P20.8	34	O	CLKOUT System Clock Output (= CPU Clock),
		O	\overline{FOUT} Programmable Frequency Output
P20.12	35	O	\overline{RSTOUT} Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. \overline{RSTOUT} remains low until the EINIT (end of initialization) instruction is executed.

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Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function
PORT1		IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. The following PORT1 pins also serve for alt. functions:
P1L.0	36	I/O	CC60 CAPCOM6: Input / Output of Channel 0
P1L.1	37	O	COUT60 CAPCOM6: Output of Channel 0
P1L.2	38	I/O	CC61 CAPCOM6: Input / Output of Channel 1
P1L.3	39	O	COUT61 CAPCOM6: Output of Channel 1
P1L.4	40	I/O	CC62 CAPCOM6: Input / Output of Channel 2
P1L.5	41	O	COUT62 CAPCOM6: Output of Channel 2
P1L.6	42	O	COUT63 Output of 10-bit Compare Channel
P1L.7	43	I	<u>CTRAP</u> CAPCOM6: Trap Input CTRAP is an input pin with an internal pullup resistor. A low level on this pin switches the CAPCOM6 compare outputs to the logic level defined by software (if enabled).
P1H.0	44	I	<u>CC6POS0</u> CAPCOM6: Position 0 Input,
		I	EX0IN Fast External Interrupt 0 Input,
		I/O	<u>CC28IO</u> CAPCOM2: CC28 Capture Inp./Compare Outp.
P1H.1	45	I	<u>CC6POS1</u> CAPCOM6: Position 1 Input,
		I	EX1IN Fast External Interrupt 1 Input,
		I/O	<u>CC29IO</u> CAPCOM2: CC29 Capture Inp./Compare Outp.
P1H.2	46	I	<u>CC6POS2</u> CAPCOM6: Position 2 Input,
		I	EX2IN Fast External Interrupt 2 Input,
		I/O	<u>CC30IO</u> CAPCOM2: CC30 Capture Inp./Compare Outp.
P1H.3	47	I	EX3IN Fast External Interrupt 3 Input,
		I	T7IN CAPCOM2: Timer T7 Count Input,
		I/O	<u>CC31IO</u> CAPCOM2: CC31 Capture Inp./Compare Outp.
P1H.4	52	I/O	CC24IO CAPCOM2: CC24 Capture Inp./Compare Outp.
P1H.5	53	I/O	CC25IO CAPCOM2: CC25 Capture Inp./Compare Outp.
P1H.6	54	I/O	CC26IO CAPCOM2: CC26 Capture Inp./Compare Outp.
P1H.7	55	I/O	CC27IO CAPCOM2: CC27 Capture Inp./Compare Outp.
XTAL2	49	O	XTAL2: Output of the oscillator amplifier circuit.
XTAL1	50	I	XTAL1: Input to the oscillator amplifier and input to the internal clock generator To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.

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Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function
P8		IO	Port 8 is a 4-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 8 outputs can be configured as push/pull or open drain drivers. The following Port 8 pins also serve for alternate functions:
P8.0	56	I/O	CC16IO CAPCOM2: CC16 Capture Inp./Compare Outp.
P8.1	57	I/O	CC17IO CAPCOM2: CC17 Capture Inp./Compare Outp.
P8.2	58	I/O	CC18IO CAPCOM2: CC18 Capture Inp./Compare Outp.
P8.3	59	I/O	CC19IO CAPCOM2: CC19 Capture Inp./Compare Outp.
P5		I	Port 5 is an 8-bit input-only port with Schmitt-Trigger characteristic. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:
P5.0	62	I	AN0
P5.1	63	I	AN1
P5.2	64	I	AN2, T3EUD GPT1 Timer T3 Ext. Up/Down Ctrl. Inp.
P5.3	1	I	AN3, T3IN GPT1 Timer T3 Count Input
P5.4	2	I	AN4, T2EUD GPT1 Timer T5 Ext. Up/Down Ctrl. Inp.
P5.5	3	I	AN5, T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.6	4	I	AN6, T2IN GPT1 Timer T2 Count Input
P5.7	5	I	AN7, T4IN GPT1 Timer T4 Count Input
V _{AGND}	60	–	Reference ground for the A/D converter.
V _{AREF}	61	–	Reference voltage for the A/D converter.
V _{DD}	7, 16, 32, 48	–	Digital Supply Voltage: +5 V during normal operation and idle mode. ≥2.5 V during power down mode.
V _{SS}	6, 17, 33, 51	–	Digital Ground.

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Note: The following behavior differences must be observed when the bidirectional reset is active:

- Bit BDRSTEN in register SYSCON cannot be changed after EINIT and is cleared automatically after a reset.
- The reset indication flags always indicate a long hardware reset.
- The PORT0 configuration is treated as if it were a hardware reset. In particular, the bootstrap loader may be activated when P0L.4 is low.
- Pin $\overline{\text{RSTIN}}$ may only be connected to external reset devices with an open drain output driver.
- A short hardware reset is extended to the duration of the internal reset sequence.

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Functional Description

The architecture of the C164SV combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. In addition the on-chip memory blocks allow the design of compact systems with maximum performance.

The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the C164SV.

Note: All time specifications refer to a CPU clock of 25 MHz (see definition in the AC Characteristics section).

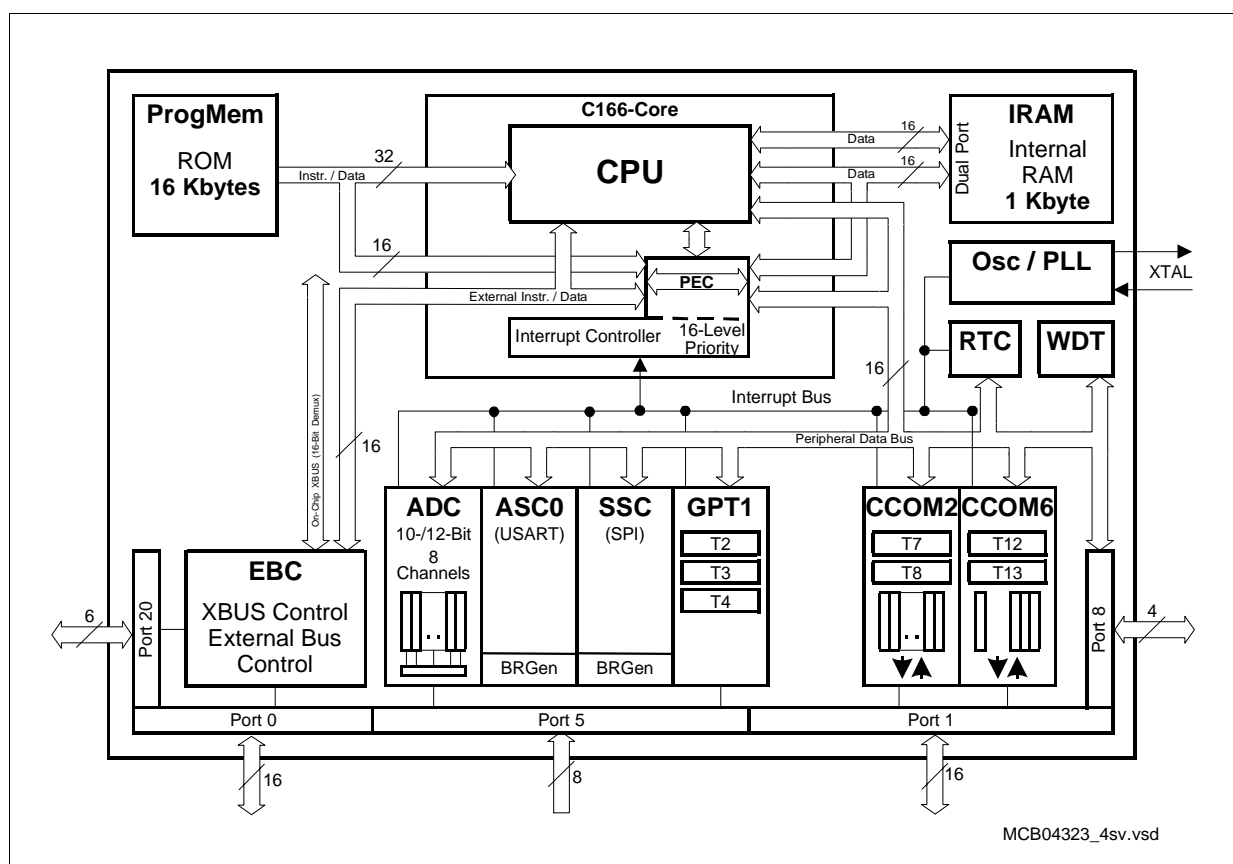


Figure 3 Block Diagram

The program memory, the internal RAM (IRAM) and the set of generic peripherals are connected to the CPU via separate buses. A fourth bus, the XBUS, connects external resources as well as additional on-chip resources, the X-Peripherals (see Figure 3).

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Memory Organization

The memory space of the C164SV is configured in a Von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which includes 16 Mbytes. The entire memory space can be accessed bitwise or wordwise. Particular portions of the on-chip memory have additionally been made directly bitaddressable.

The C164SV incorporates 16 Kbytes of on-chip mask-programmable ROM (not in the ROM-less derivative, of course) for code or constant data. The on-chip ROM can be mapped either to segment 0 or segment 1.

1 Kbyte of on-chip Internal RAM (IRAM) is provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 wordwise (R0 to R15) and/or bitwise (RL0, RH0, ..., RL7, RH7) so-called General Purpose Registers (GPRs).

1024 bytes (2×512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwise registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the C166 Family.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 64 Kbytes of external RAM and/or ROM can be connected to the microcontroller.

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External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of two different external memory access modes, which are as follows:

- 16-bit Addresses, 16-bit Data, Multiplexed
- 11-bit Addresses, 8-bit Data, Multiplexed

Both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.

In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.

Note: The programmable bus features and the window mechanism are standard features of the C166 architecture. Due to the C164SV's limited external address space, however, they can be utilized only to a small extent.

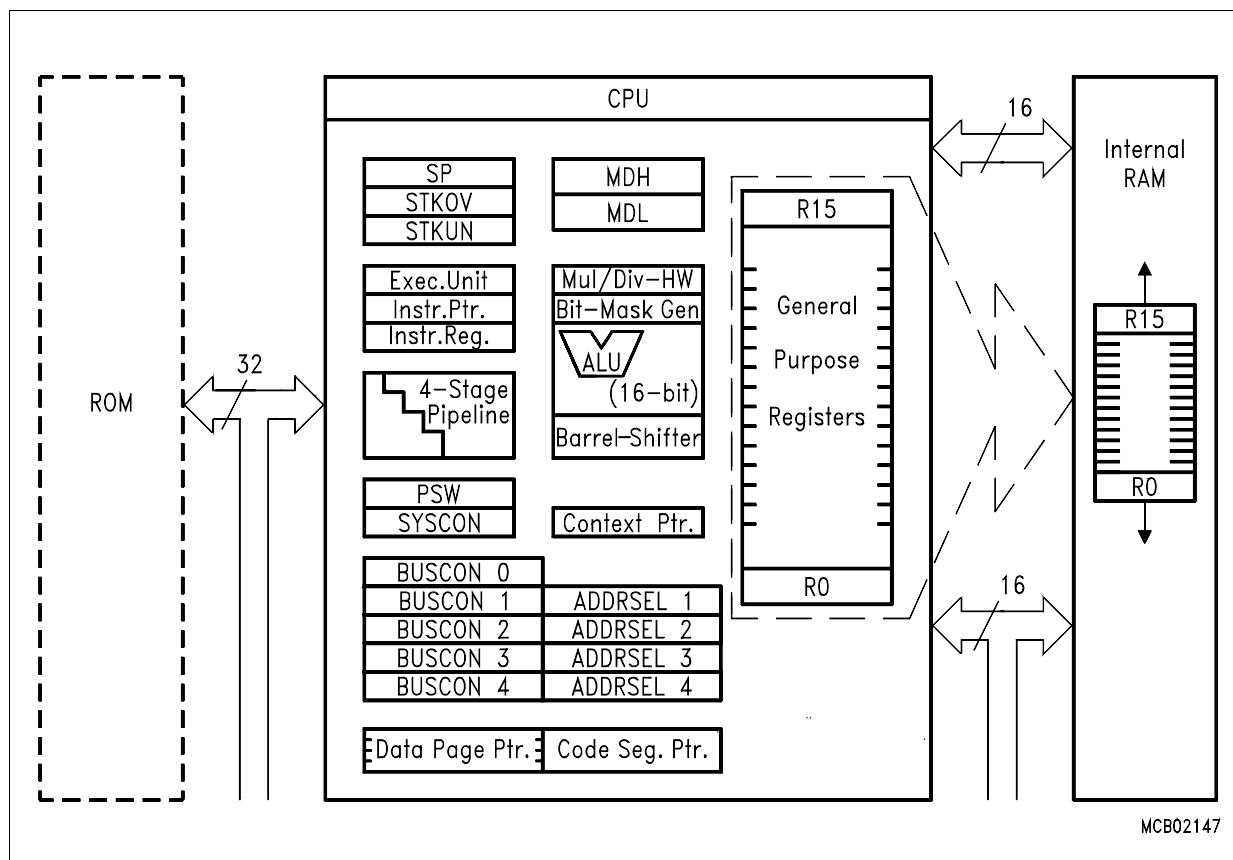
The C164SV will preferably be used in single-chip mode. Applications which require access to external resources such as peripherals or small memories, will use the 8-bit data bus with 11-bit address bus in most cases. In this case the upper pins of PORT0 can be used for the serial interfaces. If a wider address or a 16-bit data bus is required the serial interfaces cannot be used.

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Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the C164SV's instructions can be executed in just one machine cycle which requires 2 CPU clocks (4 TCL). For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16×16 bit multiplication in 5 cycles and a 32-/16-bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', reduces the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.



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Figure 4 CPU Block Diagram

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The CPU has a register context consisting of up to 16 wordwide GPRs at its disposal. These 16 GPRs are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 512 words is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient C164SV instruction set which includes the following instruction classes:

- Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

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Interrupt System

With an interrupt response time within a range from just 5 to 12 CPU clocks (in case of internal program execution), the C164SV is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the C164SV supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C164SV has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

Table 3 shows all of the possible C164SV interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not used by associated peripherals, may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

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Table 3 C164SV Interrupt Nodes

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
Fast External Interrupt 0	CC8IR	CC8IE	CC8INT	00'0060 _H	18 _H
Fast External Interrupt 1	CC9IR	CC9IE	CC9INT	00'0064 _H	19 _H
Fast External Interrupt 2	CC10IR	CC10IE	CC10INT	00'0068 _H	1A _H
Fast External Interrupt 3	CC11IR	CC11IE	CC11INT	00'006C _H	1B _H
GPT1 Timer 2	T2IR	T2IE	T2INT	00'0088 _H	22 _H
GPT1 Timer 3	T3IR	T3IE	T3INT	00'008C _H	23 _H
GPT1 Timer 4	T4IR	T4IE	T4INT	00'0090 _H	24 _H
A/D Conversion Complete	ADCIR	ADCIE	ADCINT	00'00A0 _H	28 _H
A/D Overrun Error	ADEIR	ADEIE	ADEINT	00'00A4 _H	29 _H
ASC0 Transmit	S0TIR	S0TIE	S0TINT	00'00A8 _H	2A _H
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	00'011C _H	47 _H
ASC0 Receive	S0RIR	S0RIE	S0RINT	00'00AC _H	2B _H
ASC0 Error	S0EIR	S0EIE	S0EINT	00'00B0 _H	2C _H
SSC Transmit	SCTIR	SCTIE	SCTINT	00'00B4 _H	2D _H
SSC Receive	SCRIR	SCRIE	SCRINT	00'00B8 _H	2E _H
SSC Error	SCEIR	SCEIE	SCEINT	00'00BC _H	2F _H
CAPCOM Register 16	CC16IR	CC16IE	CC16INT	00'00C0 _H	30 _H
CAPCOM Register 17	CC17IR	CC17IE	CC17INT	00'00C4 _H	31 _H
CAPCOM Register 18	CC18IR	CC18IE	CC18INT	00'00C8 _H	32 _H
CAPCOM Register 19	CC19IR	CC19IE	CC19INT	00'00CC _H	33 _H
CAPCOM Register 24	CC24IR	CC24IE	CC24INT	00'00E0 _H	38 _H
CAPCOM Register 25	CC25IR	CC25IE	CC25INT	00'00E4 _H	39 _H
CAPCOM Register 26	CC26IR	CC26IE	CC26INT	00'00E8 _H	3A _H
CAPCOM Register 27	CC27IR	CC27IE	CC27INT	00'00EC _H	3B _H
CAPCOM Timer 7	T7IR	T7IE	T7INT	00'00F4 _H	3D _H
CAPCOM Timer 8	T8IR	T8IE	T8INT	00'00F8 _H	3E _H
CAPCOM6 Interrupt	CC6IR	CC6IE	CC6INT	00'00FC _H	3F _H
PLL/OWD and RTC	XP3IR	XP3IE	XP3INT	00'010C _H	43 _H
CAPCOM 6 Timer 12	T12IR	T12IE	T12INT	00'0134 _H	4D _H

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Table 3 C164SV Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM 6 Timer 13	T13IR	T13IE	T13INT	00'0138 _H	4E _H
CAPCOM 6 Emergency	CC6EIR	CC6EIE	CC6EINT	00'013C _H	4F _H
Unassigned node	XP0IR	XP0IE	XP0INT	00'0100 _H	40 _H

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The C164SV also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called 'Hardware Traps'. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 4 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 4 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions: – Hardware Reset – Software Reset – W-dog Timer Overflow	–	RESET RESET RESET	00'0000 _H 00'0000 _H 00'0000 _H	00 _H 00 _H 00 _H	III III III
Class A Hardware Traps: – Non-Maskable Interrupt – Stack Overflow – Stack Underflow	NMI STKOF STKUF	NMITRAP STOTRAP STUTRAP	00'0008 _H 00'0010 _H 00'0018 _H	02 _H 04 _H 06 _H	II II II
Class B Hardware Traps: – Undefined Opcode – Protected Instruction Fault – Illegal Word Operand Access – Illegal Instruction Access – Illegal External Bus Access	UNDOPC PRTFLT ILLOPA ILLINA ILLBUS	BTRAP BTRAP BTRAP BTRAP BTRAP	00'0028 _H 00'0028 _H 00'0028 _H 00'0028 _H 00'0028 _H	0A _H 0A _H 0A _H 0A _H 0A _H	I I I I I
Reserved	–	–	[2C _H – 3C _H]	[0B _H – 0F _H]	–
Software Traps – TRAP Instruction	–	–	Any [00'0000 _H – 00'01FC _H] in steps of 4 _H	Any [00 _H – 7F _H]	Current CPU Priority

Preliminary

The Capture/Compare Unit CAPCOM2

The general purpose CAPCOM2 unit supports generation and control of timing sequences on up to 12 channels with a maximum resolution of 16 TCL. The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Two 16-bit timers (T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

Each dual purpose capture/compare register, which may be individually allocated to either CAPCOM timer and programmed for capture or compare function, has one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('capture'd) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event. The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers. When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

Table 5 Compare Modes (CAPCOM)

Compare Modes	Function
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated
Mode 3	Pin set '1' on match; pin reset '0' on compare time overflow; only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match; several compare events per timer period are possible. Registers CC16 & CC24 → pin CC16IO Registers CC17 & CC25 → pin CC17IO Registers CC18 & CC26 → pin CC18IO Registers CC19 & CC27 → pin CC19IO

Preliminary

The Capture/Compare Unit CAPCOM6

The CAPCOM6 unit supports generation and control of timing sequences on up to three 16-bit capture/compare channels plus one 10-bit compare channel.

In compare mode the CAPCOM6 unit provides two output signals per channel which have inverted polarity and non-overlapping pulse transitions. The compare channel can generate a single PWM output signal and is further used to modulate the capture/compare output signals.

In capture mode the contents of compare timer 12 is stored in the capture registers upon a signal transition at pins CCx.

Compare timers T12 (16-bit) and T13 (10-bit) are free running timers which are clocked by the prescaled CPU clock.

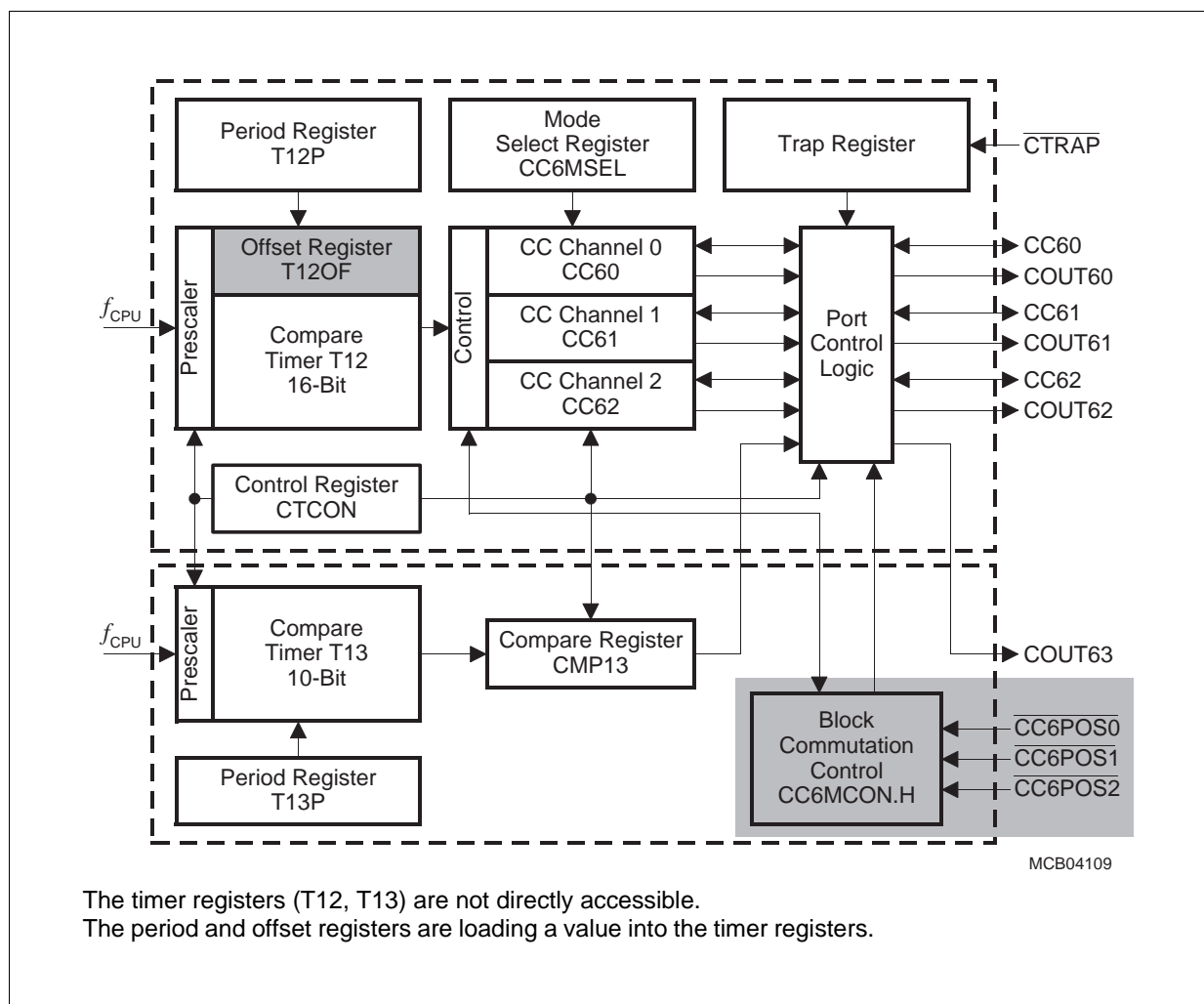


Figure 5 CAPCOM6 Block Diagram

For motor control applications both subunits may generate versatile multichannel PWM signals which are basically either controlled by compare timer 12 or by a typical hall sensor pattern at the interrupt inputs (block commutation).

Preliminary

General Purpose Timer (GPT) Unit

The GPT unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT unit incorporates three 16-bit timers. Each timer may operate independently in a number of different modes, or may be concatenated with another timer.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 16 TCL.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL.

Preliminary

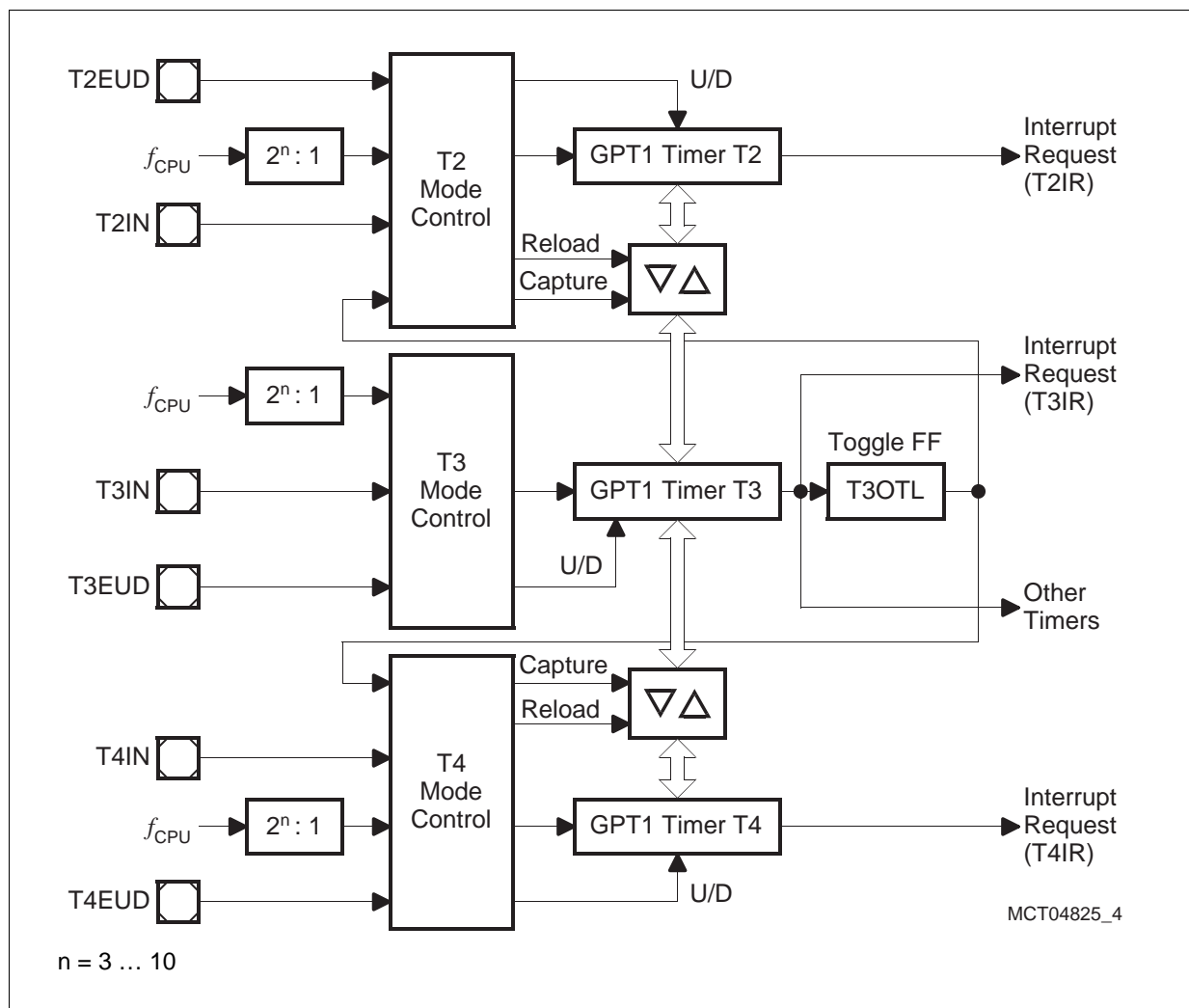


Figure 6 Block Diagram of GPT1

Preliminary

Real Time Clock

The Real Time Clock (RTC) module of the C164SV consists of a chain of 3 divider blocks, a fixed 8:1 divider, the reloadable 16-bit timer T14, and the 32-bit RTC timer (accessible via registers RTCH and RTCL). The RTC module is directly clocked with the on-chip oscillator frequency divided by 32 via a separate clock driver ($f_{RTC} = f_{OSC}/32$) and is therefore independent from the selected clock generation mode of the C164SV. All timers count up.

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time based interrupt
- 48-bit timer for long term measurements

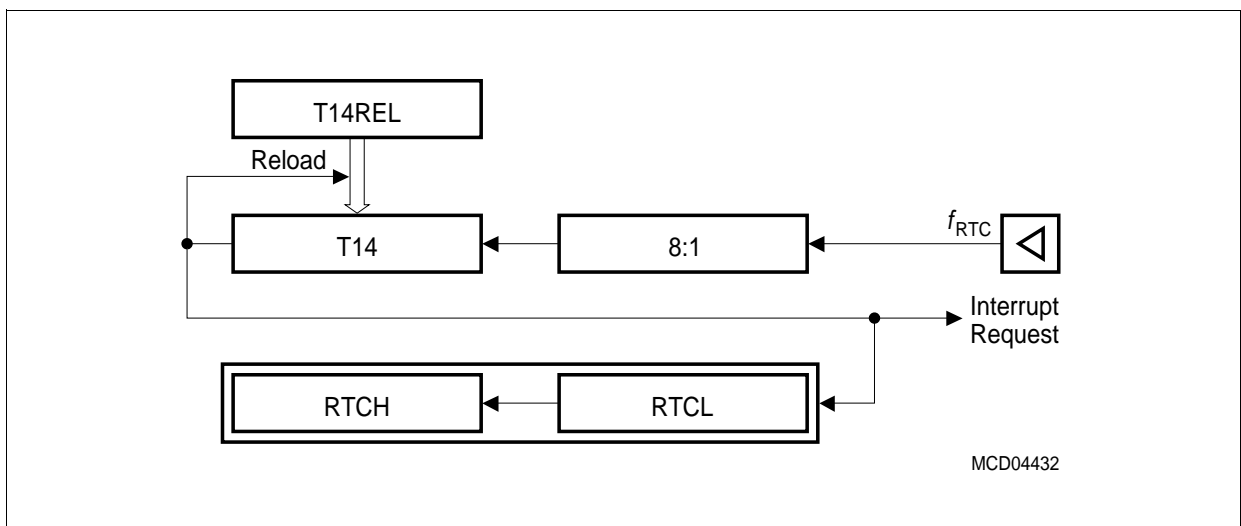


Figure 7 RTC Block Diagram

Note: The registers associated with the RTC are not affected by a reset in order to maintain the correct system time even when intermediate resets are executed.

Preliminary

A/D Converter

For analog signal measurement, a 10-bit/12-bit A/D converter with 8 multiplexed input channels and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation. The sample time (for loading the capacitors) and the conversion time is programmable and can so be adjusted to the external circuitry.

Overrun error detection/protection is provided for the conversion result register (ADDAT): either an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended in such a case until the previous result has been read.

For applications which require less than 8 analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the C164SV supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is sampled once and converted to a digital result. In the Single Channel Continuous mode, the analog level on a specified channel is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels (standard or extension) are sequentially sampled and converted. In the Auto Scan Continuous mode, the number of prespecified channels is repeatedly sampled and converted. In addition, the conversion of a specific channel can be inserted (injected) into a running sequence without disturbing this sequence. This is called Channel Injection Mode.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

After each reset and also during normal operation the ADC automatically performs calibration cycles. This automatic self-calibration constantly adjusts the converter to changing operating conditions (e.g. temperature) and compensates process variations.

These calibration cycles are part of the conversion cycle, so they do not affect the normal operation of the A/D converter.

In order to decouple analog inputs from digital noise and to avoid input trigger noise those pins used for analog input can be disconnected from the digital IO or input stages under software control. This can be selected for each pin separately via register P5DIDIS (Port 5 Digital Input Disable).

Preliminary

Serial Channels

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by two serial interfaces with different functionality, an Asynchronous/Synchronous Serial Channel (**ASC0**) and a High-Speed Synchronous Serial Channel (**SSC**).

The ASC0 is upward compatible with the serial ports of the Infineon 8-bit microcontroller families and supports full-duplex asynchronous communication at up to 781 kbit/s and half-duplex synchronous communication at up to 3.1 Mbit/s (@ 25 MHz CPU clock).

A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling 4 separate interrupt vectors are provided. In asynchronous mode, 8- or 9-bit data frames are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data plus wake up bit mode).

In synchronous mode, the ASC0 transmits or receives bytes (8 bits) synchronously to a shift clock which is generated by the ASC0. The ASC0 always shifts the LSB first. A loop back option is available for testing purposes.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmission or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated, if the last character received has not been read out of the receive buffer register at the time the reception of a new character is complete.

The SSC supports full-duplex synchronous communication at up to 6.25 Mbit/s (@ 25 MHz CPU clock). It may be configured so it interfaces with serially linked peripheral components. A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling 3 separate interrupt vectors are provided.

The SSC transmits or receives characters of 2 ... 16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB and allows the selection of shifting and latching clock edges as well as the clock polarity.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. Transmit and receive error supervise the correct handling of the data buffer. Phase and baudrate error detect incorrect serial data.

Preliminary

Watchdog Timer

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. Thus, the chip's start-up procedure is always monitored. The software has to be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset and pulls the $\overline{\text{RSTOUT}}$ pin low in order to allow external hardware components to be reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided by $2/4/128/256$. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Thus, time intervals between 20 μs and 336 ms can be monitored (@ 25 MHz).

The default Watchdog Timer interval after reset is 5.24 ms (@ 25 MHz).

Parallel Ports

The C164SV provides up to 50 I/O lines which are organized into four input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of Port 8 can be configured (pin by pin) for push/pull operation or open-drain operation via a control register. During the internal reset, all port pins are configured as inputs.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

PORT0 may be used as address and data lines when accessing external memory. Also the serial interfaces ASC0 and SSC use the upper pins of P0H.

Ports P1L, P1H, and P8 are associated with the capture inputs or compare outputs of the CAPCOM units and/or serve as external interrupt inputs.

Port 5 is used for the analog input channels to the A/D converter or timer control signals. Port 20 includes the bus control signals $\overline{\text{RD}}$, $\overline{\text{WR}}$, ALE, the configuration input EA, the the system control output $\overline{\text{RSTOUT}}$, and the system clock output CLKOUT (or the programmable frequency output FOUT).

The edge characteristics (transition time) and driver characteristics (output current) of the C164SV's port drivers can be selected via the Port Output Control registers (POCONx).

Preliminary

Oscillator Watchdog

The Oscillator Watchdog (OWD) monitors the clock signal generated by the on-chip oscillator (either with a crystal or via external clock drive). For this operation the PLL provides a clock signal which is used to supervise transitions on the oscillator clock. This PLL clock is independent from the XTAL1 clock. When the expected oscillator clock transitions are missing the OWD activates the PLL Unlock/OWD interrupt node and supplies the CPU with the PLL clock signal. Under these circumstances the PLL will oscillate with its basic frequency.

In direct drive mode the PLL base frequency is used directly ($f_{\text{CPU}} = 2 \dots 5 \text{ MHz}$).

In prescaler mode the PLL base frequency is divided by 2 ($f_{\text{CPU}} = 1 \dots 2.5 \text{ MHz}$).

Note: The CPU clock source is only switched back to the oscillator clock after a hardware reset.

The oscillator watchdog can be disabled by setting bit OWDDIS in register SYSCON. In this case (OWDDIS = '1') the PLL remains idle and provides no clock signal, while the CPU clock signal is derived directly from the oscillator clock or via prescaler or SDD. Also no interrupt request will be generated in case of a missing oscillator clock.

Note: At the end of a reset bit OWDDIS reflects the inverted level of pin \overline{RD} at that time. Thus the oscillator watchdog may also be disabled via hardware by (externally) pulling the \overline{RD} line low upon a reset, similar to the standard reset configuration via PORT0.

Preliminary

Power Management

The C164SV provides several means to control the power it consumes either at a given time or averaged over a certain timespan. Three mechanisms can be used (partly in parallel):

- **Power Saving Modes** switch the C164SV into a special operating mode (control via instructions).
Idle Mode stops the CPU while the peripherals can continue to operate.
Sleep Mode and Power Down Mode stop all clock signals and all operation (RTC may optionally continue running). Sleep Mode can be terminated by external interrupt signals.
- **Clock Generation Management** controls the distribution and the frequency of internal and external clock signals (control via register SYSCON2).
Slow Down Mode lets the C164SV run at a CPU clock frequency of $f_{OSC}/1 \dots 32$ (half for prescaler operation) which drastically reduces the consumed power. The PLL can be optionally disabled while operating in Slow Down Mode.
External circuitry can be controlled via the programmable frequency output FOUT.
- **Peripheral Management** permits temporary disabling of peripheral modules (control via register SYSCON3).
Each peripheral can separately be disabled/enabled. A group control option disables a major part of the peripheral set by setting one single bit.

The on-chip RTC supports intermittennd operation of the C164SV by generating cyclic wakeup signals. This offers full performance to quickly react on action requests while the intermittennd sleep phases greatly reduce the average power consumption of the system.

Preliminary
Instruction Set Summary

Table 6 lists the instructions of the C164SV in a condensed way.

The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the “**C166 Family Instruction Set Manual**”.

This document also provides a detailed description of each instruction.

Table 6 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16-16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise XOR, (word/byte operands)	2 / 4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL / SHR	Shift left/right direct word GPR	2
ROL / ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2

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Table 6 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
MOV(B)	Move word (byte) data	2 / 4
MOVBS	Move byte operand to word operand with sign extension	2 / 4
MOVBZ	Move byte operand to word operand with zero extension	2 / 4
JMPA, JMPI, JMPR	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
J(N)B	Jump relative if direct bit is (not) set	4
JBC	Jump relative and clear bit if direct bit is set	4
JNBS	Jump relative and set bit if direct bit is not set	4
CALLA, CALLI, CALLR	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH, POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET	Return from intra-segment subroutine	2
RETS	Return from inter-segment subroutine	2
RETP	Return from intra-segment subroutine and pop direct word register from system stack	2
RETI	Return from interrupt service subroutine	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$ -pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT	Disable Watchdog Timer	4
EINIT	Signify End-of-Initialization on $\overline{\text{RSTOUT}}$ -pin	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTENDED Register sequence	2
EXTP(R)	Begin EXTENDED Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTENDED Segment (and Register) sequence	2 / 4
NOP	Null operation	2

Preliminary
Special Function Registers Overview

Table 7 lists all SFRs which are implemented in the C164SV in alphabetical order. The following markings assist in classifying the listed registers:

“b” in the “Name” column marks **Bit-addressable** SFRs.

“E” in the “Physical Address” column marks (**E**)SFRs within the **Extended SFR-Space**.

“m” in the “Physical Address” column marks SFRs without short 8-bit address.

An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Table 7 C164SV Registers, Ordered by Name

Name		Physical Address	8-Bit Addr.	Description	Reset Value
ADCIC	b	FF98 _H	CC _H	A/D Converter End of Conversion Interrupt Control Register	0000 _H
ADCON	b	FFA0 _H	D0 _H	A/D Converter Control Register	0000 _H
ADDAT		FEA0 _H	50 _H	A/D Converter Result Register	0000 _H
ADDAT2		F0A0 _H	E 50 _H	A/D Converter 2 Result Register	0000 _H
ADDRSEL1		FE18 _H	0C _H	Address Select Register 1	0000 _H
ADDRSEL2		FE1A _H	0D _H	Address Select Register 2	0000 _H
ADDRSEL3		FE1C _H	0E _H	Address Select Register 3	0000 _H
ADDRSEL4		FE1E _H	0F _H	Address Select Register 4	0000 _H
ADEIC	b	FF9A _H	CD _H	A/D Converter Overrun Error Interrupt Control Register	0000 _H
BUSCON0	b	FF0C _H	86 _H	Bus Configuration Register 0	0000 _H
BUSCON1	b	FF14 _H	8A _H	Bus Configuration Register 1	0000 _H
BUSCON2	b	FF16 _H	8B _H	Bus Configuration Register 2	0000 _H
BUSCON3	b	FF18 _H	8C _H	Bus Configuration Register 3	0000 _H
BUSCON4	b	FF1A _H	8D _H	Bus Configuration Register 4	0000 _H
CC10IC	b	FF8C _H	C6 _H	External Interrupt 2 Control Register	0000 _H
CC11IC	b	FF8E _H	C7 _H	External Interrupt 3 Control Register	0000 _H
CC16		FE60 _H	30 _H	CAPCOM Register 16	0000 _H
CC16IC	b	F160 _H	E B0 _H	CAPCOM Reg. 16 Interrupt Ctrl. Reg.	0000 _H
CC17		FE62 _H	31 _H	CAPCOM Register 17	0000 _H
CC17IC	b	F162 _H	E B1 _H	CAPCOM Reg. 17 Interrupt Ctrl. Reg.	0000 _H

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Table 7 C164SV Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
CC18	FE64 _H	32 _H	CAPCOM Register 18	0000 _H
CC18IC	b F164 _H	E B2 _H	CAPCOM Reg. 18 Interrupt Ctrl. Reg.	0000 _H
CC19	FE66 _H	33 _H	CAPCOM Register 19	0000 _H
CC19IC	b F166 _H	E B3 _H	CAPCOM Reg. 19 Interrupt Ctrl. Reg.	0000 _H
CC20	FE68 _H	34 _H	CAPCOM Register 20	0000 _H
CC21	FE6A _H	35 _H	CAPCOM Register 21	0000 _H
CC22	FE6C _H	36 _H	CAPCOM Register 22	0000 _H
CC23	FE6E _H	37 _H	CAPCOM Register 23	0000 _H
CC24	FE70 _H	38 _H	CAPCOM Register 24	0000 _H
CC24IC	b F170 _H	E B8 _H	CAPCOM Reg. 24 Interrupt Ctrl. Reg.	0000 _H
CC25	FE72 _H	39 _H	CAPCOM Register 25	0000 _H
CC25IC	b F172 _H	E B9 _H	CAPCOM Reg. 25 Interrupt Ctrl. Reg.	0000 _H
CC26	FE74 _H	3A _H	CAPCOM Register 26	0000 _H
CC26IC	b F174 _H	E BA _H	CAPCOM Reg. 26 Interrupt Ctrl. Reg.	0000 _H
CC27	FE76 _H	3B _H	CAPCOM Register 27	0000 _H
CC27IC	b F176 _H	E BB _H	CAPCOM Reg. 27 Interrupt Ctrl. Reg.	0000 _H
CC28	FE78 _H	3C _H	CAPCOM Register 28	0000 _H
CC29	FE7A _H	3D _H	CAPCOM Register 29	0000 _H
CC30	FE7C _H	3E _H	CAPCOM Register 30	0000 _H
CC31	FE7E _H	3F _H	CAPCOM Register 31	0000 _H
CC60	FE30 _H	18 _H	CAPCOM 6 Register 0	0000 _H
CC61	FE32 _H	19 _H	CAPCOM 6 Register 1	0000 _H
CC62	FE34 _H	1A _H	CAPCOM 6 Register 2	0000 _H
CC6CIC	b F17E _H	E BF _H	CAPCOM 6 Interrupt Control Register	0000 _H
CC6EIC	b F188 _H	E C4 _H	CAPCOM 6 Emergency Interr. Ctrl. Reg.	0000 _H
CC6MCON	b FF32 _H	99 _H	CAPCOM 6 Mode Control Register	00FF _H
CC6MIC	b FF36 _H	9B _H	CAPCOM 6 Mode Interrupt Ctrl. Reg.	0000 _H
CC6MSEL	F036 _H	E 1B _H	CAPCOM 6 Mode Select Register	0000 _H
CC8IC	b FF88 _H	C4 _H	External Interrupt 0 Control Register	0000 _H
CC9IC	b FF8A _H	C5 _H	External Interrupt 1 Control Register	0000 _H

Preliminary
Table 7 C164SV Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
CCM4	b FF22 _H	91 _H	CAPCOM Mode Control Register 4	0000 _H
CCM5	b FF24 _H	92 _H	CAPCOM Mode Control Register 5	0000 _H
CCM6	b FF26 _H	93 _H	CAPCOM Mode Control Register 6	0000 _H
CCM7	b FF28 _H	94 _H	CAPCOM Mode Control Register 7	0000 _H
CMP13	FE36 _H	1B _H	CAPCOM 6 Timer 13 Compare Reg.	0000 _H
CP	FE10 _H	08 _H	CPU Context Pointer Register	FC00 _H
CSP	FE08 _H	04 _H	CPU Code Segment Pointer Register (8 bits, not directly writeable)	0000 _H
CTCON	b FF30 _H	98 _H	CAPCOM 6 Compare Timer Ctrl. Reg.	1010 _H
DP0H	b F102 _H	E 81 _H	P0H Direction Control Register	00 _H
DP0L	b F100 _H	E 80 _H	P0L Direction Control Register	00 _H
DP1H	b F106 _H	E 83 _H	P1H Direction Control Register	00 _H
DP1L	b F104 _H	E 82 _H	P1L Direction Control Register	00 _H
DP20	b FFB6 _H	DB _H	Port 20 Direction Control Register	1000 _H
DP8	b FFD6 _H	EB _H	Port 8 Direction Control Register	00 _H
DPP0	FE00 _H	00 _H	CPU Data Page Pointer 0 Reg. (10 bits)	0000 _H
DPP1	FE02 _H	01 _H	CPU Data Page Pointer 1 Reg. (10 bits)	0001 _H
DPP2	FE04 _H	02 _H	CPU Data Page Pointer 2 Reg. (10 bits)	0002 _H
DPP3	FE06 _H	03 _H	CPU Data Page Pointer 3 Reg. (10 bits)	0003 _H
EXICON	b F1C0 _H	E E0 _H	External Interrupt Control Register	0000 _H
EXISEL	b F1DA _H	E ED _H	External Interrupt Source Select Reg.	0000 _H
FOCON	b FFAA _H	D5 _H	Frequency Output Control Register	0000 _H
IDCHIP	F07C _H	E 3E _H	Identifier	XXXX _H
IDMANUF	F07E _H	E 3F _H	Identifier	1820 _H
IDMEM	F07A _H	E 3D _H	Identifier	X008 _H
IDMEM2	F076 _H	E 3B _H	Identifier	0000 _H
IDPROG	F078 _H	E 3C _H	Identifier	XXXX _H
ISNC	b F1DE _H	E EF _H	Interrupt Subnode Control Register	0000 _H
MDC	b FF0E _H	87 _H	CPU Multiply Divide Control Register	0000 _H
MDH	FE0C _H	06 _H	CPU Multiply Divide Reg. – High Word	0000 _H

Preliminary
Table 7 C164SV Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
MDL	FE0E _H	07 _H	CPU Multiply Divide Reg. – Low Word	0000 _H
ODP8	b F1D6 _H E	EB _H	Port 8 Open Drain Control Register	00 _H
ONES	b FF1E _H	8F _H	Constant Value 1's Register (read only)	FFFF _H
P0H	b FF02 _H	81 _H	Port 0 High Reg. (Upper half of PORT0)	00 _H
P0L	b FF00 _H	80 _H	Port 0 Low Reg. (Lower half of PORT0)	00 _H
P1H	b FF06 _H	83 _H	Port 1 High Reg. (Upper half of PORT1)	00 _H
P1L	b FF04 _H	82 _H	Port 1 Low Reg. (Lower half of PORT1)	00 _H
P20	b FFB4 _H	DA _H	Port 20 Register (6 bits)	0000 _H
P5	b FFA2 _H	D1 _H	Port 5 Register (read only)	XXXX _H
P5DIDIS	b FFA4 _H	D2 _H	Port 5 Digital Input Disable Register	0000 _H
P8	b FFD4 _H	EA _H	Port 8 Register (4 bits)	00 _H
PECC0	FEC0 _H	60 _H	PEC Channel 0 Control Register	0000 _H
PECC1	FEC2 _H	61 _H	PEC Channel 1 Control Register	0000 _H
PECC2	FEC4 _H	62 _H	PEC Channel 2 Control Register	0000 _H
PECC3	FEC6 _H	63 _H	PEC Channel 3 Control Register	0000 _H
PECC4	FEC8 _H	64 _H	PEC Channel 4 Control Register	0000 _H
PECC5	FECA _H	65 _H	PEC Channel 5 Control Register	0000 _H
PECC6	FECC _H	66 _H	PEC Channel 6 Control Register	0000 _H
PECC7	FECE _H	67 _H	PEC Channel 7 Control Register	0000 _H
POCON0H	F082 _H E	41 _H	Port P0H Output Control Register	0011 _H
POCON0L	F080 _H E	40 _H	Port P0L Output Control Register	0011 _H
POCON1H	F086 _H E	43 _H	Port P1H Output Control Register	0011 _H
POCON1L	F084 _H E	42 _H	Port P1L Output Control Register	0011 _H
POCON20	F0AA _H E	55 _H	Port P20 Output Control Register	0000 _H
POCON8	F092 _H E	49 _H	Port P8 Output Control Register	0022 _H
PSW	b FF10 _H	88 _H	CPU Program Status Word	0000 _H
RP0H	b F108 _H E	84 _H	System Startup Config. Reg. (Rd. only)	XX _H
RSTCON	b F1E0 _H m	---	Reset Control Register	00XX _H
RTCH	F0D6 _H E	6B _H	RTC High Register	no
RTCL	F0D4 _H E	6A _H	RTC Low Register	no

Preliminary
Table 7 C164SV Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
S0BG	FEB4 _H	5A _H	Serial Channel 0 Baud Rate Generator Reload Register	0000 _H
S0CON	b FFB0 _H	D8 _H	Serial Channel 0 Control Register	0000 _H
S0EIC	b FF70 _H	B8 _H	Serial Channel 0 Error Interrupt Ctrl. Reg.	0000 _H
S0RBUF	FEB2 _H	59 _H	Serial Channel 0 Receive Buffer Reg. (read only)	XXXX _H
S0RIC	b FF6E _H	B7 _H	Serial Channel 0 Receive Interrupt Control Register	0000 _H
S0TBIC	b F19C _H	E CE _H	Serial Channel 0 Transmit Buffer Interrupt Control Register	0000 _H
S0TBUF	FEB0 _H	58 _H	Serial Channel 0 Transmit Buffer Reg. (write only)	0000 _H
S0TIC	b FF6C _H	B6 _H	Serial Channel 0 Transmit Interrupt Control Register	0000 _H
SP	FE12 _H	09 _H	CPU System Stack Pointer Register	FC00 _H
SSCBR	F0B4 _H	E 5A _H	SSC Baudrate Register	0000 _H
SSCON	b FFB2 _H	D9 _H	SSC Control Register	0000 _H
SSCEIC	b FF76 _H	BB _H	SSC Error Interrupt Control Register	0000 _H
SSCRB	F0B2 _H	E 59 _H	SSC Receive Buffer	XXXX _H
SSCRIC	b FF74 _H	BA _H	SSC Receive Interrupt Control Register	0000 _H
SSCTB	F0B0 _H	E 58 _H	SSC Transmit Buffer	0000 _H
SSCTIC	b FF72 _H	B9 _H	SSC Transmit Interrupt Control Register	0000 _H
STKOV	FE14 _H	0A _H	CPU Stack Overflow Pointer Register	FA00 _H
STKUN	FE16 _H	0B _H	CPU Stack Underflow Pointer Register	FC00 _H
SYSCON	b FF12 _H	89 _H	CPU System Configuration Register	¹⁾ 0xx0 _H
SYSCON1	b F1DC _H	E EE _H	CPU System Configuration Register 1	0000 _H
SYSCON2	b F1D0 _H	E E8 _H	CPU System Configuration Register 2	0000 _H
SYSCON3	b F1D4 _H	E EA _H	CPU System Configuration Register 3	0000 _H
T12IC	b F190 _H	E C8 _H	CAPCOM 6 Timer 12 Interrupt Ctrl. Reg.	0000 _H
T12OF	F034 _H	E 1A _H	CAPCOM 6 Timer 12 Offset Register	0000 _H

Preliminary
Table 7 C164SV Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
T12P	F030 _H	E 18 _H	CAPCOM 6 Timer 12 Period Register	0000 _H
T13IC	b F198 _H	E CC _H	CAPCOM 6 Timer 13 Interrupt Ctrl. Reg.	0000 _H
T13P	F032 _H	E 19 _H	CAPCOM 6 Timer 13 Period Register	0000 _H
T14	F0D2 _H	E 69 _H	RTC Timer 14 Register	no
T14REL	F0D0 _H	E 68 _H	RTC Timer 14 Reload Register	no
T2	FE40 _H	20 _H	GPT1 Timer 2 Register	0000 _H
T2CON	b FF40 _H	A0 _H	GPT1 Timer 2 Control Register	0000 _H
T2IC	b FF60 _H	B0 _H	GPT1 Timer 2 Interrupt Control Register	0000 _H
T3	FE42 _H	21 _H	GPT1 Timer 3 Register	0000 _H
T3CON	b FF42 _H	A1 _H	GPT1 Timer 3 Control Register	0000 _H
T3IC	b FF62 _H	B1 _H	GPT1 Timer 3 Interrupt Control Register	0000 _H
T4	FE44 _H	22 _H	GPT1 Timer 4 Register	0000 _H
T4CON	b FF44 _H	A2 _H	GPT1 Timer 4 Control Register	0000 _H
T4IC	b FF64 _H	B2 _H	GPT1 Timer 4 Interrupt Control Register	0000 _H
T7	F050 _H	E 28 _H	CAPCOM Timer 7 Register	0000 _H
T78CON	b FF20 _H	90 _H	CAPCOM Timer 7 and 8 Ctrl. Reg.	0000 _H
T7IC	b F17A _H	E BD _H	CAPCOM Timer 7 Interrupt Ctrl. Reg.	0000 _H
T7REL	F054 _H	E 2A _H	CAPCOM Timer 7 Reload Register	0000 _H
T8	F052 _H	E 29 _H	CAPCOM Timer 8 Register	0000 _H
T8IC	b F17C _H	E BE _H	CAPCOM Timer 8 Interrupt Ctrl. Reg.	0000 _H
T8REL	F056 _H	E 2B _H	CAPCOM Timer 8 Reload Register	0000 _H
TFR	b FFAC _H	D6 _H	Trap Flag Register	0000 _H
TRCON	b FF34 _H	9A _H	CAPCOM 6 Trap Enable Ctrl. Reg.	00XX _H
WDT	FEAE _H	57 _H	Watchdog Timer Register (read only)	0000 _H
WDTCON	FFAE _H	D7 _H	Watchdog Timer Control Register	²⁾ 00xx _H
XP0IC	b F186 _H	E C3 _H	Unassigned Interrupt Control Reg.	0000 _H
XP3IC	b F19E _H	E CF _H	PLL/RTC Interrupt Control Register	0000 _H
ZEROS	b FF1C _H	8E _H	Constant Value 0's Register (read only)	0000 _H

¹⁾ The system configuration is selected during reset.

²⁾ The reset value depends on the indicated reset source.

Preliminary
Absolute Maximum Ratings
Table 8 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	T_{ST}	-65	150	°C	–
Junction temperature	T_J	-40	150	°C	under bias
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	-0.5	6.5	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	$V_{DD} + 0.5$	V	–
Input current on any pin during overload condition	–	-10	10	mA	–
Absolute sum of all input currents during overload condition	–	–	100	mA	–
Power dissipation	P_{DISS}	–	1.5	W	–

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Preliminary
Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the C164SV. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 9 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Digital supply voltage	V_{DD}	4.5	5.5	V	Active mode, $f_{CPUmax} = 25$ MHz
		2.5 ¹⁾	5.5	V	PowerDown mode
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	–	±5	mA	Per pin ²⁾³⁾
Absolute sum of overload currents	$\Sigma I_{OV} $	–	50	mA	³⁾
External Load Capacitance	C_L	–	100	pF	Pin drivers in default mode ⁴⁾
Ambient temperature	T_A	0	70	°C	SAB-C164SV ...
		-40	85	°C	SAF-C164SV ...
		-40	125	°C	SAK-C164SV ...

¹⁾ Output voltages and output currents will be reduced when V_{DD} leaves the range defined for active mode.

²⁾ Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD} + 0.5$ V or $V_{OV} < V_{SS} - 0.5$ V). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltage must remain within the specified limits. Proper operation is not guaranteed if overload conditions occur on functional pins line XTAL1, RD, WR, etc.

³⁾ Not 100% tested, guaranteed by design and characterization.

⁴⁾ The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability (C_L).

Preliminary

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C164SV and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (Controller Characteristics):

The logic of the C164SV will provide signals with the respective characteristics.

SR (System Requirement):

The external system must provide signals with the respective characteristics to the C164SV.

DC Characteristics

(Operating Conditions apply)¹⁾

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Input low voltage (TTL, all except XTAL1)	V_{IL}	SR	-0.5	$0.2 V_{DD} - 0.1$	V	–
Input low voltage XTAL1	V_{IL2}	SR	-0.5	$0.3 V_{DD}$	V	–
Input high voltage (TTL, all except \overline{RSTIN} , XTAL1)	V_{IH}	SR	$0.2 V_{DD} + 0.9$	$V_{DD} + 0.5$	V	–
Input high voltage \overline{RSTIN} (when operated as input)	V_{IH1}	SR	$0.6 V_{DD}$	$V_{DD} + 0.5$	V	–
Input high voltage XTAL1	V_{IH2}	SR	$0.7 V_{DD}$	$V_{DD} + 0.5$	V	–
Output low voltage ²⁾	V_{OL}	CC	–	1.0	V	$I_{OL} \leq I_{OLmax}^{3)}$
			–	0.45	V	$I_{OL} \leq I_{OLnom}^{3)4)}$
Output high voltage ⁵⁾	V_{OH}	CC	$V_{DD} - 1.0$	–	V	$I_{OH} \geq I_{OHmax}^{3)}$
			$V_{DD} - 0.45$	–	V	$I_{OH} \geq I_{OHnom}^{3)4)}$
Input leakage current (Port 5)	I_{OZ1}	CC	–	± 200	nA	$0 V < V_{IN} < V_{DD}$
Input leakage current (all other)	I_{OZ2}	CC	–	± 500	nA	$0.45 V < V_{IN} < V_{DD}$
\overline{RSTIN} inactive current ⁶⁾	$I_{RSTH}^{7)}$		–	-10	μA	$V_{IN} = V_{IH1}$
\overline{RSTIN} active current ⁶⁾	$I_{RSTL}^{8)}$		-100	–	μA	$V_{IN} = V_{IL}$
$\overline{RD}/\overline{WR}$ inact. current ⁹⁾	$I_{RWH}^{7)}$		–	-40	μA	$V_{OUT} = 2.4 V$
$\overline{RD}/\overline{WR}$ active current ⁹⁾	$I_{RWL}^{8)}$		-500	–	μA	$V_{OUT} = V_{OLmax}$

Preliminary
DC Characteristics (cont'd)
 (Operating Conditions apply)¹⁾

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
ALE inactive current ⁹⁾	I_{ALEL} ⁷⁾	–	40	μA	$V_{OUT} = V_{OLmax}$
ALE active current ⁹⁾	I_{ALEH} ⁸⁾	500	–	μA	$V_{OUT} = 2.4 V$
PORT0 configuration current ¹⁰⁾	I_{POH} ⁷⁾	–	-10	μA	$V_{IN} = V_{IHmin}$
	I_{POL} ⁸⁾	-100	–	μA	$V_{IN} = V_{ILmax}$
XTAL1 input current	I_{IL} CC	–	±20	μA	$0 V < V_{IN} < V_{DD}$
Pin capacitance ¹¹⁾ (digital inputs/outputs)	C_{IO} CC	–	10	pF	$f = 1 MHz$ $T_A = 25 °C$

- 1) Keeping signal levels within the levels specified in this table, ensures operation without overload conditions. For signal levels outside these specifications also refer to the specification of the overload current I_{OV} .
- 2) For pin \overline{RSTIN} this specification is only valid in bidirectional reset mode.
- 3) The maximum deliverable output current of a port driver depends on the selected output driver mode, see [Table 10, Current Limits for Port Output Drivers](#). The limit for pin groups must be respected.
- 4) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DD}$). However, only the levels for nominal output currents are guaranteed.
- 5) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.
- 6) These parameters describe the \overline{RSTIN} pullup, which equals a resistance of ca. 50 to 250 kΩ.
- 7) The maximum current may be drawn while the respective signal line remains inactive.
- 8) The minimum current must be drawn in order to drive the respective signal line active.
- 9) This specification is valid during Reset and during Adapt-mode.
- 10) This specification is valid during Reset if required for configuration, and during Adapt-mode.
- 11) Not 100% tested, guaranteed by design and characterization.

Table 10 Current Limits for Port Output Drivers

Port Output Driver Mode	Maximum Output Current (I_{OLmax} , $-I_{OHmax}$) ¹⁾	Nominal Output Current (I_{OLnom} , $-I_{OHnom}$)
Strong driver	10 mA	2.5 mA
Medium driver	4.0 mA	1.0 mA
Weak driver	0.5 mA	0.1 mA

- 1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring port output pins the total output current in each direction (ΣI_{OL} and $\Sigma -I_{OH}$) must remain below 50 mA.

Preliminary
Power Consumption C164SV

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Power supply current (active) with all peripherals active	I_{DD}	–	$1 + 1.8 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IL}$ f_{CPU} in [MHz] ¹⁾
Idle mode supply current with all peripherals active	I_{IDX}	–	$1 + 0.9 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IH1}$ f_{CPU} in [MHz] ¹⁾
Idle mode supply current with all peripherals deactivated, PLL off, SDD factor = 32	I_{IDO} ²⁾	–	$500 + 50 \times f_{OSC}$	μA	$\overline{RSTIN} = V_{IH1}$ f_{OSC} in [MHz] ¹⁾
Sleep and Power-down mode supply current with RTC running	I_{PDR} ²⁾	–	$200 + 25 \times f_{OSC}$	μA	$V_{DD} = V_{DDmax}$ f_{OSC} in [MHz] ³⁾
Sleep and Power-down mode supply current with RTC disabled	I_{PDO}	–	25	μA	$V_{DD} = V_{DDmax}$ ³⁾

1) The supply current is a function of the operating frequency. This dependency is illustrated in [Figure 9](#). These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH} .

2) This parameter is determined mainly by the current consumed by the oscillator (see [Figure 8](#)). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The values given refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

3) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at $V_{DD} - 0.1$ V to V_{DD} , all outputs (including pins configured as outputs) disconnected.

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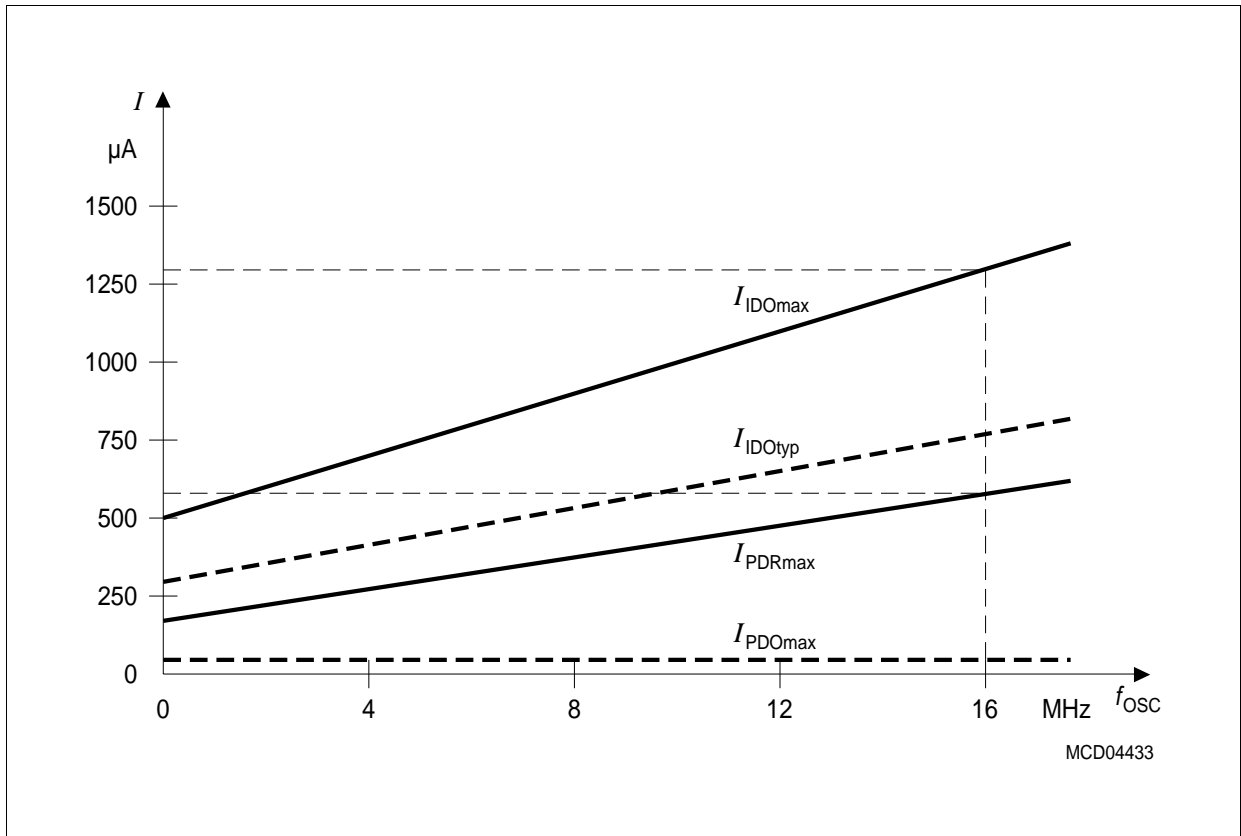


Figure 8 Idle and Power Down Supply Current as a Function of Oscillator Frequency

Preliminary

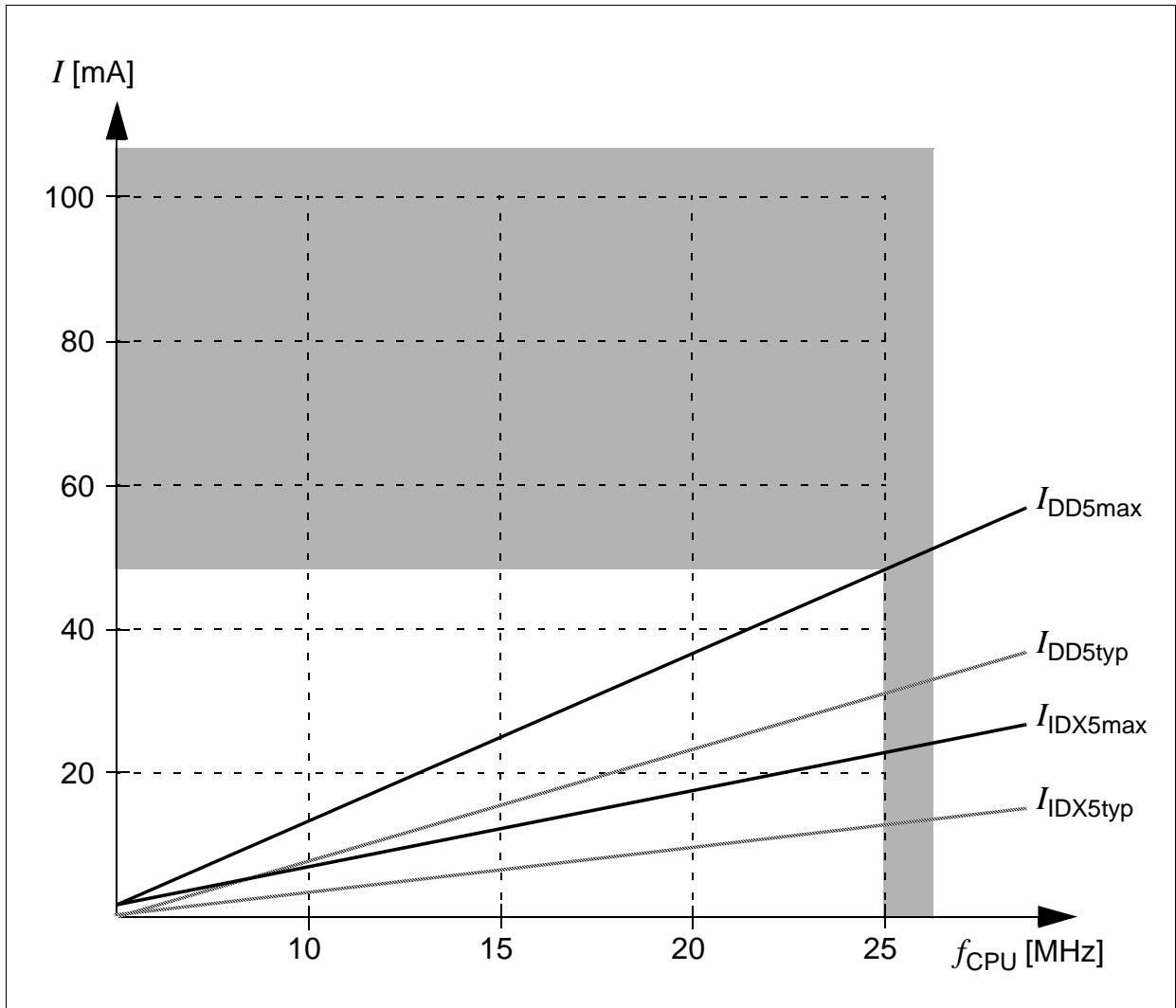


Figure 9 Supply/Idle Current as a Function of Operating Frequency

Preliminary

AC Characteristics

Definition of Internal Timing

The internal operation of the C164SV is controlled by the internal CPU clock f_{CPU} . Both edges of the CPU clock can trigger internal (e.g. pipeline) or external (e.g. bus cycles) operations.

The specification of the external timing (AC Characteristics) therefore depends on the time between two consecutive edges of the CPU clock, called “TCL” (see [Figure 10](#)).

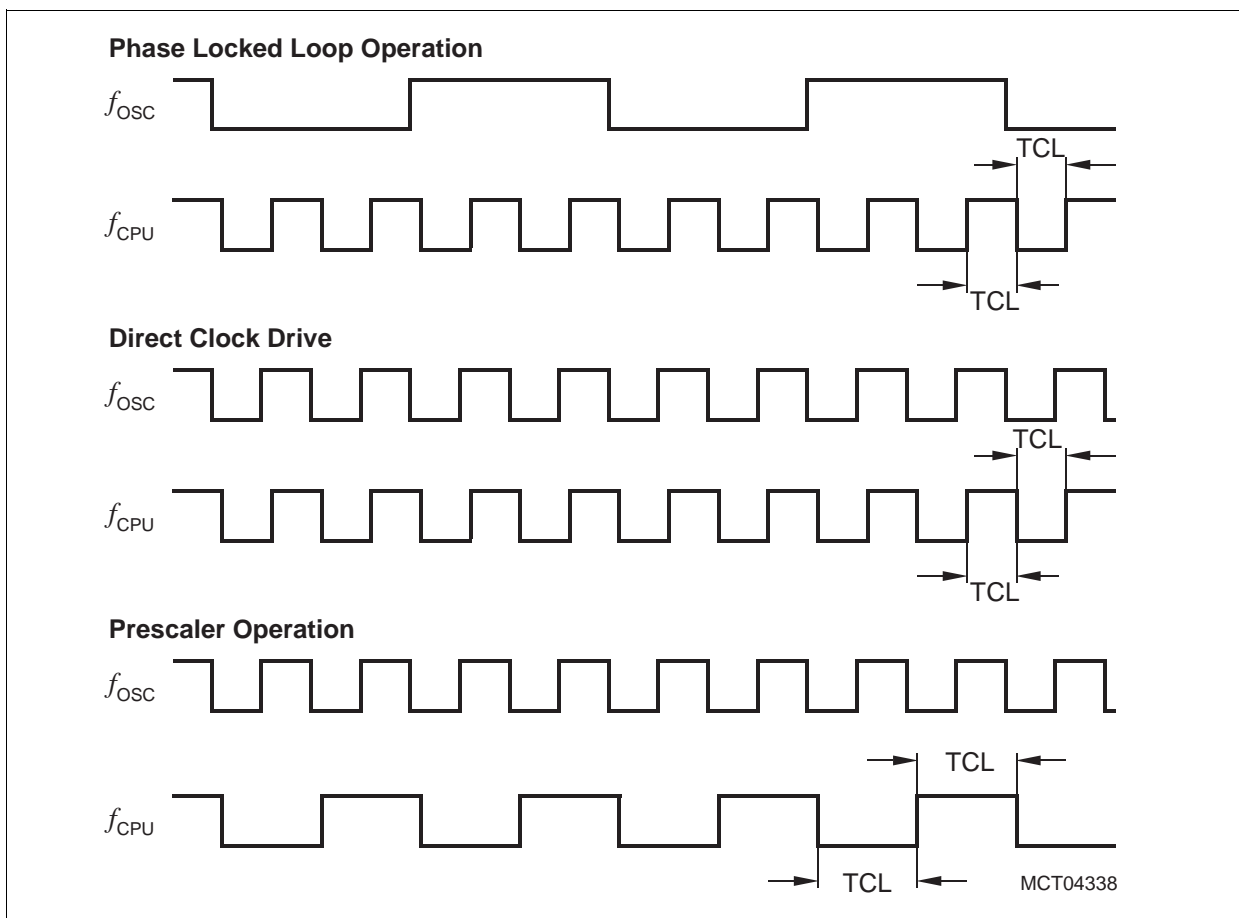


Figure 10 Generation Mechanisms for the CPU Clock

The CPU clock signal f_{CPU} can be generated from the oscillator clock signal f_{OSC} via different mechanisms. The duration of TCLs and their variation (and also the derived external timing) depends on the used mechanism to generate f_{CPU} . This influence must be regarded when calculating the timings for the C164SV.

Note: The example for PLL operation shown in [Figure 10](#) refers to a PLL factor of 4.

The used mechanism to generate the basic CPU clock is selected by bitfield CLKCFG in register RP0H.7-5.

Upon a long hardware reset register RP0H is loaded with the logic levels present on the upper half of PORT0 (P0H), i.e. bitfield CLKCFG represents the logic levels on pins

Preliminary

P0.15-13 (P0H.7-5). Register RP0H can be loaded from the upper half of register RSTCON under software control.

Table 11 associates the combinations of these three bits with the respective clock generation mode.

Table 11 C164SV Clock Generation Modes

CLKCFG ¹⁾ (RP0H.7-5)	CPU Frequency $f_{\text{CPU}} = f_{\text{OSC}} \times F$	External Clock Input Range ²⁾	Notes
1 1 1	$f_{\text{OSC}} \times 4$	2.5 to 6.25 MHz	Default configuration
1 1 0	$f_{\text{OSC}} \times 3$	3.33 to 8.33 MHz	–
1 0 1	$f_{\text{OSC}} \times 2$	5 to 12.5 MHz	–
1 0 0	$f_{\text{OSC}} \times 5$	2 to 5 MHz	–
0 1 1	$f_{\text{OSC}} \times 1$	1 to 25 MHz	Direct drive ³⁾
0 1 0	$f_{\text{OSC}} \times 1.5$	6.66 to 16.66 MHz	–
0 0 1	$f_{\text{OSC}} / 2$	2 to 50 MHz	CPU clock via prescaler
0 0 0	$f_{\text{OSC}} \times 2.5$	4 to 10 MHz	–

¹⁾ Please note that pin P0.15 (corresponding to RP0H.7) is inverted in emulation mode, and thus also in EHM.

²⁾ The external clock input range refers to a CPU clock range of 10 ... 25 MHz.

³⁾ The maximum frequency depends on the duty cycle of the external clock signal.

Prescaler Operation

When prescaler operation is configured (CLKCFG = 001_B) the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.

The frequency of f_{CPU} is half the frequency of f_{OSC} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{OSC} .

The timings listed in the AC Characteristics that refer to TCLs therefore can be calculated using the period of f_{OSC} for any TCL.

Phase Locked Loop

When PLL operation is configured (via CLKCFG) the on-chip phase locked loop is enabled and provides the CPU clock (see **Table 11**). The PLL multiplies the input frequency by the factor **F** which is selected via the combination of bits RP0H.7-5 (i.e. $f_{\text{CPU}} = f_{\text{OSC}} \times F$). With every **F**'th transition of f_{OSC} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly, i.e. the CPU clock frequency does not change abruptly.

Preliminary

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{OSC} . The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCLs.

The timings listed in the AC Characteristics that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances. The actual minimum value for TCL depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCL is lower than for one single TCL (see formula and [Figure 11](#)).

For a period of $N \times TCL$ the minimum value is computed using the corresponding deviation D_N :

$$(N \times TCL)_{min} = N \times TCL_{NOM} - D_N; D_N [ns] = \pm(13.3 + N \times 6.3)/f_{CPU} [MHz],$$

where N = number of consecutive TCLs and $1 \leq N \leq 40$.

So for a period of 3 TCLs @ 25 MHz (i.e. $N = 3$): $D_3 = (13.3 + 3 \times 6.3)/25 = 1.288$ ns, and $(3TCL)_{min} = 3TCL_{NOM} - 1.288$ ns = 58.7 ns (@ $f_{CPU} = 25$ MHz).

This is especially important for bus cycles using waitstates and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is neglectible.

Note: For all periods longer than 40 TCL the $N = 40$ value can be used (see [Figure 11](#)).

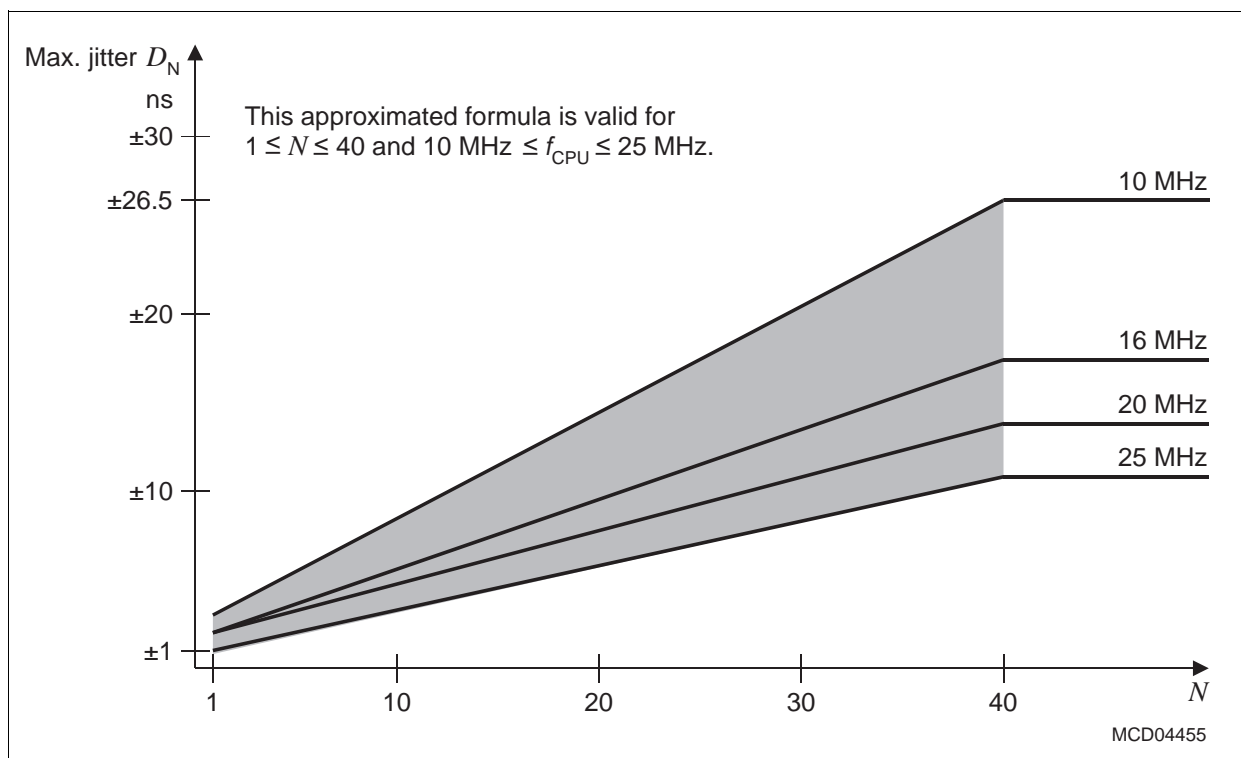


Figure 11 Approximated Maximum Accumulated PLL Jitter

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Direct Drive

When direct drive is configured (CLKCFG = 011_B) the on-chip phase locked loop is disabled and the CPU clock is directly driven from the internal oscillator with the input clock signal.

The frequency of f_{CPU} directly follows the frequency of f_{OSC} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{OSC} .

The timings listed below that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances. This minimum value can be calculated via the following formula:

$$\text{TCL}_{\min} = 1/f_{\text{OSC}} \times \text{DC}_{\min} \quad (\text{DC} = \text{duty cycle})$$

For two consecutive TCLs the deviation caused by the duty cycle of f_{OSC} is compensated so the duration of 2TCL is always $1/f_{\text{OSC}}$. The minimum value TCL_{\min} therefore has to be used only once for timings that require an odd number of TCLs (1, 3, ...). Timings that require an even number of TCLs (2, 4, ...) may use the formula $2\text{TCL} = 1/f_{\text{OSC}}$.

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AC Characteristics

External Clock Drive XTAL1

(Operating Conditions apply)

Table 12 External Clock Drive Characteristics

Parameter	Symbol		Direct Drive 1:1		Prescaler 2:1		PLL 1:N		Unit
			min.	max.	min.	max.	min.	max.	
Oscillator period	t_{OSC}	SR	40	–	20	–	60 ¹⁾	500 ¹⁾	ns
High time ²⁾	t_1	SR	20 ³⁾	–	6	–	10	–	ns
Low time ²⁾	t_2	SR	20 ³⁾	–	6	–	10	–	ns
Rise time ²⁾	t_3	SR	–	8	–	5	–	10	ns
Fall time ²⁾	t_4	SR	–	8	–	5	–	10	ns

- 1) The minimum and maximum oscillator periods for PLL operation depend on the selected CPU clock generation mode. Please see respective table above.
- 2) The clock input signal must reach the defined levels V_{IL2} and V_{IH2} .
- 3) The minimum high and low time refers to a duty cycle of 50%. The maximum operating frequency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.

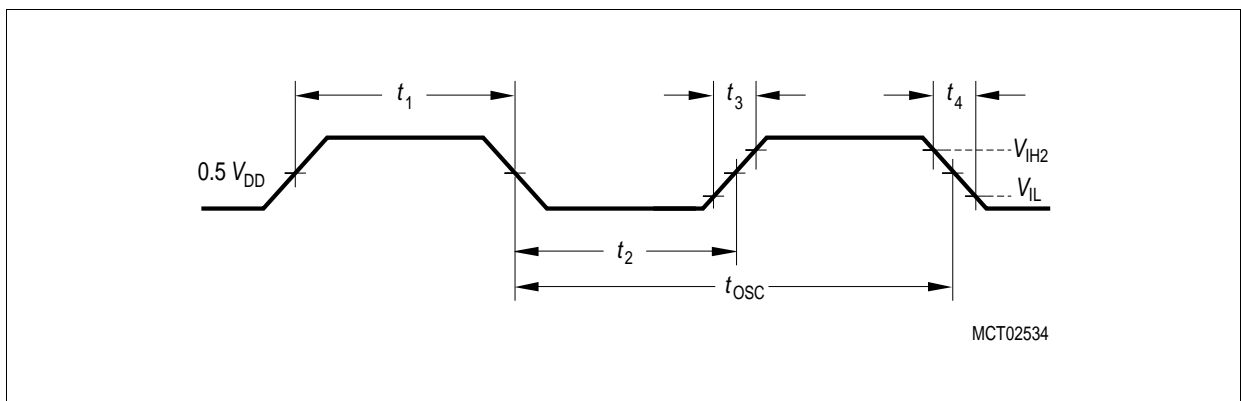


Figure 12 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal, the oscillator frequency is limited to a range of 4 MHz to 16 MHz.

It is strongly recommended to measure the oscillation allowance (or margin) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.

When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is guaranteed by design only (not 100% tested).

Preliminary
A/D Converter Characteristics

(Operating Conditions apply)

Table 13 A/D Converter Characteristics

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Analog reference supply	V_{AREF} SR	4.0	$V_{DD} + 0.1$	V	
Analog reference ground	V_{AGND} SR	$V_{SS} - 0.1$	$V_{SS} + 0.2$	V	–
Analog input voltage range	V_{AIN} SR	V_{AGND}	V_{AREF}	V	1)
Basic clock frequency	f_{BC}	0.5	6.25	MHz	2)
Conversion time ³⁾	t_{C10} CC	–	$40 t_{BC} + t_S + 2t_{CPU}$	–	10-bit conv. $t_{CPU} = 1 / f_{CPU}$
	t_{C12} CC	–	$46 t_{BC} + t_S + 2t_{CPU}$	–	12-bit conv. ⁴⁾ $t_{CPU} = 1 / f_{CPU}$
Calibration time after reset	t_{CAL} CC	–	$3328 t_{BC}$	–	5)
Total unadjusted error	TUE CC	–	± 2	LSB	10-bit conv. ⁶⁾⁷⁾
			± 4	LSB	12-bit conv. ⁶⁾
Internal resistance of reference voltage source	R_{AREF} SR	–	$t_{BC} / 60 - 0.25$	k Ω	t_{BC} in [ns] ⁸⁾⁹⁾
Internal resistance of analog source	R_{ASRC} SR	–	$t_S / 450 - 0.25$	k Ω	t_S in [ns] ⁹⁾¹⁰⁾
ADC input capacitance	C_{AIN} CC	–	33	pF	9)

1) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be X000_H or X3FF_H, respectively.

2) The limit values for f_{BC} must not be exceeded when selecting the CPU frequency and the ADCTC setting.

3) This parameter includes the sample time t_S , the time for determining the digital result and the time to load the result register with the conversion result.

Values for the basic clock t_{BC} depend on programming and can be taken from [Table 14](#).

This parameter depends on the ADC control logic. It is not a real maximum value, but rather a fixum.

4) For 12-bit conversions the CPU clock frequency must be limited to $f_{CPU} \leq 20$ MHz to achieve the specified TUE limits.

5) During the reset calibration conversions can be executed (with the current accuracy). The time required for these conversions is added to the total reset calibration time.

6) TUE is tested at $V_{AREF} = V_{DD} + 0.1$ V, $V_{AGND} = 0$ V. It is guaranteed by design for all other voltages within the defined voltage range.

The specified TUE is guaranteed only if the absolute sum of input overload currents on Port 5 pins (see I_{OV} specification) does not exceed 10 mA.

During the reset calibration sequence the TUE may reach twice the indicated maximum value.

Preliminary

- 7) If the analog reference supply voltage exceeds the power supply voltage by up to 0.2 V (i.e. $V_{AREF} = V_{DD} + 0.2 \text{ V}$) the maximum TUE is increased to $\pm 3 \text{ LSB}$. This range is not 100% tested.
- 8) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference voltage source must allow the capacitance to reach its respective voltage level within each conversion step. The maximum internal resistance results from the programmed conversion timing.
- 9) Not 100% tested, guaranteed by design and characterization.
- 10) During the sample time the input capacitance C_{AIN} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S . After the end of the sample time t_S , changes of the analog input voltage have no effect on the conversion result. Values for the sample time t_S depend on programming and can be taken from [Table 14](#).

Sample time and conversion time of the C164SV's A/D Converter are programmable. [Table 14](#) should be used to calculate the above timings.

The limit values for f_{BC} must not be exceeded when selecting ADCTC.

Table 14 A/D Converter Computation Table

ADCON.15 14 (ADCTC)	A/D Converter Basic Clock f_{BC}	ADCON.13 12 (ADSTC)	Sample time t_S
00	$f_{CPU} / 4$	00	$t_{BC} \times 8$
01	$f_{CPU} / 2$	01	$t_{BC} \times 16$
10	$f_{CPU} / 16$	10	$t_{BC} \times 32$
11	$f_{CPU} / 8$	11	$t_{BC} \times 64$

Timing Example for 10-bit Conversion:

Assumptions: $f_{CPU} = 25 \text{ MHz}$ (i.e. $t_{CPU} = 40 \text{ ns}$), ADCTC = 00_B, ADSTC = 00_B.
 Basic clock $f_{BC} = f_{CPU}/4 = 6.25 \text{ MHz}$, i.e. $t_{BC} = 160 \text{ ns}$.
 Sample time $t_S = t_{BC} \times 8 = 1280 \text{ ns}$.
 Conversion 10-bit $t_{C10} = t_S + 40 t_{BC} + 2 t_{CPU} = (1280 + 6400 + 80) \text{ ns} = 7.8 \mu\text{s}$.

Timing Example for 12-bit Conversion:

Assumptions: $f_{CPU} = 20 \text{ MHz}$ (i.e. $t_{CPU} = 50 \text{ ns}$), ADCTC = 00_B, ADSTC = 00_B.
 Basic clock $f_{BC} = f_{CPU}/4 = 5.0 \text{ MHz}$, i.e. $t_{BC} = 200 \text{ ns}$.
 Sample time $t_S = t_{BC} \times 8 = 1600 \text{ ns}$.
 Conversion 10-bit $t_{C10} = t_S + 40 t_{BC} + 2 t_{CPU} = (1600 + 8000 + 100) \text{ ns} = 9.7 \mu\text{s}$.
 Conversion 12-bit $t_{C12} = t_S + 46 t_{BC} + 2 t_{CPU} = (1600 + 9200 + 100) \text{ ns} = 10.9 \mu\text{s}$.

Preliminary

Testing Waveforms

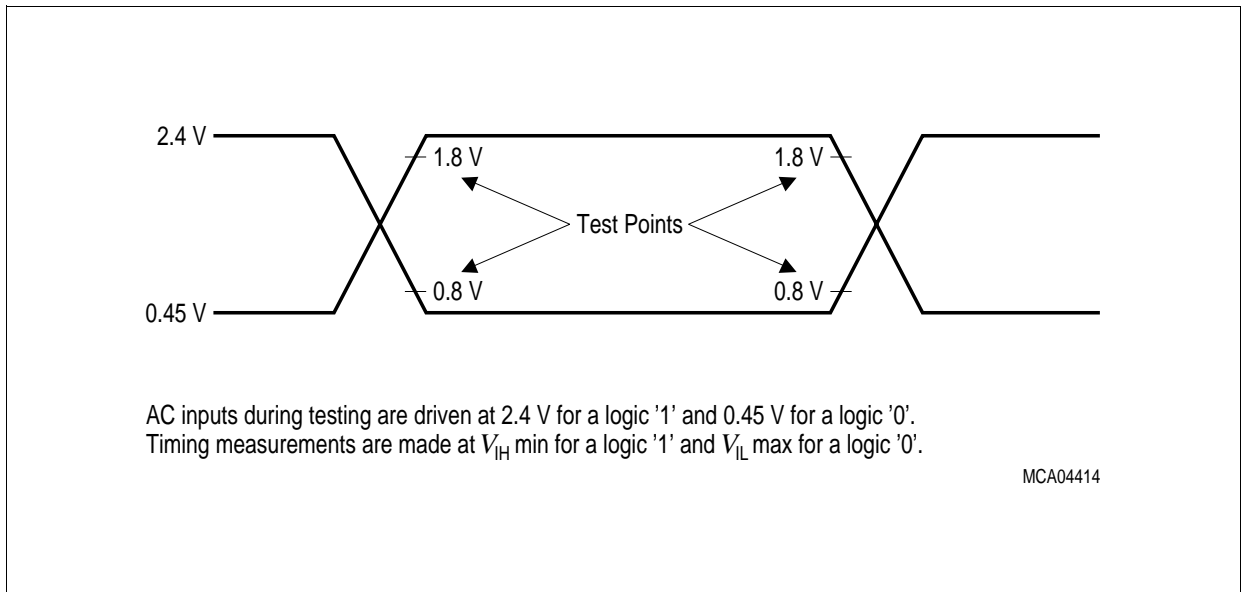


Figure 13 Input Output Waveforms

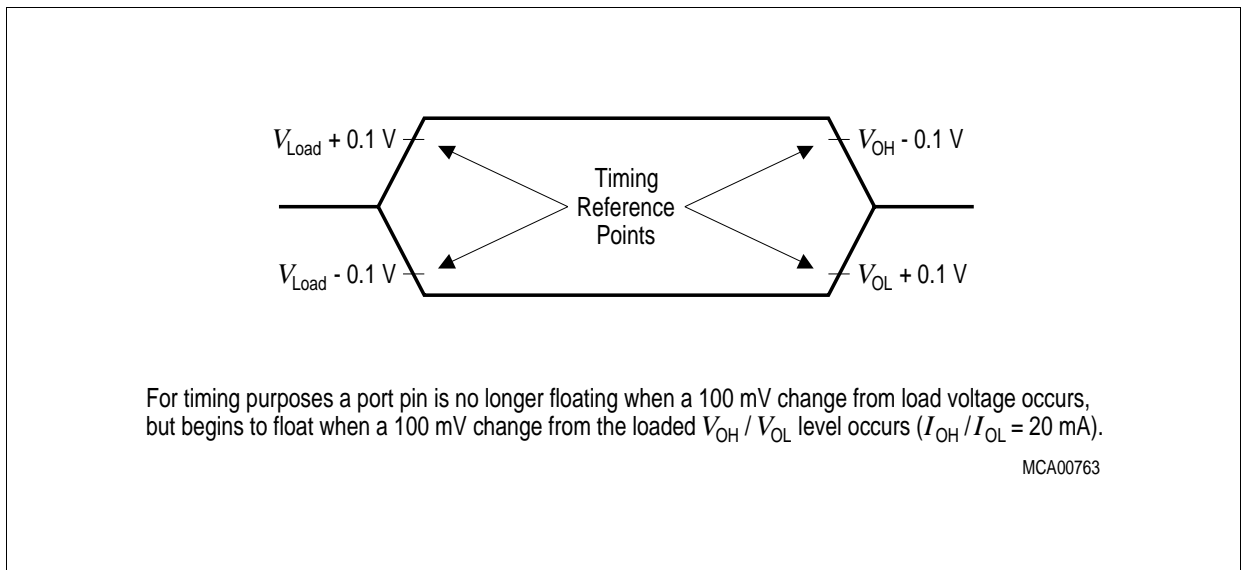


Figure 14 Float Waveforms

Preliminary
Memory Cycle Variables

The timing tables below use three variables which are derived from the BUSCONx registers and represent the special characteristics of the programmed memory cycle. The following table describes, how these variables are to be computed.

Table 15 Memory Cycle Variables

Description	Symbol	Values
ALE Extension	t_A	$TCL \times \langle ALECTL \rangle$
Memory Cycle Time Waitstates	t_C	$2TCL \times (15 - \langle MCTC \rangle)$
Memory Tristate Time	t_F	$2TCL \times (1 - \langle MTTC \rangle)$

Note: Please respect the maximum operating frequency of the respective derivative.

AC Characteristics
Multiplexed Bus

(Operating Conditions apply)

ALE cycle time = $6TCL + 2t_A + t_C + t_F$ (120 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	$10 + t_A$	–	$TCL - 10 + t_A$	–	ns
Address setup to ALE	t_6	CC	$4 + t_A$	–	$TCL - 16 + t_A$	–	ns
Address hold after ALE	t_7	CC	$10 + t_A$	–	$TCL - 10 + t_A$	–	ns
ALE falling edge to \overline{RD} , \overline{WR} (with RW-delay)	t_8	CC	$10 + t_A$	–	$TCL - 10 + t_A$	–	ns
ALE falling edge to \overline{RD} , \overline{WR} (no RW-delay)	t_9	CC	$-10 + t_A$	–	$-10 + t_A$	–	ns
Address float after \overline{RD} , \overline{WR} (with RW-delay)	t_{10}	CC	–	6	–	6	ns
Address float after \overline{RD} , \overline{WR} (no RW-delay)	t_{11}	CC	–	26	–	$TCL + 6$	ns
\overline{RD} , \overline{WR} low time (with RW-delay)	t_{12}	CC	$30 + t_C$	–	$2TCL - 10 + t_C$	–	ns

Preliminary
Multiplexed Bus (cont'd)

(Operating Conditions apply)

 ALE cycle time = $6\text{ TCL} + 2t_A + t_C + t_F$ (120 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol	Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
		min.	max.	min.	max.	
$\overline{\text{RD}}$, $\overline{\text{WR}}$ low time (no RW-delay)	t_{13} CC	$50 + t_C$	–	$3\text{TCL} - 10 + t_C$	–	ns
$\overline{\text{RD}}$ to valid data in (with RW-delay)	t_{14} SR	–	$20 + t_C$	–	$2\text{TCL} - 20 + t_C$	ns
$\overline{\text{RD}}$ to valid data in (no RW-delay)	t_{15} SR	–	$40 + t_C$	–	$3\text{TCL} - 20 + t_C$	ns
ALE low to valid data in	t_{16} SR	–	$40 + t_A + t_C$	–	$3\text{TCL} - 20 + t_A + t_C$	ns
Address to valid data in	t_{17} SR	–	$50 + 2t_A + t_C$	–	$4\text{TCL} - 30 + 2t_A + t_C$	ns
Data hold after $\overline{\text{RD}}$ rising edge	t_{18} SR	0	–	0	–	ns
Data float after $\overline{\text{RD}}$	t_{19} SR	–	$26 + t_F$	–	$2\text{TCL} - 14 + t_F$	ns
Data valid to $\overline{\text{WR}}$	t_{22} CC	$20 + t_C$	–	$2\text{TCL} - 20 + t_C$	–	ns
Data hold after $\overline{\text{WR}}$	t_{23} CC	$26 + t_F$	–	$2\text{TCL} - 14 + t_F$	–	ns
$\overline{\text{ALE}}$ rising edge after $\overline{\text{RD}}$, $\overline{\text{WR}}$	t_{25} CC	$26 + t_F$	–	$2\text{TCL} - 14 + t_F$	–	ns
Address hold after $\overline{\text{RD}}$, $\overline{\text{WR}}$	t_{27} CC	$26 + t_F$	–	$2\text{TCL} - 14 + t_F$	–	ns

Preliminary

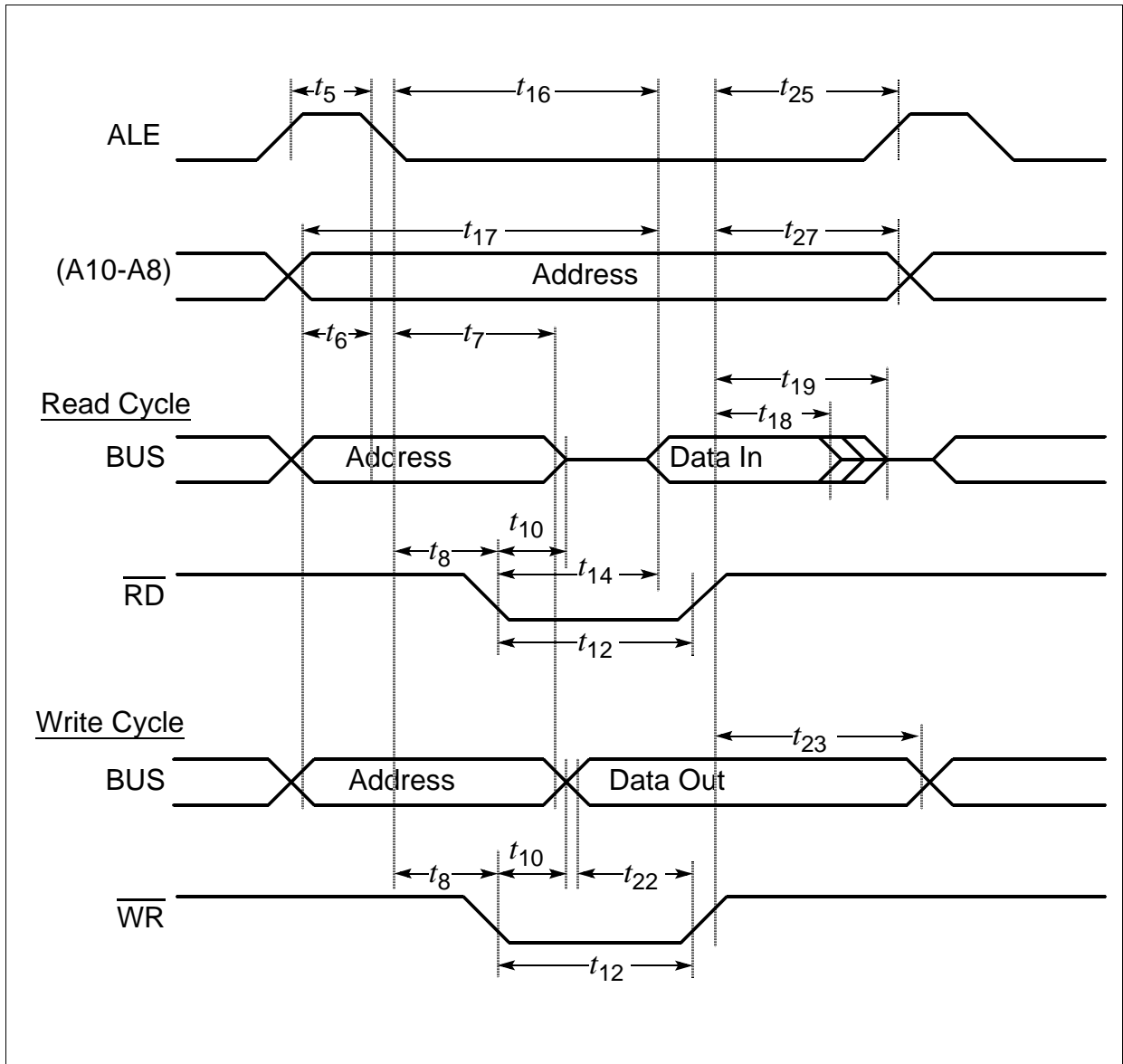


Figure 15 External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Normal ALE

Preliminary

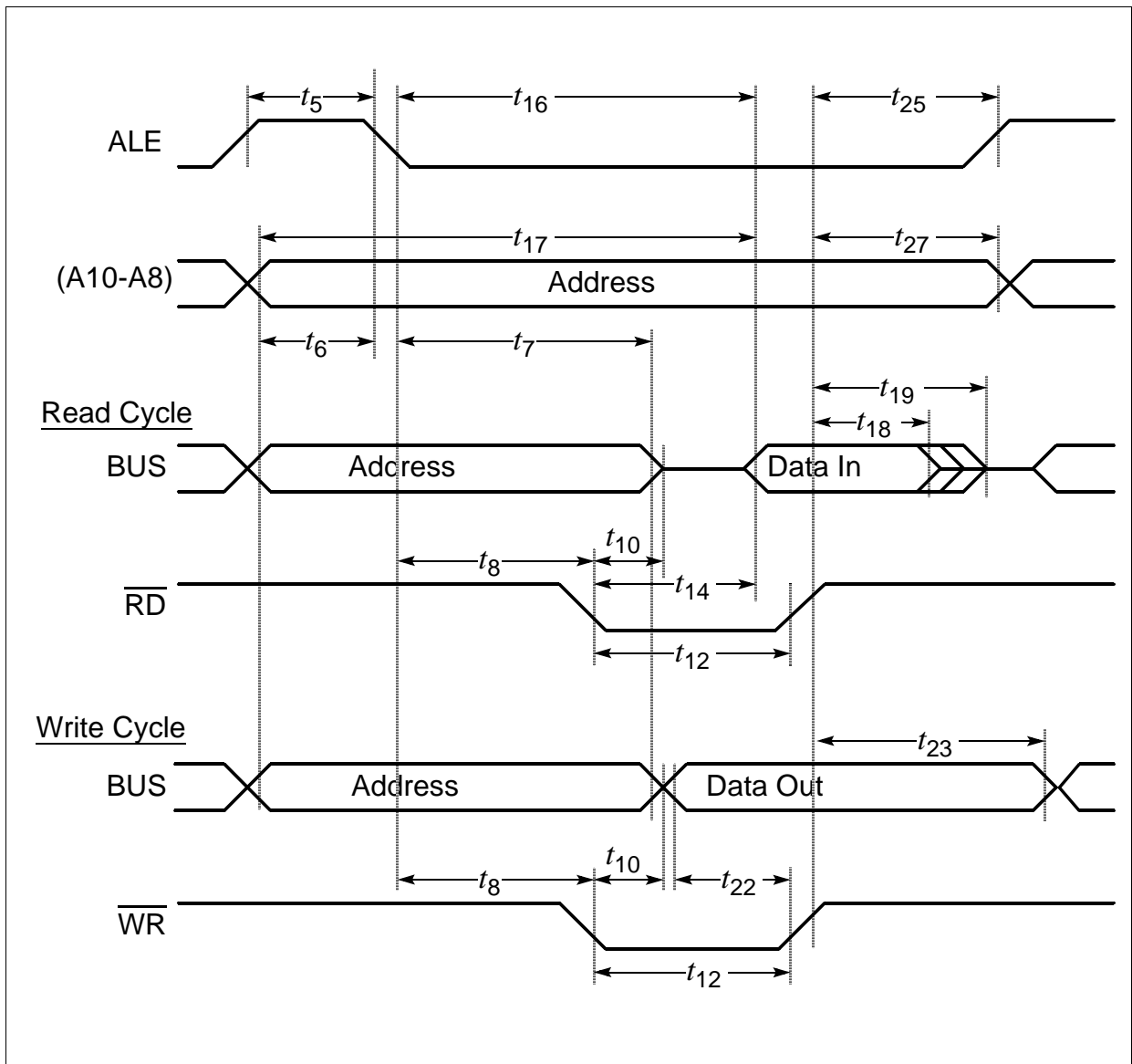
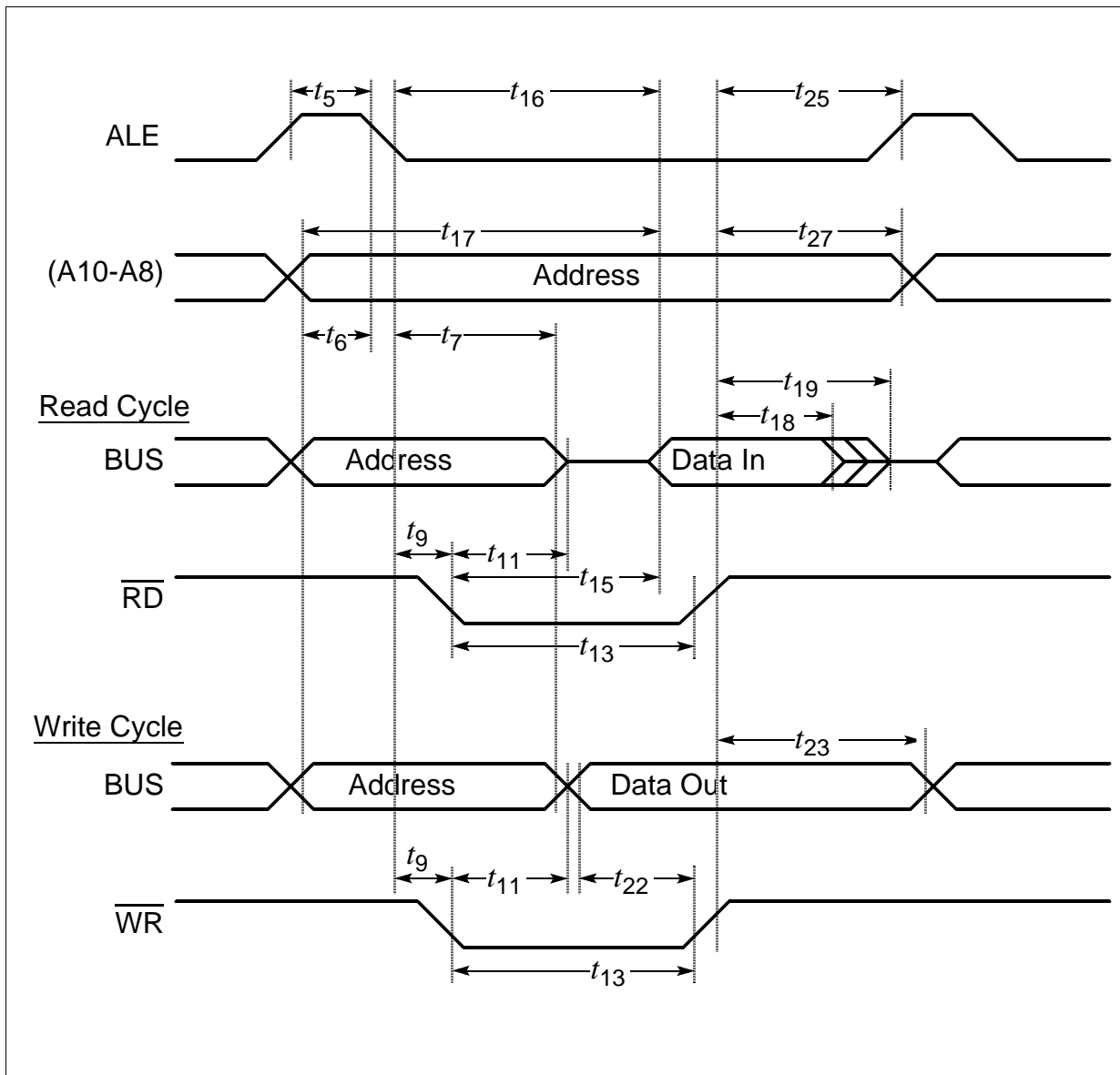


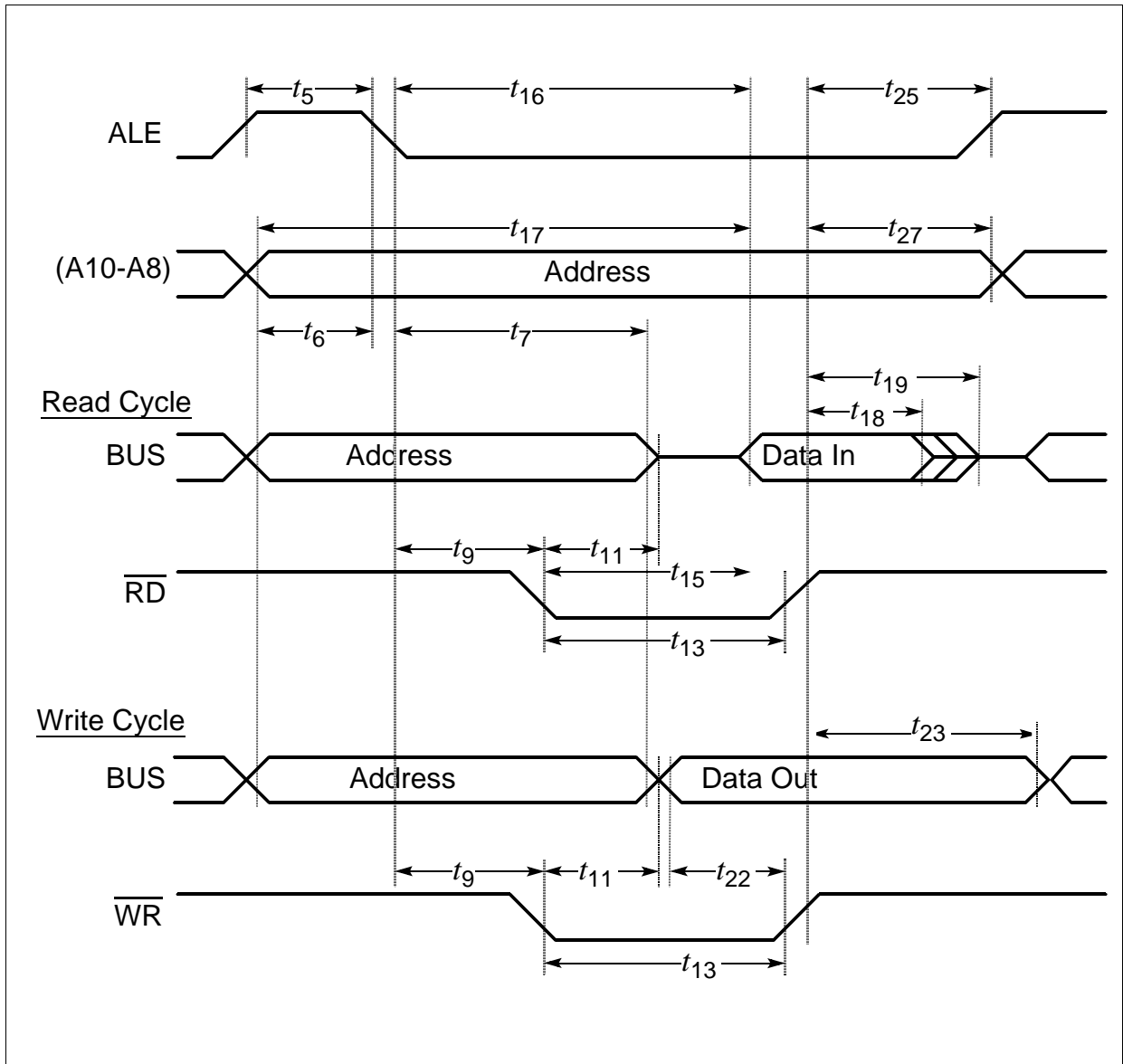
Figure 16 External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Extended ALE

Preliminary



**Figure 17 External Memory Cycle:
Multiplexed Bus, No Read/Write Delay, Normal ALE**

Preliminary



**Figure 18 External Memory Cycle:
Multiplexed Bus, No Read/Write Delay, Extended ALE**

Preliminary

AC Characteristics

CLKOUT

(Operating Conditions apply)

Parameter	Symbol	Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
		min.	max.	min.	max.	
CLKOUT cycle time	t_{29} CC	40	40	2TCL	2TCL	ns
CLKOUT high time	t_{30} CC	14	–	TCL - 6	–	ns
CLKOUT low time	t_{31} CC	10	–	TCL - 10	–	ns
CLKOUT rise time	t_{32} CC	–	4	–	4	ns
CLKOUT fall time	t_{33} CC	–	4	–	4	ns
CLKOUT rising edge to ALE falling edge	t_{34} CC	$0 + t_A$	$10 + t_A$	$0 + t_A$	$10 + t_A$	ns

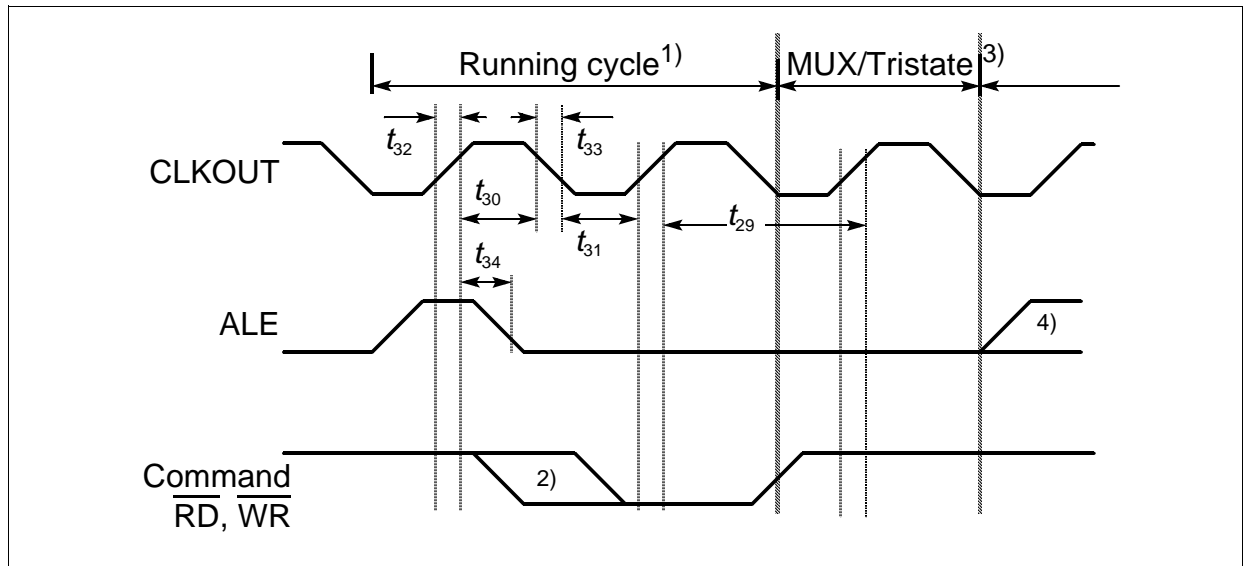


Figure 19 CLKOUT Timing

Notes

- 1) Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).
- 2) The leading edge of the respective command depends on RW-delay.
- 3) Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here.
For a multiplexed bus with MTTC waitstate this delay is 2 CLKOUT cycles.
- 4) The next external bus cycle may start here.

Preliminary

Package Outlines

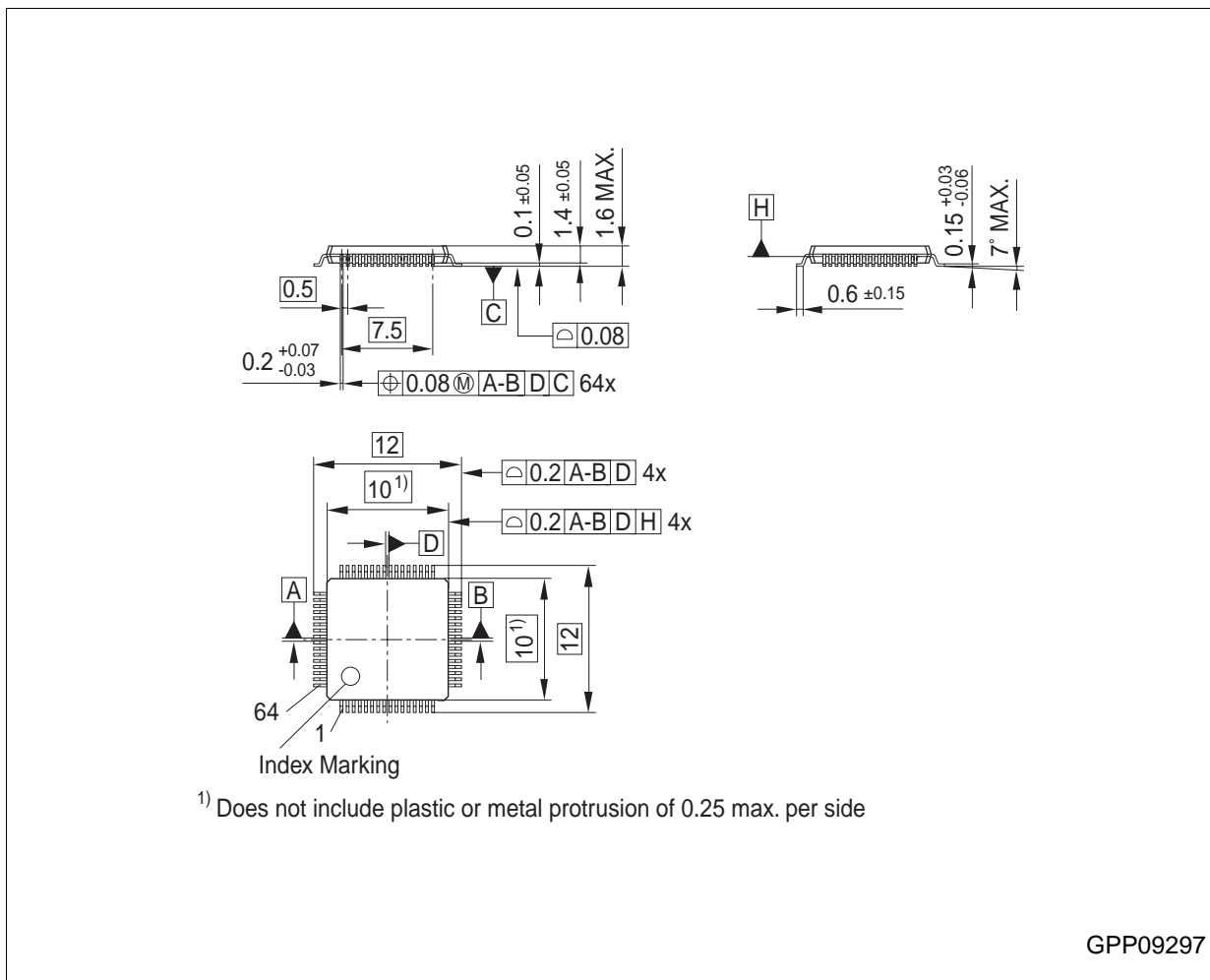


Figure 20 P-TQFP-64-8 (Plastic Metric Quad Flat Package)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": <http://www.infineon.com/products>.

SMD = Surface Mounted Device

Dimensions in mm

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