Infineon Microcontrollers - C16x Family Comparison

(**please refer to current version of Data Sheet, User's Manual and Errata Sheet**)

			Comparison C164-OTP, -ROM						
		Type:	C164CI-8E OTP				C164CI-8R ROM		**Remarks**
		Step:	Ax	Bx	Cx	Dx	Ax	Cx	
1	**Documentation**								
2	**User's Manual** and **Data Sheet**		see current errata sheet						
3	**V_{DD} / V_{SS} lines**	**internal/external lines separated, ADC connected to internal supply via double bond**	✓			-	-		
4		**int+ext / ADC + choke device**	-			✓	✓		
5		**internal/external supply connected via 'ring' structure, separate supply for ADC**	-			✓	-		EMC improvements
6	**Reset**								
7	**While EA# = High during Reset (single chip mode)**	**Internal ROM memory cell (003Eh) = Reset Configuration (solution for C164CI-8R only)**	-			-	✓ (if bit CM=0)		**Single ChipMode Reset Configuration has to be configured in the ROM mask (at address 003Eh) - see "Documentation Update" in the current Errata Sheet**
8	**Single Chip Mode Reset**	**Port 0 PullUps disabled during Reset (EA# = 1)**	-			✓	✓		**C164CI-8R**: Single Chip Mode Reset only if bit CM=0
9	**While EA# = High during Reset (single chip mode)**	**Default Configuration and software setting of register RSTCON** **After EINIT the Unlock Sequence is necessary to change RSTCON.**	-			✓	-		**Default configuration:** - **CLKCFG** = 001_B (Prescaler Mode: fcpu = fosc/2) - **SALSEL** = 01_B, **CSSEL** = 10_B (No segment address and chip select lines) - **WRC** = 1_B (SYSCON.WRCFG = 0_B i.e. WR# + BHE#) - **BTYP** = 11_B (BUSCON0.BTYP = 11_B: i.e. 16-bit MUX bus) - **SMOD:** no
10	**While EA# = Low during Reset (ext. bus mode)**	**Modification of system configuration in register RSTCON by software** **After EINIT the Unlock Sequence is necessary to change RSTCON.**	-			✓	-		**Startup configuration during reset on port 0**
11	**Reset Prolongation**	**2048 TCL** **Bitfield RSTLEN in register RSTCON**	-			✓	-		**extended duration, may be useful e.g. to provide additional settling for external configuration signals at high CPU clock frequencies**
12	**Bootstrap Loader**	**Bus Mode Reset: EA# = LOW** **Activation: P0L.4 tied to LOW**	✓			✓	✓		**PullDown for Port 0 pin: 8kOhm without external load - see AP1637xx**
13		**Single Chip Reset: EA# = High** **Activation: RD# tied to LOW**	same as Bus Mode Reset			✓	✓ (if bit CM=0)		**PullDown for RD# pin: 2kOhm without external load - see AP1637xx** ***Note:*** Max. BSL baudrate depends on f_{CPU} after reset (default: $f_{OSC}/2$)
14		**OTP programming: CHM enabled by default in BSL mode (when EA# = High = Single chip Mode)**	-			✓	-		**To verify the OTP contents the OTP read sequence has to be used see User's Manual "OTP Programming Example"** **OPCTRL = 0x0003;** /*enable module 1st*/ **OPAD = 0x7F00;** /*address in OTP*/ **OPCTRL = 0x0002;** /*enable module RD active*/ **OPCTRL = 0x0003;** /* enable module*/ **var1 = OPDAT;** /* read current data */
15	**ID Registers**	**IDCHIP**	0A01h	0A02h	0A03h 0A06h	0A04h 0A05h	Cx: 0A0xh Sx: 1B0xh		High Byte = Basic Type, Low Byte = Chip Generation Cx: with CAN; Sx: without CAN
16		**IDMEM, IDPROG**	4010h, 9340h				1010h, 0000h		Memory Identification, Programming Voltage
17	**f_{CPU} max @ V_{DD}=5V**	**[MHz]**	**20**			**25**	**25**		
18	**Variable Frequency Output**	**Pin P3.15, CLKOUT, FOUT** **Register FOCON**	-			✓	✓		**Can be enabled only when SYSCON.8 (CLKEN) = 0** **enable alternate function: P3.15 = 1, DP3.15 = 1**
19	**On Chip Memory**								
20	**XRAM**	2Kbytes: 0x00E000...0x00E7FF	-			2 Kbytes	2 Kbytes		to enable XRAM bit XPEN in register SYSCON has to be set before execution of EINIT
21	**Ext. Bus Interface**								
22	**BUSCON switch WaitState**	**additional Tristate Wait State if a different Address Window is used**	-			✓	-		selected with BUSCONx.11 = 1 (Default: compatible mode with BUSCONx.11 = 0)
23	**Early Write**	**rising edge 1 TCL earlier (WR# and WR-Data while ADDR = stable)**	-			✓	-		selected with BUSCONx.8 = 1 (Default: compatible mode with BUSCONx.8 = 0)
24	**Interrupts**								
25	**Alternate Interrupt Inputs**	**EXISEL**	✓			✓	✓		The input source for the fast external interrupts (controlled via register EXICON) can be derived either from the associated port pin EXnIN or from an alternate source.
26		EXI0SS: CAN_RxD (Int. Control: CC8IC)	✓			✓	✓		
27		EXI2SS: RxD0 (Int. Control: CC10IC)	-			✓	-		
28		EXI3SS: SCLK (Int. Control: CC11IC)	-			✓	-		
29	**CAPCOM Units**								
30	**CAPCOM2**	**Port 1H can be used as CC24...27 Comp. Output**	-			✓	- **+ see CAPCOM.4**		**see erratum CAPCOM.4** **(SW Access to P1H overwrites CAPCOM HW Settings)**
31		**Registers (CCx, CCxIC, CCMy) / Pins available**	**8 (16) / 4 I/O+4 I**			**16 / 8 I/O**	**8 (16) / 4 I/O+4 I**		
32	**CAPCOM6**	**Functional differences lead to application restrictions**	**V1.0**	**V3.0**	**V3.1**	**V5.0**	**V4.0**		**no functional changes between versions x.0 and x.1,** **see page "Infineon C16x Family - CAPCOM6 Functionality"**
33		**corrected block commutation table (for left rotation too)**	-			✓	-		**corrected for Rotate Left**
34		**Trap Control for CAPCOM6 Timers: enhanced CTRAP function**	-			✓	-		**TRCON: TREN5...0, TT13DIS, TT12DIS** **additional switch TT12DIS (Trap function for Timer T12 is disabled)**
35	**Watchdog Timer**								
36	**WDTCON**	**WDTCON.7 = WDTPRE**	-			✓	-		WDTCON.7 = 1 enables an additional prescaler by 2 for the WDT input clock
37	**X-Peripherals**								
38	**CAN**	**full CAN module**	**CAN1**				**CAN1**		
39		**P4 Open Drain function**	-			✓	-		
40		***CAN interface line assignment controlled by SW:*** ***Default: CAN_RxD, CAN_TxD disconnected !***	-			**P4.5...6** **P8.0...1** **P8.2...3**	-		The receive and transmit line of the CAN module may be assigned to several port pins of the C16x under software control. This assignment is selected via bitfield IPC (Interface Port Connection) in register PCIR (if bit CCE in register CSR is set 1st)
41		**CAN** register IR (char @ 0xEF02) replaced by **PCIR** (int @ 0xEF02) with bitfield **IPC**	-			✓	-		
42		**Clock Prescaler Control Bit CPS in Register CSR**	-			✓	✓		CPS=1: Fast mode: the input clock is used directly 1:1. The minimum input frequency to achieve a baudrate of 1 MBaud is f_{CPU} = 8 MHz. Default: compatible mode = division by 2
43	**Ports, Pin Driver Control**								
44	**Special Thresholds**	**PICON register**			✓		✓		
45		P4LIN	-			✓	-		
46	**Port Output Edge Control**	**2 groups (Bus / Non Bus Pins) (register PDCR)**	-	-	✓	-	✓		
47	**new Port Output Edge and Driver Control**	**each Nibble of Port and Control Lines (registers POCONx)**	-			✓	-		
48	**New Temperature Compensation**	**PTCR new**	-			✓	-		The temperature compensation is based on a 100 KHz reference clock - see bitfield TCDIV in register PTCR (**disabled by default**)
49	**Sleep Mode**	**SYSCON1: SLEEPCON** specific Idle Mode (start: instruction IDLE) - CPU disabled - Peripherals and **WDT** disabled - RTC enabled or disabled	-			✓	✓		**SYSCON1** - SLEEP Mode Configuration (after EINIT Unlock sequence required) 00: Normal IDLE mode 01: SLEEP mode, with RTC running 10: Reserved. 11: SLEEP mode, with RTC and oscillator stopped
50	**Emulation Mode**								
51	**CS-Inputs**	CAN1	-			P3.9	-		

Comparison C164-OTP, -ROM

Module version of CAPCOM6	Used for product	additional functional changes in contrast to C164CI User's Manual V1.1 (i.e. accumulating from version to version!)
V1	• C164CI-8E OTP step AA	None
V2	• C167E2 BondOut	• outputs in case of trap condition (CTRAP) are not switched to initial values (CC6MCON / "COINI"), but to port register P1L instead – affects whole P1L, i.e. also COUT63 ==> selection for single outputs with bits TRENn in TRCON not useable any more. Original concept: No distinction between initial values and signal polarities. That means, the initial values have to be set in such a way, that for a bridge circuitry either highside or lowside switches are initially switched on. On the other hand, a trap condition requires to have all switches OFF ! (e.g. emergency switch-off in case of short circuits)
V3	• C164CI-8E OTP step BA..BC • C164CI-8E OTP step CA	• Update from shadow latches (in center aligned mode) not only on zero match, but on period match, too. • In center aligned mode with every zero match of Timer T12 all channels are reset to their initial states. (*A)
V4	• C164CI/SI-8R ROM all existing steps • C164CI/SI-LM ROMless all existing steps • C167E3 BondOut	• Necessary exception (!) to feature "reset with zero match" (*A): If a compare match for a channel occurs together with zero match of T12, this channel is always set to its active state. • If a compare match of a channel happens simultaneously with a period match of T12, this channel is always reset to inactive state. • Initial values in "COINI-Bits" (CC6MCON.0..5) now have a shadow latch as well !!! and for update bit STE12 is to be set. (*B) • The automatic capture on channel 0 in block commutation mode will now generate an interrupt by setting bit CC6IR in CC6IC with every new Hall-Pattern. (please refer to User's Manual C164CI Version 1.1, 1998-08, Figure 17-10 or User's Manual C164 1999-09 V 2.0)
V5	• C164CI-8EM since step DA • C164CM-4EF • C164CM-4RF	• new switches TT12DIS and TT13DIS available • outputs in case of trap condition (CTRAP) can now be switched to initial values (when TT12DIS or TT13DIS is set to "1"). • standard commutation tables have been implemented for both turning directions (i.e. with zero degrees phase shift).

In general:

- Shadow latch transfers (or update from shadow latches, respectively) in edge aligned mode take place with period match of T12.
- After a shadow latch transfer occurred, the effects of new values in CCx registers cannot take place before the next "comparison event", i.e. when writing value 0 to a CCx and setting bit STE12 after period match, but before zero match of T12, for example, the next zero match will cause the transfer, but for the comparison still the old value is relevant. Yet, with the second zero match of T12 after setting STE12 the compare match of that channel will occur together with the zero match.
- In opposite to that, the changing of other shadowed CAPCOM6-registers, like the COINI-Bits (CC6MCON.0..5) (possible since V4 of the CAPCOM6! (*B)) will affect the output pins with the very next shadow latch transfer!

This means for the "workaround for 0% and 100% duty cycle" as well as for general usage:

- It is extremely important at which moment in time (relatively to T12 matches) you trigger updating from the shadow latches by setting STE12!