Application Note AN-1120

Buffer Interface with Negative Gate Bias for Desat Protected HVICs used in High Power Applications

By
Marco Palma - International Rectifier
Niels H. Petersen - Grundfos

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In this application note, a buffer circuit with negative gate drive capability for the gate driver families IR2x14(1)SSPBF and IR2x38(1)QPBF are presented. This circuit boosts the power capability of these devices, enabling their use in high power applications. The circuit includes negative turn-off for power switches and embeds all the new features integrated in these new HVIC families: automatic desaturation detection and soft shutdown to open a short-circuit. The proposed circuit has been successfully tested and adopted in a real inverter application.

Introduction

The IR2x14(1)SSPBF gate driver family is designed for medium power, half-bridge gate driving. The high-current capability (2 A source, 3 A sink) of the drive stages and the 20 V capable output stages allow these devices to control switches in low to medium power applications (up to 10 kW). The IR2x38(1)QPBF is a high voltage, 3-phase IGBT gate driver family suited for AC motor drive applications.

In both families, each output stage has three separate gate control pins to allow flexible customization of the IGBT gate charge. These families are designed specifically to protect half-bridge and three-phase inverter switches. Desaturation detection of the power switch is fully integrated, resulting in an increased system reliability and drastically reduced part count and layout size. Moreover, anti-shoot-through and undervoltage lockout are embedded for both the high and low voltage side.

For higher power applications, a buffer stage that increases the sinking and sourcing current capability of the gate driver may be needed. At the same time the buffer stage should preserve the new embedded features of these families. Moreover, some high power module manufacturers require/suggest negative bias to safely turn-off IGBTs.

This application note presents a circuit that:

- increases the sinking/sourcing current capability of the IR2x14(1)SSPBF and IR2x38(1)Q;
- allows negative voltage driving capability (+15 V turn-on, -5 V turn-off);
  while preserving all of the newly embedded features of these devices.

This circuit has been tested in a real inverter application with three IR2214SSPBF HVICs and it can be adapted to similar applications.

The remainder of this application note presents the solution for the IR2x14(1)SSPBF, but the same circuit can easily be adapted to the IR2x38(1)QPBF gate driver family.

Schematic

Typical application circuit

A typical application circuit for the IR2x14(1)SSPBF is shown in Fig. 1. To simplify the schematic, only the pin connections to the power stage are shown. Moreover, in this application the floating V_B-V_S voltage is usually obtained with a bootstrap network from the V_{CC} supply. The three resistors connected to each gate of the IGBTs are used for the turn-on, turn-off, and soft shutdown functions needed by the application. Please refer to the datasheet and to Design Tip **DT04-4**, both available at www.irf.com, for more details regarding how to use the IR2x14(1)SSPBF in the typical configuration.

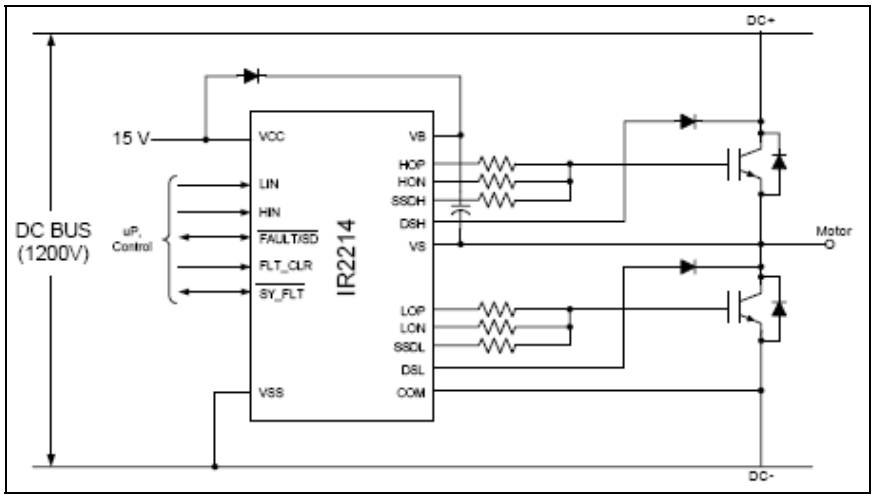

Figure 1 – IR2x14(1)SSPBF typical application circuit

Buffer with negative gate reverse bias voltage block diagram

The block diagram of the interface circuit needed to allow the buffered drive with negative gate reverse bias is shown in Fig. 2. This interface circuitry is put between the pins of the gate driver and the gate resistors. The assumption in this schematic is that the floating voltages V_B and -5 V (referred to V_S) are supplied from an isolated power supply. Also for the low-side IGBT an auxiliary power supply of -5 V (referred to COM) is needed. The interface circuit needs to preserve the independence between the channels HOP, HON, and SSDH in the high-side and between the channels LOP, LON, and SSDL in the low-side. Moreover, the negative voltage shall never reach the pins of the gate driver. The two interface blocks are conceptually the same, so, in next section, only the high-side interface is presented. The same ideas apply to the low-side interface.

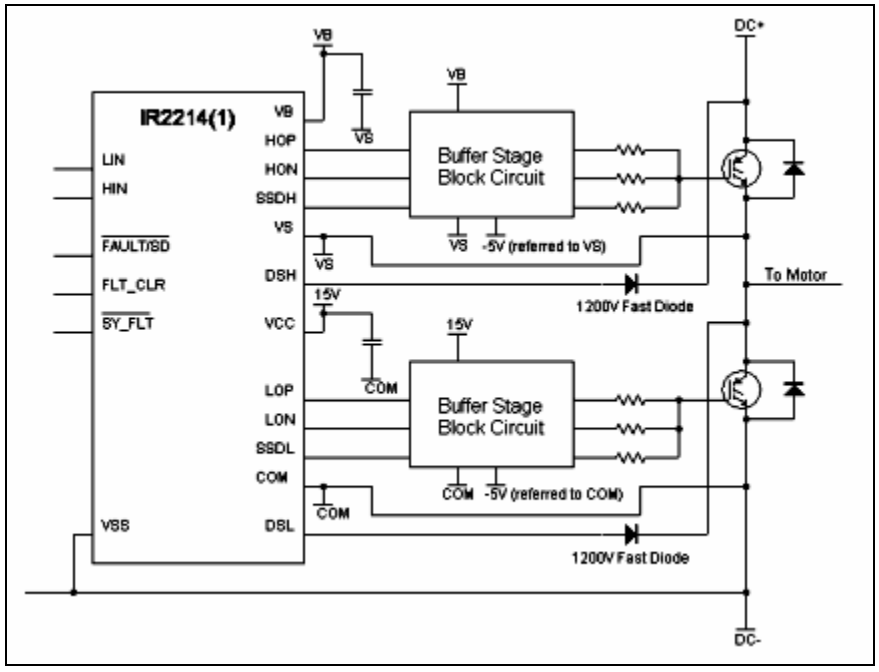

Figure 2 – Buffer with negative gate reverse bias block diagram

Buffer Stage Schematic

The schematic of the interface circuitry is presented in Fig. 3. A brief explanation for each component follows.

The power supplies +15 V and -5 V can be obtained using a flyback circuit with a center tap on the winding to get the reference voltage node.

- HOPBUF is the buffered version of the HOP signal and it is used during normal operation to turn-on the IGBT. When HOP is on, also HOPBUF is on, while HON, HONBUF, SSDH and SSDHBUF are in high impedance.
- HONBUF is the buffered version of the HON signal and it is used during normal operation to turn-off with negative voltage the IGBT. When HON is on, also HONBUF is on, while HOP, HOPBUF, SSDH and SSDHBUF are in high impedance.
- SSDHBUF is the buffered version of the SSDH signal and it is used during the first phase of a short-circuit to softly shutdown the IGBT. When SSDH is on, also SSDHBUF is on, while HON, HONBUF, HOP and HOPBUF are kept in high impedance.
- D1 is used to boost HOP turn-off when HON turns on and to boost HON turn-off when HOP turns on. R5 and R8 are used to put both HOPBUF and HONBUF channels in high impedance when SSDH is on (during soft shutdown). This allows a third channel (SSDHBUF) to handle the short-circuit event separately.
- R13 is used to keep the SSDH pin to a known fixed voltage (+15 V) when the SSDH pin is in high impedance (during normal operation).
- Q1 is used during soft shutdown to drive the gate down to zero voltage before the HONBUF channel comes back into action. Thanks to Q1, negative voltage cannot reach the IR2x14(1)SSPBF SSDH pin (when HONBUF is on).
- MOS X1b and X3 act as first stage inverter for the HOP signal. They allow replicating HOP signal after X2a and they are also used to drive X2a into high impedance during short-circuit. X3 is used to boost the turn-off of the X2a, thus boosting the turn-off of the IGBT. X3 is important to avoid the cross conduction between X2a and X2b.
- R4 and C1 are used to control the turn-on of the MOS X2a, limiting the cross conduction between X2a and X2b. Moreover R4 is used to limit the cross conduction between X3 and X1b during switching.
- X2a is a 30 V 0.20 Ω PMOS (IRF7509); it replicates the operation of the HOP pin of the IR2x14(1)SS, but it can withstand a negative voltage, because its V_{DS} breakdown voltage is 30 V. It is driven in high impedance during short-circuit. With this circuit, IR2x14(1)SSPBF HOP pin never sees a negative voltage during operation.
- X1a, D2 (15 V Zener) and R10 are used as a first stage inverter for the HON channel. This configuration can allow the use of a negative bias, but when this stage is on, there is approximately 23 mA of static current consumption. It is not possible to use an NMOS together with X1a because the negative voltage would reach the IR2x14(1)SSPBF HON pin. This static consumption does not allow the bootstrap power supply to be used. But with this configuration, a negative voltage cannot reach the IR2x14(1)SSPBF HON during operation.
- X2b is a 30 V 0.11 Ω NMOS (IRF7509); it replicates the operation of HON pin of the IR2x14(1)SS, but it can allow a negative bias to the IGBT gate. Its V_{DS} breakdown voltage is 30 V. Moreover it is driven in high impedance during short-circuit for a period that lasts from 5.7 µs to 13.5 µs. This allows the SSDH pin intervention.

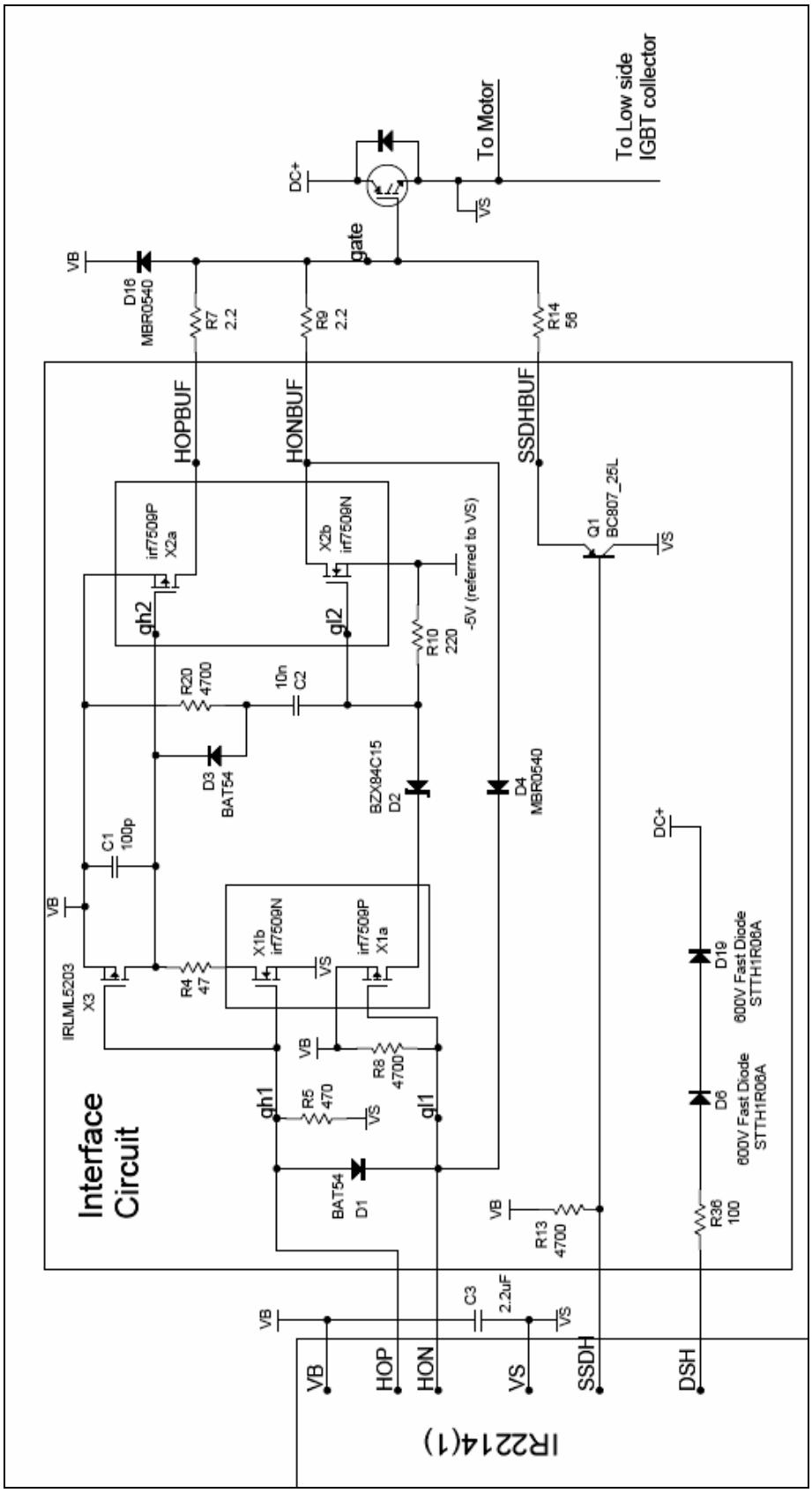

Figure 3 - Interface circuitry schematic

- D3, R20 and C2 are used during normal operation to boost the turn-off of X2b when X2a is turning on. This is achieved thanks to the capacitor C2. D3 is used to have the boost effect only for the turn-off of X2b. This results in a boost effect when the IGBT is turned on.
- D4 is used only during power up sequence because it keeps the IGBT gate low until the power supplies are settled.

V_S-V_{SS} negative voltage spikes

When this circuitry is used with high power modules, negative V_S-V_{SS} voltage spikes may appear at the V_S pin of the IR2x14(1)SSPBF gate driver during leg commutations. This is due to unavoidable parasitic inductances in the power circuit. To limit the amplitude and the duration of these negative voltage spikes, a circuit as in Fig. 4 can be added near the IR2x14(1)SSPBF chip. The right value of the resistor depends on the application layout, and it can be in the range of few ohms. The resistor is inserted to limit the specified peak current in the diodes. In this circuit two 600 V diodes are used because the sum of the forward recovery voltage of two 600 V diodes and the recovery time (typ. 10 V+10 V=20 V for 100 ns) are lower than the forward recovery voltage and time of a single 1200 V diode (typ. 35 V for 900 ns). The resistor can be put either in series as in Fig. 4, or it can be placed between V_S pin and IGBT emitter pin (please look at DT04-4 for further details). Because of the power range of this application, the values of the gate resistors are comparable to the value of the limiting resistor shown in the Fig. 4. To avoid interference of this resistor in the gate charge – discharge loop net, the approach as in Fig. 4 has been chosen and its function has been successfully proven in the lab. Figure 4 also presents the COM-V_{SS} swing limiter which is used to limit the unbalance of COM respect to V_{SS} during commutation.

IGBT gate clamping during short-circuit

During short-circuit, the peak of the short-circuit current depends on V_{GE} which is augmented by the feedback of the dV/dt through the gate-collector capacitance. The effect can be overcome by clamping the V_{GE} safely with a diode connected from the gate of the IGBT to the local power supply capacitor (V_B for the high-side and V_{CC} for the low-side). An example is shown in Fig. 5.

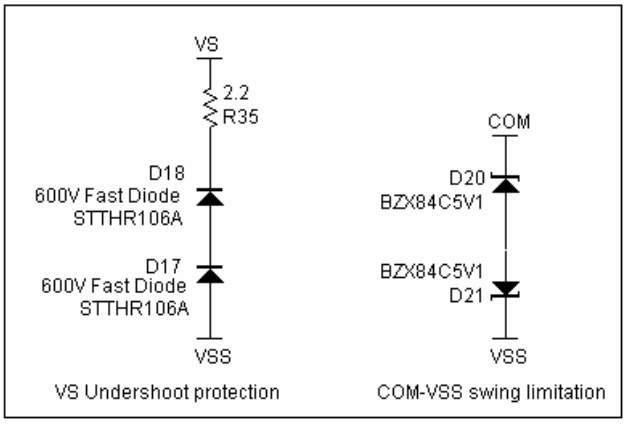

Figure 4 - V_S-V_{SS} negative voltage spikes protection and COM-V_{SS} swing limitation

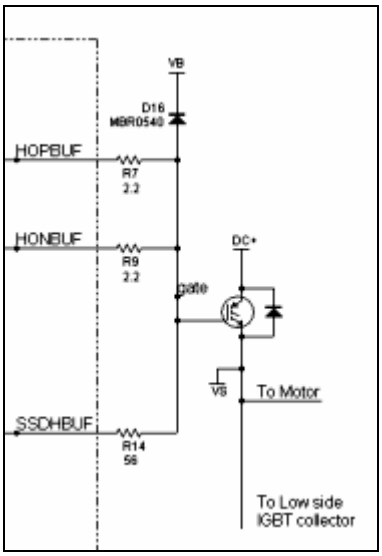

Figure 5 - V_{GE} clamping during short-circuit

Simulation results

The simulation results in the next paragraph have been obtained with a 70 nF capacitor connected in place of the IGBT, to simulate 1400 nC gate charge and discharge. The value 1400 nC is the typical charge for a 150 A (at 100 °C) 1200 V IGBT.

Turn-on behavior

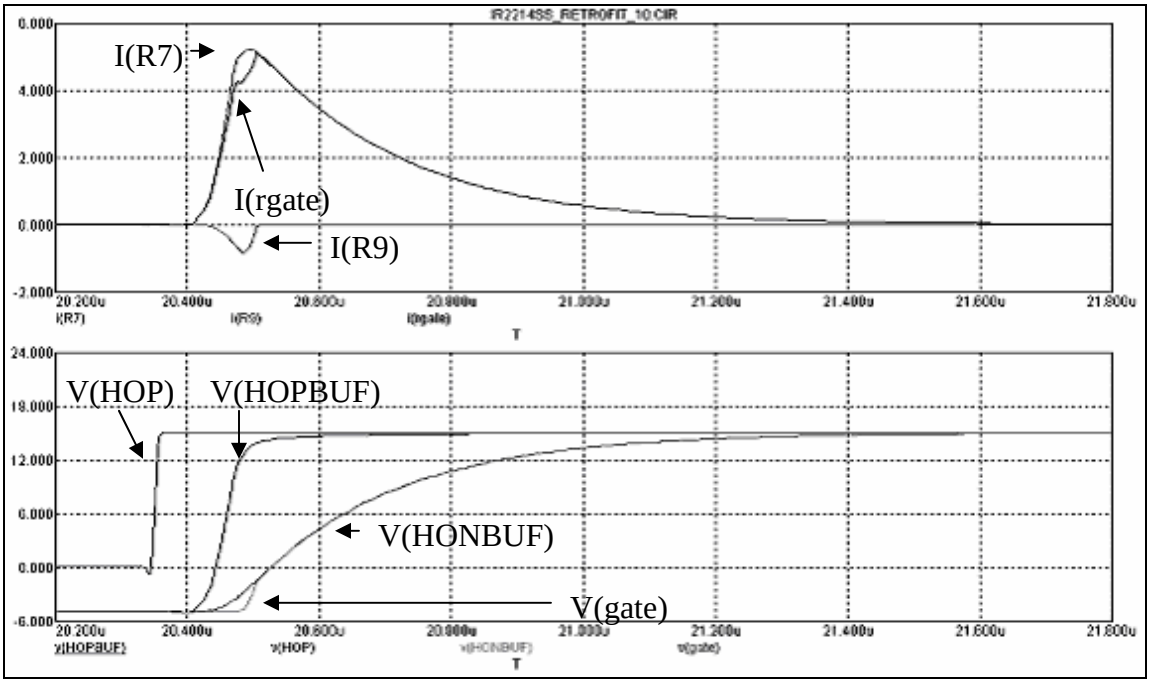

Figure 6 – Turn-on behavior

- In Fig. 6 the upper diagram shows:
  - the current flowing in the capacitor (it represent the equivalent gate charge current);
  - the current flowing in R7 through the MOS X2a;
  - the current flowing in R9 through the MOS X2b;
- In Fig. 6 the lower diagram shows:
  - the HOP voltage;
  - the HOPBUF voltage;
  - the capacitor voltage (it represent the equivalent gate voltage);
  - the HONBUF voltage (X2b is off but the voltage rises through R9).

Turn-off behavior

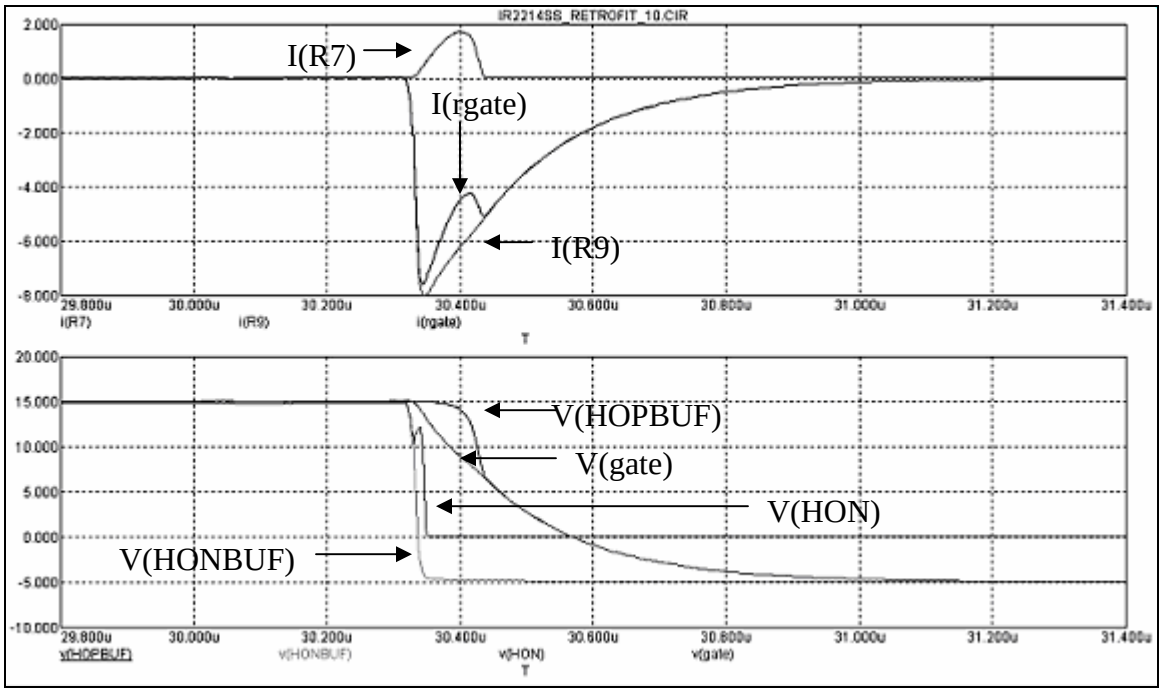

Figure 7 – Turn-off behavior

- In Fig. 7 the upper diagram shows:
  - the current flowing from the capacitor (it represent the equivalent gate discharge current);
  - the current flowing in R7 through the MOS X2a;
  - the current flowing in R9 through the MOS X2b;
- In Fig. 7 the lower diagram shows:
  - the HON voltage;
  - the HOPBUF voltage (X2a is off but the voltage rises through R7);
  - the capacitor voltage (it represent the equivalent gate voltage);
  - the HONBUF voltage.

Soft Shutdown behavior

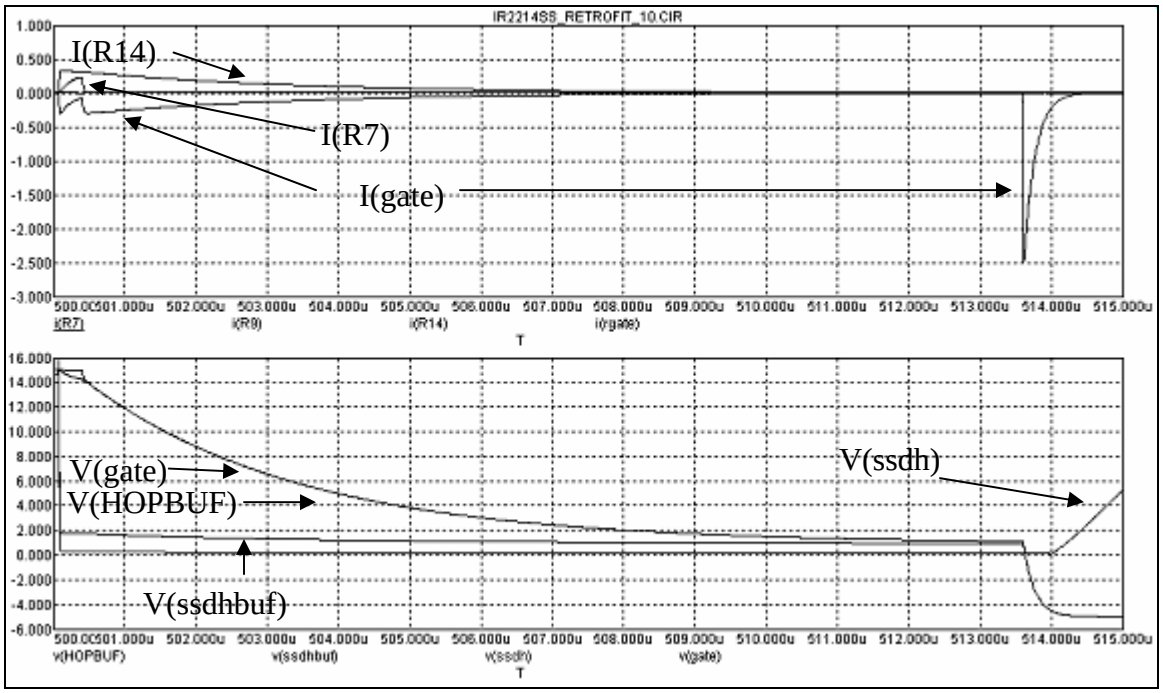

Figure 8 - Soft shutdown behavior

- In Fig. 8 the upper diagram shows:
  - the current flowing from the capacitor (it represent the equivalent gate discharge current);
  - the current flowing in R7 through the MOS X2a;
  - the current flowing in R9 through the MOS X2b;
  - the current flowing through R14.
- In Fig. 8 the lower diagram shows:
  - the SSDH voltage;
  - the SSDHBUF voltage;
  - the HOPBUF voltage;
  - the capacitor voltage (it represents the equivalent gate voltage).

Experimental Results

This circuit has been evaluated in a 1200 V 100 A IGBT inverter application. Turn-on, turn-off, and V_S-V_{SS} undershoot behaviors have been tested.

- In Fig. 9 the turn-on behavior of a high-side IGBT with DC bus voltage of 600 V and a current of 80 A is shown.
- In Fig. 10 the turn-on of a high-side IGBT with DC bus voltage of 600 V and a current of 80 A is shown. The swing of COM-V_{SS} is limited by Zener diodes.
- In Fig. 11 the turn-off of a high-side IGBT with DC bus voltage of 600 V and a current of 80 A is shown.
- In Fig. 12 the V_S-V_{SS} negative spike following a turn-off of a high-side IGBT with DC bus voltage of 350 V and a current of 100 A is shown.

Figure 9	Measure Points		Sensitivity
Channel	**+**	**-**	**1 µs /div**
3	DC+	Out B	100 V
4	Gate High phase B	Emitter High phase B	5 V
A	I_C*V_{CE}		25 kW
B	I_C = 80 A		50 A
Eon Area (A)	6.7		[mJ]
I_C rise time 20-80%	14		[ns]
V_{CE} fall time 80-20%	80		[ns]

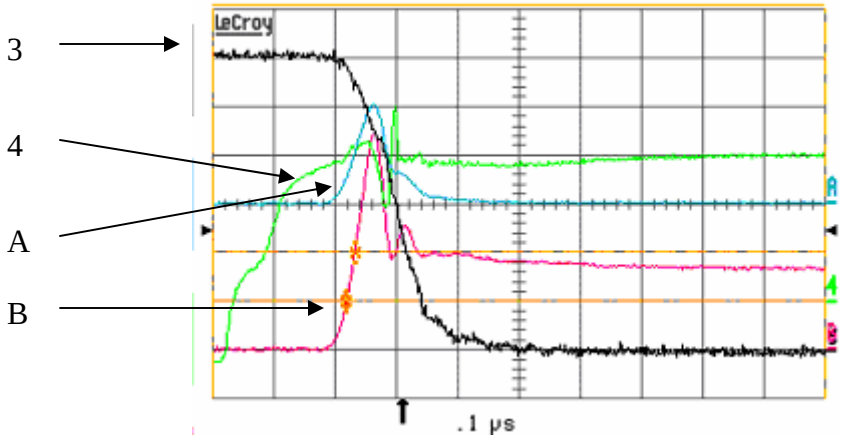

Figure 9 – Turn-on high-side IGBT V_{DC}=600 V I_C=80 A

Figure 10	Measure Points		Sensitivity
Channel	+	-	**1 µs /div**
3	DC+	Out B	100 V
4	COM phase B	V_{SS} phase B	5 V
A	I_C*V_{CE}		25 kW
B	I_C = 80 A		50 A
Eon Area (A)	6.67		[mJ]
I_C rise time 20-80%	13.5		[ns]
V_{CE} fall time 80-20%	63.2		[ns]

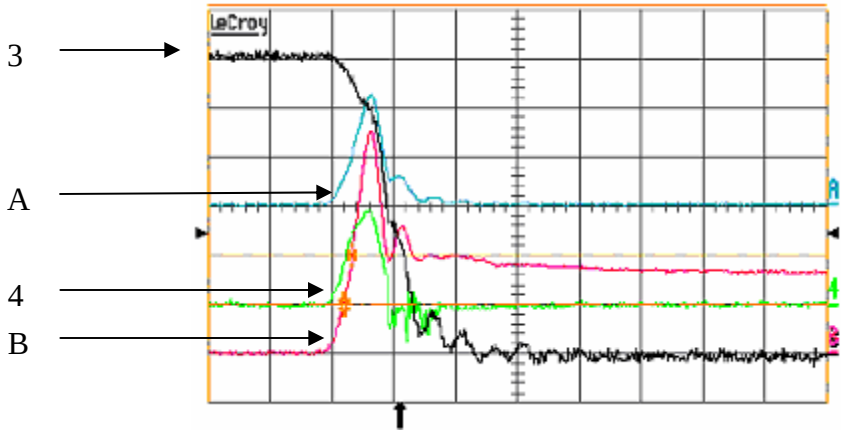

Figure 10 – Turn-on high-side IGBT V_{DC}=600 V I_C=80 A - V_{SS}-COM detail

Channel	Measure Points		Sensitivity
Figure 11	**+**	**-**	**1 µs /div**
3	DC+	Out C	100 V
4	Gate high phase C	Emitter high phase C	5 V
A	I_C*V_{CE}		25 kW
B	I_C = 80 A		50 A
Eoff Area (A)	3.7		[mJ]
I_C fall time 80-20%	15		[ns]
V_{CE} rise time 20-80%	53		[ns]

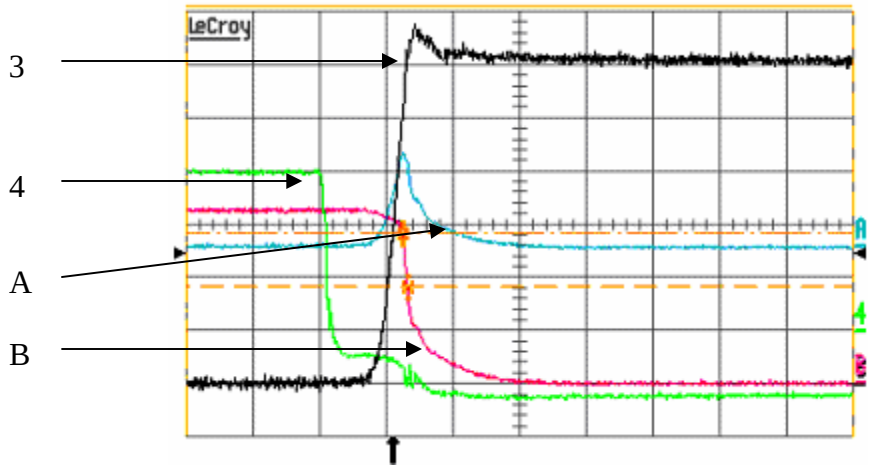

Figure 11 – Turn-off high-side IGBT phase C V_{DC}=600 V I_C=80 A

Channel	Measure Points		Sensitivity
Figure 12	**+**	**-**	**1 µs /div**
3	DC+	Out B	100 V
4	V_S phase C	V_{SS} phase C	50 V
B	I_C = 100 A		50 A
V_{DC}	350		[V]
V_S-V_{SS}	-28		[V]

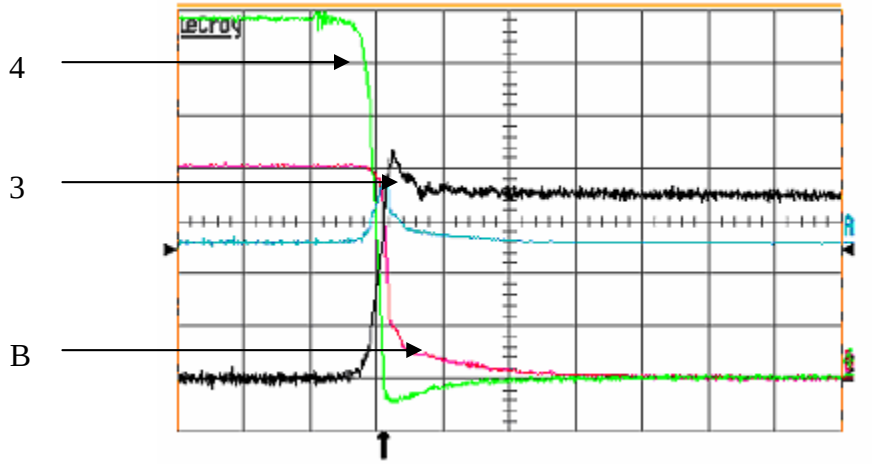

Figure 12 – Turn-off high-side IGBT phase C – V_{DC}=350 V I_C=100 A - V_S-V_{SS} detail – effect of protection circuit

Conclusions

A buffer circuit with negative bias voltage driving capability has been presented for the gate driver families IR2x14(1)SSPBF and IR2x38(1)QPBF. This circuit boosts the power capability of these devices and enables their use in high power applications. The circuit includes negative turn-off for switches and embeds all the new features integrated in these new HVIC families. The proposed circuit has been successfully tested and adopted in a real IGBT inverter application.