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Buck Converter: Negative Spike at Phase Node

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1 Introduction

This application note is discussing the observable negative spike in modern hard-switching step-down converter applications. Ways to deal with the phenomenon and the root cause will be revealed.

2 Circuit Analysis

The negative spike occurs during control-MOSFET (HS-FET) turn-off. The voltage at the phase node falls rapidly, crosses zero and reaches a rather significant negative voltage (perhaps of the same or even higher magnitude as the input voltage of the circuit) for a few nanoseconds before quickly declining.

To understand this behavior the circuit of a step-down converter will be analyzed.

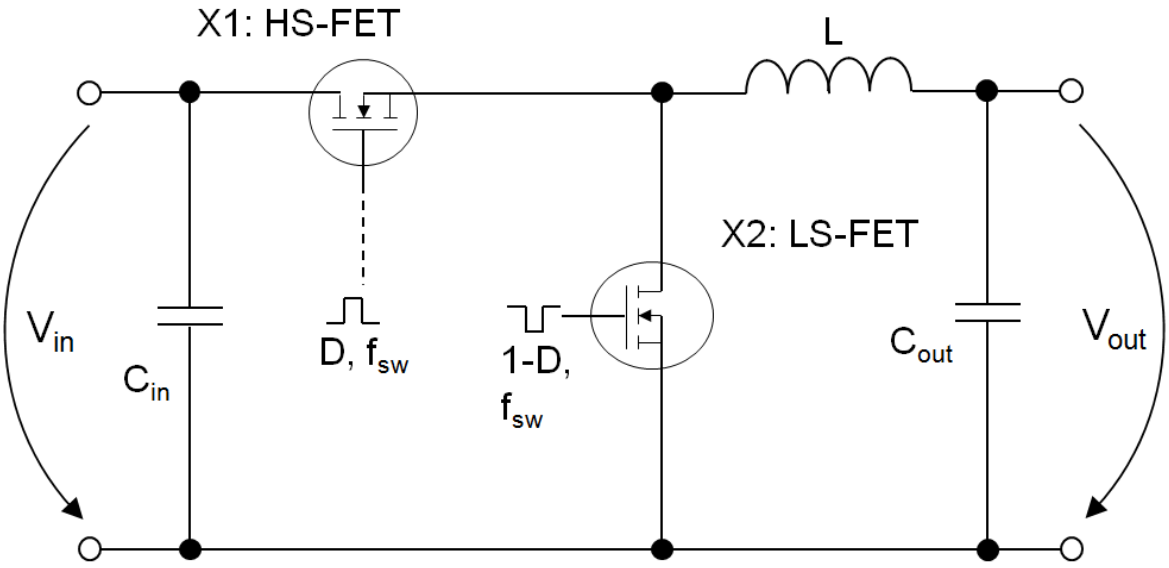

Figure 1 Standard buck-converter with synchronous rectification

X1 represents the HS-MOSFET with its output capacitance. The synchronous rectifier is represented by X2 – also with its inherent output capacitance. During the freewheeling period of the current in X2, the voltage at the phase node is clamped to GND via the body diode of the synchronous rectifier and should never fall below about

-1 V. However, reality shows otherwise. Therefore it can be concluded that the circuit shown in fig. 1 is not representing the elements causing the negative voltage spike to occur. After introduction of parasitic inductances into the critical commutation loop the analysis of the turn-off event reveals the reason for the negative spike (fig. 2).

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An assumption for further considerations is that the voltage drop across X2 is zero as the forward voltage of the body diode (~0.7 V) is small compared to the observable spike

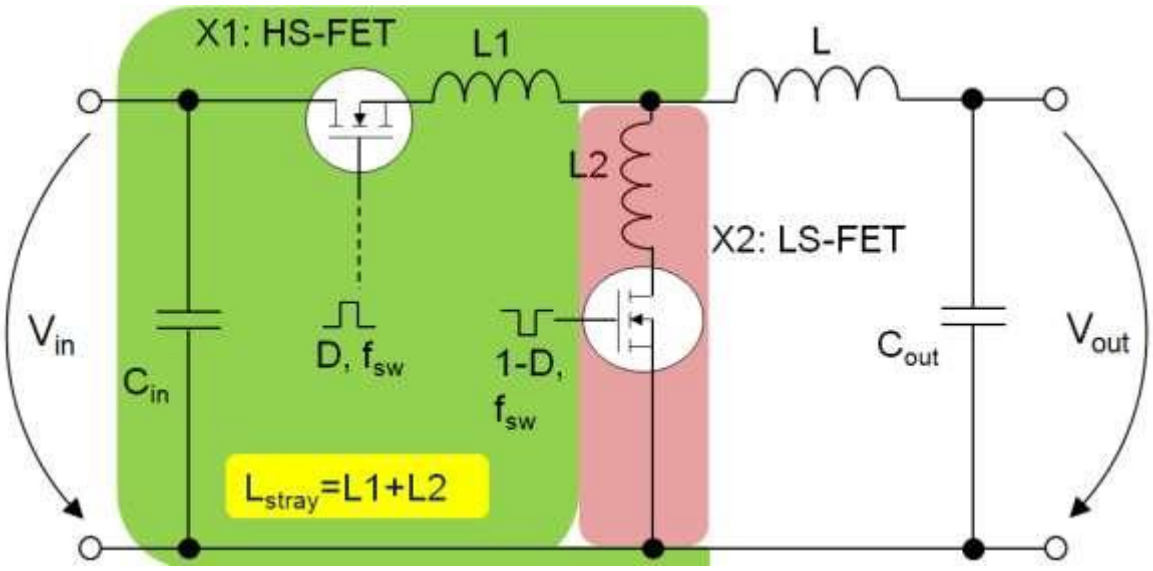

Figure 2 Highlighting the critical loop inductance, i.e. the current commutation path

L_{stray} is the total value of the critical loop inductance consisting of L1 and L2. L2 is the part of L_{stray} that is located in the synchronous rectification path, i.e. between GND and phase node. L1 is the part of the L_{stray} that is not part of L2. Another assumption is that the HS-MOSFET is switching so fast that the current transition is only limited by the stray inductance L_{stray}. This will provide the worst case for the negative spike.

When the HS-MOSFET turns off the current through it will decrease. The resulting di/dt then induces a voltage on the parasitic inductance L1. Since the output current in the inductor L can be considered constant for the switching event the current ramp-up in stray inductance L2 has to occur at the same di/dt as in L1. The induced voltage across L1 and L2 can be that high that in a worst case scenario the HS-MOSFET reaches avalanche breakdown and the voltage is clamped by the MOSFET. In this worst case scenario the MOSFET is represented by a Zener-diode as shown on the right hand side in fig. 3.

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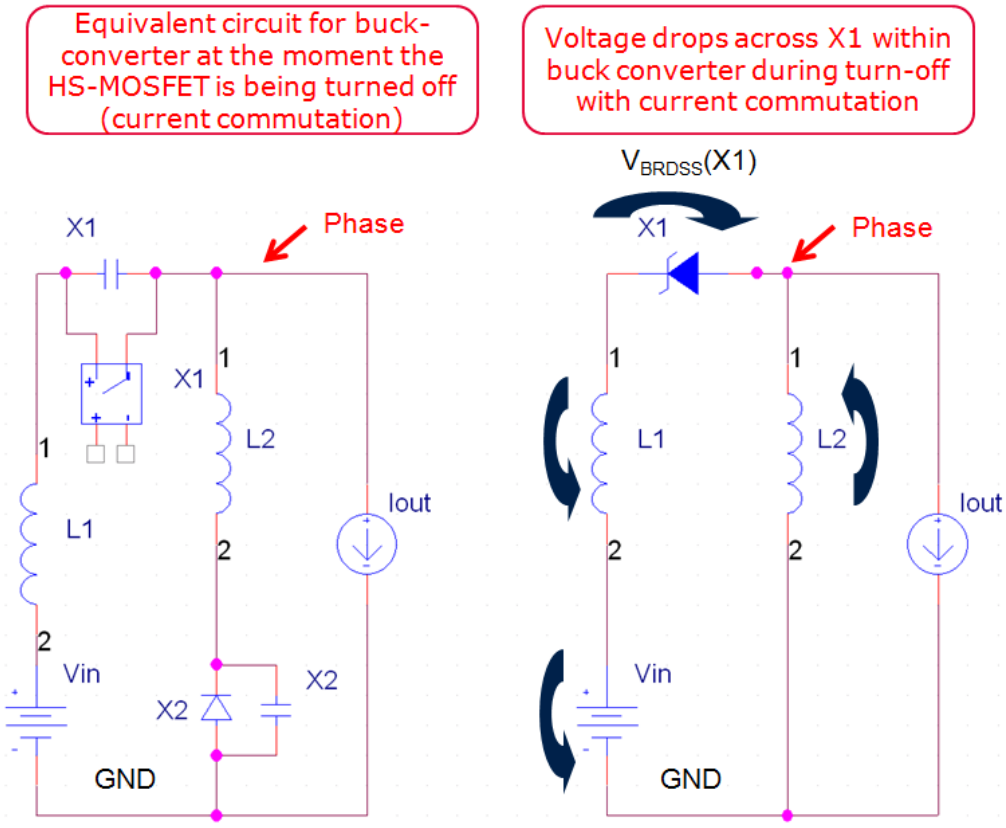

Figure 3 Analysis schematic for negative spike event

The phase node voltage can be calculated by applying the Kirchhoff law for voltages with respect to the phase node:

$$V_{Phase} = V_{in} + V_{L1} - V_{BRDSS}(X1)$$

$$V_{L1} = -L_1 \cdot \frac{di}{dt} \; ; \quad V_{L2} = -L_2 \cdot \frac{di}{dt}$$

$$V_{L1} = V_{L2} \cdot \frac{L_1}{L_2}$$

$$V_{Phase} = V_{in} + V_{L2}\frac{L_1}{L_2} - V_{BRDSS}(X1)$$

$$V_{Phase} = -V_{L2}$$

$$0 = V_{L2}\left(1 + \frac{L_1}{L_2}\right) + V_{in} - V_{BRDSS}(X1)$$

$$V_{Phase} = -V_{L2} = \frac{L_2}{L_{Stray}}\left[V_{in} - V_{BRDSS}(X1)\right]$$

with $L_{Stray} = L_1 + L_2$

It can be seen that undershoot of the phase node voltage depends only on the breakdown voltage of the HS-MOSFET, the input voltage and the distribution of the partial loop inductance in the synchronous rectifier path to the total stray inductance.

In case the MOSFET does not reach avalanche the term VBRDSS(X1) in the above equation can be replaced by the maximum voltage across the MOSFET. This maximum voltage across the MOSFET will always be higher than V_{in} during the turn off event as long as a parasitic inductance L_{stray} is present. Therefore, even in the most common case when the MOSFET is not reaching avalanche (as switching speed is slow and energy stored in the stray inductance can be dissipated in the switching MOSFET while overshoot voltage will be limited by the output capacitance of X2) undershoot at the phase node depends on:

- ratio between L2 and L_{stray}
- input voltage

3 Switching Loss

From the equations above one can see that the only design variables to reduce the negative spike lay within the board layout and package choice for the MOSFETs and capacitors as the choice of the package will influence L_{stray} and its distribution.

To reduce the undershoot voltage L2/L_{stray} should be small. One way to accomplish that is to enlarge L1. This however would be a bad choice as it increases L_{stray} and will lead to more dynamic power loss. The impact of L_{stray} on dissipated energy can be calculated as:

$$E_L = \frac{1}{2} L_{stray} \cdot I_{Peak}$$

This is valid for inductively limited switching, i.e. the current rising and falling slopes are only determined by L_{stray} and not by the MOSFET switching speed. Assuming a peak current of 35 A and a stray inductance of 1 nH the dissipated energy per switching period is:

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$$E_{Switch} = \frac{1}{2} 1nH \cdot 35\ A = 612.5nWs$$

For a buck converter switching at 300 kHz each nanohenry stray inductance corresponds to an increase in switching loss of:

$$P_{Switch} = f_{SW} \cdot E_{SW} = 300kHz \cdot 612.5nWs = 183.75mW$$

Therefore an increase of L1 by 1 nH would decrease the undershoot at phase node but at the same time increase the switching losses by about 180 mW. The only way to achieve the goal of reduced undershoot without sacrificing efficiency is by shifting the existing loop inductance so that L2 is minimized.
In practice this is rather straight forward. Primarily a low inductive advanced package such as SuperSO-8, S3O8 or CanPAK should be chosen. The lowest value for L2 is achieved when:
- the GND return path from the load is entering the source of the LS-MOSFET before reaching the closest input decoupling MLCC and
- the inductor is connected as close as possible to the drain of the LS-MOSFET.

These measures insure lowest undershoot without sacrificing efficiency. Connecting the driver should follow the thinking and take the reference potential also directly from the source of the LS-MOSFET.

Unfortunately many times these considerations are not part of the design process and the undershoot issue will be found once the board is being tested. A typical countermeasure is the addition of an external gate resistor that provides a means to control the speed of the MOSFET. Another way to reduce undershoot is to use a slower older generation FET technology. Indeed, slowing down the switching speed of the MOSFET will effectively reduce the voltage spikes during transient events. However, reducing the switching speed of MOSFETs will increase switching losses and overall system efficiency will drop as can be seen in figure 4.

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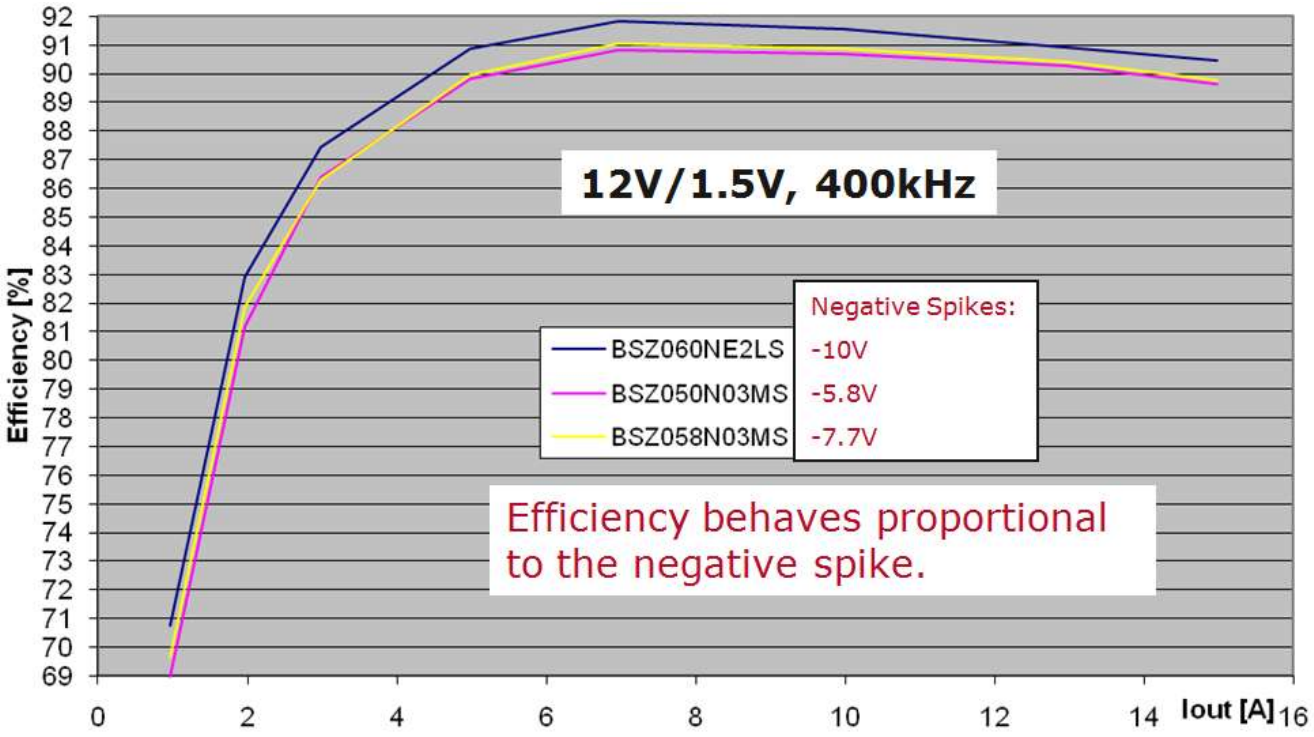

Figure 4 Example of how switching speed impacts the efficiency, RDSON of all parts is about identical and its impact is minor as it can be observed by comparison of BSZ050N03MS (5.0 mΩ @ VGS=10 V) and BSZ058N03MS (5.8 mΩ @ VGS=10 V). BSZ060NE2LS has 6.0 mΩ @ V

4 Detailed Spike Analysis

In fig. 5 the phase node voltage is shown for BSZ060NE2LS. The undershoot voltage reaches -10V as seen in the oscilloscope screenshot. For this particular measurement the following parameters are given:

L_{Stray} = 1 nH	I_{Peak} = 35 A	V_{IN} = 12 V
BSC060NE2LS	Q_{OSS}(12 V) = 5.8 nC	Q_{OSS}(25 V) = 8.9 nQ

Question: When switching extremely fast, what limits the magnitude of the

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spike?

In order to find the answer one has to investigate the energy of the spike and its effects.

Assuming the worst case, i.e. instantaneous switching, all energy stored in L_{stray} is causing the voltage to rise across the MOSFET. Without its output capacitance any MOSFET would reach its breakdown voltage and clamp the voltage until the energy has been dissipated. In reality the output capacitance absorbs energy and a non- infinite value for the spike voltage can be obtained.

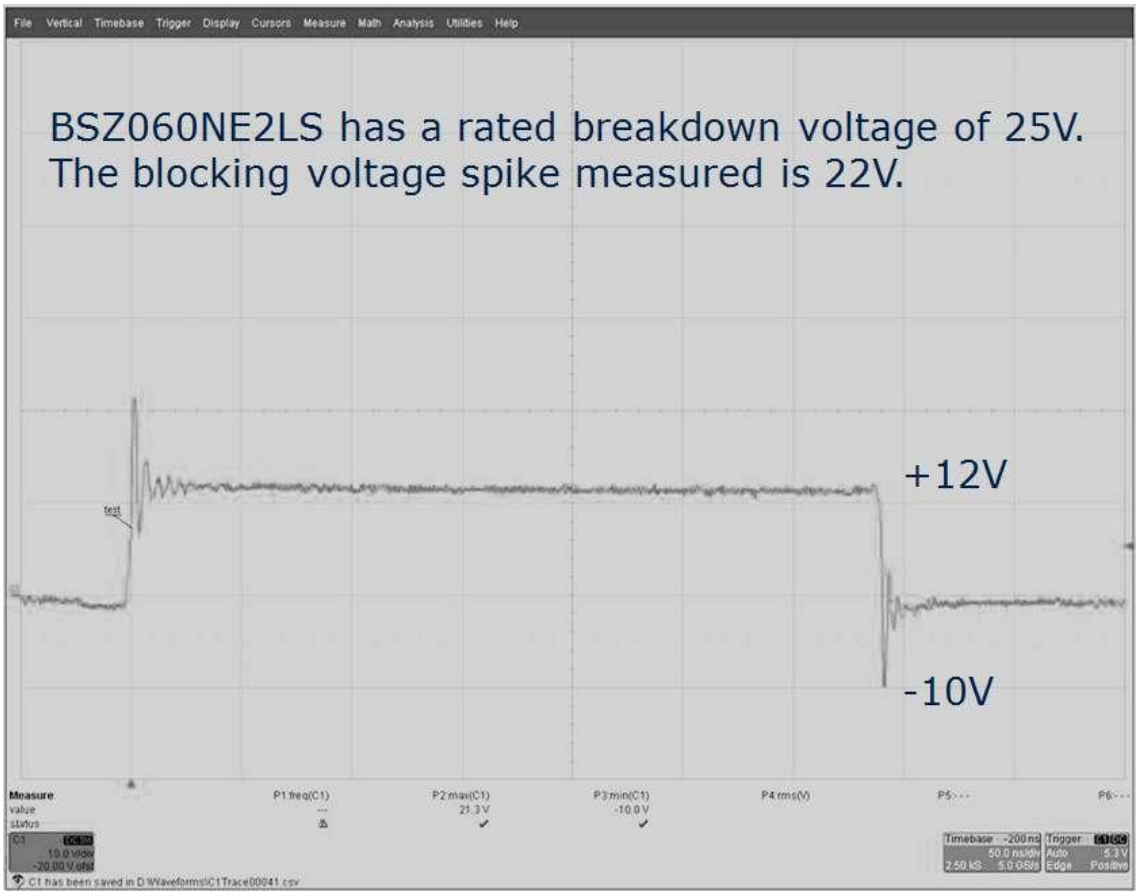

Figure 5 Measured spike

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For the example discussed before the energy dissipated in a switching period (equals the energy E_L stored in L_{stray}) was 612.5 nWs. The output capacitance of the MOSFET holds the energy related to the input voltage:

$$E_{CIN} = \frac{1}{2} Q_{OSS}(V_{IN}) \cdot V_{IN} = 0.5 \cdot 5.8nC \cdot 12V = 34.8nWs$$

At breakdown voltage the output capacitance contains the energy of:

$$E_{CVBRDSS} = \frac{1}{2} Q_{OSS}(V_{NBRDSS}) \cdot V_{IVBRDSS} = 0.5 \cdot 9nC \cdot 25V = 112.5nWs$$

That leaves a fixed amount of energy that can be absorbed by the output capacitance:

$$E_{Absorb} = E_{CVBRDSS} - E_{CIN} = 112.5nWs - 34.8nWs = 77.7nWs$$

Here is the dilemma: 612.5 nWs have to be absorbed by the MOSFET's output capacitance but it is only capable of absorbing 77.7 nWs. The excess energy of $612.5nWs - 77.7nWs = 534.8nWs$

will be dissipated in avalanche.

However, the waveform in fig. 5 does not show any indication of avalanche. That means the energy stored in L_{stray} will be dissipated in another way. In the following it will be shown that the additional power dissipation emanates from increased turn – off loss due to source feedback on the gate drive voltage of the HS-FET.

So far we assumed instantaneous inductive switching during turn-off. In this assumption it is not considered that the source feedback voltage caused by the source inductance of the HS-MOSFET during the turn-off process will effectively slow down the switching speed of the device. To calculate the impact of this feedback mechanism the current slew rate is derived from:

$$di/dt = \frac{V_{BRDSS} - V_{IN}}{L_{stray}} = \frac{25V - 12V}{1nH} = 13A/ns$$

Therefore, the turn-off of 35 A peak current without source feedback would take

$$t_{OFF} = \frac{I_{Peak}}{di/dt} = \frac{35A}{13A/ns} = 2.7n$$

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However there is the need to account for the voltage feedback of the source inductance of the HS-MOSFET.

As an example 15 % of L_{stray} will be assumed as HS-MOSFET source inductance $L_{HS\text{-}source}$ which leads to an introduced gate to source feedback voltage of

$$V_{fb} = -L_{HS-source} \cdot 13A/ns$$
$$= -0.15 \cdot 1nH \cdot 13A/ns = 1.95V$$

With 1.95 V feedback the turn-off becomes delayed and energy is dissipated in the longer transition.

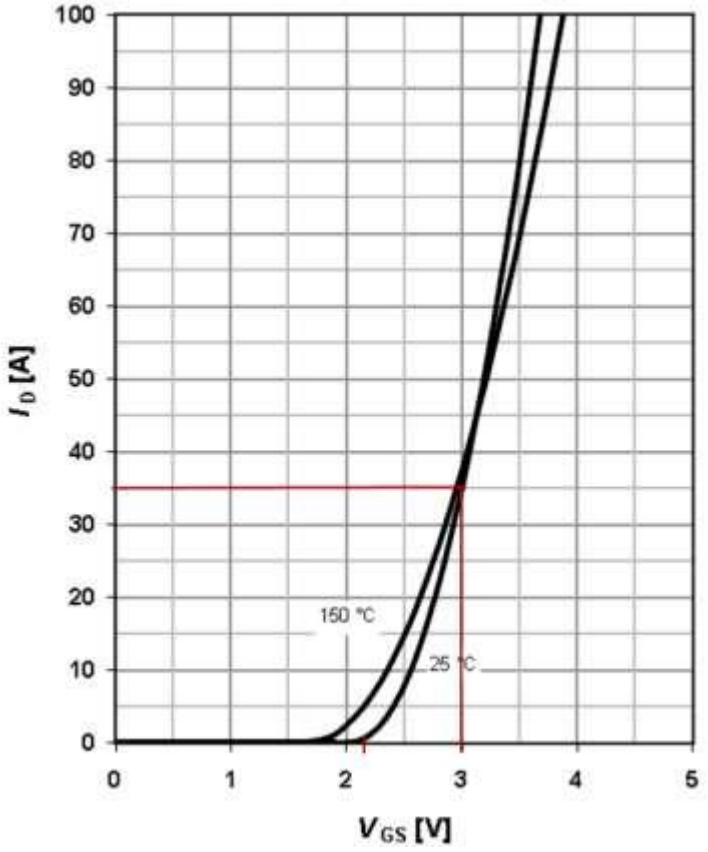

Figure 6 Transfer characteristic of the BSZ060NE2LS (Tj as parameter)

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Transitioning from V_{GS} = 3 V (35 A) to V_{GS} = 2.2 V (~0) in case of the BSZ060NE2LS (see fig. 6) yields the following transition times:

R_{Gtot} = 1.5 Ω C_{iss} = 670 pF $\tau = R_{Gtot} \cdot C_{iss} = 1.5\Omega \cdot 670\,pF = 1ns$ $v = V_0 \cdot e^{-t/\tau}$

No feedback: $t = -\tau \cdot \ln {}^{v}\!/\!_{V} = -1ns \cdot \ln {}^{2.2V}\!/\!_{3V} = 0.31ns$

1.95 V feedback: $t = -\tau \cdot \ln {}^{v}\!/\!_{V} = -1ns \cdot \ln {}^{2.2V - 1.95V}\!/\!_{3V - 1.95V} = 1.43ns$

The commutation starts when the gate-source voltage has reached 3 V.

The maximum energy that will be dissipated in the turn-off process is:

$$E_{trans} = \int V_{DS} \cdot I_D(t)dt = 0.5 \cdot V_{DS} \cdot I_{Peak} \cdot t_{trans}$$
$$= 0.5 \cdot 25\text{V} \cdot 35\text{A} \cdot 1.43\text{ns} = 625.625\text{nWs}$$

That is more than the amount that was not accounted for (534.8 nWs) in the capacitive storage. Hence the MOSFET will not reach its breakdown voltage.

For the case shown here it means:

- The device is working in the optimal range. No avalanche is observed (note that a 25 V rated MOSFET has in fact a higher breakdown voltage which also increases with operating temperature further).
- The small loop inductance (1 nH) enables fast transitions (high di/dt) and leads to small energy dissipation.
- The main portion of the inductive energy is dissipated in the channel of the MOSFET as switching loss. Only a fraction is causing the charge of the output capacitance.
- The small output capacitance causes voltage spikes that are significantly observable but have low energy associated.
- Reliability is not impacted by the spike occurrence because the higher efficiency leads to lower operating temperatures. This will more than compensate for the brief voltage events.

The calculations have been done under the assumption of a SuperSO8 package that has some source feedback. Given the use of a CanPAK with proper routing and driver decoupling the source inductance can be much smaller almost eliminating source feedback voltage which results in higher efficiency.

Specifically with CanPAK a symmetric decoupling can be done reducing the stray inductance well below 1 nH which attributes to very benign voltage spikes overall.

5 Driver

The negative voltage spike at the phase node is connected to the driver IC. Usually driver ICs have sufficiently large ratings for the phase node voltage allowing for negative spikes. However, especially when having 5 V driver ICs, the rating is usually smaller and reason for concerns.
Fig. 7 shows part of the driver output stage connected to the power circuit.

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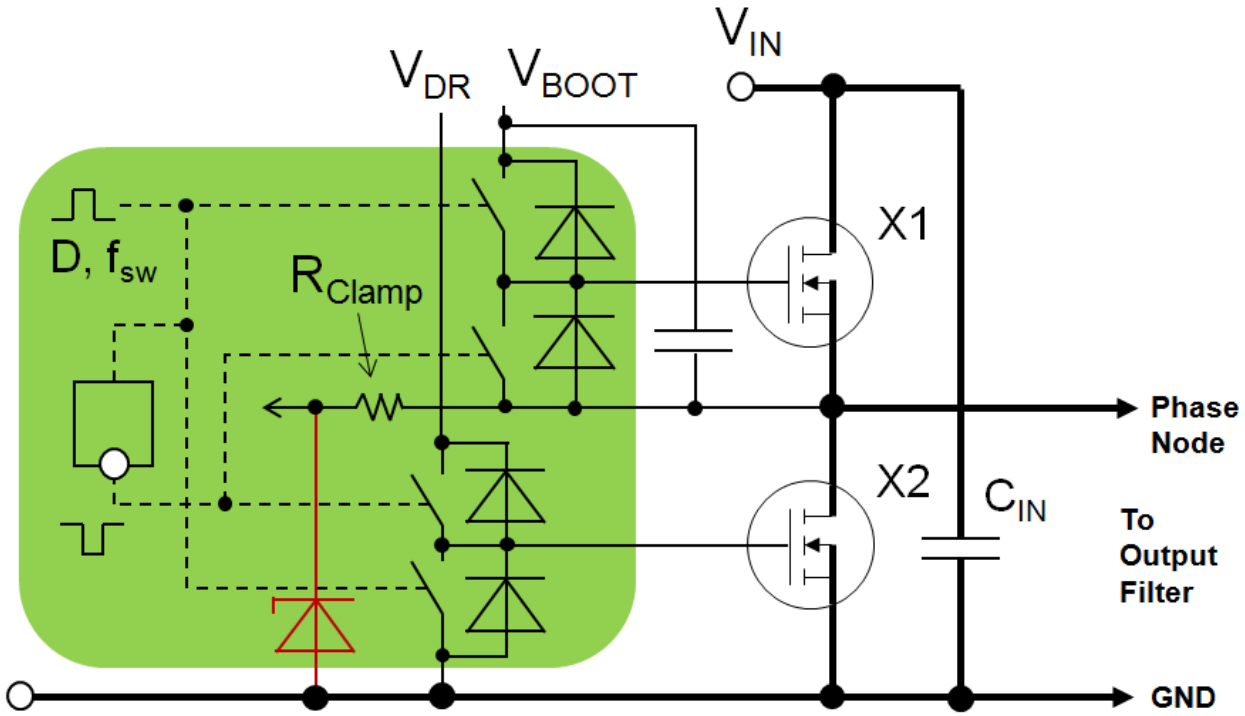

Figure 7 Clamped voltage protection for phase node by (red) clamp structure, voltage drops across R_{Clamp}

The internal phase node voltage is clamped by a dedicated clamp structure consisting of a resistor R_{Clamp} and a Zener-Diode. The capability of how much energy can be absorbed by this clamping structure depends on the permissible power dissipation of R_{Clamp} and the Zener structure.

The driver datasheet usually specifies a permissible negative (and positive) voltage that can be applied for a limited time at the phase pin and exceeds the max DC rating for that pin. This indicates the presence of an internal clamp structure. In practice the spike magnitude is often bigger but the time of exposure much shorter than the stated datasheet conditions. In such a case the dissipated energy per cycle has to be considered and compared with the maximum allowable per cycle energy dissipation of the internal clamp structure. As an example here is an excerpt of a driver datasheet specifying the following:

- V_{VCC} = -0.3…+6.5 V
- V_{PVCC} = -0.3…+6.5 V
- V_{Phase} = -1.0…+30 V
- $V_{Phase\text{-}pulsed}$ = -10….+35 V for t_{pulse} < 30 ns
- f_{sw} = 0.1…2 MHz

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Based on the DC vs. pulse rating for the positive spike one can conclude that the clamp structure can sustain additional +5 V for 30 ns on a cycle by cycle base for up to 2 MHz switching frequency across its clamp resistor compared to the DC rating.

$$E_{RClamp} = \frac{V_{RClamp}^2}{R_{Clamp}} \cdot t_{Pulse}$$

The energy across the clamp resistor can be calculated as:

That implies that a spike of double magnitude but a quarter of the pulse length compared to the maximum datasheet rating will result in the same dissipated energy across the clamp resistor.

The total power dissipation of the clamping structure is: $E_{Clamp} = V_{Spike} \frac{V_{Spike} - V_{Clamp}}{R_{Clamp}} \cdot t_{Pulse}$

For shortened pulse duration the spike voltage of identical energy can be obtained as:

$$V_{Spike} = \frac{V_{Clamp}}{2} + \sqrt{\frac{V_{Clamp}^2}{4} + \frac{E_{Clamp} \cdot R_{Clamp}}{t_{Pulse}}}$$

On the concrete example the maximum clamping energy is: $E_{Clamp} = 35V \cdot \frac{35V - 30V}{R_{Clamp}} \cdot 30ns = \frac{5250nV^2 s}{R_{Clamp}}$

Assuming a spike duration of 5 ns instead will permit a maximum spike voltage of:

$$\begin{aligned} V_{overshoot} = V_{Spike} - V_{DCrating} &= \frac{30V}{2} + \sqrt{\frac{(30V)^2}{4} + \frac{5250nV^2 s}{5ns}} - 30V \\ &= 15V + 35.7V - 30V \\ &= 20.7V \end{aligned}$$

Using the same energy in the claming resistor the spike voltage for the negative spike can be calculated as:

$$^{2}_{Spike} - 2V_{Spike} \cdot V_{Clamp} \quad ^{2}_{Clamp} - \frac{E_{Clampmax} \cdot R_{Clamp}}{t_{Clamp}} = 0$$

$$V_{Spike} = V_{Clamp} + \sqrt{\frac{E_{Clampmax} \cdot R_{Clamp}}{t_{Clamp}}}$$

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$$V_{Undershoot} = V_{RClamp} = V_{Spike} - V_{Clamp} = \sqrt{\frac{750nV^2s}{5ns}} = 12.2V$$

Usually these negative spikes are in the 1 ns ... 4 ns range. Therefore it can be concluded that the driver operates very reliably although the driver specification does not account for that condition. Still it should be checked with the driver manufacturer whether there are other reasons that might prevent the driver from operating under high negative spike conditions.

Another important aspect for the driver is the way it is connected to the power MOSFETs.

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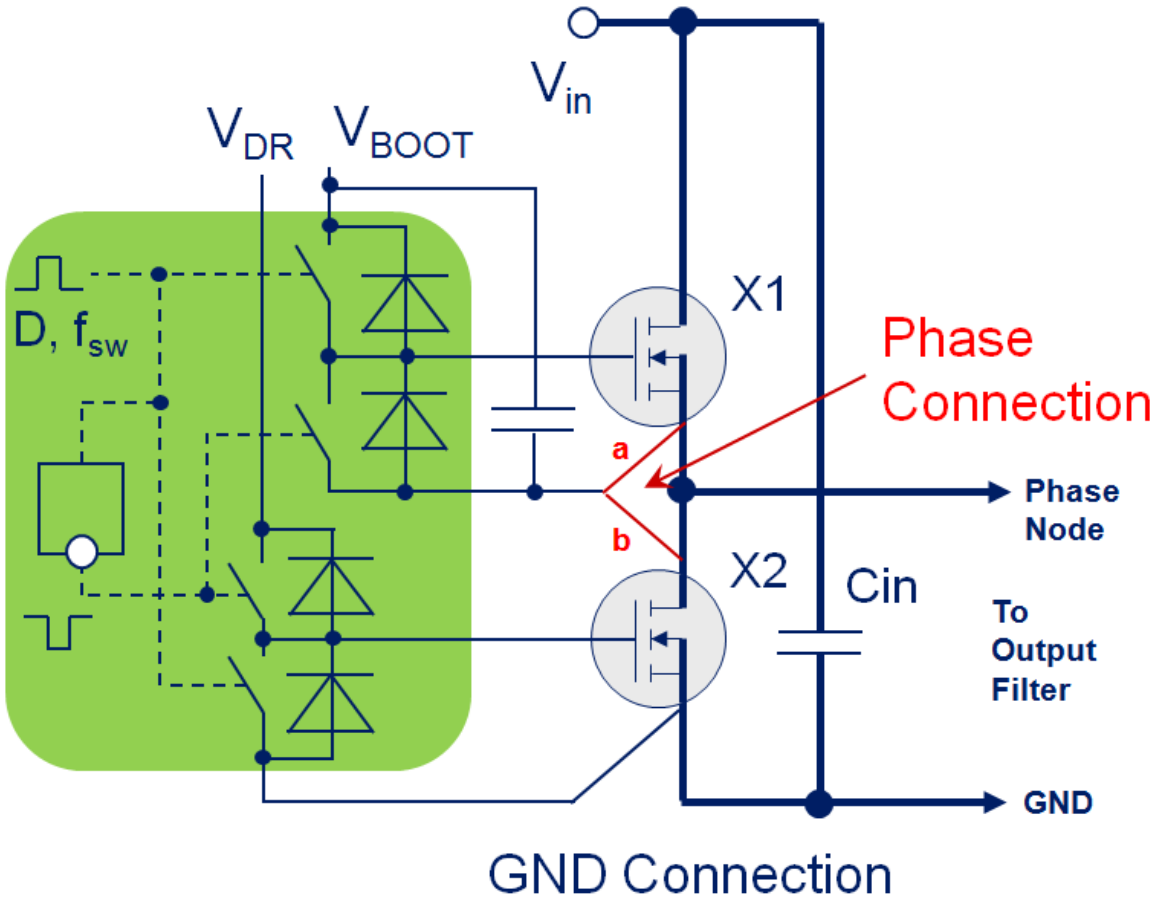

Figure 8 Ground and phase node connections impacting negative spike observable by the driver

The ground connection between driver and power stage should be done in the way depicted in fig. 8, i.e. the driver ground should be connected to the synchronous rectifier MOSFET directly without having a current path in common with the power circuit. This reduces the L2 contribution to the package of X2.

For the phase connection of the driver the following has to be considered: Making connection “b” instead of “a” (see fig. 8) reduces the L2 contribution to the package of X2 on the phase node side and therefore will reduce the negative undershoot as explained in section 1. However, all parasitic phase node inductance will be source feedback for the control FET X1 and hence slow down the switch. That in return will increase switching losses

and efficiency will suffer significantly.

The only solution to reduce the negative spike level and keep efficiency high is to choose connection “a” while keeping the switching node interconnect between both MOSFETs as small as possible.

6 Summary

As shown the phenomenon of strong negative phase node spikes is part of fast switching modern voltage regulators. It is mainly caused by the fast commutation of the switched current in the critical loop combined with a specific distribution of parasitic inductances.

For integrated devices such as DrMOS, the current commutation speed (di/dt) can be significantly higher than for discrete MOSFETs. At the same time the MOSFETs in these integrated devices are almost ideally coupled to the driver with very little source feedback. That makes the negative spike issue for DrMOS (and other integrated devices) virtually nonexistent for the driver.

For discrete designs it is important to follow these basic design rules:

- Keep the commutation loop as small as possible to allow for lowest inductive energy in the circuit
- Minimize the partial loop inductance in the synchronous rectifier path to achieve the lowest negative spike
- Couple the driver ground as closely to the synchronous rectifier ground as possible, connect it in Kelvin style, i.e. avoid common current between the driver ground connection and the power ground current flow
- Do not compromise switching speed for the sake of lower spike unless there are no other options.