Bringing GaN on Si Based Power Devices to Market

The Status of the GaNpowIR™ platform at International Rectifier

The availability of new power electronics based on commercially viable wide band gap semiconductors such as GaN on silicon power devices fabricated in silicon foundries, provides the required performance to cost value proposition to enable lower economic barrier to adoption for energy efficient power delivery architectures needed to significantly reduce global energy consumption in the coming decades.

By Michael A. Briere, ACOO Enterprises LLC, under contract by International Rectifier

It is well established that due to increases in standard of living throughout the world, total energy con-sumption is expected to increase by at least 35 % over the next 20 years [1].

It is less well known that a significant reduction in worldwide energy consumption can be achieved through the wide spread adoption of improved load architectures [2,3]. In total, over 25 % of worldwide annual energy consumption can be saved through widespread (i.e. >90 %) adoption of these efficient load technologies enabled by advanced power electronics. This energy conservation represent over $ 2 Trillion/year in cost savings (at $ 45/barrel oil prices), far greater than the approximately $ 50 Billion/year market for power electronics today.

The energy savings are, for the most part, achieved through the nature of the working load, though the performance of the loads requires substantial, optimized and intelligent power electronics. Even though both the required loads and the necessary power electronic architectures are, in principle, presently available to implement these energy saving solutions, adoption is expected to remain relatively anemic for at least another decade. This is due to the price premium which is passed to the end consumer of the complete systems incorporating these energy efficient solutions. Only when this premium is substantially reduced or eliminated, will the adoption of energy efficient systems approach dominance, a necessary requirement for substantial worldwide energy savings. The reduction of total system costs can be substantially enabled by intelligent power electronics which optimize performance/cost.

Modern power electronics solutions provide an array of system level enhancements such as communi-cation protocols, load condition reporting, as well as optimal balancing and coordination and protection of power conversion sub-systems and loads. As important as these advances have been, it is the continued progress in the performance of the power converter sub-systems themselves that have enabled increasingly dense and efficient working loads.

Value in Power

It can be argued that the intrinsic value proposition of the power conversion sub-systems is den-sity*efficiency/cost. This performance/cost figure of merit (FOM) for power processing is the equivalent driving force behind innovation as the logic unit/ $ FOM is to the well known Moore's law of the data processing industry. There have been significant advancements in both FOMs over the past 40 years. It can be argued that the most significant advances in energy conversion efficiency* density/cost have been achieved through requisite improvements in the power devices used. Generally, advances through improved circuit architectures, from linear to switching regulation, hard to soft switching, passive to synchronous rectification, etc., have all been accomplished by leveraging the inherent capabilities and avoiding the inherent limitation of the power switch components used. It can therefore be expected that radically improved power switch performance might well drive a revolution in power electronic architec-tures and systems.

The ability of power semiconductor devices to enhance the power electronics performance/cost figure of merit can be simplified by its own price/ performance figure of merit, namely switching power loss* ohmic power loss *cost, where the switching power loss reflects the thermal limitation of density, most often achieved through increasing switching frequency and subsequent reduction in output filter components. For inverter circuits this can be referred to by Ets* Vceon*cost, for silicon based IGBT switch/ di-ode pairs. For dc-dc converter circuits such as common buck regulators, the FOM is R(ds)on*Qsw*cost.

Since the advent of commercially viable silicon power FETs, introduced some 30 years ago, enabled the widespread adoption of switch-mode power supplies, replacing the linear regulator as the dominant power architecture, the silicon power FET has become the dominant power device. The silicon based IGBT, combining the ease of charge control with the benefits of conductivity modulated drift resistivity, has been another mainstay, especially in the lower frequency conversion systems, e.g. motor drive inverters. Of course, the same minority carrier injection that provides for lower ohmic losses also increases switching losses through the effects of subsequent tail currents. Over the last 3 decades significant engineering efforts have driven the improvement in the performance figure of merit of these silicon power devices by more than an order of magnitude. However, as this technology approaches maturity, it becomes increasingly expensive to achieve even modest improvements in the device FOM. It is estimated that less than a factor of two improvement will be economically feasible to achieve for 30 V FETs [4], with perhaps a factor of five possible for 600 – 1200 V silicon IGBTs [5].

If further advances in power device performance are required by future electronic loads, as is currently apparent, then these advances must be achieved through the use of alternative materials. Necessary further advances in power device performance must be achieved through the use of alterna-tive materials. One of the most promising alternatives to silicon is gallium nitride based power devices.

Even though the basic GaN HEMT transistor was first invented over 15 years ago by M. Asif Khan [6], significant development efforts on practical power devices using GaN-on-Si technology have been fairly recent, predominantly in the past 5-7 years. GaN based power devices are expected to improve rapidly over the next 10 to 20 years. In fact, it is expected that an order of magnitude in improvement in the key device performance FOMs will be achieved over the next five years.

In addition to efficiency improvements, the use of wide band gap semiconductors instead of state of the art silicon based devices for power electronic systems allows the reduction of size/weight of the conver-sion subsystems by between 2 and 10 fold, due to significant reduction in cooling system requirements, further promoting adoption.

Commercialisation Barriers Overcome

There have been however, several significant barriers to the commercialization of GaN based power devices. Chief amongst these is the cost of production. The production of power devices includes the costs of substrate, epitaxy, device fabrication, packaging, support electronics and development.

The viable economic based limit of about $ 3 / cm2 for substrate and epitaxy cost set by the power de-vice marketplace is exceeded by all substrate choices except silicon wafers.

Next to the cost of substrate and epitaxial layers, device fabrication costs are the most critical. In fact, currently, substrate diameters of at least 150 mm are required to achieve widespread commercial viability for power device fabrication. To gain broad adoption of alternative material based power devices, fabrication costs must approach that of silicon based power devices. Such device fabrication costs are only achievable if high volume (> 10,000 wafers/week), high yielding standard (silicon compatible) semiconductor fabrication lines are used. Similarly, the volume necessary to support the broad power device market (10 million 150 mm wafer equivalents per year) requires scalability in device manufacture provided most readily by existing silicon device fabrication facilities and silicon substrate supply.

One example of a technology program that has been developed to address these issues is the GaN-powIR platform of International Rectifier [3]. This technology platform uses GaN-on Si hetero-epitaxy and device fabrication processing that can be performed in a standard modern silicon CMOS manufacturing line with little modification to equipment or process discipline. Therefore, this technology platform is able to provide power devices with compellingly superior performance/cost FOMs compared to silicon which will promote widespread adoption.

One of the most fundamental challenges to the commercialization of GaN based power devices is the development of cost effective, high yielding, high throughput III-Nitride epitaxial processes on large diameter silicon wafers. The intrinsic mismatch in both lattice constant and thermal coefficient of expan-sion with the requisite III-Nitride epitaxial films causes threading dislocations, as well as significant macroscopic film stresses, which result in excessive wafer bow and plastic deformation (cracks) in the films. These issues have been addressed by engineering the proprietary epitaxial film growth on standard thickness (625 um) 150 mm (111) silicon wafers to both eliminate most of the threading dislocations, resulting in 109 cm-2, predominately edge dislocations for 2 um thick films (comparable to similar thickness films grown on SiC), as well as compensating for the stresses due to thermal coefficient mis-matches. These result in a high quality device layer. In addition, the resulting wafer bow of < 20 um (3 sigma), is well within the required limit for device fabrication of < 60 um. It should be noted that truly crack free material to within 0.5 mm of the wafer edge are consistently produced by this process in manufacturing volume

GaNpowIR devices

Much of the reported constructions for GaN devices to date utilize Schottky gates and subsequently ex-hibit device leakage in operation of mA/mm of gate width. For a power device, which often has an effec-tive gate width on the order of 1 meter, such gate leakage would result in an unacceptable power loss/heating. Similarly, the maximum operating voltage has often been specified at reverse bias source-drain current densities of mA/mm of gate width. Another challenge, therefore, is the reduction of these leakage currents to less than 1 uA/mm. This has been achieved through the combined use of a pro-prietary insulated gate construction and improved III-Nitride epitaxial film quality. This has resulted in gate and drain-source leakages of 10 pA/mm, as shown in Figure 1. A punchthrough limited S-D breakdown of > 40 V is seen for Vg= -20V, for these devices, with Lg=0.3 um and gate-drain and gate-source spacing of 1 um.

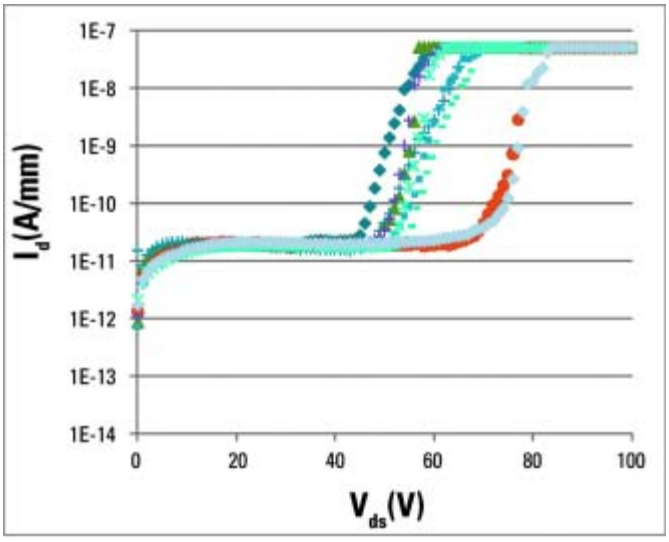

Figure 1: Reverse bias drain leakage behavior for LV GaNpowIR device (Lg=0.3 um) at room tem-perature.

The first product release to production in early 2010 on the IR GaNpowIR technology platform is a 30 A capable 12V buck converter power stage product, the iP2010. It incorporates the control and synchro-nous rectifying switches together with the intelligent gate driver in a low parasitic LGA package. Figure 2 shows the measured power conversion efficiency for this first generation low voltage GaN product com-pared to competitive silicon based solutions. As can be seen, the GaN based power device solutions offer significant advantages over silicon based alternatives. The devices from this first generation GaNpowIR low voltage platform achieved the targeted performance figure of merit (Ron*Qg) of 30 mohm-nC (packaged). Next

generation low voltage devices are expected to exhibit less than 20 mohm-nC with comparable state of the art silicon devices still above 40 mohm-nC.

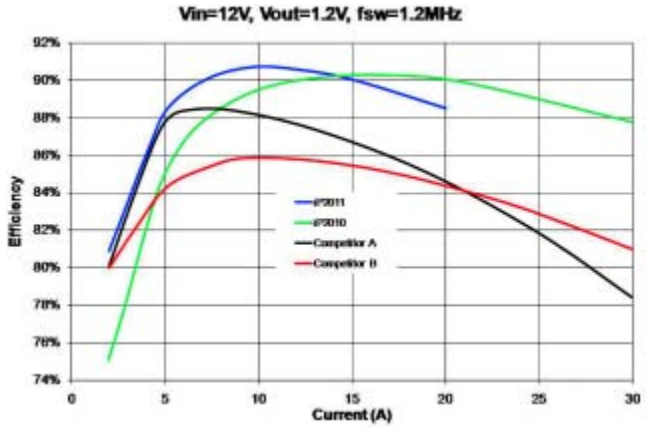

Figure 2: Measured power conversion efficiency for initial GaNpowIR product,iP2010 and planned product iP2011, 12 Vin to 1.2 Vout POL converter power stages operating at 1200 kHz compared to es-timated performance of two silicon based alternatives

These devices are very rugged in their intended application of 12V to 1 V buck regulators, as can been seen in Figure 3, where the forward biased safe operating area (FBSOA) is shown for such low voltage power devices, far exceeding the requirements of the application. The resulting ratio, for these 850 mm gate width device, of Ion/Ioff of > 10 10 is substantially better than reported elsewhere for GaN based devices.

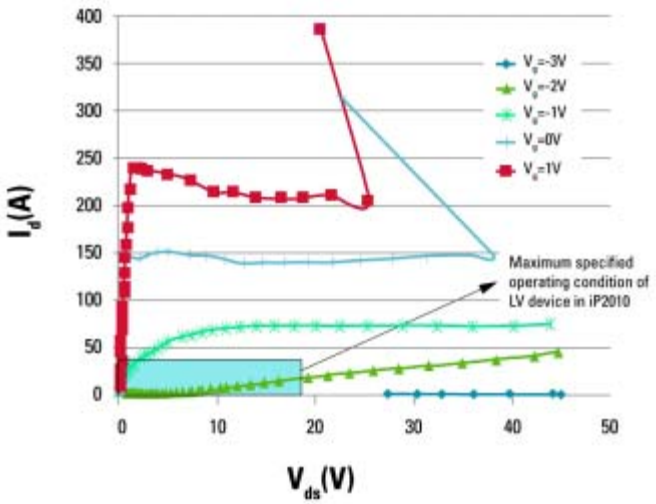

Figure 3: Forward biased SOA for low voltage GaN based power devices intended for 12Vin power conversion applications.

Similarly, early 600 V GaNpowIR devices exhibit off-state leakage currents less than 50 nA/mm (with Vg=-10V), far better than the 100 to 1000 uA/mm reported elsewhere, providing an Ion/Ioff ratio of > 10 7, where Ioff is measured at 600 V.

As is the case in SiC based unipolar devices, GaN based HEMT exhibit negligible minority carrier in-duced reverse recovery charge. The resulting transient reverse recovery current is determined essentially by capacitive components. This leads to much more desirable characteristics as shown in Figure 4, where the GaN based device exhibits nearly an order of magnitude better performance than silicon based alternatives. In this way, the greatest advantages achieved through the use of expensive SiC dio-des in the removal of harmonic filtering snubber circuits in applications such as power factor correction AC-DC converters can be likewise achieved through the use of much less expensive GaNpowIR rectifier products.

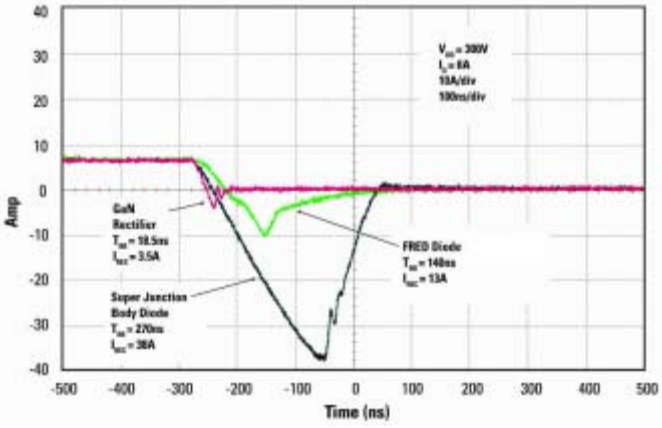

Figure 4: Transient reverse current measurements for 600 V GaNpowIR HEMT, Si Fast Recovery di-ode and Si superjunction FET body diode.

This advantage of low switching losses can further be seen in the on-off transition induced losses for 600 V GaNpowIR HEMTs (Eoff) at 24 uJ, as compared to that of state-of-the-art silicon based superjunction FETs, 38 uJ, and best in class, low loss silicon IGBTs at 144 uJ (tested at 300V and 6A). In fact, even in this early stage of development, GaNpowIR switches exhibit at least a factor of 4 improvement in the Vceon*Esw figure of merit vs state of the art silicon based alternatives.

One approach to provide GaN based products with drop in replacement capability in existing power electronic systems is the cascade of a low voltage silicon device and a high voltage GaN HEMT. This provides normally off behavior with a well established, robust drive interface. The transfer characteristics of such a prototype is shown in Figure 5, exhibiting a Vt of about + 3V, consistent with today's HV switch applications. Figure 6 shows the output characteristics for this same pair, providing well behaved on-state behavior.

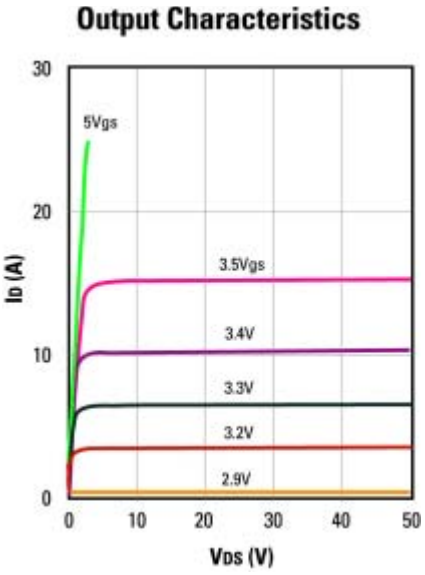

Figure 5, Transfer characteristics for a proto-type cascade pairing of a low voltage silicon FET and an early 600 V GaNpowIR HEMT.

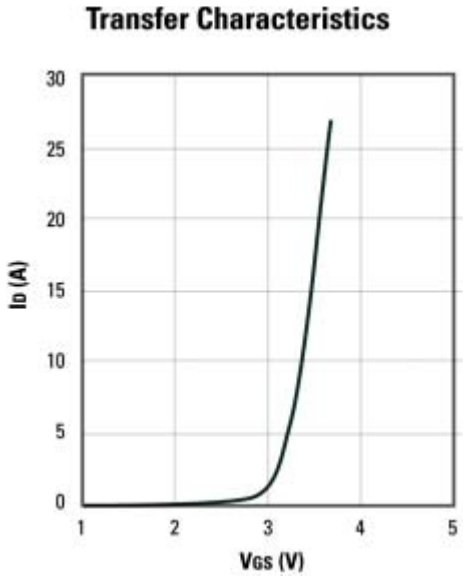

Figure 6, On-state output characteristics for a proto-type cascade pairing of a low voltage silicon FET and a 600 V GaNpowIR HEMT

Device yield is an important challenge for the commercialization of large area power devices. It is eco-nomically imperative that yields > 80 % are commonly achieved for large devices (e.g. > 10 mm2). Such yields have been demonstrated achievable using this technology platform, demonstrating the ne-cessary level of process maturity for commercialization.

Finally, the stability of device in-circuit performance is a prerequisite to commercialisation. The critical FOM, Rdson shows excellent stability under accelerated conditions for > 6000 hrs. In fact, over 7,000,000 device hrs of reliability testing, with up to 9000 hours per device, has shown performance in line with silicon based device specifications. Figure 7, shows the excellent stability of the gate dielectric, measured at Vg=-7.5V, rated at -8.5 V max for low voltage devices, under extreme accelerated stress conditions of Vg=-50 V at 150 C for over 3000 hrs.

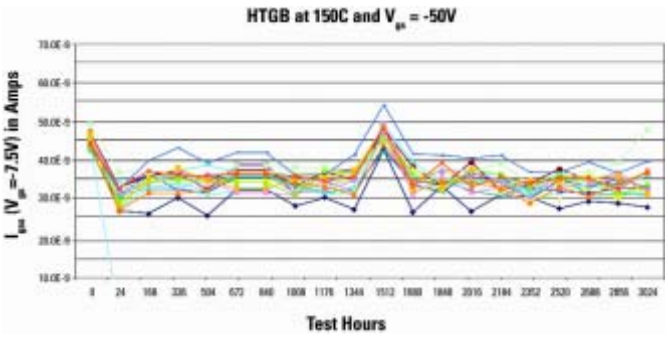

Figure 7: Stability of gate leakage current over 3000 hrs with -50 V applied to the -8.5 V rated gates at 150 °C. Lg= 0.3 um, Wg= 2600 mm.

Drain leakage current has also proven very stable under 26 V reverse bias stress with Vg=-7V at 175 C for over 3000 hrs. Importantly, Figure 8 shows that no physical degradation in the AlGaN barrier layer is found at the gate edge under all applied stress conditions. In addition to conditions already identified, this includes (a) Vd=26 V, Vg=-14 V at 150 C) for > 3000 Hours, (b) Vd= 34 V, Vg=-22 V at 150 C > 600 hrs, (c) forward conduction of I=200 mA/mm with Vd= 25 V. This is significantly better than results reported elsewhere for GaN based HEMTs [7]. This is expected due to the significantly reduced gate leakage currents found when using a gate dielectric instead of a metal-semiconductor gate construction.

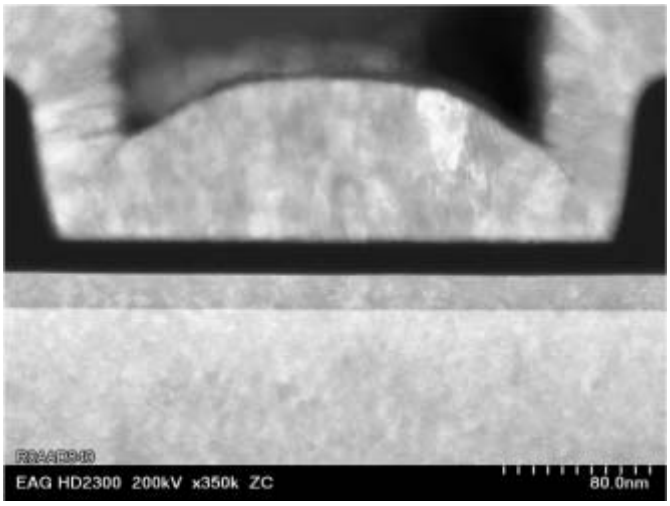

Figure 8: TEM cross section of low voltage device gate region, showing no degradation at gate edge of AlGaN barrier after 3000 hrs under stress at 26 Vds and -7Vgs condition at 175 C.

Conclusion

A great opportunity exists to significantly impact future global energy consumption, with its many socio-logical, environmental and economic consequences. A cost effective means of producing GaN based power devices will help achieve the necessary adoption rates to meet this challenge. International Recti-fier's GaNpowIR platform is such a technology platform, demonstrating required performance from 20 to 600 V devices. Excellent device stability and long term reliability performance has been shown for initial low voltage power devices.

References

www.eia.doe.gov/iea
Lidow, A., APEC 2005 Planery Talk and Briere, M.A., S2k Conference 2005
M.A. Briere, Proceedings of PCIM Europe 2009 and Briere, M.A., Power Electronics Europe (7), October / November 2008 pp. 29-31
Ikeda et.al. ISPSD 2008 p. 289
Nakagawa, A., ISPSD 2006 p.1
Khan, M.A. et.al, Appl. Phys. Lett (63) p.3470, 1993.
J. Joh and J del Alamo, IEDM 2006 p1-4

www.irf.com