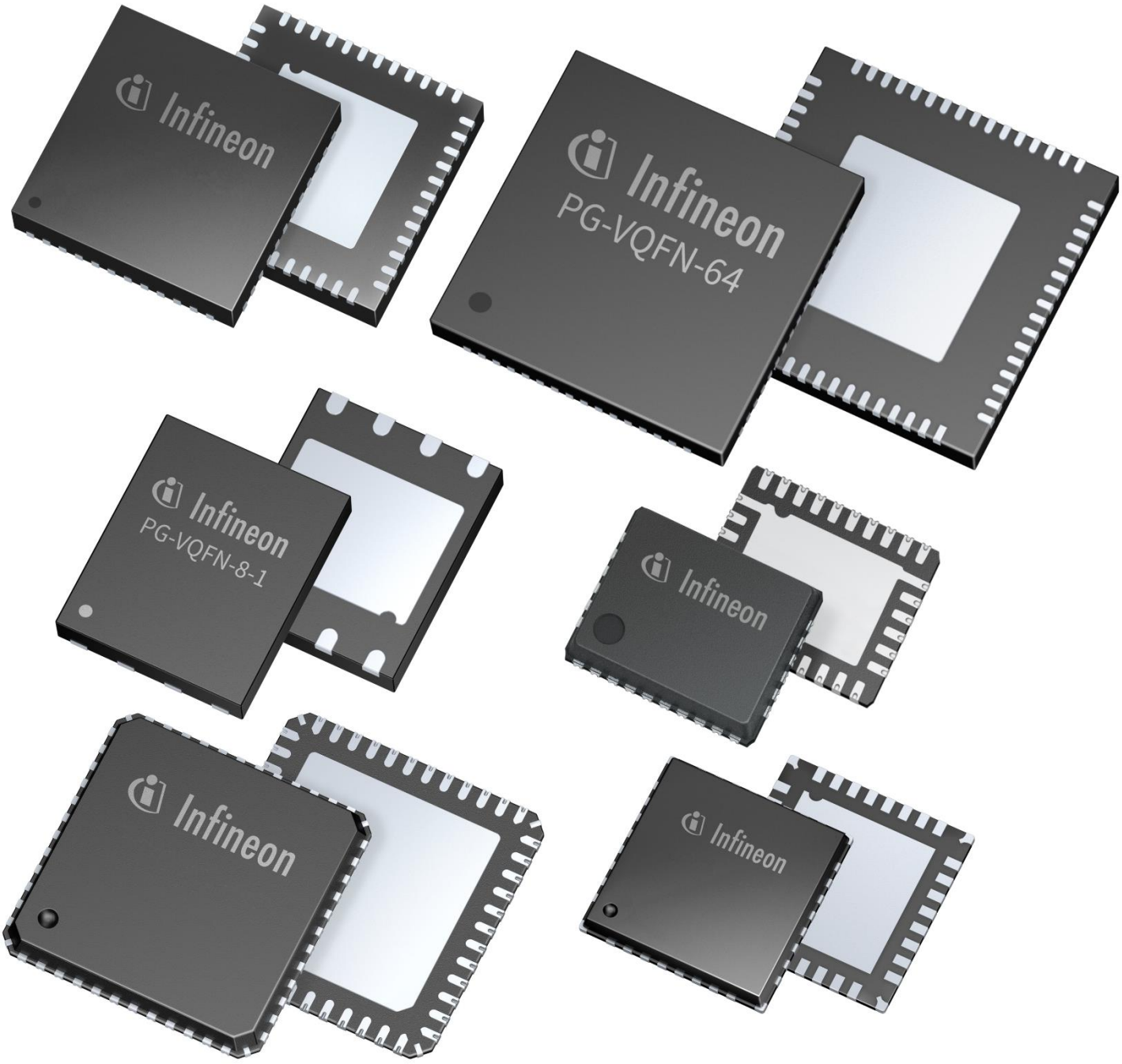
Recommendations for Board Assembly of Infineon Discrete Quad-Flat No-Lead Packages



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Acronyms and Abbreviations

AOI	Automated Optical Inspection
AXI	Automated X-ray Inspection
ChSn	Chemically deposited matte tin
DFN	Dual-Flat No-Leads
ESD	Electrostatic Discharge
IQFN	Integrated Quad-Flat No-lead
LTI	Lead Tip Inspection
MSL	Moisture-Sensitivity Level
Ni/Pd/Au	Nickel/Palladium/Gold
NSMD	Non-Solder Mask Defined
PG	Plastic Green
PCB	Printed Circuit Board
PPF	Pre-Plated lead Frame
QFN	Quad-Flat No-lead
SAC	Tin Silver Copper (SnAgCu)
SMD	Solder Mask Defined
SMD	Surface-Mount Device
SMT	Surface-Mount Technology
TSLP	Thin Small Leadless Package
TSNP	Thin Small Non-leaded Package
UQFN	Ultra thin profile Quad-Flat No-lead
VQFN	Very thin profile Quad-Flat No-lead

1 Package Description

This document provides information about the Surface Mount Technology (SMT) board assembly of discrete device Quad Flat No-lead packages (QFN). This document does not discuss Integrated Quad-Flat No-lead packages (IQFN) or Thin Small Leadless/Non-Leaded Packages (TSLP/TSNP). These package families are described in separate documents.

1.1 QFN Package Type

The Infineon QFN package family includes different thickness variants such as Very thin profile (VQFN) or Ultra thin profile (UQFN). Package versions such as VQFN-8 or VQFN-10 with terminals on only two sides are also called Dual Flat No-Lead packages (DFN). **Figure 1** shows examples of the discrete device QFN package family.

- PG-UQFN packages
- PG-VQFN packages

PG = Plastic Green
V = Very thin profile
U = Ultra thin profile
QFN = Quad Flat No-lead

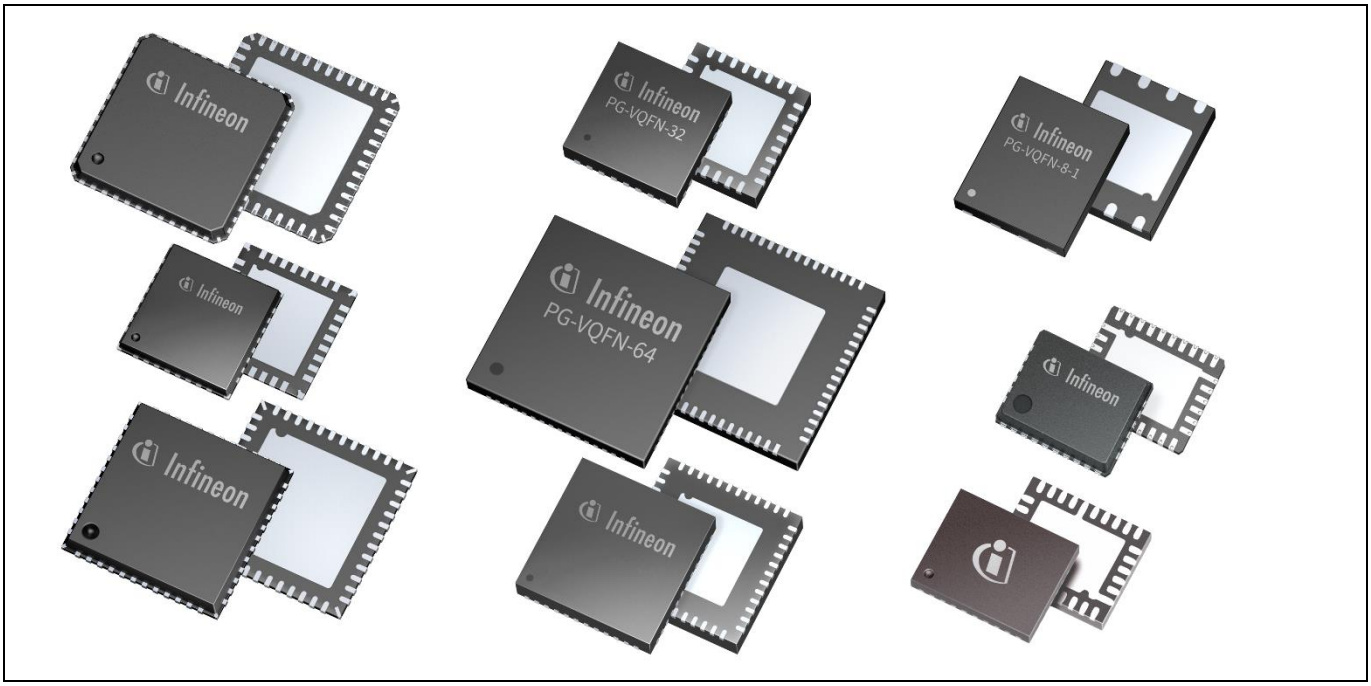

Figure 1 Examples of QFN packages for discrete devices.

1.2 Package Features and General Handling Guidelines

General Handling Guidelines

Semiconductor devices are sensitive to excessive electrostatic discharge (ESD), moisture, mechanical handling, and contamination. Therefore, they require specific precautionary measures to ensure that they are not damaged during transport, storage, handling, and processing.

For further information about component handling, please refer to the *General Recommendations for Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

Internal Construction

QFN are near-chip-scale plastic encapsulated packages with a copper leadframe using perimeter lands on the bottom of the package to provide electrical and thermal contact to the Printed Circuit Board (PCB). The packages are designed with an exposed die pad for optimal heat transfer into the PCB. The footprint features at least one but in most cases two symmetry axis.

The die and the leadframe are usually connected electrically by wire bond connections. The die is attached to an exposed pad as shown in **Figure 2**. The packages are available as either map or cavity mold versions.

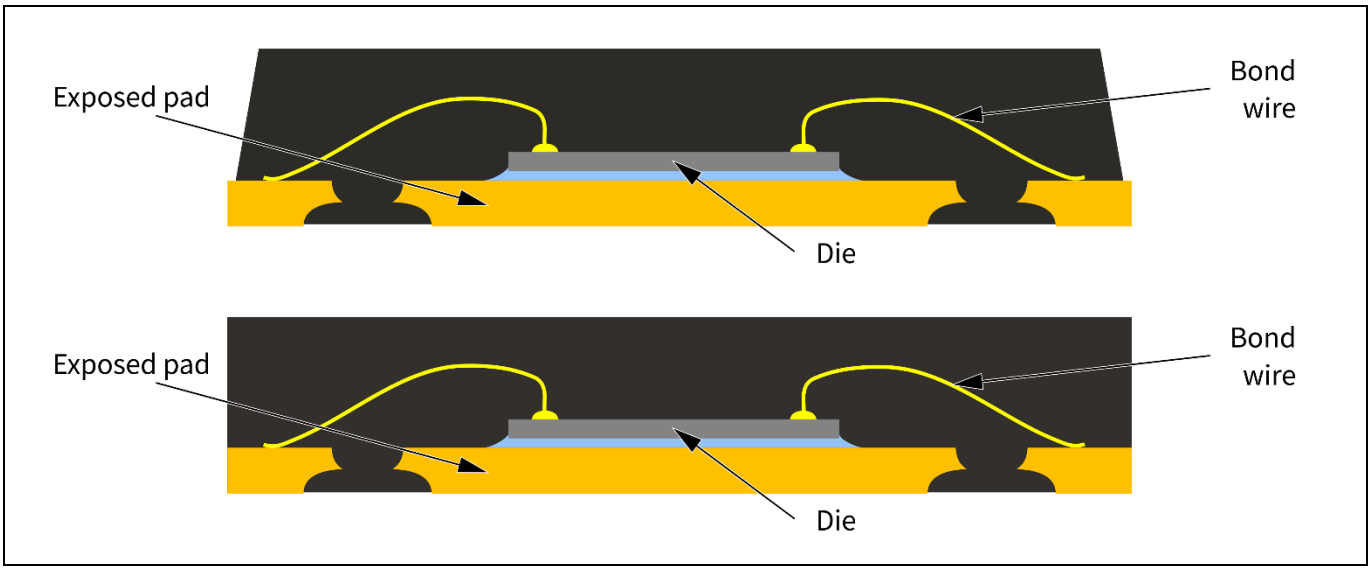

Figure 2 Schematics showing the general setups of VQFN packages as either a cavity mold version with stamped leadframe (top) or as a map mold version with sawn leadframe (bottom).

Terminal Design

The non-leaded land pattern provides for optimal electrical performance due to decreased conductor lengths, while optimizing the package-to-chip ratio.

The leadframe singulation can be created by sawing array molded packages or punching individually molded packages. This results in different shapes of the package flank and the terminals, as can be seen in **Figure 3**. The solder joints are mainly formed underneath the package. The tips of such terminals often have bare copper (e.g. cut edges) and are therefore not intended to wet with solder by design according to IPC-A-610 [6].

Lead Tip Inspection (LTI) features provide a partial or full plating of the terminal tip, as can be seen in **Figure 3**. The features allow for reproducible Automated Optical Inspection (AOI) of the solder joint connection.

For further information about LTI features, please contact your local Infineon sales, application or quality engineer.

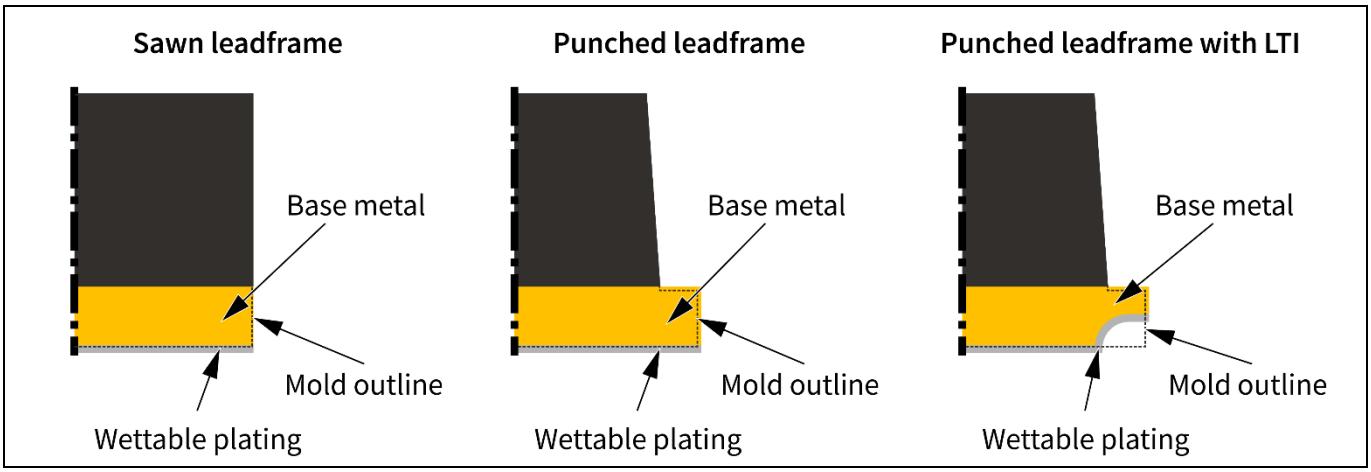

Figure 3 Schematic comparison of various QFN terminal designs.

Figure 4 and **Figure 5** show cross-sections of stamped terminals with and without LTI featured terminals.

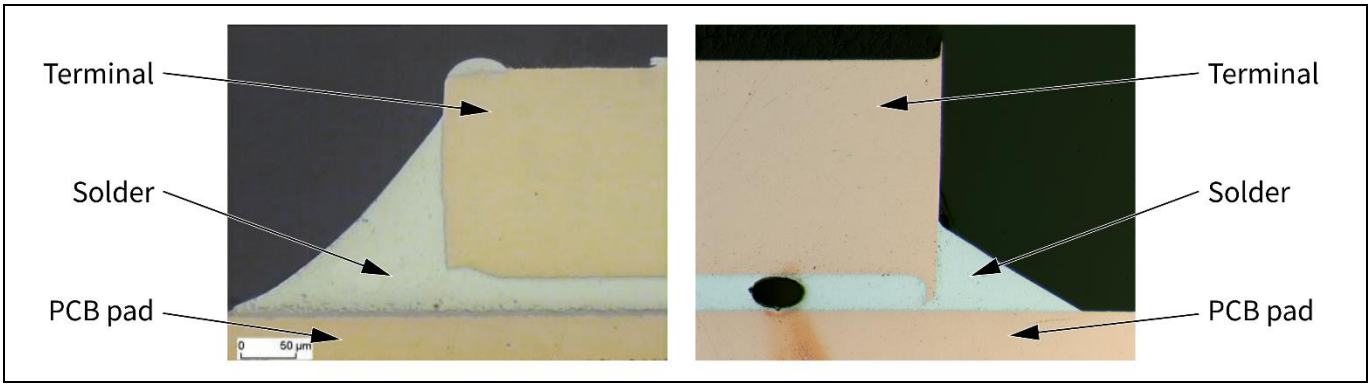

Figure 4 Cross sections of a stamped QFN (left) and a sawn (right) terminal.

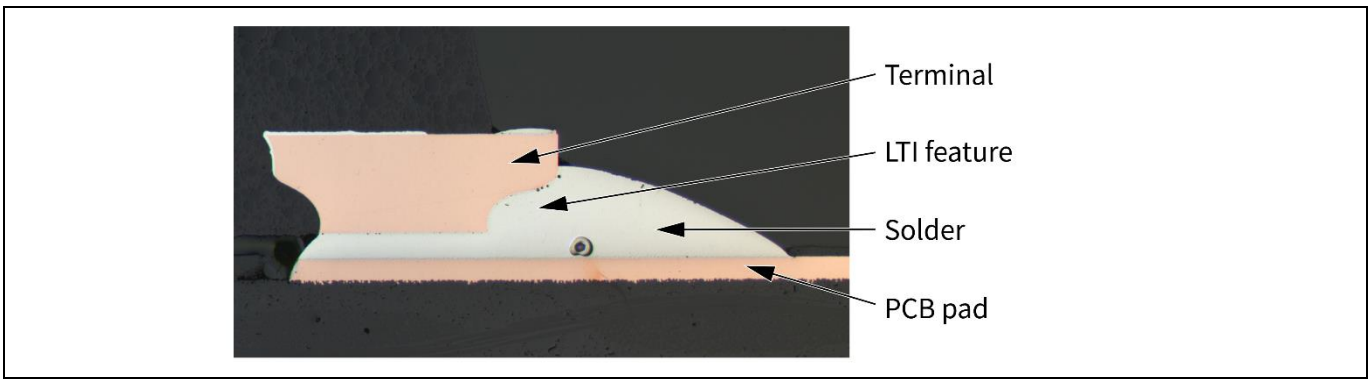

Figure 5 Cross section of a QFN component with “dimple” LTI terminal.

Terminal Plating

Most of the Infineon discrete QFN packages feature a chemically deposited matte tin (ChSn) surface finish that is applied to the base metal by a post-mold process. The Pre-Plated lead Frame (PPF) provides an alternative solderable surface that is already deposited on the leadframe prior to the die attach process. The PPF surfaces

basically consist of a nickel/palladium/gold (Ni/Pd/Au) stack-up. While the ChSn melts during during reflow, the sacrificial Au layer of the PPF surface is dissolved. The solder connection is then made to the Ni-layer.

2 Printed Circuit Board

2.1 Routing

Printed circuit board design and construction are key factors for achieving solder joints with high reliability. Packages with exposed pads should not be placed opposite one another on either side of a PCB if double-sided mounting is used. This will stiffen the assembly and cause solder joints to fatigue earlier than in a design in which the components are offset. Furthermore, board stiffness itself has a significant influence on the reliability of the solder joint interconnect if the system is used in critical temperature-cycling conditions.

2.2 Pad Design

The quality and reliability of interconnect solder joints to the board are affected by:

- Pad type (Solder Mask Defined, SMD or Non-Solder Mask Defined, NSMD)
- Specific pad dimensions
- Pad finish (also called metallization or final finish)
- Via layout and technology

It is recommended to use a Non-Solder Mask Defined PCB pads in which the solder mask opening is larger than the copper pad. The copper pad etching process is more capable and stable compared with the solder mask in terms of dimensional tolerances and registration accuracy. Therefore, smaller copper pads can be defined more accurately. The mixture of different pad registration types in one footprint is not recommended.

Beside their electrical function, the exposed pads on the landing area of the QFN packages are designed to conduct thermal loads into the PCB in order to optimize thermal performance. Therefore, the exposed pad area on the PCB should be at least congruent with the area of the package, if not larger. If the central die pad is not used as a “thermal pad,” it is still a connection to ground. Using a PCB pad of the same size as the package pad will increase the solder joint reliability, and the electrical performance for some applications.

Some packages feature open copper form the tie-bar at the bottom-side of the component. **Figure 6** shows how these areas should be kept free from open metal structures on the PCB by defining “keep-out areas”.

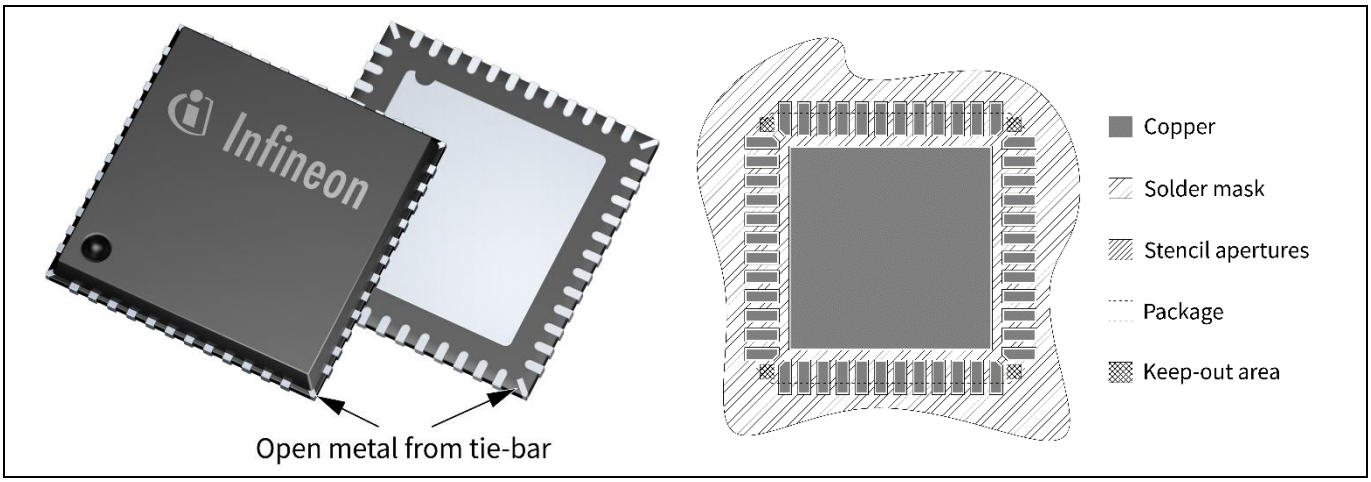

Figure 6 Open metal from tie-bar on the package underside (left) and respective keep-out area in the PCB footprint design (right).

Discrete QFN packages have terminals that reach the package outline regardless of the mold technology. Standard version terminals feature bare copper areas with cut edges that are not intended to be wettable by

design (see also IPC-A-610 [6]). Consequently, the standard terminals are of bottom-only type. Component versions with so called ”dimple” LTI features allow for controlled additional partial sidewall wetting, as can be seen in **Figure 7**.

In order to support the self-aligning effect by the liquid solder wetting forces during reflow, it is recommended to extend the perimeter PCB pads by approx. 250 µm beyond the package outline and by approx. 50 µm in the heel region of the terminal.

Generally, an optimal PCB design depends on the specific application as well as on the specific design rules of the chosen board manufacturer.

For further information about PCB design, please refer to the *General Recommendations for Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

2.3 Pad Design for LTI Features

The “dimple” LTI feature extends the wettable area of the terminal to its tip (see **Figure 5** and **Figure 7**). This allows for the formation of a solder joint meniscus with reproducible height, which is especially important for Automated Optical Inspection (AOI).

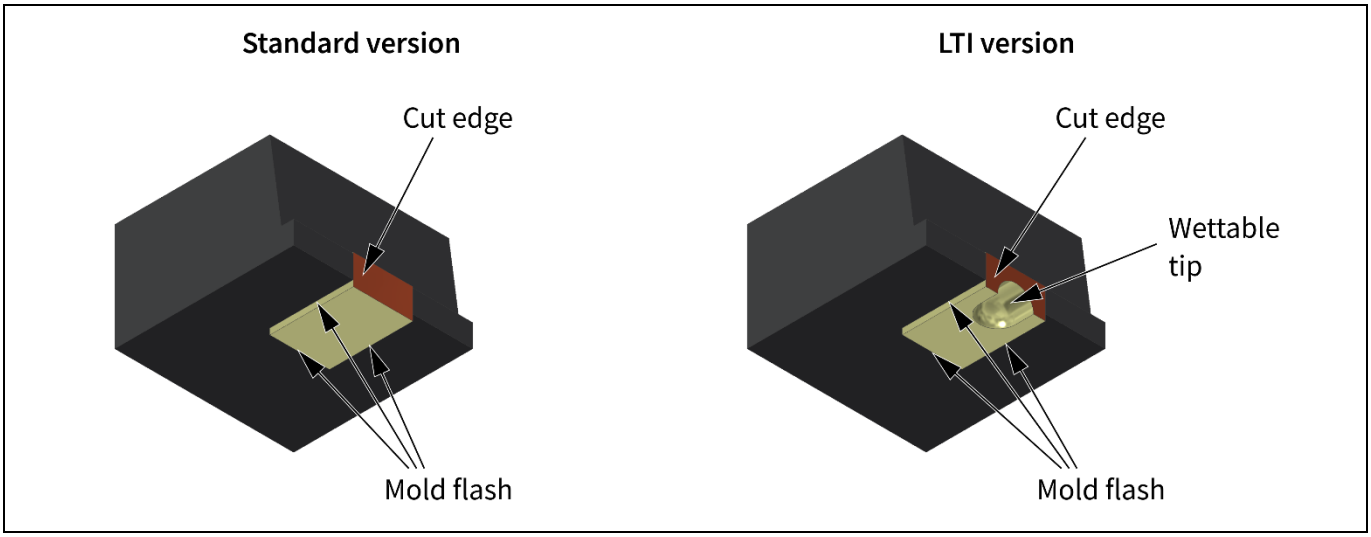

Figure 7 Models of the basic terminal types with wettable areas on bottom only (left) and with wettable sidewall due to “dimple” LTI (right).

In order to ensure optimal results during the AOI, the pad extension should be increased from the above mentioned approx. 250 µm to more than 400 µm. The solder paste volume should be accordingly increased by a sufficient amount to ensure homogeneous and reproducible solder joint fillet formation at the terminal tip. The increased extension of the PCB pad for LTI featured terminals for optimal solder meniscus formation is shown schematically in **Figure 8**.

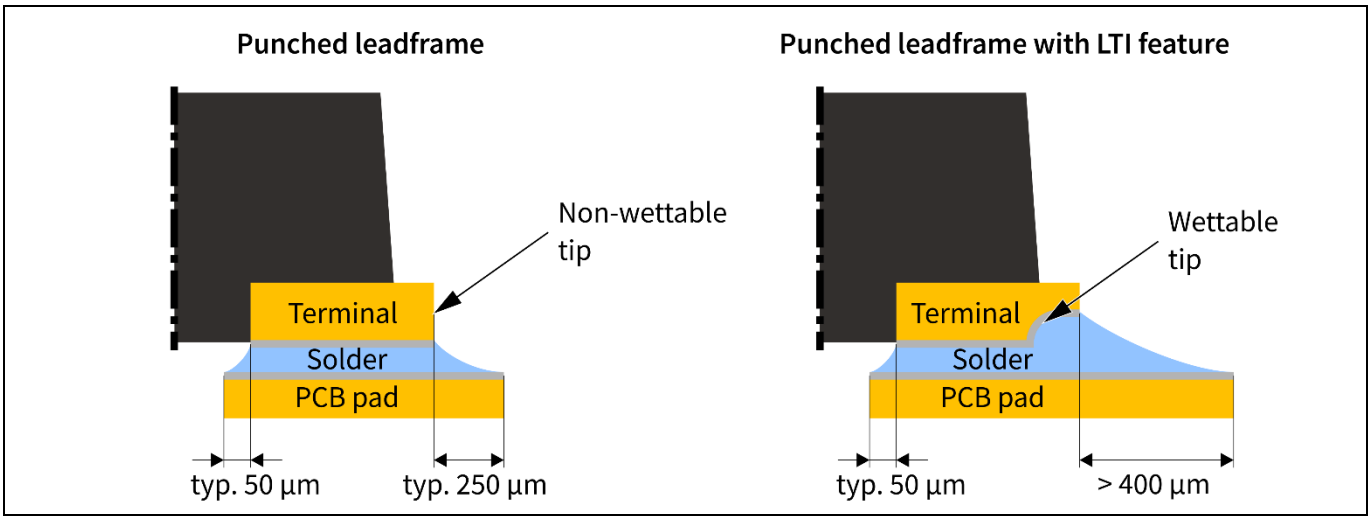

Figure 8 Schematic of punched leadframe without (left) and with "dimple" LTI feature (right). For complete LTI functionality, a distinct solder meniscus must be formed at the terminal tip by sufficient extension of the pad over the package edge.

Further details and specific footprint recommendations can be found in the package data base on the Infineon web page [1]. Please choose a specific package when searching the data base, which will then show an example of the stencil aperture layout for each package.

For further information about pad design for LTI, please refer to the *General Recommendations for Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

2.4 Via-in-Pad Design

Thermal and electrical connections to the inner and/or bottom copper planes of the PCB are usually created by plated through-hole vias in the board. The heat is then transfered from the chip over the package die pad and the solder joint to the thermal pad on the board and through the PCB by the thermal vias.

The diameter and the number of vias in the thermal pad depend on the specific thermal requirements of the final product, the power consumption of the product, the application, and the construction of the PCB. A typical hole diameter for thermal vias is 0.2 - 0.5 mm. An array with 1.0 - 1.2 mm pitch can be a reasonable starting point for further design optimization. The implementation of thermal vias has several impacts on the board assembly as outlined below. A constant increase of number of vias does not necessarily translates into a constant decrease of the thermal resistance of the entire assembly set-up. Thermal and electrical analysis and/or testing together with a proper board assembly design procedure are recommended to determine the optimum number of vias needed.

One of the primary exposed pad design objectives, besides the thermal management, should be to avoid the penetration of the vias by solder. Consequences of solder penetration can be a decreased stand-off between the PCB and the package, an increased void formation ultimately resulting in an insufficient solder joint area, or surplus solder on the opposite side of the PCB.

A first approach for risk reduction should be the prevention of a direct print of solder paste on the via orifice. Since the stencil for large area prints such as on die pads is usually segmented, it is a good practice to position the vias under the beam intesections of the aperture as shown in **Figure 9**. With such an approach, a good solder joint on a central die pad can be formed using vias that remain open on both sides of the board.

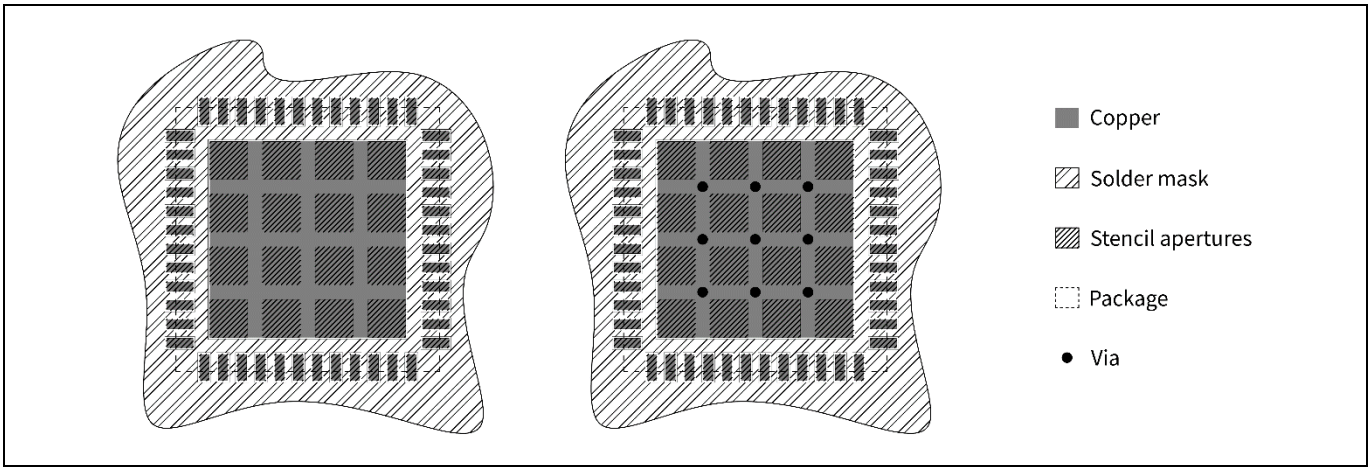

Figure 9 Examples of solder mask defined footprint variants without (left) and with (right) via-in-pad design. The segmentation of the stencil is combined with the via positioning.

Despite the precautionary stencil design approach, surplus solder can move into the via, driven by wetting forces. If the solder then protrudes to the opposite side of the PCB, it may interfere with a second solder paste print process. To minimize the effect, dummy areas on the opposite side as shown in **Figure 10** can catch the surplus solder to avoid beading and solder lumping.

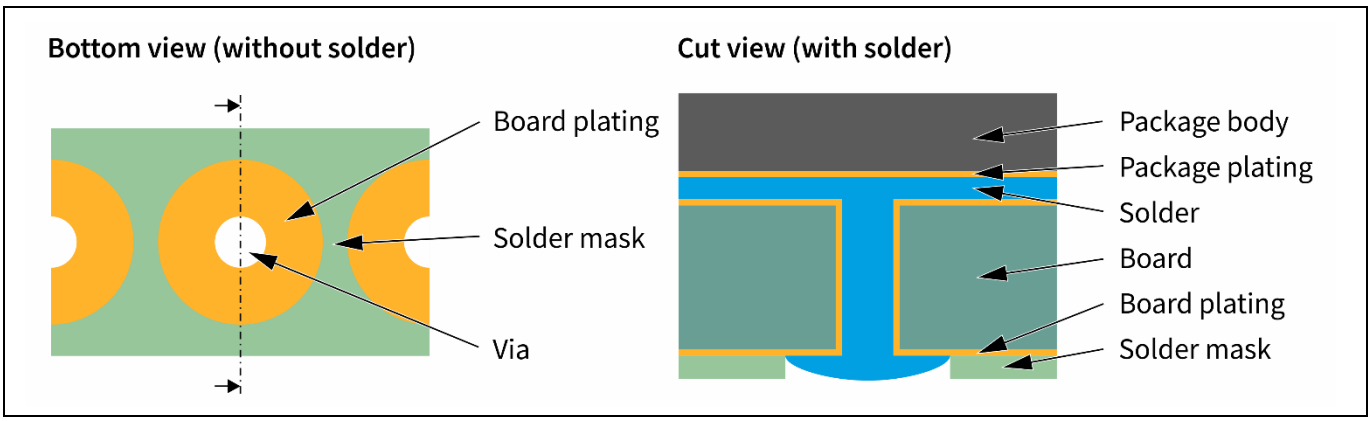

Figure 10 Wettable “dummy” area on the opposite side of the board, which surrounds the vias to act as a buffer for surplus solder.

In case the solder variance in volume below the die pad is too high due to the wetting of vias, they can be closed by “tenting”. This process includes covering of the vias by a solder mask (e.g. dry-film solder mask). If the via tenting is done only on the opposite side of the board, the voiding rate will increase significantly. Another method to close vias is called “plugging” (filling with epoxy), followed by overplating. Very small vias (100 µm in diameter or smaller) should be filled with copper and overplated. In both cases the specification of a planar filling is necessary to avoid cavities that will work as traps for gases, forming voids during reflow soldering.

In case it is not necessary to provide a direct connection from the solder pad under the exposed die pad to the inner layers of the PCB, the vias can be placed next to the footprint near the package and covered with solder mask.

For further information about vias in pad, please refer to the *General Recommendations for Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3 PCB Assembly

3.1 Solder Paste Stencil

In SMT, the solder paste is applied onto the PCB metal pads by stencil printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. While an excessive solder paste volume will cause solder bridging, an insufficient solder paste volume can lead to reduced solder spreading between all contact surfaces. To ensure a uniform and sufficiently high solder paste transfer to the PCB, laser-cut (mostly made from stainless steel) or electroformed stencils (nickel) are preferred. The latter are applied especially when fine-pitch components are assembled.

The stencil apertures are usually of the same dimensions as the relevant pad on the PCB (not counting in possible edge rounding). The PCB pad of the die-pad should be slightly increased (by 25-50 µm all round the component pad). In most cases the thickness of a stencil has to be matched to the needs of all components on the PCB. For QFN packages of pitch up to 0.5 mm, it is recommended to use stencils of 100-120 µm thickness. For pitch 0.65 mm, a 150 µm stencil thickness might be applicable. The rounding of aperture corners (approx. 50 µm) can stabilize the paste transfer. This can be helpful when dealing with fine-pitch components. However, one has to keep in mind that at the same time in most cases the paste transfer quantity of the stencil apertures is decreased.

The solder paste volume in apertures larger than approximately 5 mm may be scooped out depending on the specific squeegee pressure and rigidity. Such apertures are necessary for many die pad prints and should be segmented into smaller areas. Internal investigations have shown that the ratio between stencil openings and die pad can vary from 50% to 65%. The resulting solder joint stand-off of the entire package then ranges from 40 µm to 60 µm. When reducing the die pad print, potential vias in pad have to be considered, as described in the previous section. The apertures should be arranged in a regular matrix with sizes between 0.4 mm^2 - 1.0 mm^2 depending on the via density and thermal pad size. **Figure 9** provides an overview of the general approach.

For individual design adaptations to reach the optimum amount of solder the stencil thickness, the PCB pad finish, quality, solder masking, via layout, and the solder paste type should all be considered. In every case, application-specific experiments are recommended.

Further details and specific stencil aperture recommendations can be found in the Infineon package data base that is available on the Infineon web page [1]. Please choose a specific package when searching the data base, which will then show an example of the stencil aperture layout for each package.

For further information about solder stencil design, please refer to the *General Recommendations for Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3.2 Solder Paste

Pb-free solder pastes typically contain some type of SnAgCu alloy (SAC solder with typically 1-4% Ag and <1% Cu). The most common alloy is SAC305 (3.0 % Ag and 0.5 % Cu). The average alloy particle size must be suitable for printing the solder stencil aperture dimensions. Depending on the specific pin width, Type 3 pastes might work depending on the specific stencil aperture size and therefore solder paste transfer efficiency. Using Type 4 paste or higher is recommended for the assembly of QFN components.

The solder alloy particles are dispersed in a blend of liquid flux and chemical additives (approx. 50% by volume or 10% by weight) forming a creamy paste. The flux and chemical solvents have various functions such as adjusting the viscosity of the paste for stencil printing or removing contaminants and oxides on the surface.

The solder paste solvents have to evaporate during reflow soldering while residues of the flux will remain on the joint. The capacity of the flux additive for removing oxides is given by its activation level, which also affects the potential need for removing the flux residuals after the assembly. For components such as QFN in which the solder joint is formed mainly on the package bottom side, a “no-clean” paste is recommended to avoid subsequent cleaning underneath the package. The small gaps make cleaning highly difficult if not impossible. Certain precautions have to be taken if any kinds of flux residues remain on the board prior to any kind of coating.

Generally, solder paste is sensitive to age, temperature, and humidity. Please follow the handling recommendations of the paste manufacturer.

3.3 Component Placement

Although the self-alignment effect due to the surface tension of the liquid solder will support the formation of reliable solder joints, the components have to be placed accurately depending on their geometry. Positioning the packages manually is not recommended, especially for packages with small terminals and pitch. An automated pick-and-place machine is recommended to obtain reliable solder joints.

Component placement accuracies of +/-50 µm and less are obtained with modern automatic component placement machines using vision systems. With these systems, both the PCB and the components are optically measured and the components are placed on the PCB at their programmed positions. The fiducials on the PCB are located either on the edge of the PCB for the entire PCB, or at additional individual mounting positions (local fiducials). These fiducials are detected by a vision system immediately prior to the mounting process.

For further information about component placement, please refer to the *General Recommendations for Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3.4 Reflow Soldering

For PCB assembly of the QFN packaged components, the widely used method of reflow soldering in a forced convection oven is recommended. Soldering in a nitrogen atmosphere can generally improve the solder joint quality but is not necessary to create a reliable joint.

The soldering profile should be in accordance with the recommendations of the solder paste manufacturer to achieve optimal solder joint quality. The position and the surrounding of the component on the PCB, as well as the PCB thickness, can influence the solder joint temperature significantly.

Minimum Reflow Conditions

The lower temperatures and durations of an optimal reflow profile must stay above those of the solderability qualification. The solderability of the terminals of Infineon components is tested according to the standards IEC 60068-2-58 and J-STD-002 [2][3].

Maximum Reflow Conditions and Cycles

Components that are Moisture-Sensitivity Level (MSL) classified by Infineon have been tested by three reflow runs in accordance with the J-STD-020 standard, including a double-sided reflow and one rework cycle. The maximum temperatures must not be exceeded during board assembly. Please refer to the product barcode label on the packing material that states this maximum reflow temperature according to the J-STD-020 [4] standard as well as the MSL according to the J-STD-033 standard [5].

QFN packages are generally suited for mounting on double-sided PCBs. If the solder joint thickness is a critical dimension, solder joints of components on the first side will again reflow in the second step. In the reflow zone

of the oven (i.e. where the solder is liquid), the components are only held in place by wetting forces from the molten solder. Gravity acting in the opposite direction will elongate the solder joints, unlike joints on the top side, where gravity will force the components nearer to the PCB surface. This shape will be frozen during cooling and therefore will result in a higher stand-off on the bottom side after the reflow process. Heavy vibrations in a reflow oven may cause devices to drop off the PCB.

For further information about reflow soldering, please refer to the *General Recommendations for Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

4 Cleaning

After the soldering process, some flux residues may remain on the board, especially near the solder joints. Generally, cleaning beneath a component with bottom-only terminals is difficult due to the small gap between the component body and the PCB. Therefore, a “no-clean” flux is recommended whose residues usually do not have to be removed after the soldering process.

In case the solder joints have to be cleaned, the cleaning method (e.g. ultrasonic, spray, or vapor cleaning) and cleaning solution have to be selected while taking into account the type of package, the flux used in the solder paste (rosin/resin-based, water-soluble, etc.) as well as the environmental and safety aspects. Even small residues of the cleaning solution should be removed or dried out very thoroughly. For recommended cleaning solutions, please contact the solder paste or flux manufacturer.

5 Inspection

5.1 Optical Solder Joint Inspection

Compared to leaded SMD components (e.g. the gullwing type), the solder joints of QFN packages are mainly formed underneath the package. The tips of the terminals often have bare copper (cut or stamped edges) that are not designed to be wetted by solder according to IPC-A-610 [6]. Non-wetting of such tips is not a criterion for rejection, as can be seen in **Figure 11**. Consequently, visual inspection of such solder joints with conventional Automated Optical Inspection (AOI) systems may not be reliable.

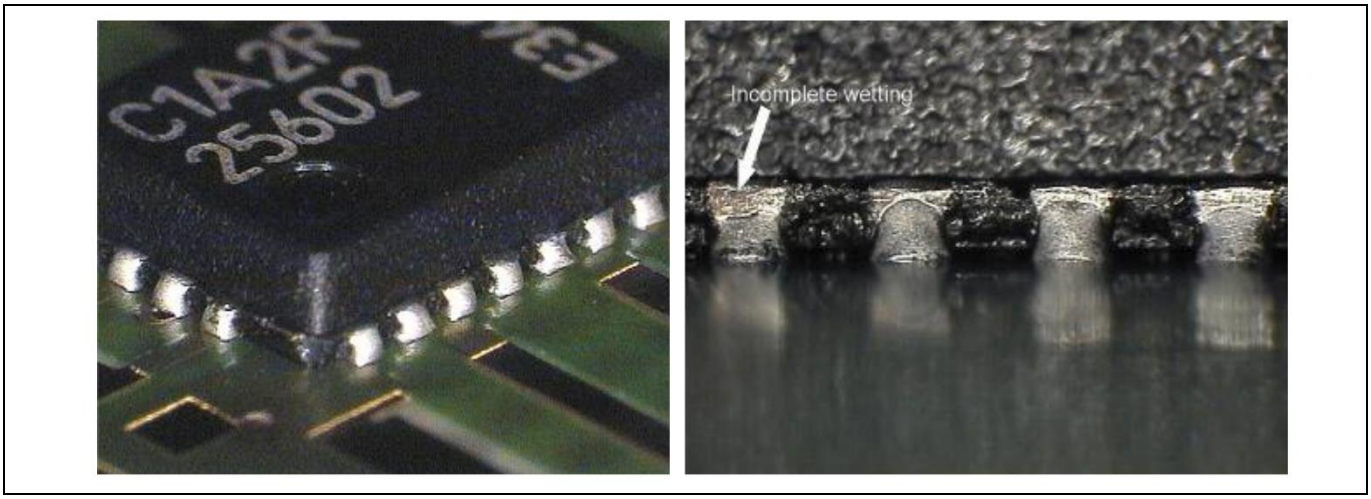

Figure 11 Photograph of a soldered VQFN package (left). Non-wetting of the terminal side wall is not a criterion for rejection (right).

QFN packages with an LTI feature allow for reproducible solder meniscus formation on the sidewall. Since the plating of the landing area is of the same kind as that on the terminal sidewall, the LTI features provide information about the solderability of the metallization below the component. Consequently, it is possible to utilize conventional AOI systems.

There are terminals that are fused with a die pad e.g. for electrical or construction reasons. **Figure 12** shows a VQFN-32 with such terminals together with stand-alone ones. In case the terminal is fused with the exposed pad, the solder joint fillet formation on that terminal may differ from the stand-alone one. The effect is shown in **Figure 13**.

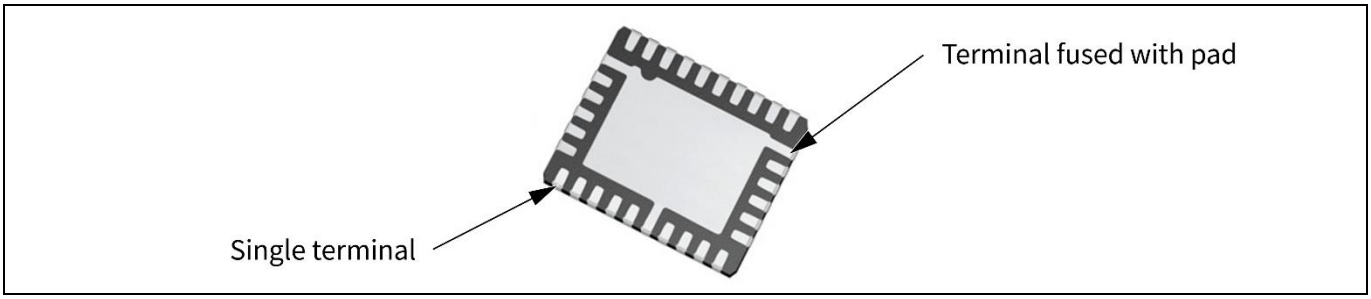

Figure 12 VQFN-32 package landing area with some terminals that are fused with the pad.

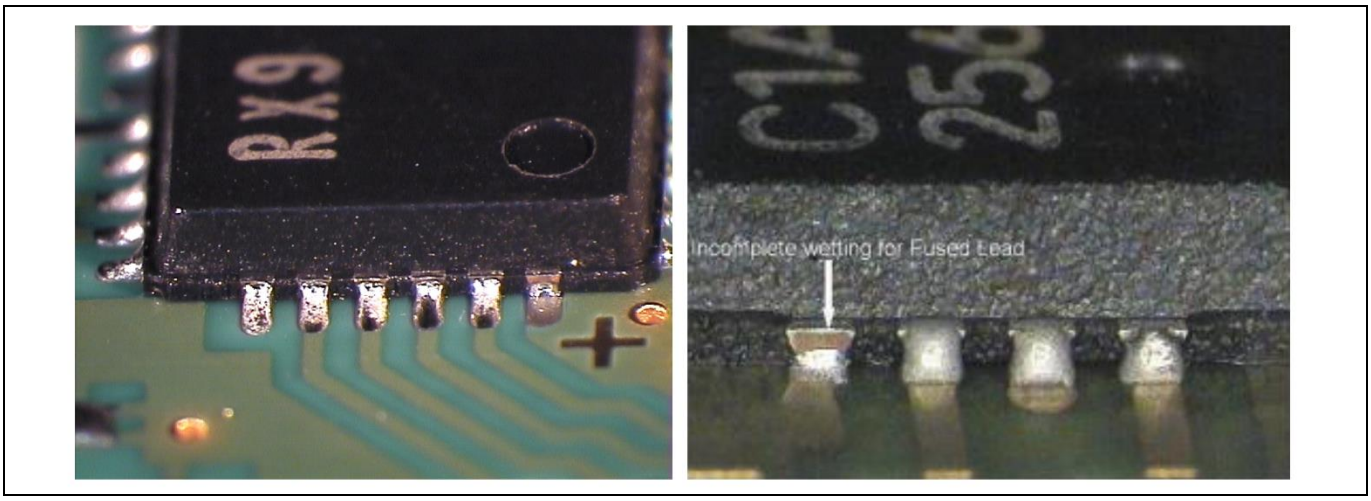

Figure 13 Photograph of terminals with (left) and without (right) LTI features that are fused with the pad.

For engineering tasks, cross-sectioning can provide detailed information about the solder-joint quality. Due to its destructive nature, cross-sectioning during monitoring is not practical.

5.2 X-Ray Solder Joint Inspection

Automated X-ray Inspection (AXI) systems are appropriate for efficient inline control of components that cannot be inspected properly by optical systems. AXI systems are available as 2D and 3D solutions. They usually consist of an X-ray camera and the hardware and software needed for inspecting, controlling, analyzing, and data transferring routines. These reliable systems enable the user to detect soldering defects such as poor soldering, bridging, voiding, and missing parts. However, other defects such as broken solder joints are not easily detectable by X-ray.

Figure 14 shows a typical X-ray photograph of a VQFN package. Internal solder joints, wirebonds, leadframe, and the solder joints that connect the package to the PCB are visible. Large exposed pads may tend to increase voiding because they do not provide a sufficient ratio between volume and surface necessary for proper outgassing of the organic compounds during reflow. Generally, the extent of voiding depends on the board pad size, the via and stencil layout, the solder paste, and the reflow profile. For thermal evaluations, the entire thermal path must be considered as well as all boundary conditions such as the application environment or the electrical use of the component.

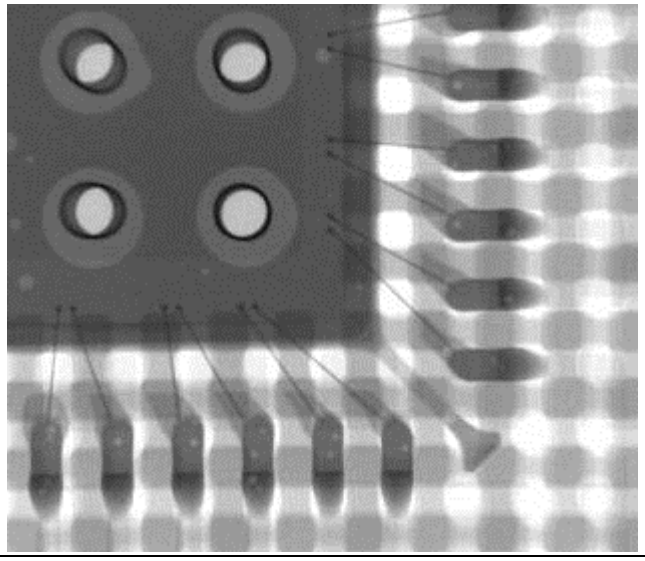

Figure 14 Typical X-ray image of a soldered VQFN package. Investigations have shown that voids similar in size and amount to those shown in this image do not reduce the package reliability.

6 Rework

Single solder joint repair of bottom-only terminated packages is highly difficult, if not impossible, and is therefore generally not recommended. Furthermore, the reuse of de-soldered components is not recommended. The de-soldered components should be replaced by new ones.

A rework process is commonly done on special rework equipment. There are various systems available that meet the requirements for reworking SMD packages. All handling guidelines discussed in this document have to be respected. Special focus should be on the following items:

- Due to the decreased automation level given by the general rework approach, even higher care compared to standard assembly must be taken. Tools that do not damage the component mechanically have to be chosen. Mechanical forces that do not necessarily cause visible external damage can still cause internal damage that reduces the component's reliability. A proper handling system with vacuum nozzle may be the gentlest process and is therefore recommended. However, the impact of rework tools has to be assessed properly. In general, more manual handling increases the effort for documentation, training, and monitoring of the rework process(es).
- During rework, special care must be taken concerning the proper moisture level of the component according to the J-STD-033. Drying the PCB and the component prior to rework might be necessary. A proper drying procedure for SMD packages is described in the international J-STD-033 standard [3]. Please also refer to the recommendations of your PCB manufacturer and take all specific needs of components, PCB, and other materials into account.
- Whatever heating system is used (hot air, infrared, hot plate, etc.), the applied temperature profile at the component must never exceed the maximum temperature according to the J-STD-020 standard. Depending on the specific heating profile used during rework, components adjacent to the mounting location might also experience a further "reflow run" in terms of the J-STD-020 standard [2]. Internal investigations have shown that the temperature profile must be recorded.

In case a component is suspected to be defective and a failure analysis planned, the component should not be removed from the PCB. The entire PCB with components should be sent to Infineon. This guarantees that no further damage is caused to the component, which may hinder the failure analysis or even make it impossible.

Note: For failure analysis at Infineon, the entire PCB must be shipped in order to avoid damages to the component by its removal from the board.

For further information about component rework on PCB, please refer to the General Recommendations for Assembly of Infineon Packages document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

7 References

[1] Infineon: Packages. www.infineon.com\packages.

[2] International Electrotechnical Commission: IEC 60068-2-58. Environmental testing - Part 2-58: Tests - Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD).

[3] Electronic Components Industry Association, Assembly and Joining Processes and JEDEC Solid State Technology Association Committee: EIA/IPC/JEDEC J-STD-002. Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires.

[4] JEDEC Solid State Technology Association: IPC/JEDEC J-STD-020. Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices.

[5] JEDEC Solid State Technology Association: IPC/JEDEC J-STD-033. Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.

[6] Association Connecting Electronics Industries: IPC-A-610. Acceptability of Printed Boards Training and Certification program.

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All	Complete review

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