Recommendations for board assembly of transistor packages with metal can

About this document

Scope and purpose

This document provides additional information on the board mounting of Infineon devices with the package type WDSON.

Intended audience

This document addresses all users that are handling the pad and stencil design, the board mounting or the rework of the herein discussed Infineon devices.

Table of contents

1 Package description

The DirectFET™ family is a surface-mounted semiconductor technology designed primarily for board-mounted power applications. It eliminates unnecessary elements of packaging that contribute to higher inductance and resistance, both thermal and electrical, so that its power capabilities exceed those of comparably sized packages.

DirectFET™ technology facilitates dual-sided cooling of surface mounted power MOSFET devices. This allows for double power and current densities, which in turn reduces component count and system cost. These benefits result from the presence of solderable contacts on the surface of the silicon die for connecting the gate and source to the printed circuit board (PCB). A copper clip attached to the back of the die provides the drain connection. Devices in the DirectFET™ range vary but, typically, there are three electrical connections (gate, source and drain). Each of the two drain rails might be divided into two PCB pads increasing the overall number of mechanical joints.

1.1 WDSON package type

The growing outline range for DirectFET™ products is covered by the very very thin profile dual small outline non-leaded (WDSON) package type. It covers various can sizes and device outlines. There are ‘plus’ variants that use thinner dies to improve electrical performance and efficiency. All devices are pre-soldered with a tin-silver-copper alloy (Sn96.5 Ag3.0 Cu0.5 – SAC05) to improve soldering performance. There are also variants qualified for the automotive industry, which have a gate marker of **AU** instead of ●.

Figure 1 shows examples of WDSON packages with standardized pad layouts. For more details about individual devices, refer to the relevant product data sheet and package outline drawing.

- MG-WDSON

MG = metal green
W = very very thin profile
D = dual
SON = small outline non-leaded

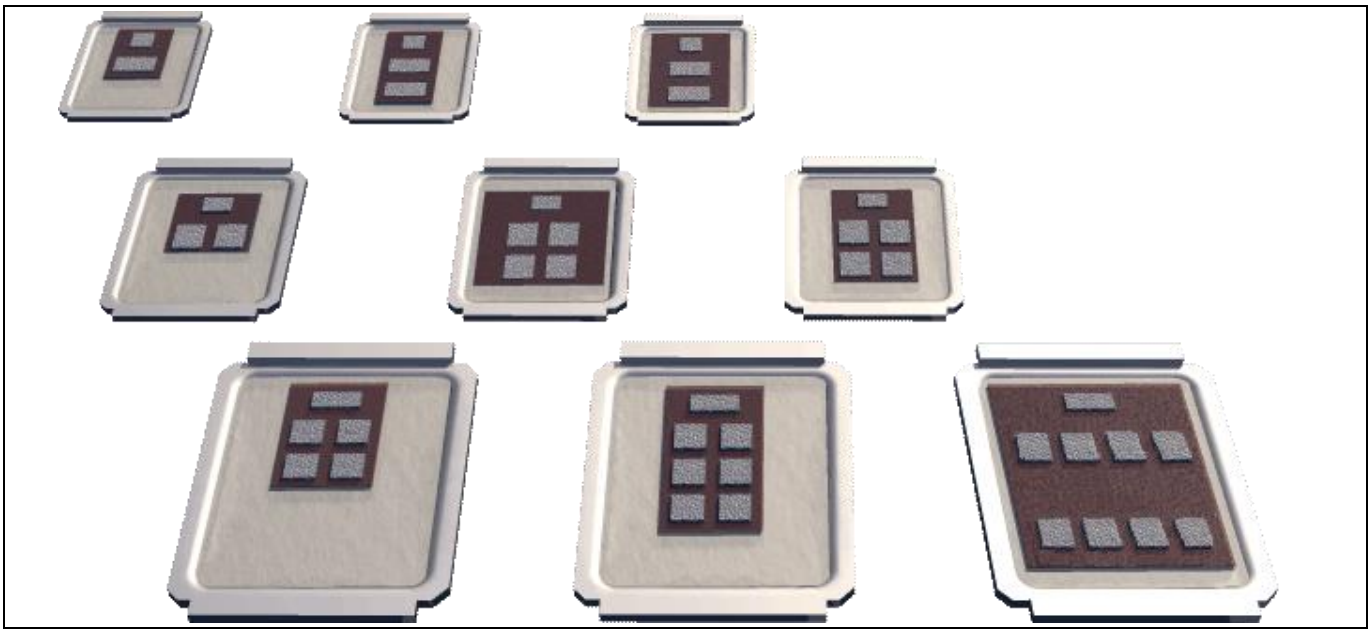

Figure 1 Examples of WDSON packages with standardized pad layouts.

1.2 Package features and general handling guidelines

General handling guidelines

Semiconductor devices are sensitive to excessive electrostatic discharge (ESD), moisture, mechanical handling, and contamination. Therefore, they require specific precautionary measures to ensure that they are not damaged during transport, storage, handling, and processing.

For further information about component handling, please refer to the *General recommendations for board assembly of Infineon packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

Product labelling

Figure 2 shows how WDSON packages are labeled. The part number, batch number and date code are provided to support product traceability.

Note: The dot (or AU on automotive devices) shows at which end of the device the gate pad is located. It is not Pin 1.

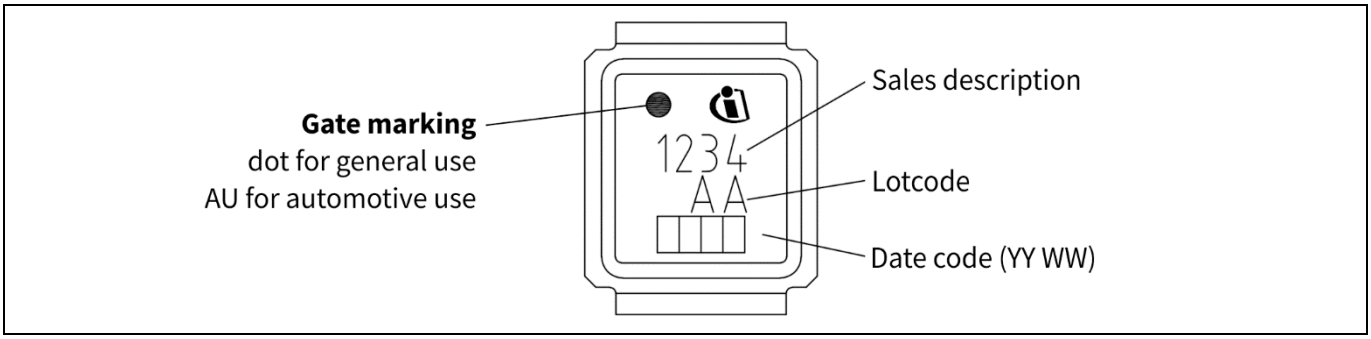

Figure 2 Different types of device markings for a WDSON package.

Internal construction

WDSON packages use a specific construction technique to make source and gate connections directly to the die surface (see Figure 1). The remainder of the surface is coated with passivation to protect it and to control the position, shape and size of the solder contacts between device and substrate.

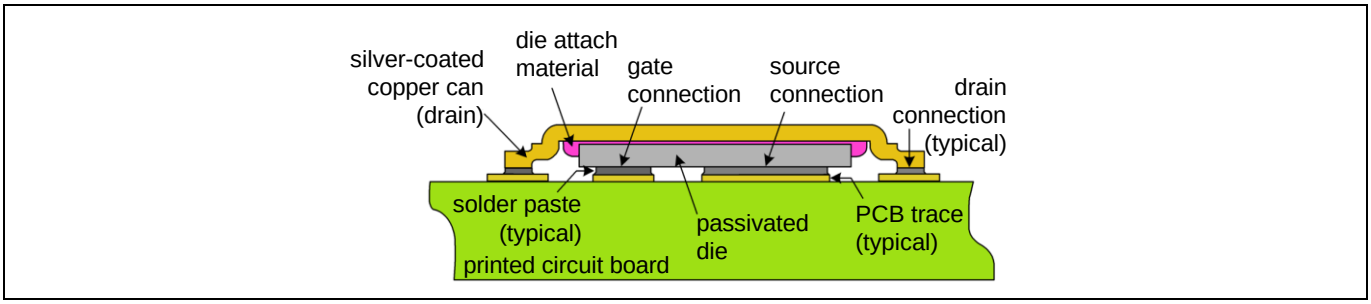

Figure 3 Schematic showing the inner setup of a WDSON package.

1 Package description

Termination design

WDSON packages are bottom-only terminated having pre-soldered bumps. Recessing the die within the package as shown in Figure 4 forces a standoff between die and substrate, which helps to reduce solder balling problems and improves device reliability.

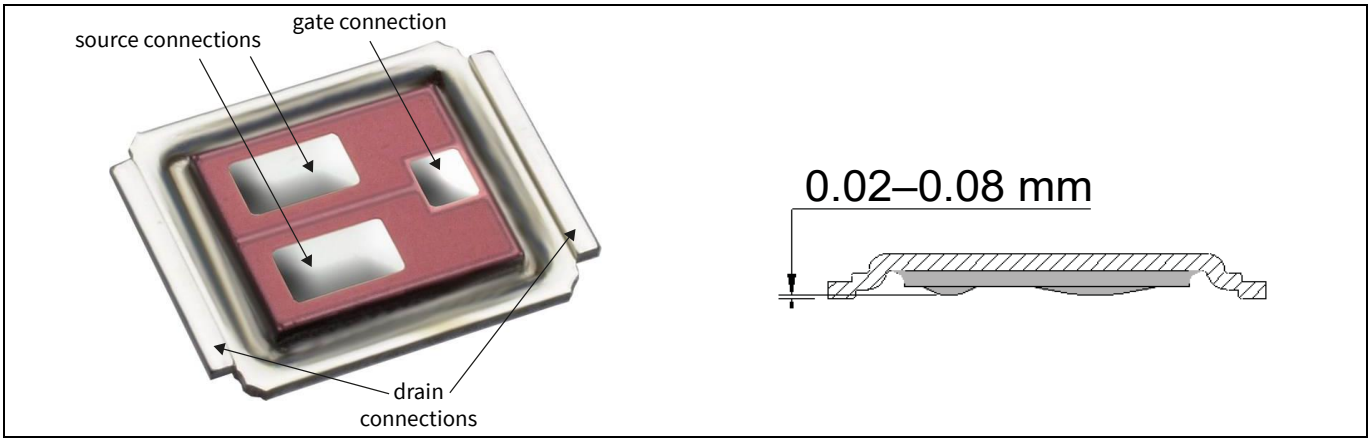

Figure 4 Termination types and planarity of device pads and can.

Termination plating

The WDSON solder bumps consist of SAC305, which melts readily during standard lead-free reflow processes. The drain connections at the landing areas of the can are plated with selective silver. These surfaces are similarly easy to solder. Both finishes provide a reliable solder joint.

2 Printed circuit board

2.1 Routing

Printed circuit board design and construction are key factors for achieving solder joints with high reliability. Packages with exposed pads should not be placed opposite to each other on either side of a PCB if double-sided mounting is used. This will stiffen the assembly and cause solder joints to fatigue earlier than in a design in which the components are offset. Furthermore, the board stiffness itself has a significant influence on the reliability of the solder joint interconnect if the system is used in critical temperature-cycling conditions.

2.2 Pad design

The quality and reliability of interconnect solder joints to the board are affected by:

- Pad type (solder mask defined, SMD or non-solder mask defined, NSMD)
- Specific pad dimensions
- Pad finish (also called metallization or final finish)
- Via layout and technology

The drain connection is formed by a plated copper can, which is bonded to the drain side of the silicon die. The can has two contact areas, both of which must be soldered to the substrate although one can be used solely as a mechanical anchor. Using tracks of similar size under both drain contacts will help to ensure that the device does not tilt during reflowing.

Figure 5 shows typical contact configurations of WDSON packages, covering most devices in the range. Specific pad assignments are shown in the data sheet for each product. The device outline code indicates the can size and number of source pads as shown in Table 1.

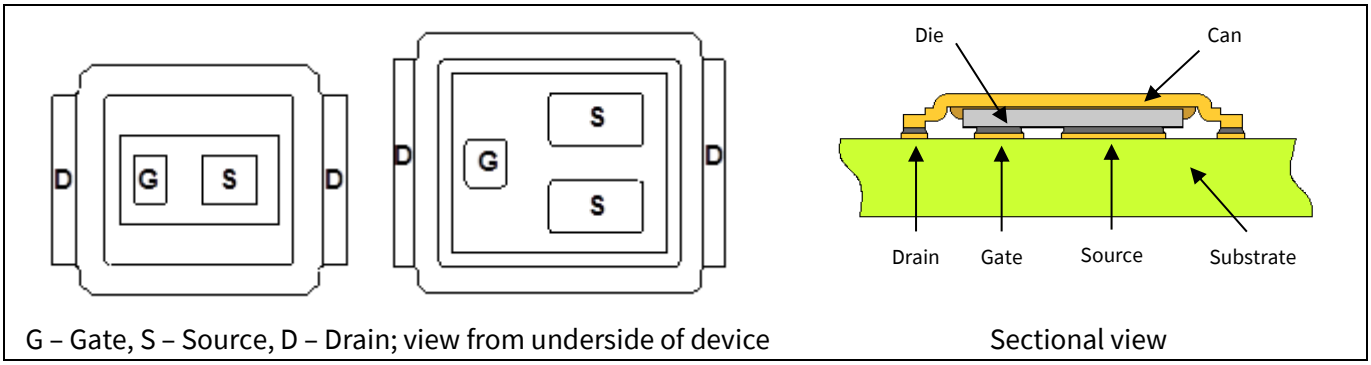

Figure 5 Contact configurations of different WDSON packages.

Table 1 Relation of can size and number of source pads.

Can size		Number of source pads
S	Small	1 or 2
M	Medium	2 or 4
L	Large	4, 6, 8 or 10

To achieve low-loss track layouts, WDSON packages were designed for use with SMD pad layout. Although the devices can be used with NSMD (copper defined) pad layouts, these have not been evaluated. The outline of WDSON packages and the use of SMD pads contribute to efficient substrate design. Large-area tracks optimize

electrical and thermal performance. Figure 6 shows such an approach for paralleling multiple devices. A minimum separation of 0.500 mm (0.020") is recommended. The separation can be adjusted to reflect local process capabilities but should allow for rework. Micro-screen design and de-soldering tool type may affect how closely devices are placed to each other and to other components. Mixing SMD and NSMD pad layouts in one PCB footprint is not recommended.

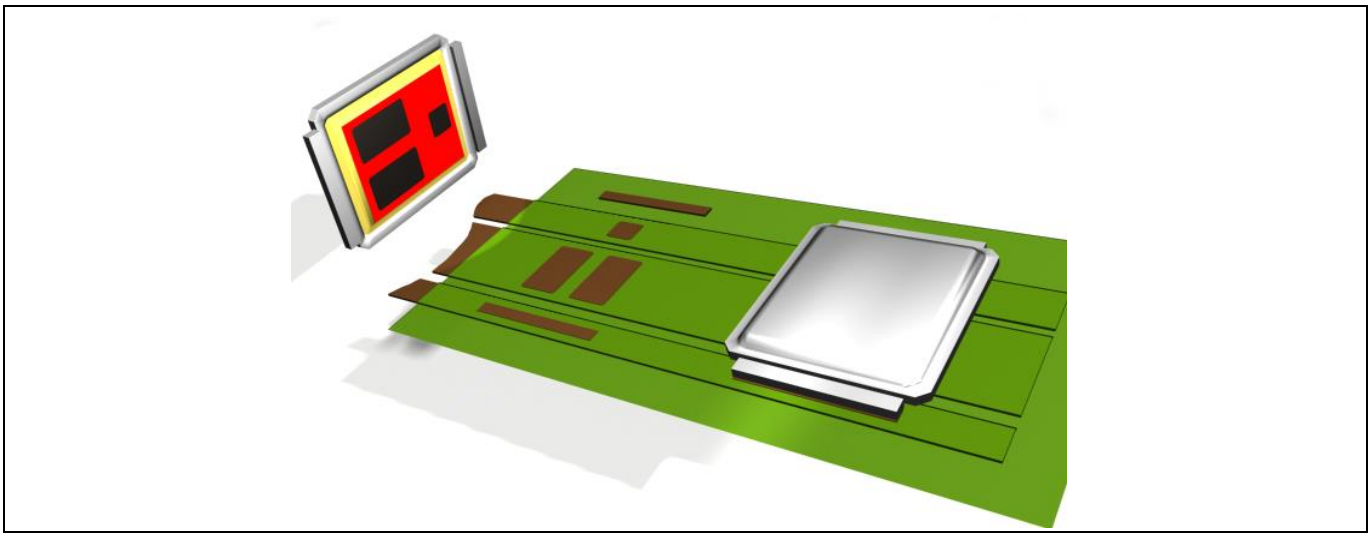

Figure 6 Placing WDSON packages in parallel by facilitating SMD pads on large area tracks.

As it is common to have some level of solder mask misalignment during PCB manufacture, most PCB layout software has about 0.1 mm of solder mask opening expansion to compensate. This default expansion setting can enlarge the SMD pad openings too much and cause soldering problems on WDSON packages. Therefore, it is recommended that the expansion is set to zero for all package pads.

The PCB copper polygons must be larger than the package pads and arranged as shown in Figure 8. This allows the solder mask to shift by up to 0.1 mm while retaining the recommended opening dimensions on all package pads. In other words, the PCB polygon area underneath any of the package pads should be at least 0.102 mm larger than the package solder mask openings. Areas shaded in green represent pads on the package. Areas outlined in red represent minimum pad opening areas required to ensure that the correct amount of solder paste is transferred by using 80% stencil openings.

2.3 Thermal management

WDSON packages are designed to deliver superior thermal performance due to the metal can. In many applications, heatsinks are not required but they may sometimes be applied to achieve even greater cooling. The use of insulated metal substrate (IMS) may also be suitable depending on the specific application.

For optimum thermal performance it is recommended to attach heatsinks to the substrate using clips, screws or other fasteners as shown in Figure 7. If limited board space prevents this, they may be attached to the top of devices only. When heatsinks are attached to the top of devices without mechanical fastenings to the substrate, potential mechanical stresses on the heatsink, however, must be considered. Such stresses will be transferred to the device and may cause mechanical damage and, in extreme cases, device failure.

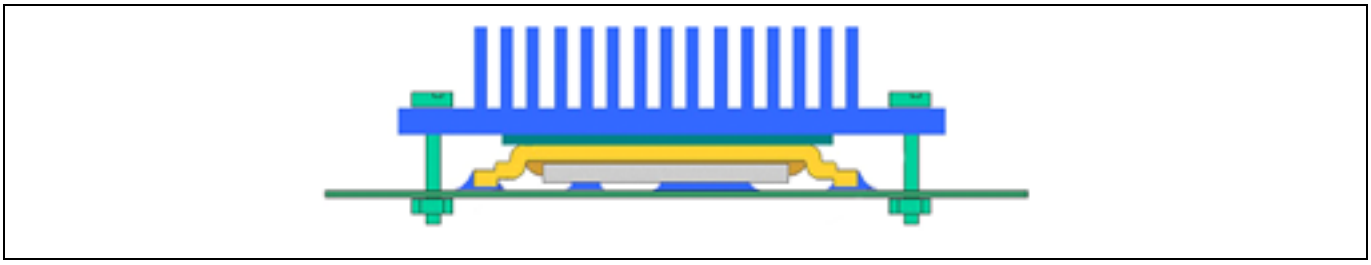

Figure 7 Concept of a heatsink that is attached to the substrate by screws

For further information about thermal management using heat sinks, please refer to the relevant application notes and datasheets or contact your local sales, application, or quality engineer.

2.4 Via design

Thermal and electrical connections to the inner and/or bottom copper planes of the PCB are usually created by plated through-hole vias in the board. The heat and current flow are then transferred from the device through the solder joint and vias to e.g. ground or heat slug copper planes.

It is not recommended to use via-in-pad for typical applications but rather place them close to the pads as shown in Figure 8. A typical via outside diameter is of 0.635 mm with a plating thickness of roughly 20 µm.

When using tented vias (via openings are covered by the solder mask), the space left between the package pads and the vias is not critical. When using untented vias, the via pads must be at least 0.05 mm from the package pads to prevent solder paste flowing from the pads into the via openings. To achieve this, the via pads should have a solder mask expansion of 0.05 mm. As the via pads are about 0.15 mm in diameter, the 0.05 mm solder mask expansion plus the 0.05 mm spacing of the via pads from the package pads provides a tolerance of about 0.1 mm in the alignment of the solder mask. The via pads retain about 0.1 mm for manufacturing tolerance.

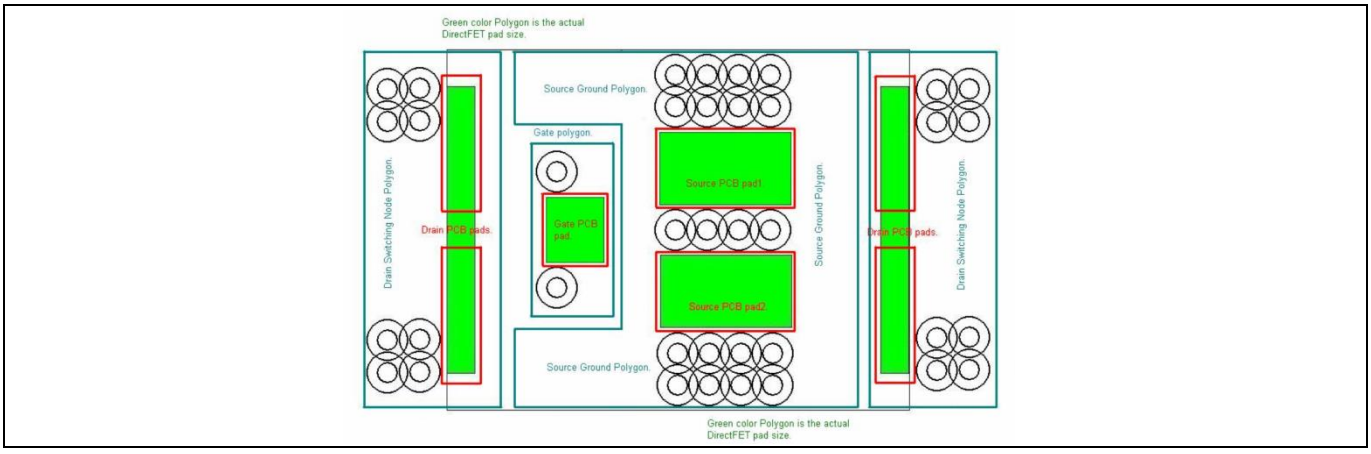

Figure 8 Example of a low-side pad design with vias outside the pads.

For further information about via design, please refer to the *General recommendations for board assembly of Infineon packages* document that is available on the Infineon web page [1]. For application specific routing recommendations, please refer to the relevant application notes and datasheets or contact your local sales, application, or quality engineer.

3 PCB assembly

3.1 Solder paste stencil

In SMT the solder paste is applied onto the PCB metal pads by stencil printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. While an excessive solder paste volume will cause solder bridging, an insufficient solder paste volume can lead to reduced solder spreading between all contact surfaces. To ensure a uniform and sufficiently high solder paste transfer to the PCB, laser-cut (mostly made from stainless steel) are preferred.

The WDSON package designs are based on a print reduction of 25% (equivalent to printing 75% of the PCB pad area). The designs assume a stencil thickness of 150 µm (6 mil); they should be revised for other thicknesses. WDSON packages can be used with thicknesses of 100 µm-250 µm (4 mil-10 mil). Stencils thinner than 100 µm are unsuitable because they deposit insufficient solder paste to make good solder joints with the die; high reductions sometimes create similar problems. Stencils in the range of 130 µm-200 µm (5 mil-8 mil), with suitable reductions, give the best results.

Post-reflow evaluations can help to assess how a stencil is performing within a given process. Two main problem areas can be addressed by improving stencil design:

- Solder balling around the perimeter of the die. This can be caused by too much solder paste, in which case the stencil might need to be reduced by more than 25%. The reduction can be symmetrical but biasing it unevenly may help to prevent solder balling; the product specific stencil designs have apertures moved further from the die edge for this reason. Solder balling can result from other external factors, such as the moisture content of the board and incorrect ramp rates or insufficient soak times in the reflow profile. Leadless packages like WDSON can sometime accentuate existing deficiencies within a process.
- Misshapen joints. If the joints are smaller or seem to be only partially made, this might suggest that there is insufficient solder to make the joint. If, however, the joints have what appear to be additional areas extending from their edges, they are usually the result of too much solder; this almost certainly the case if solder balls are also present. Insufficient solder can also cause voiding but this is more likely to arise from other factors, including surface finish, solder paste and substrate condition.

For individual design adaptations to reach the optimum amount of solder the stencil thickness, the PCB pad finish, quality, solder masking, via layout, and the solder paste type should all be considered. In every case, application-specific experiments are recommended.

Further details and specific stencil aperture recommendations can be found in the Infineon package database that is available on the Infineon web page [1]. Please choose a specific package when searching the database, which will then show an example of the stencil aperture layout for each package.

For further information about solder stencil design, please refer to the *General recommendations for board assembly of Infineon packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3.2 Solder paste

Pb-free solder pastes typically contain some sort of SnAgCu alloy (SAC solder with typically 1-4% Ag and < 1% Cu). The most common alloy is SAC305 (3.0% Ag and 0.5% Cu). The average alloy particle size must be suitable for printing the solder stencil aperture dimensions. The usage of paste type 4 or of higher type (with lower grain size of the solder alloy powder) is recommended for the assembly of the packages discussed in this document.

The solder alloy particles are dispersed in a blend of liquid flux and chemical additives (approx. 50% by volume or 10% by weight), forming a creamy paste. The flux and chemical solvents have various functions such as

adjusting the viscosity and rheology of the paste for stencil printing or removing contaminants and oxides on the surface.

The properties of pastes vary from manufacturer to manufacturer, meaning that some perform better than others. In general, high slumping pastes tend to suffer more from solder balling than slump-resistant pastes; solder balling is discussed in the next section on stencil design. In addition, some pastes appear to be more prone to voiding than others.

The solder paste solvents have to evaporate during reflow soldering, while residues of the flux will remain on the joint. The capacity of the flux additive for removing oxides is given by its activation level, which also affects the potential need for removing the flux residuals after the assembly. For leadless packages in which the solder joint is formed mainly on the package bottom side, a “no-clean” paste is recommended to avoid subsequent cleaning steps underneath the package. The small gaps make cleaning highly difficult if not impossible. No-clean fluxes are designed to be fully cured or ‘caramelized’ during the reflow process, forming an inert varnish-like residue that need not to be washed off or removed.

Some solder pastes (marketed as ‘probeable’ or ‘pin-testable’) contain fluxes that remain soft or tacky for up to a month to enable underlying PCB pads to be electrically probed on an automated test system using pins or needle-type probes. Unfortunately, as the residues remain acidic and chemically active until they harden, they can cause electrical leakage and/or corrosion, especially in damp or moist environments. Therefore, Infineon recommends that assemblies using probeable or pin-testable solder pastes are not exposed to their intended operating environment or subjected to reliability testing that involves moisture testing until the flux residues are fully cured. Alternatively, such assemblies can be baked after electrical testing to cure the flux more quickly.

Note: *Infineon recommends that assemblies using ‘probeable’ or ‘pin-testable’ solder pastes shall be baked after electrical testing to cure the flux. They shall not be directly subjected to their intended operating environment or any environment that involves moisture.*

Vision systems may be used for inspection of solder paste depots after printing. They can either be integrated into the printer or as separate automated solder paste inspection (SPI) equipment. The lateral solder paste coverage as well as the volume can be measured. Adequate acceptance criteria have to be defined based on the manufacturing setup.

Generally, solder paste is sensitive to age, temperature, and humidity. Please follow the handling recommendations of the paste manufacturer.

3.3 Component placement

The liquid solder may support the formation of proper joints with the self-alignment effect that is caused by the surface tension. The components, however, have to be placed accurately depending on their geometry. Positioning the packages manually is not recommended, especially for packages with small terminations and pitch. An automated pick-and-place machine is recommended to obtain reliable solder joints.

Component placement accuracies of +/-50 µm and less are obtained with modern automatic component placement machines using vision systems. With these systems, both the PCB and the components are optically measured and the components are placed on the PCB at their programmed positions. The fiducials on the PCB are usually located on the edge of the PCB. Additional fiducials close to individual mounting positions (local fiducials) are also possible. These fiducials are detected by a vision system immediately prior to the mounting process.

The WDSON packages might feature a standoff between the landing areas of the can and the solder bumps of up to 100 µm. A proper contact between the printed solder paste and the package bumps can be ensured by applying an adequate placement force or over-travel rather than touchless placement.

Note: It is not recommended to apply touchless placement but rather assemble the components onto the PCB with a specific placement force.

For further information about component placement, please refer to the *General recommendations for board assembly of Infineon packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3.4 Reflow soldering

For PCB assembly of the WDSON packages, the widely used method of reflow soldering in a forced convection oven is recommended. Soldering in a nitrogen atmosphere can generally improve the solder joint quality but is not necessary to create a reliable joint.

The soldering profile should be in accordance with the recommendations of the solder paste manufacturer to achieve optimal solder joint quality. The position and the surrounding of the component on the PCB, as well as the PCB thickness, can influence the solder joint temperature significantly. Power packages where leakage currents and shorting below the component have to be considered should be soldered with decreased flux spreading. Therefore, it is recommended to optimize the reflow profile in such a way that excessive flux or solder spattering is avoided.

The WDSON package is designed to have superior thermal resistance properties. For this reason, it is essential that the core of the substrate reaches thermal equilibrium during the pre-heating stage of the reflow profile to ensure that adequate thermal energy reaches the solder joint.

Maximum reflow conditions and cycles

Components that are moisture-sensitivity level (MSL) classified by Infineon have been tested by three reflow runs in accordance with the J-STD-020 standard, including a double-sided reflow and one rework cycle. The maximum temperatures must not be exceeded during board assembly. Please refer to the product barcode label on the packing material that states this maximum reflow temperature according to the J-STD-020 [4] standard as well as the MSL according to the J-STD-033 standard [5].

Infineon WDSON packages are generally suited for mounting on double-sided PCBs. Solder joints of components on the first side will again reflow in the second step. In the reflow zone of the oven (i.e. where the solder is liquid), the components are only held in place by wetting forces from the molten solder. Gravity acting in the opposite direction will elongate the solder joints, unlike joints on the top side, where gravity will force the components closer to the PCB surface. This shape will be preserved during cooling and therefore will result in a higher stand-off on the bottom side after the reflow process.

For further information about reflow soldering, please refer to the *General recommendations for board assembly of Infineon packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

4 Cleaning

After the soldering process, some flux residues may remain on the board, especially near the solder joints. Generally, cleaning beneath a component with bottom-only terminations is difficult due to the small gap between the component body and the PCB. Therefore, a “no-clean” flux is recommended whose residues usually do not have to be removed after the soldering process.

In case the solder joints have to be cleaned, the cleaning method (e.g. ultrasonic, spray, or vapor cleaning) and cleaning solution have to be selected while taking into account the type of package, the flux used in the solder paste (rosin/resin-based, water-soluble, etc.) as well as the environmental and safety aspects. Even small residues of the cleaning solution should be removed or dried out very thoroughly. For recommended cleaning solutions, please contact the solder paste or flux manufacturer.

5 Underfill

An underfill process may improve board-level reliability, but this depends highly on the underfill material properties, the individual mounting situation of the package, and the general application requirements of the entire system.

In case of questions on underfilling WDSON packages, please contact your local sales, application, or quality engineer.

6 Inspection

6.1 Optical solder joint inspection

The drain connections on a WDSON package are external, conventionally filleted solder joints as can be seen in Figure 9. This means that they can be inspected by automated optical inspection (AOI) in accordance with industry standards such as IPC-A-610 [6].

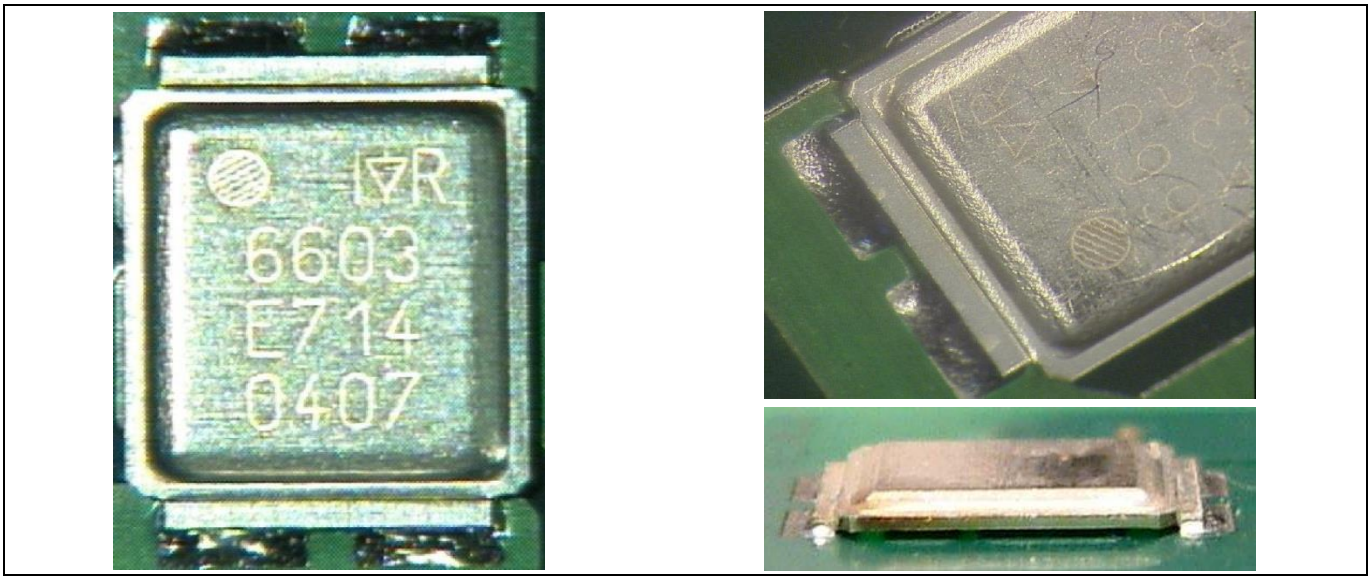

Figure 9 Photographs of solder fillets on the drain

A visual inspection of the gate and source solder joints with conventional optical equipment is not possible. Endoscopes provide and alternative kind of inspection equipment. An optical head can be brought close to the solder joints and certain failures such as opens and shorts can be detected. It must be considered that the setup of such an inspection might cause additional effort. The method is not considered suitable for in-line inspection.

For engineering tasks, cross-sectioning can provide detailed information about the solder-joint quality. Due to its destructive nature, cross-sectioning during monitoring is not practical.

6.2 X-ray solder joint inspection

Automated X-ray inspection (AXI) systems are appropriate for efficient inline control of components where solder joints are formed below them. These joints cannot be inspected properly by optical systems. X-ray inspection systems are available as batch or inline, 2D or 3D solutions. They usually consist of an X-ray camera and the hardware and software needed for inspection, controlling, analyzing, and data transferring routines. These reliable systems enable the user to detect soldering defects such as poor soldering, bridging, voiding, and missing parts. Other defects such as broken solder joints are, however, not easily detectable by X-ray.

Figure 10 shows typical X-ray photographs of WDSON packages. The can outline, PCB features, and the solder joints that connect the package to the PCB are visible. Large exposed pads may tend to increased voiding because they do not provide a sufficient ratio between volume and surface necessary for proper outgassing of the organic compounds during reflow. Generally, the extent of voiding depends on the board pad size and plating, the stencil layout, the solder paste, and the reflow profile. For thermal evaluations, the entire thermal path must be considered as well as all boundary conditions such as the application environment or the electrical use of the component.

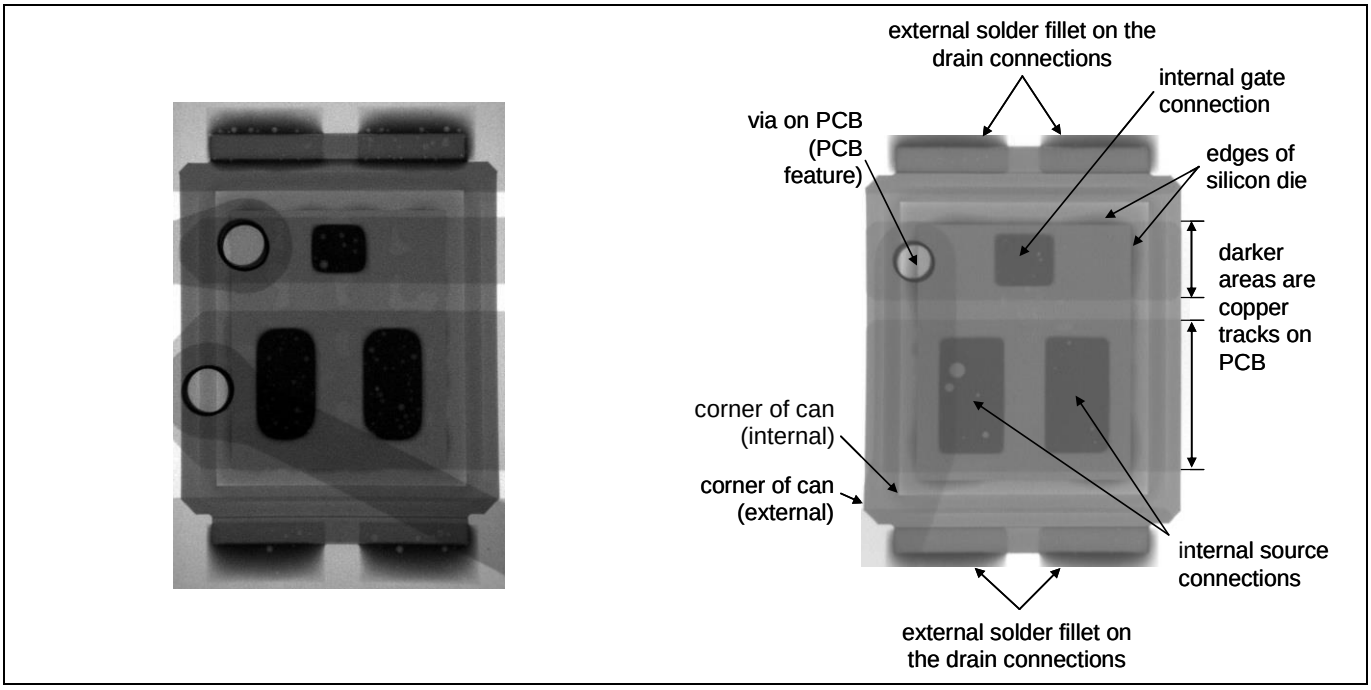

Figure 10 Typical X-ray images of a mounted WDSON package

6.3 Failure catalogue

Optical inspection can detect several possible assembly issues, including devices that are twisted, rotated, tilted, and both twisted and tilted at once.

However, as the direct gate and source contacts are within the outline of a WDSON package, X-ray microscopy is needed to inspect the inner solder joints with confidence. Assembly issues such as bridging, solder balling, voiding or a generally low solder joint connection can be detected.

The images in this section were deliberately created for illustrative purposes. They do not commonly arise in practice.

Misplaced devices

Twisted devices are mounted on the pads with a considerable rotation, as shown in Figure 11. The device is clearly twisted but external solder fillets are still visible on all four drain contacts. The X-ray shows good solder joints on the gate and source contacts.

Twisted devices should be rejected if one of the following statements applies:

- There is less than 75% coverage on gate or source contacts
- There is less than 50% coverage on drain contacts

Rotated devices are mounted the wrong way around (180° rotation), as shown in Figure 11. Although the external solder fillets on the drain contacts are good, the X-ray reveals the problems with the gate and source contacts. You can see in the photograph that the device markings are upside down.

Rotated devices shall be rejected.

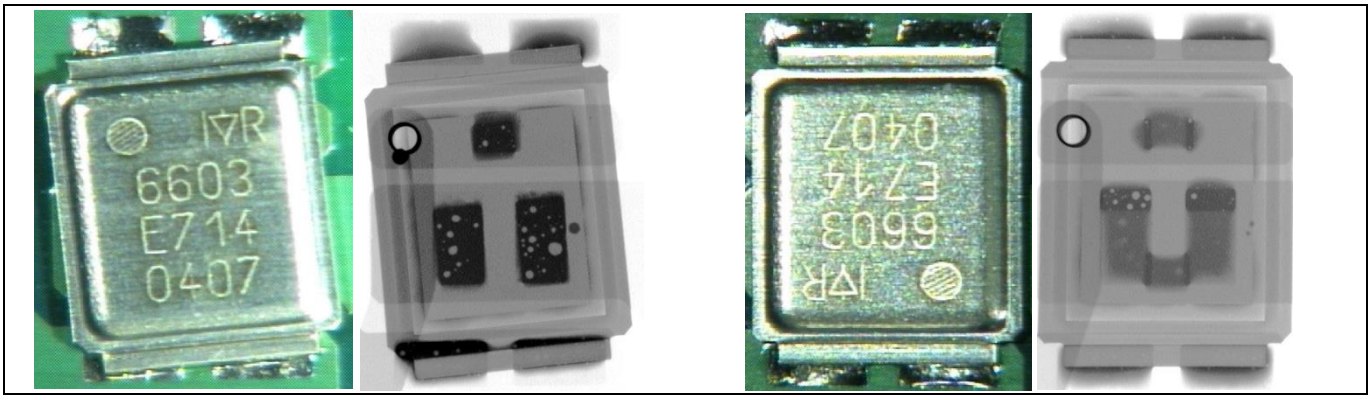

Figure 11 Optical and X-ray images of twisted devices (left) and 180° rotated devices (right)

Tilted devices are not in parallel to the PCB plane. Figure 12 shows an example. Although the device is self-centered, visual inspection from above reveals more solder on the bottom drain contacts in the photograph than on the top ones. This indicates a problem with the solder process: solder has been sucked underneath the device. Visual inspection from the side reveals that the device is tilted by more than 3° from the PCB. This again indicates a problem with solder under the device. The X-ray confirms the problem; it also reveals that the gate contact is not made and the tops of the source contacts are indistinct, indicating that the joints are tapered.

Figure 12 also shows images of devices that are tilted as well as twisted. Visual inspection from above reveals the twist and from the side reveals the tilt. The X-ray shows the combined effects, with the contact area reduced by the twist and the pad definition impaired by the tilt. The contacts on the right side of the device are poorly made.

Tilted or tilted as well as twisted devices should be rejected if one of the following statements applies:

- There is less than 75% coverage on gate or source contacts
- There is less than 50% coverage on drain contacts
- The angle of tilt exceeds 3°

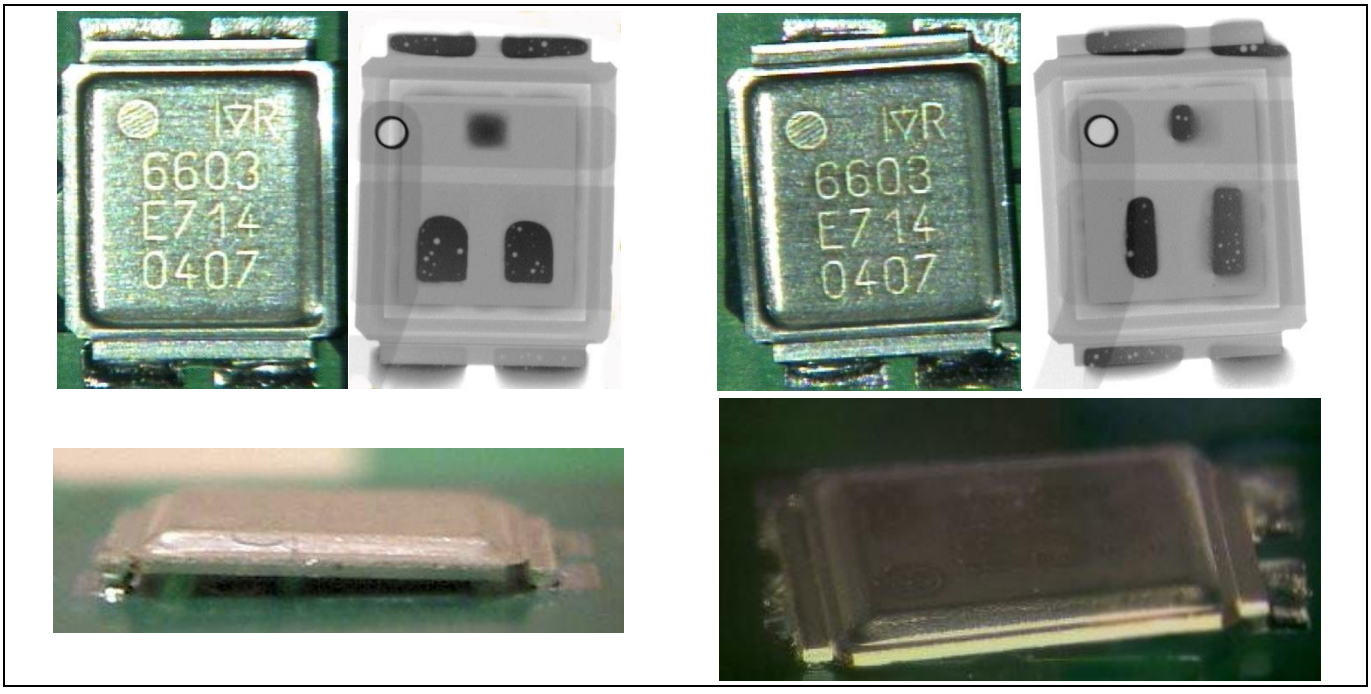

Figure 12 Optical and X-ray images of tilted devices (left) and tilted as well as twisted devices (right)

Reduced joint connection area

Voids are describing holes in an otherwise closed solder joint connection. They can be a natural effect of the outgassing organics from solder paste flux. To evaluate accurately the degree of solder voiding, it is important to use imaging and/or calculation software. Estimating a percentage intuitively from an image invariably leads to inaccurate, usually exaggerated, results. Figure 13 shows two examples of solder joint voids. Despite their different appearance, measurements reveal a total void area of 13% in both cases.

Reject criteria must be based on the specific system application requirements i.e. thermal and/or electrical. Reference numbers on typical voiding levels can be found e.g. in IPC-A-610 [6].

In case of poorly formed joints, only part of the intended wettable area of the pad is in contact. In its most extreme form, it may result in open circuits. Poorly formed solder joints appear on X-ray images as irregular patterns and shapes. Examples are shown in Figure 13. As with voiding, the use of imaging and/or calculation software to evaluate the extent of the affected area is highly recommended.

Poorly formed joints should be rejected if the following statement applies:

- There is less than 75% coverage on the contacts

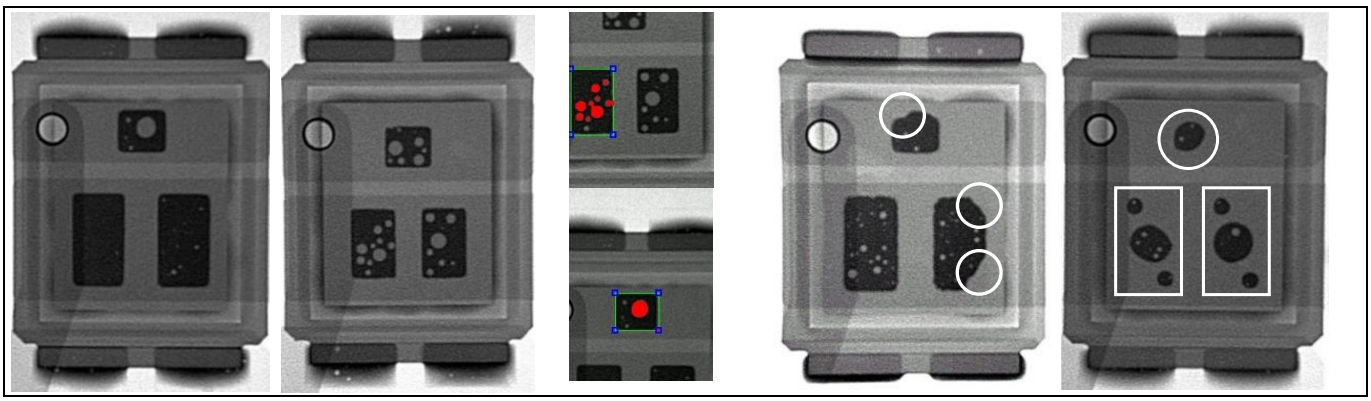

Figure 13 Examples with solder joint voiding (left) and poorly formed joints (right)

Open circuits describe failed joints where there is no electrical connection. Open circuits appear on X-ray images as pads that are faint and/or poorly defined. Figure 14 shows two examples of open circuits:

- The image on the left shows an open connection on a source pad. There is no electrical connection so this device would have to be rejected or reworked.
- The image on the left shows a drain rail where one of the two pads is open. This should be rejected because it has a maximum of 50% coverage, even if the other joint is perfect.

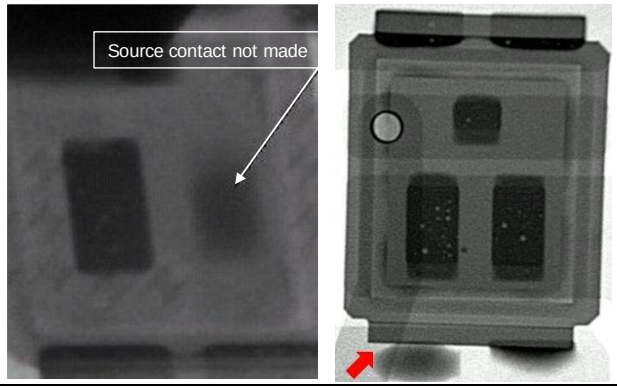

Figure 14 Examples of open circuits

Solder shorts and balling

Solder balls describe spheres of excess solder left after reflowing as marked in Figure 15. In its most extreme form, it may result in short circuits.

As with any SMD, the aim in assembling WDSON packages is to achieve good solder coverage of the joint area without solder balling. However, it is not always possible to achieve the ideal amount of solder, and solder balls sometimes form. In addition to solder quantity, an incorrect reflow profile (e.g. ramp rate too high) can cause solder balling; this happens because the solvent and/or flux boils, ejecting solder particles from the solder bulk.

Although solder balling is not desirable, a few solder balls need not necessarily be an issue. There is no evidence to suggest that solder balling impairs the function, performance or reliability of WDSON packages. This is because, once the device has been mounted, any solder balls cannot move to an area where they will cause an electrical short. In addition, the die surface is covered with a passivation material that protects it.

Only solder balls next to the gate pad, as shown in Figure 15, are likely to present problems. Although the ball will not itself cause an electrical short, a smear of flux, solder particles or contaminants could lead to an electrical short or leakage in certain circumstances. This is very rare but can be exacerbated if the device shifts during reflow.

When inspecting solder balls, consider:

- Position: Solder balls are a concern only when they occur next to the gate pad, between it and the closest drain pad.
- Shorting: Use electrical tests to check for shorts. If there are no shorts when the device is mounted, there is no evidence to suggest that solder balls can cause shorting later.

The number and size of solder balls is not important. However, if solder balls occur often, use SPC (Statistical Process Control) techniques to identify and address the cause.

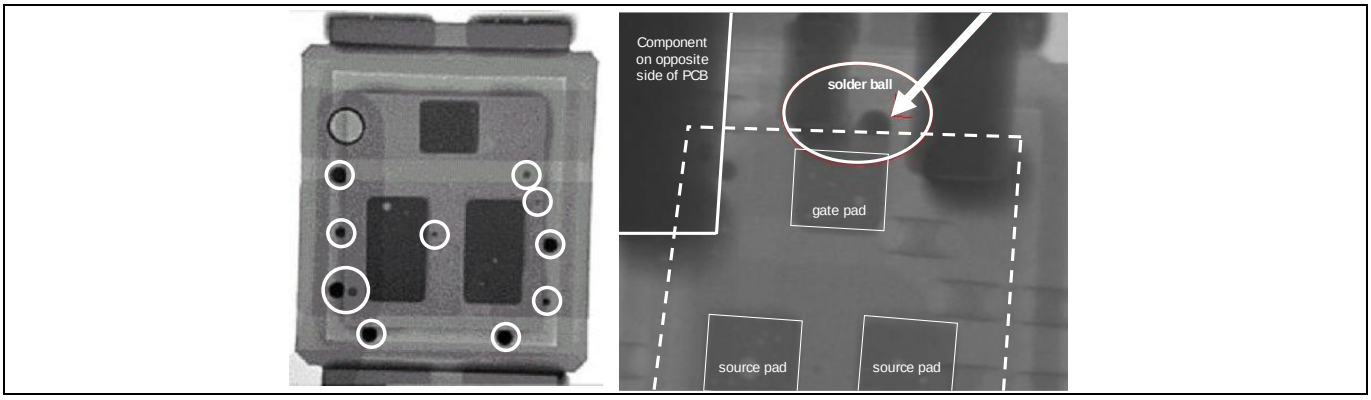

Figure 15 Examples of randomly distributes solder balls (left) and critical solder balls between two pads (right)

Short circuits describe non-intended electrical connections between contacts that should be isolated. Like solder balling, it results from excess solder. Figure 16 shows two examples of short circuits:

- The image on the left shows a solder bridge between the source pads. Although this is undesirable, it is acceptable because the pads are electrically common.
- The image on the right shows a solder bridge between the gate pad and a track on the PCB. This must be rejected or reworked. It might be detected in electrical testing if not by X-ray.

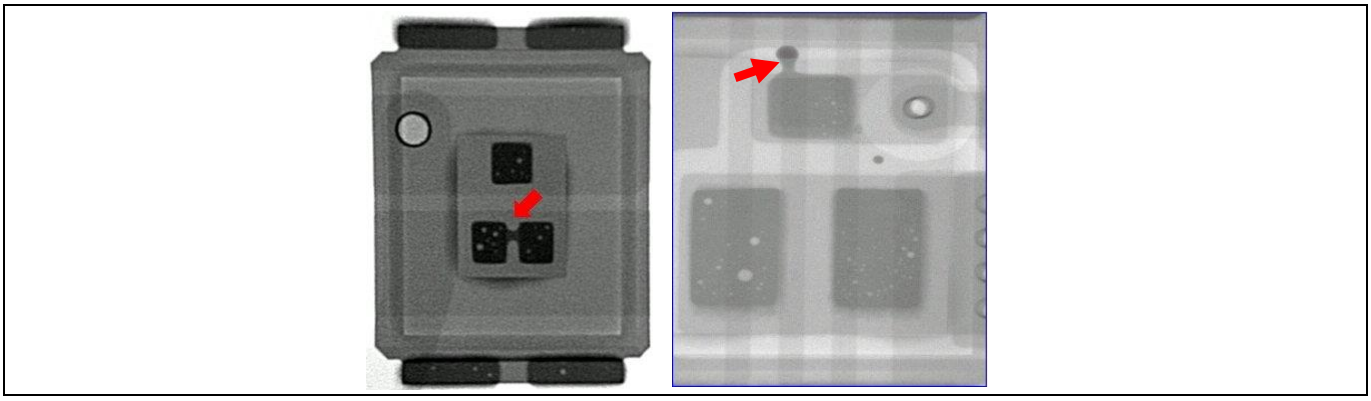

Figure 16 Examples of short circuits

Board design issues

In addition to their role in inspecting for processing faults, X-rays can reveal board design issues.

Figure 17 shows the gate pad on the PCB extending beyond the edge of the die. Although the border of passivated silicon between the edge of the gate contact and the edge of the die on the device should prevent problems from arising, PCB pads should be defined accurately.

Figure 17 also shows poor edge definition on solder joints. The cause is the lack of a solder mask to define the gate and source pads; they are defined only by the edge of the copper track.

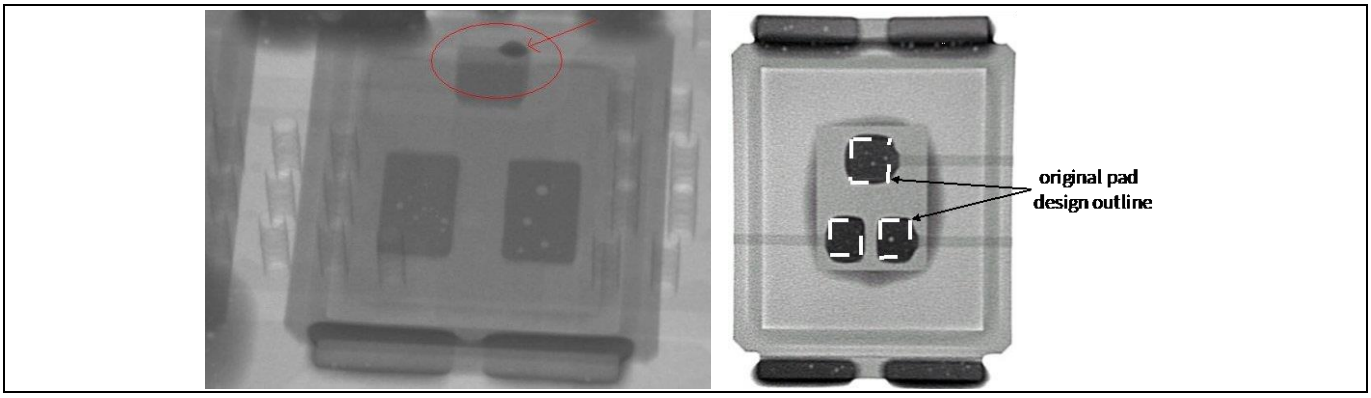

Figure 17 Over-sized gate pad on PCB (left) and absence of a solder mask to define pads (right)

7 Rework

Infineon WDSON package solder joints are generally reworkable. The reuse of de-soldered components is not recommended. The de-soldered components should be replaced by new ones.

A rework process of SMD packages is commonly done on special rework equipment. There are various systems available that meet the requirements for reworking SMD packages. All handling guidelines discussed in this document have to be respected. Special focus should be on the following items:

- Due to the decreased automation level given by the general rework approach, even higher care compared to standard assembly must be taken. Tools that do not damage the component mechanically have to be chosen. Mechanical forces that do not necessarily cause visible external damage can still cause internal damage that reduces the component's reliability. A proper handling system with vacuum nozzle may be the gentlest process and is therefore recommended. However, the impact of rework tools has to be assessed properly. In general, more manual handling increases the effort for documentation, training, and monitoring of the rework process(es).
- During rework, special care must be taken concerning the proper moisture level of the SMD component according to the J-STD-033. Drying the PCB and the component prior to rework might be necessary. A proper drying procedure for SMD packages is described in the international J-STD-033 standard [5]. Please also refer to the recommendations of your PCB manufacturer and take all specific needs of components, PCB, and other materials into account.
- Whatever heating system is used (hot air, infrared, hot plate, etc.), the applied temperature profile at the component must never exceed the maximum temperature according to the J-STD-020 standard. Depending on the specific heating profile used during rework, components adjacent to the mounting location might also experience a further "reflow run" in terms of the J-STD-020 standard [4]. Internal investigations have shown that the temperature profile must be recorded.

If a device is suspected to be defective and a failure analysis is planned, Infineon usually expects customers to de-solder the component prior to return to Infineon. The component shall be returned in a proper condition according to the original package outlines.

In some special cases such as solder joint inspection Infineon may request that the PCB or part of the PCB with the component still attached should be sent to Infineon.

Note: *Before returning a device for failure analysis at Infineon, please clarify the return condition of the suspected component (i.e. onboard or de-soldered) with the Infineon Application Engineer or Customer Quality Manager who supports your company.*

For further information about component rework on PCB, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

8 Acronyms and abbreviations

AOI	automated optical inspection
AXI	automated x-ray inspection
ESD	electrostatic discharge
IMS	insulated metal substrate
I/O	input/output
MG	metal green
MOSFET	metal-oxide-semiconductor field-effect transistor
MSL	moisture-sensitivity level
NSMD	non-solder mask defined pad
PCB	printed circuit board
SAC	tin silver copper (SnAgCu)
SMD	solder mask defined
SMD	surface-mount device
SMT	surface-mount technology
WDSON	very very thin profile dual small outline non-leaded

References

[1] Infineon: Packages. https://www.infineon.com/packages.

[2] International Electrotechnical Commission: IEC 60068-2-58. Environmental testing - Part 2-58: Tests - Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD).

[3] Electronic Components Industry Association, Assembly and Joining Processes and JEDEC Solid State Technology Association Committee: EIA/IPC/JEDEC J-STD-002. Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires.

[4] JEDEC Solid State Technology Association: IPC/JEDEC J-STD-020C – July 2004. Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices.

[5] JEDEC Solid State Technology Association: IPC/JEDEC J-STD-033D – April 2018. Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.

[6] Association Connecting Electronics Industries: IPC-A-610. Acceptability of Electronic Assemblies.

Revision history

Document revision	Date	Major changes since the last revision
3.00	2022-09-23	Complete update of document template and structure, review of technical content

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2022-09-23

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
B179-I1316-V3-7600-EU-EC

IMPORTANT NOTICE

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.