BTN7030-1EPA Design and PCB guideline Application Note

About this document

Scope and purpose

This document compiles application hints for the application of the BTN7030-1EPA, the NovalithIC™ Lite. This document must be used in conjunction with the device datasheets.

Intended audience

Developers, working with the BTN7030-1EPA.

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1 Introduction

The NovalithIC™ Lite is part of an integrated half-bridge family, suitable for driving DC motors and solenoids.

The device is a monolithic chip integrated in SMART7 technology. BTN7030-1EPA is a protected half-bridge with integrated driver, providing protection and diagnosis functions. The high side power stage is built using a N-channel vertical power MOSFET with charge pump, while the low side power stage uses no charge pump. This device has an exposed pad which ensures better cooling.

1.1 External components

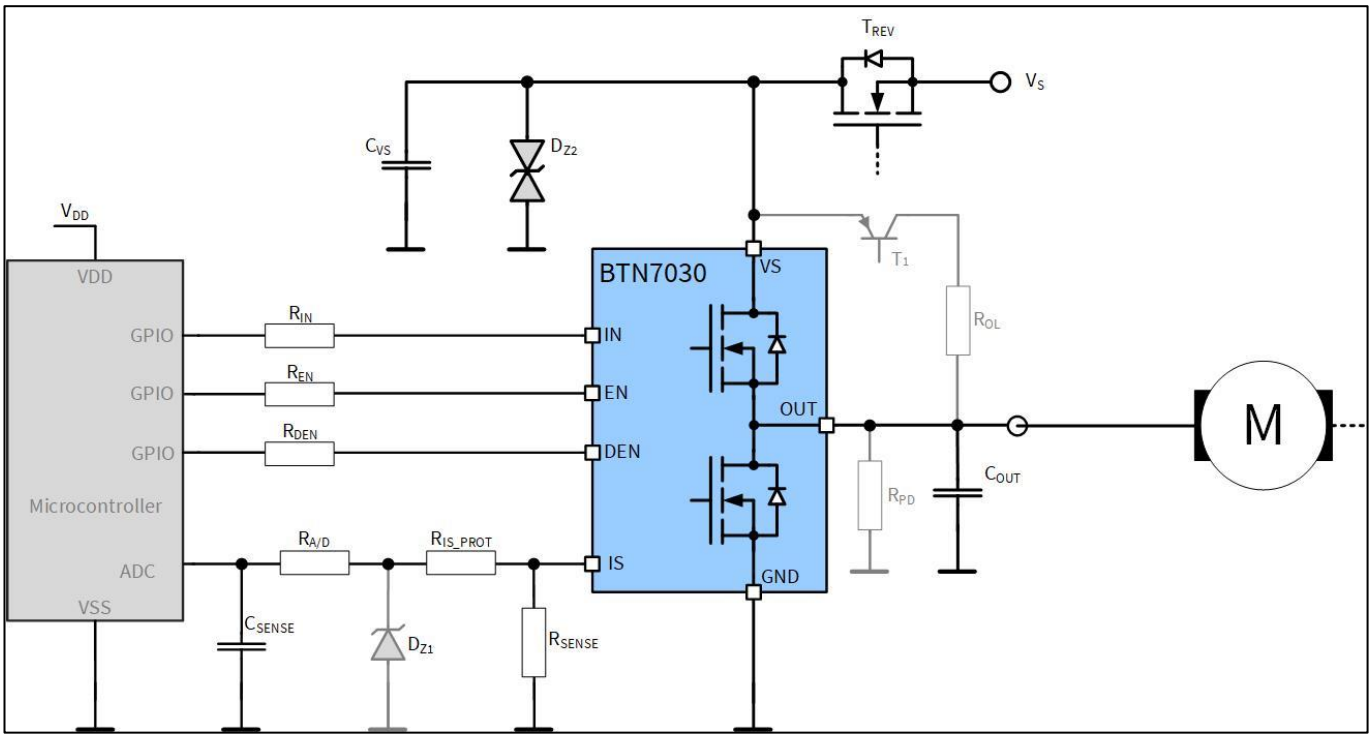


Figure 1 Application circuit example

Components in the external circuitry:

- C_{VS}: filtering voltage spikes on the battery line. This electrolytic capacitor is required to keep the voltage ripple at the Vs-pin low during switching operation. It is usually recommended that the voltage ripple at the Vs-pin to the GND-pin is kept below 1 V (ΔV_S) peak to peak. The value of CVS must be aligned accordingly. The layout is very important too. , this capacitor should be positioned with very short wiring close to the NovalithIC™ Lite chip. This must be done to keep the parasitic inductors of the PCB-wires as small as possible. Equation below shows how to calculate the right value of this capacitor.

  For more details please refer to NovalithIC™ half-bridge family BTN89xx.

$$C_{VS} = \frac{I_{nom} * T_{PWM} * duty\_cycle}{\Delta V_S}$$

- C_{OUT}: This ceramic capacitor helps improve the EMI and the ESD performance of the application. Good results have been achieved with a value of 100 nF. To keep the RF and ESD out of the board, the capacitor is most effective when positioned directly on the board connector. In addition, the parasitic inductance could be kept low by placing at least two vias for the connection to the GND-layer.
- T_{REV}, D_{Z2}, R_{IS_PROT}: reverse battery protection.
- R_{SENSE}: Resistor to generate a current sensing voltage from the IS.
- C_{SENSE}: SENSE signal stabilization. A time constant ($R_{A/D}$ * C_{SENSE}) longer than 1 us is recommended. Ceramic capacitor for EMI improvement. In case the current should be measured during the PWM-phase, this capacitor must be adapted to the ON-time inside the PWM-phase. GND connection with at least two GND-vias. A good value is 1 nF. R_{IN}, R_{EN}, R_{DEN}: Protection of the microcontroller and device during overvoltage and during loss of ground.
- R_{PD}: Output polarization (pull-down). Can be used for open load in OFF diagnosis in H-bridge configuration, thus R_{OL} and T_1 wouldn't be required. It is **highly recommended** to use the pull-down (R_{PD} = 47kΩ) resistors to ensure a stable ground of the load in OFF-state. These pull-down resistors ensure that there is no voltage potential stressing the low-side MOSFETs and enables short to VS detection in OFF-state.
- R_{OL}: Output polarization (pull-up). Ensure polarization of the output during open load in OFF diagnosis, together with T_1.
- T_1: Switch the battery voltage for open load in OFF diagnosis, together with R_{OL}.
- D_{Z2}: Protection during overvoltage and in case of loss of battery while driving an inductive load.
- R_{IS_PROT}: Protection during overvoltage, reverse polarity, loss of ground. Value to be tuned according to microcontroller specifications, together with $R_{A/D}$.
- $R_{A/D}$: Protection of microcontroller ADC input during overvoltage, reverse polarity, loss of ground. Value to be tuned according to microcontroller specifications, together with R_{IS_PROT}.

2 Design guideline

For a safe and efficient motor control design, discrete components are needed, both for proper operation of the device regardless of application type, and those dependent on the application characteristics.

2.1 Schematic and layout design rules

Figure 2 show an example of a schematic plus a corresponding layout for a half-bridge motor control with NovalithIC™ Lite. The output traces are made 3 times thicker that input (18mil) in order to endure the spikes of output current that can go up to 28A in corner cases.

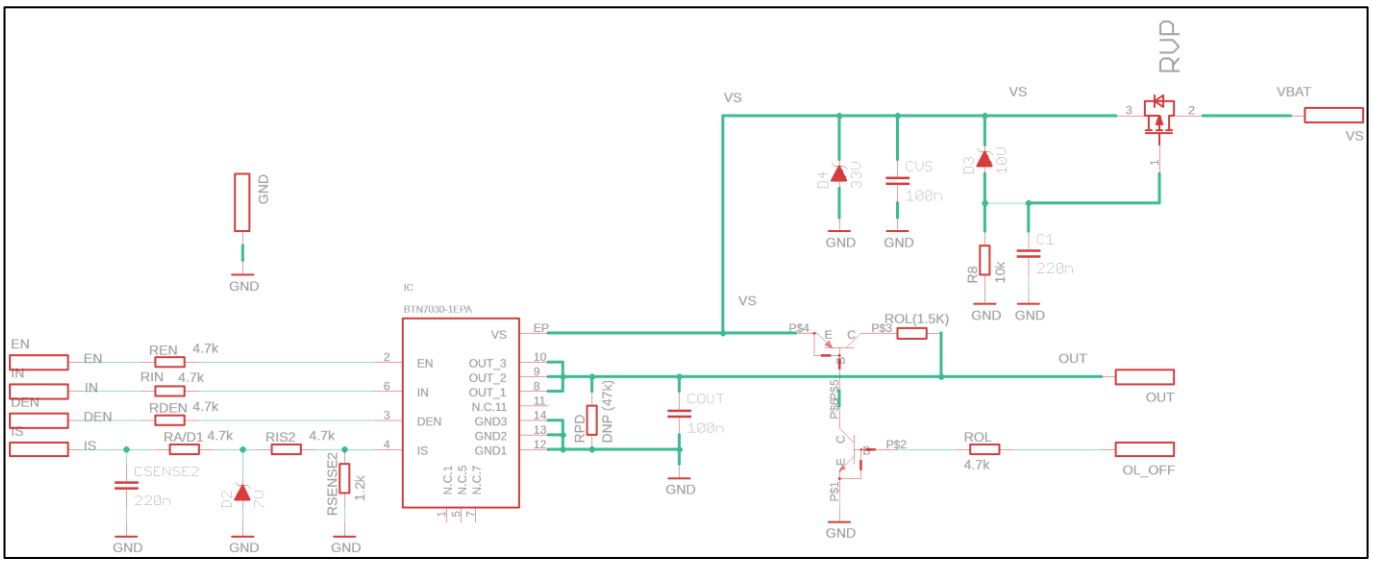
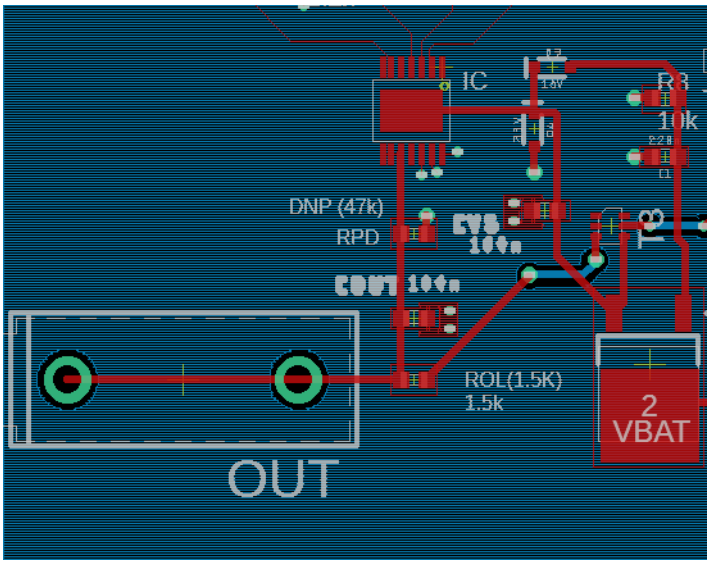


Figure 3 Example of a BTN7030-1EPA PCB output stage



3 PCB layout suggestion

3.1 Layout constraints

Depending on the technical requirements and application different approaches for dissipating the thermal energy from a PCB exist. A very common solution for applications using SMART 7 technology is a PCB with natural convection, i.e. without any cooling devices and non-blown air. In this case only the surface of the copper area, where the chips are mounted, can be used to dissipate the heat into the air. In order to achieve comparable measurement- or simulation results for the thermal behavior of the design two major standards are used:

1. $R_{thJA1s0p}$ – PCB JEDEC 1s0p board: footprint only or with cooling Cu (300 mm^2 , 600 mm^2 or 1000 mm^2)
2. $R_{thJA2s2p}$ – PCB JEDEC 2s2p board

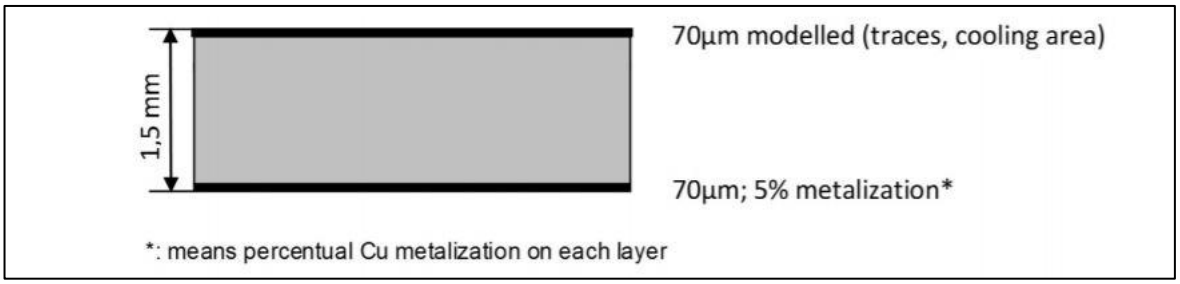


Figure 4 Cross section of JEDEC 1s0p board

On the 1s0p board, the cooling area of the cooling surface is located at the top. Additional wires (traces) are located at the bottom of the board (see **Figure 4**). **Figure 5** shows a standardized 1s0p PCB board with 600 mm^2 cooling area which will be used for measurements or simulations.

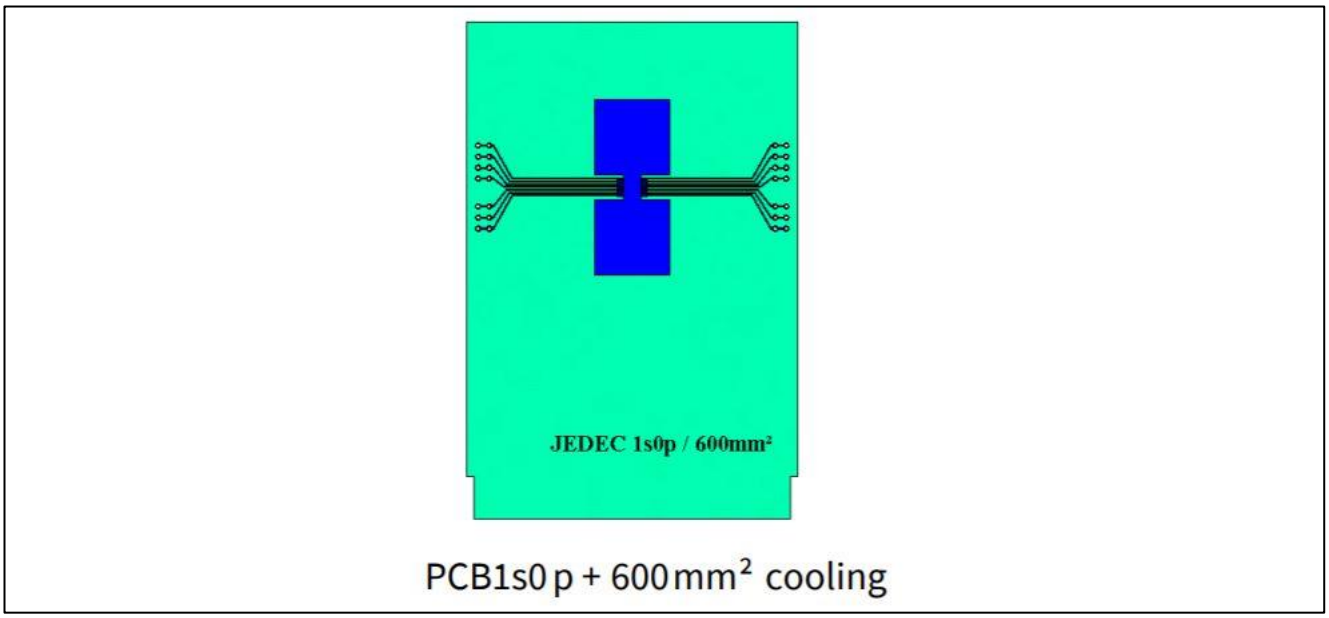


Figure 5 Standardized JEDEC 1s0p PCB board

The blue areas represent the entire cooling surface; the connecting leads in this example are on the same layer. **Figure 6** shows a cross-section of a JEDEC 2s2p PCB board used for simulations and measurements. The upper, the first internal and the lower layer are connected by means of thermal vias. This increases the surface of the copper area significantly.

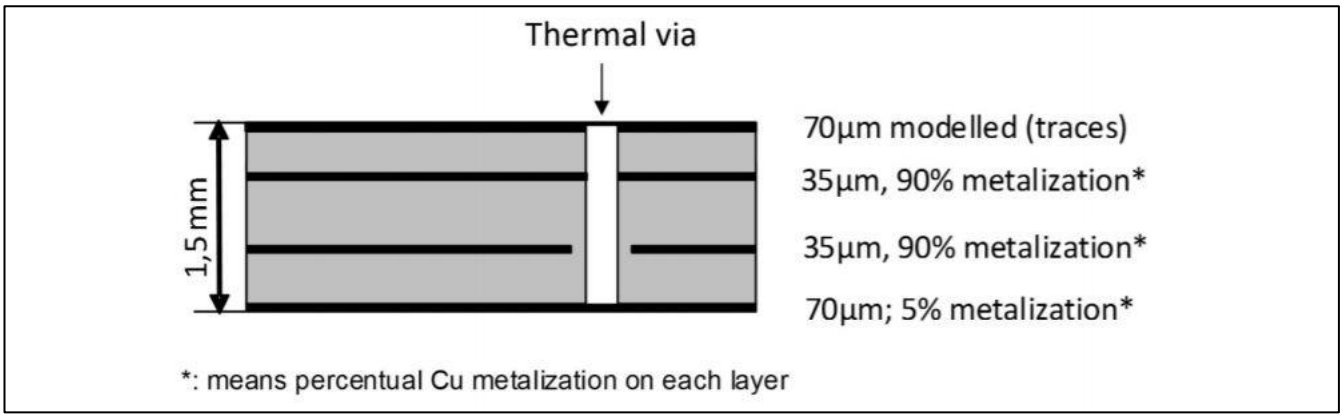


Figure 6 Cross section of JEDEC 2s2p board

The internal layer should of course not be as highly loaded, because that would make it more difficult to dissipate the heat. However, it acts as a small capacitor and can quickly absorb a certain amount of heat. Depending on available space it is also possible to provide a larger copper area for extra cooling at the top layer as well.

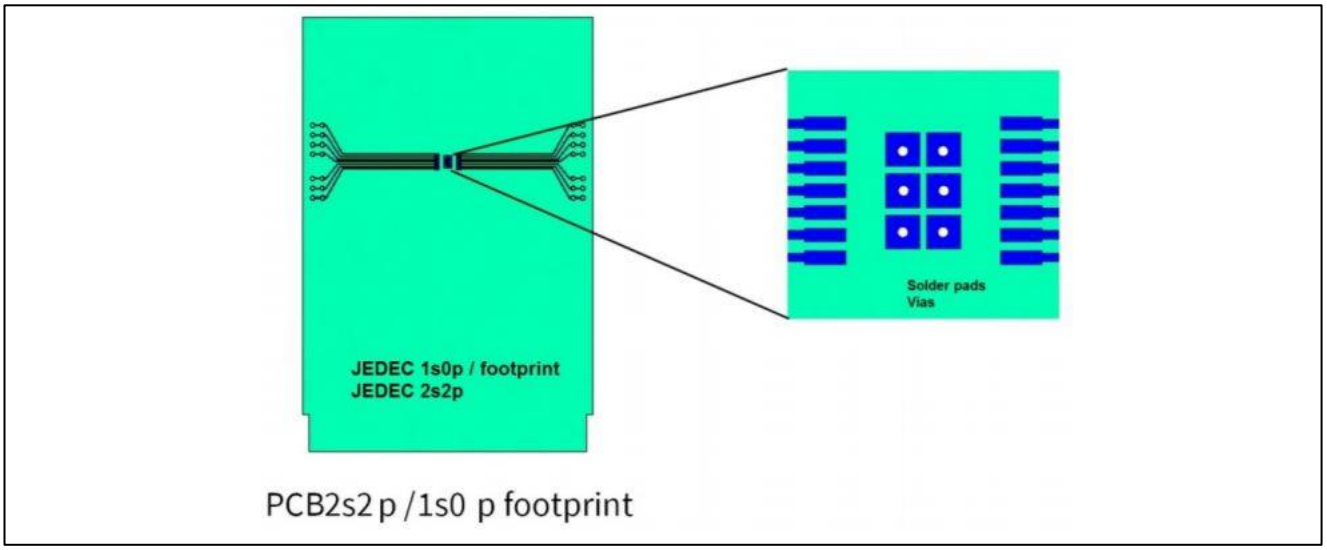


Figure 7 Standardized JEDEC 2s2p PCB board with vias at the solder pad PG-TSDSO-14

3.1.1 Placement of thermal vias

When using PCBs with JEDEC 2s2p, thermal vias are needed to ensure the thermal flow to the different layers. **Figure 8** shows a recommended arrangement of vias for the PG-TSDSO-14 package according to the standard JEDEC 51-5. The blue areas are only shown in the layout system; on the PCB only copper is visible. This is to show the locations where vias are located or where the pins can be soldered.

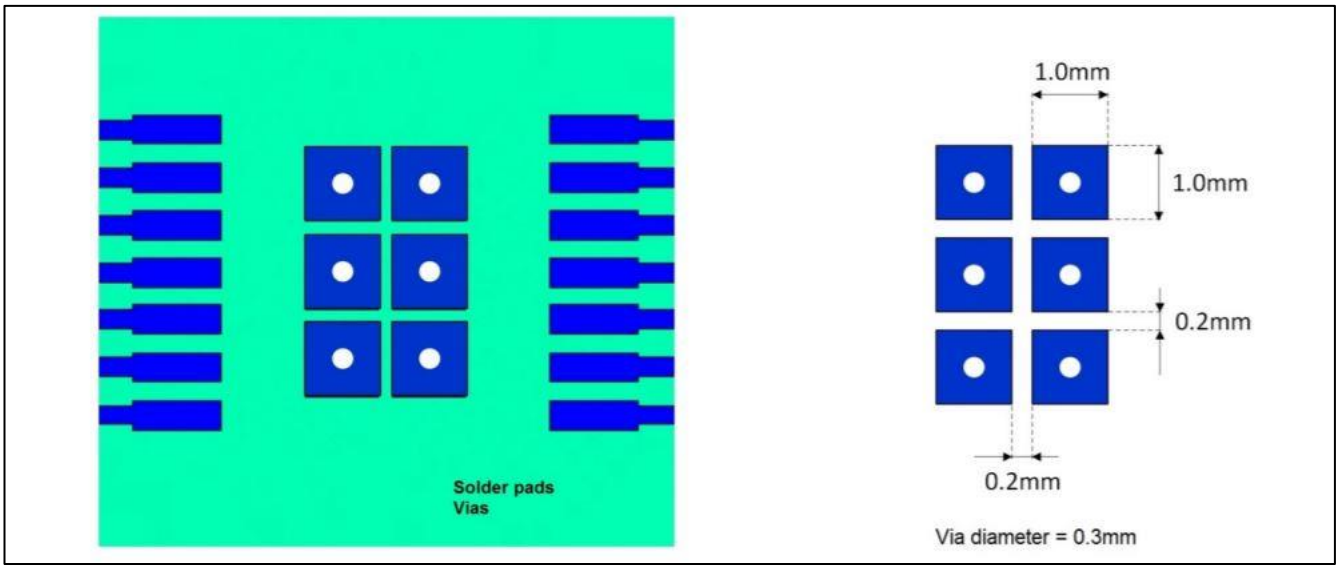


Figure 8 Specification of thermal via layout and array pattern for PG-TSDSO-14 related to JEDEC 51-5

When comparing the package PG-TSDSO-14 with the layout (not to scale), a number of possibilities for optimization are revealed because the area of the vias does not completely cover the area of the exposed pad on the chip (see **Figure 9**). For example, it is possible to implement more vias. Of course, a minimum distance between pattern and PINs must be maintained in order to ensure a corresponding insulation resistance.

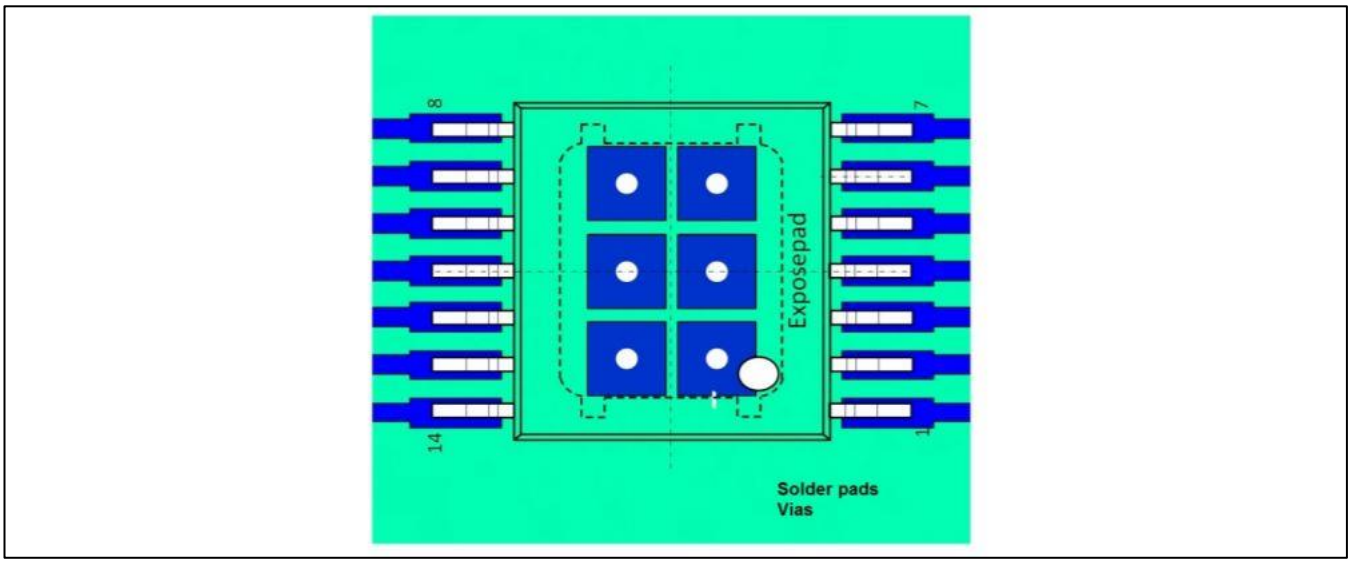


Figure 9 Via layout versus package PG-TSDSO-14

Another problem arises from the fact that some assembly companies are unable to process this type of via connections (vias directly under the package) due to soldering problems. In this case other ways of implementing thermal vias must be developed and tested.
For more details on design rules please see the application note Thermal behavior of PROFET™ +2 12V in PG-TSDSO-14 package.

3.2 Ground reference

Depending on the different functionalities, different ground references for each pin of the NovalithIC™ Lite have to be considered, especially in high current applications, in which ground shifts might occur due to parasitic inductances and line resistances of the PCB.

Based on the example schematic in **Figure 2 Example of a half-bridge schematic with NovalithIC™** , the different ground reference concepts are illustrated in **Figure 10**.

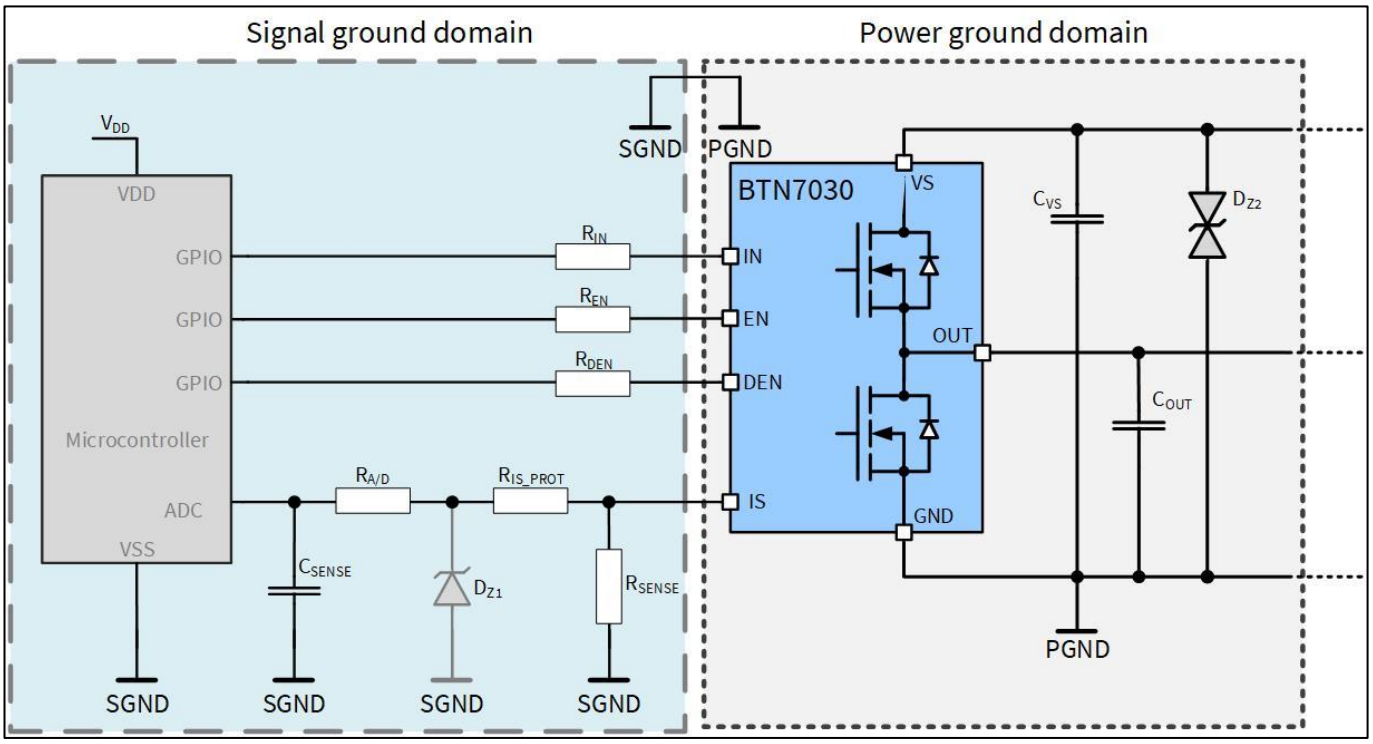


Figure 10 Simplified schematic illustrating the ground references for the signal ground (SGND) and power ground (PGND) of BTN7030-1EPA

Design rules for the ground reference:

- **IS-pin**: The reference ground for the current sense and failure flag detection is ideally the Analog-to-Digital Converter's / Microcontroller's ground as the IS-pin is a current source. If this is implemented, the absolute maximum ratings shall be respected, also in the case of ground shift between the microcontroller's (signal-) ground and the device's ground (GND-pin). Thus it is recommended to connect R_{sense} and C_{sense} to the signal ground (SGND) as shown in **Figure 10**, thus eliminating the influence of ground shift.
- **IN/EN/DEN-pins**: For the digital input pins IN, EN and DEN the internal ground reference is the GND-pin of the NovalithIC™ Lite. Therefore it should be ensured that a ground shift between the microcontroller's ground and the device's ground (GND-pin) does not influence the switching behavior, and that the absolute maximum ratings of the IN, EN and DEN pins are respected.

4 Revision history

Document version	Date of release	Description of changes
1.2	2021-01-25	Typos fixed
1.1	2020-11-24	C_{VS} explanation is added
1.0	2020-08-28	First release

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