BTN7030-1EPA Diagnosis and Protection Application Note

About this document

Scope and purpose

This document compiles application hints for the application of the BTN7030-1EPA, the NovalithIC™ Lite. This document must be used in conjunction with the device datasheets, which contain full technical details, specifications and description of operation.

Intended audience

Developers, working with the BTN7030-1EPA.

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1 Introduction

The NovalithIC™ Lite is part of an integrated half-bridge family, suitable for driving DC motors and solenoids.

The device is a monolithic chip integrated in SMART7 technology. BTN7030-1EPA is a protected half-bridge with integrated driver, providing protection and diagnosis functions. The high side power stage is built using a N-channel vertical power MOSFET with charge pump, while the low side power stage uses no charge pump. This device has an exposed pad which ensures better cooling capabilities.

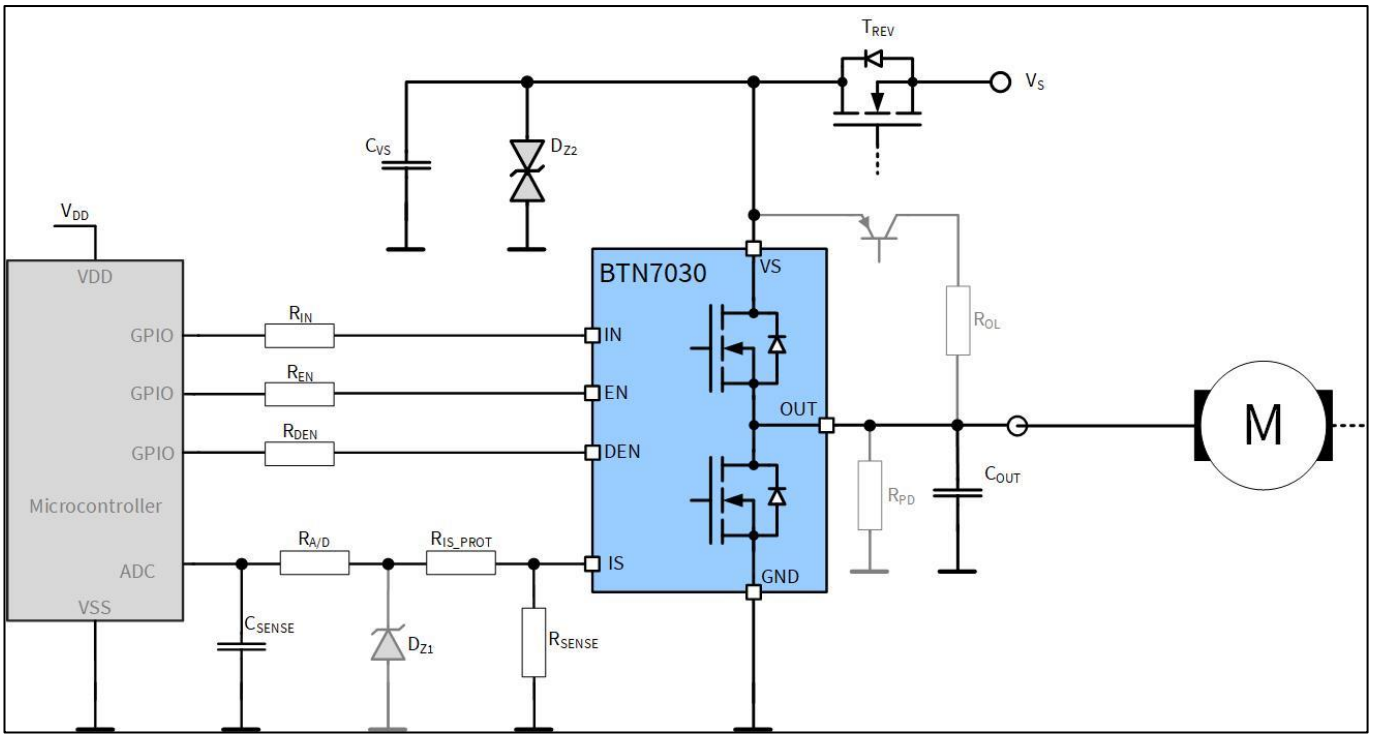

Figure 1 Application circuit example

2 Diagnosis

For diagnosis purpose, the BTN7030-1EPA provides a combination of digital and analog signals at pin IS. These signals are generically named SENSE signals. In case of disabled diagnostic (DEN set LOW), IS pin becomes high impedance (Z). Diagnosis is performed in both ON and OFF states.

2.1 Diagnosis in ON

2.1.1 Current sense (kILIS)

NovalithIC™ Lite device has a current sensing feature for the high-side switch. This means that the when the high-side stage is conducting load current (I_L) is mirrored on the SENSE pin, as shown in ***Equation 1***.

$$I_{IS} = \frac{I_L}{k_{ILIS}}, I_{IS} > I_{IS(EN)}$$

Equation 1

The accuracy of the sense current depends on temperature and load current. I_{IS} increases linearly with I_L output current through the high-side switch until I_L reaches the overload detection current $I_{L(OVLx)}$. In case of open load at the output stage (I_L close to 0 A), the maximum sense current $I_{IS(EN)}$ (no load, diagnosis enabled) is specified. This condition is shown in **Figure 2**. The blue line represents the ideal k_{ILIS} line, while the red lines show the behavior of a typical product.

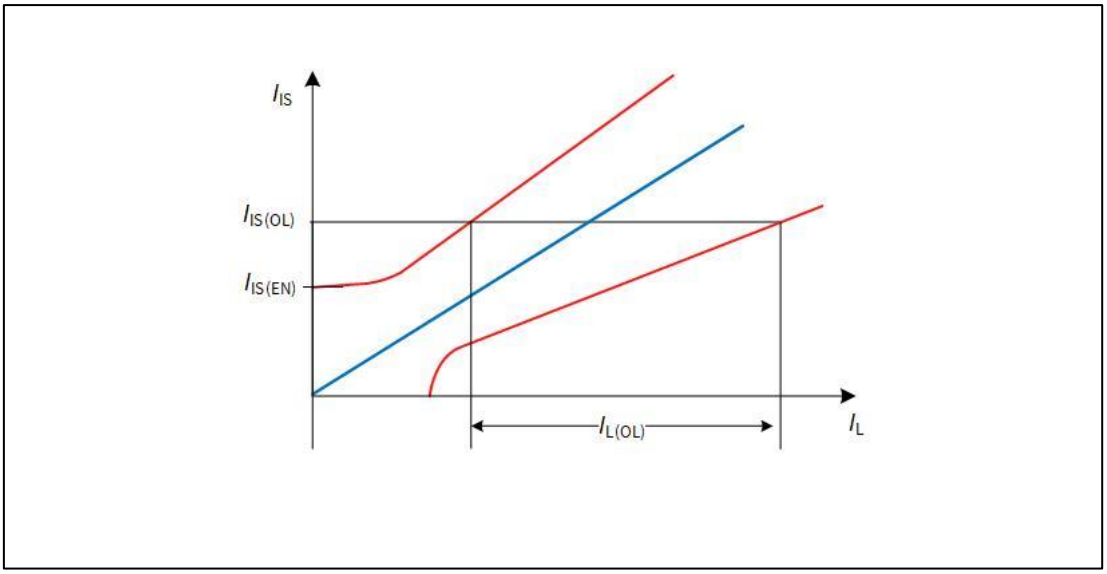

Figure 2 Current sense ratio in open load at ON condition

An external RC filter between IS pin and microcontroller ADC input pin is recommended to reduce signal ripple and oscillations (a minimum time constant of 1 µs for the RC filter is recommended).

The k_{ILIS} factor is specified with limits that take into account effects due to temperature, supply voltage and manufacturing process. When using the typical k_{ILIS} value presicion of ±5% is obtained.

Tighter limits are possible (within a defined current window) with calibration:

- a well-defined and precise current ($I_{L(CAL)}$) is applied at the output during end of line test at customer side • the corresponding current at IS pin is measured and the k_{ILIS} is calculated (k_{ILIS} @ $I_{L(CAL)}$)
- within the current range going from $I_{L(CAL)\_L}$ to $I_{L(CAL)\_H}$ the k_{ILIS} is equal to k_{ILIS} @ $I_{L(CAL)}$ with limits defined by Δk_{ILIS} The derating of k_{ILIS} after calibration is calculated using the formulas in Current sense Δk_{ILIS} calculation formulas and it is specified by Δk_{ILIS}.

The calibration is intended to be performed at $T_{A(CAL)}$ = 25°C. Here are the Δk_{ILIS} calculation formulas:

$$\Delta k_{ILIS,MAX} = 100 * MAX\left(\frac{k_{ILIS}@I_{L(CAL)\_L}}{k_{ILIS}@I_{L(CAL)}} - 1, \frac{k_{ILIS}@I_{L(CAL)_H}}{k_{ILIS}@I_{L(CAL)}} - 1\right)$$

$$\Delta k_{ILIS,MIN} = 100 * MIN\left(\frac{k_{ILIS}@I_{L(CAL)\_L}}{k_{ILIS}@I_{L(CAL)}} - 1, \frac{k_{ILIS}@I_{L(CAL)_H}}{k_{ILIS}@I_{L(CAL)}} - 1\right)$$

Equation 2

Figure 3 Current on the IS pin following the OUT current in normal operation mode

Using the **Equation 1** together with the values from **Figure 3** it is shown that the device is behaving correctly:

$$I_{IS} = \frac{V_{IS}}{R_{SENSE}} = 1.7\ A\ , I_{OUT} = 7.3\ A, kILIS = \frac{7.3\ A}{1.7\ A} = 4300$$

2.1.2 Fault current ($I_{IS(FAULT)}$)

There are number of situations in which the value of the current on IS pin signals that a fault condition is met. In this case there is no following of the output current value. These are all situations in which internal latch = 1 and DEN = HIGH and one of the following situations occur:

- Short circuit to GND (HS switch)
- Short circuit to Battery (LS switch)
- Overtemperature on HS or LS switch
- Overcurrent on HS or LS switch

In **Figure 4** the situation where the OUT is shorted to GND is shown, in this case $I_{IS} = I_{IS(FAULT)} \approx 5.5$ mA.

Figure 4 Short to GND causing $I_{IS(FAULT)}$ on IS pin

3 Protection

3.1 Undervoltage protection

In case of an Undervoltage detection, both high and low-side stages will be swichted OFF until the supply voltage V_S is above the operative threshold $V_{S(OP),}$ the channel is switched ON again with a hysteresis of $V_{S(HYS)}$. In this case there is no reflection on the IS current value.

Figure 5 shows how the the relationship between supply voltage and output stage in case of the undervoltage situation and recovery from it.

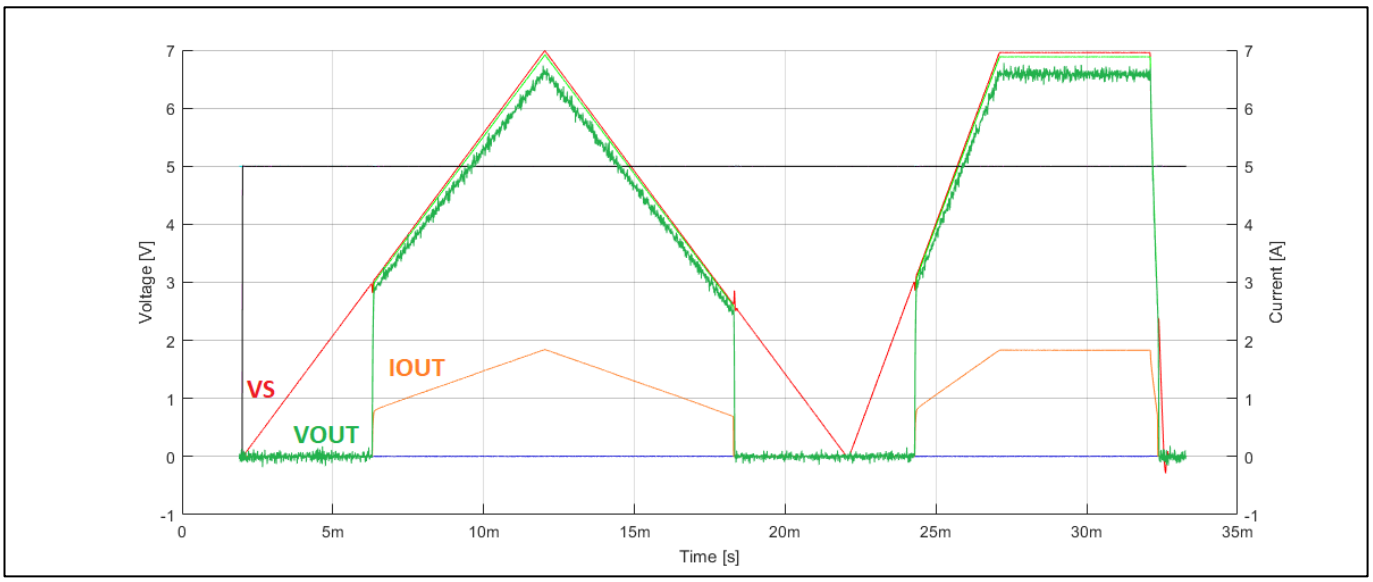

Figure 5 Undervoltage and recovery behavior of the OUT stage

3.2 Overtemperature and overvoltage protection

An increase of the junction temperature T_J above the thresholds $T_{J(SD)}$ switches OFF both the high-side and low-side output stages to prevent destruction. Overtemperature is signaled on IS pin as the $I_{IS(FAULT)}$, and this value stays as long as the internal latch is 1, as shown in ***Figure 6***. Even if the device has reached the restart condition it won't be mirrored onto IS pin as long as the internal latch is not de-latched.

This is a very good way to save the device from destruction when being exposed to high temperatures.

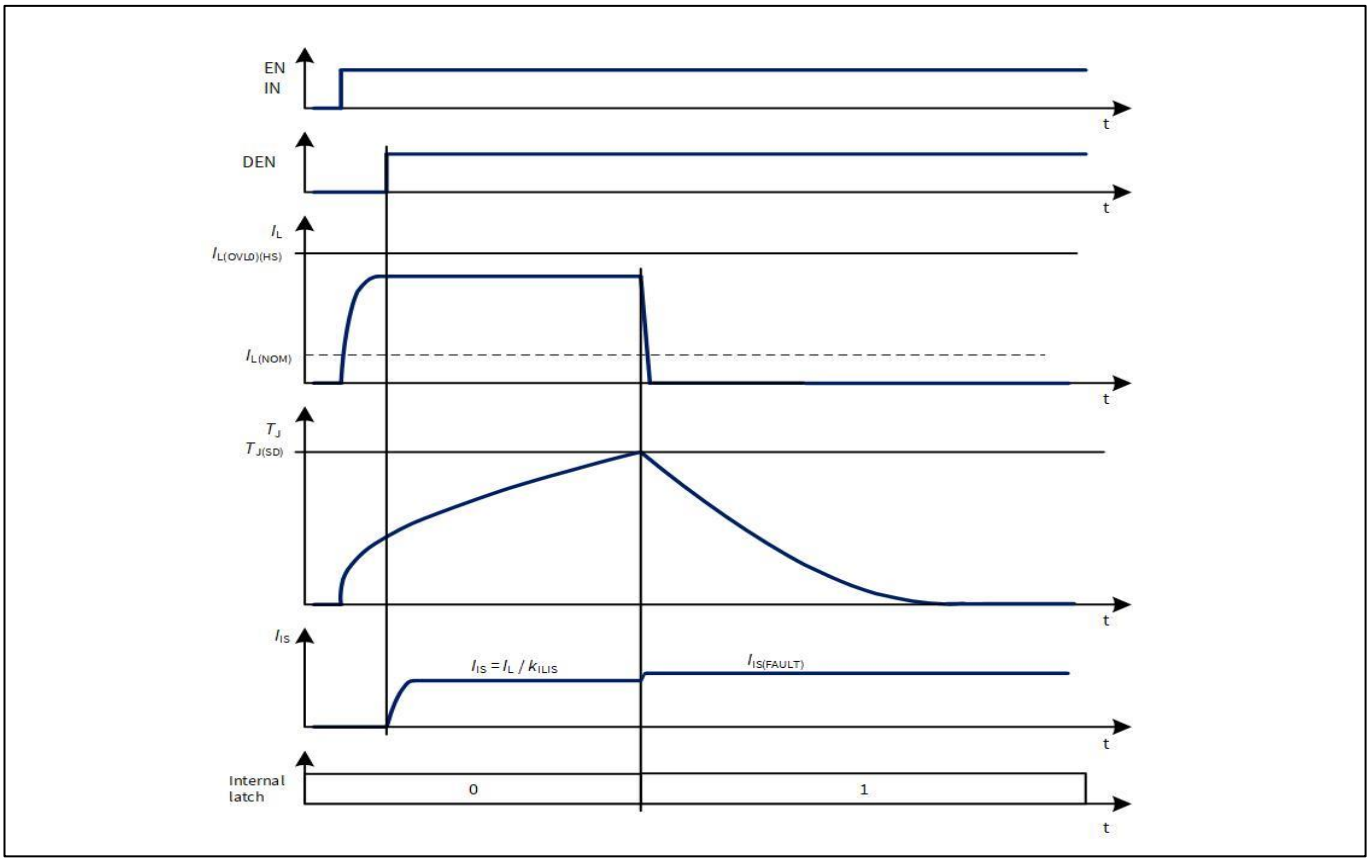

Figure 6 Overtemperature protection, with EN = "high" and load to GND

Also, **Figure 7** shows the situation in which the overvoltage caused overtemperature protection activation. IN this case the device is again switched OFF and setting the current on IS pin is set to $I_{IS(FAULT)}$.

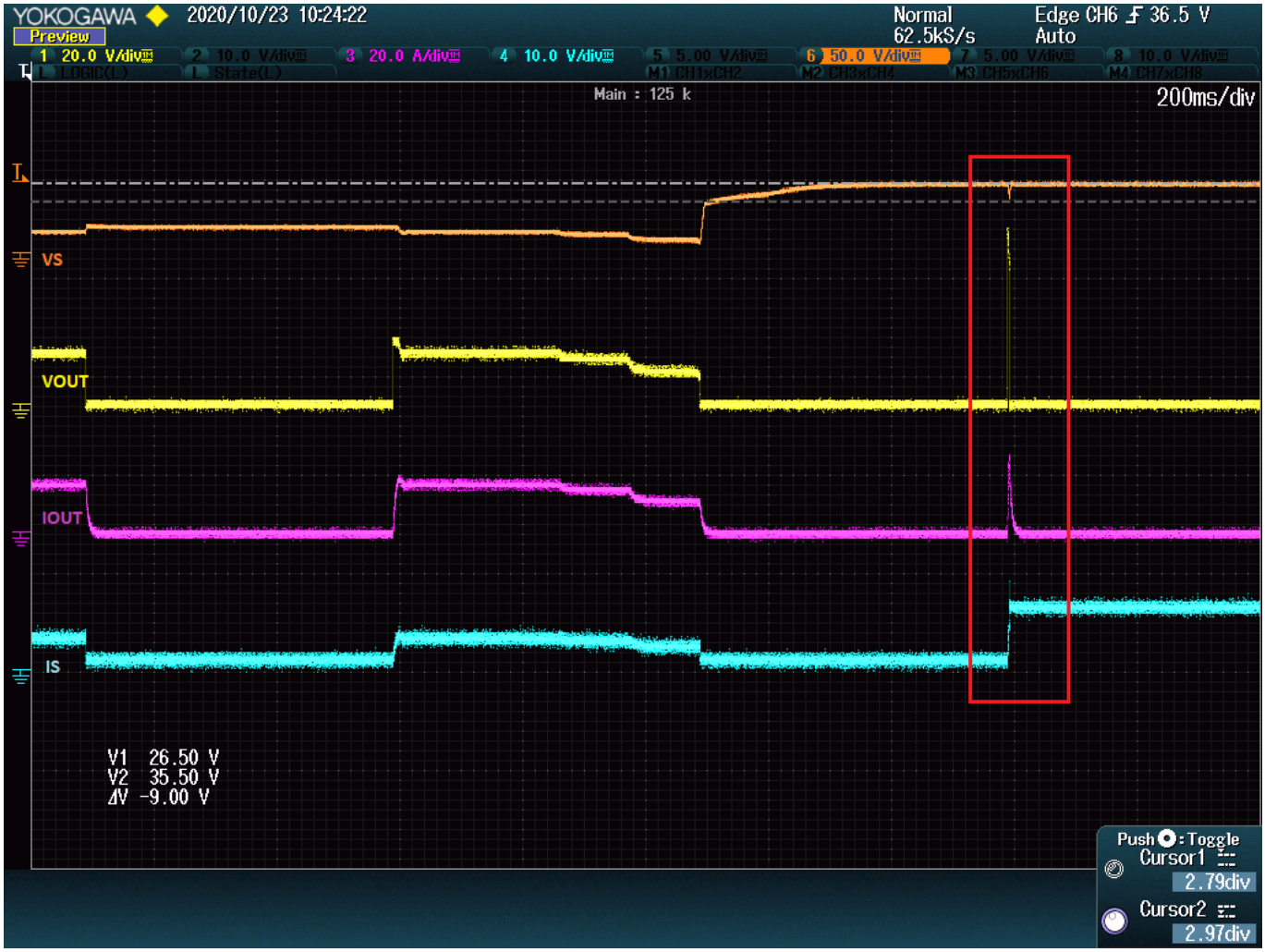

Figure 7 Overvoltage activating overtemperature protection

The clamping structure limits the negative / positive output voltage so that $V_{DS(xS)} = V_{DS(CLAMP)}$, for both the high-side and low-side output stage.

3.3 Cross current protection

In half-bridge applications it has to be assured that the high-side and low-side power output stages are not conducting at the same time, connecting directly the battery voltage to GND. This is assured by a circuit in the driver logic, generating a so called **dead time** ($t_{BLANK(xS-xS)}$) between switching off one power output stages and switching on the other. This is ensured by monitoring the state of the MOSFETs.

As a result of this cross current protection passive freewheeling can be observed both on high-side and low-side switch, as shown in **Figure 8**.

If for example, low-side switch was conducting and is switched OFF, for the duration of $t_{BLANK(LS-HS)}$ both low-side and high-side switch will be switched OFF. During this time current will flow through the body diode of the high-side switch and that will result in the short spike of the output voltage, current and maybe also supply voltage.

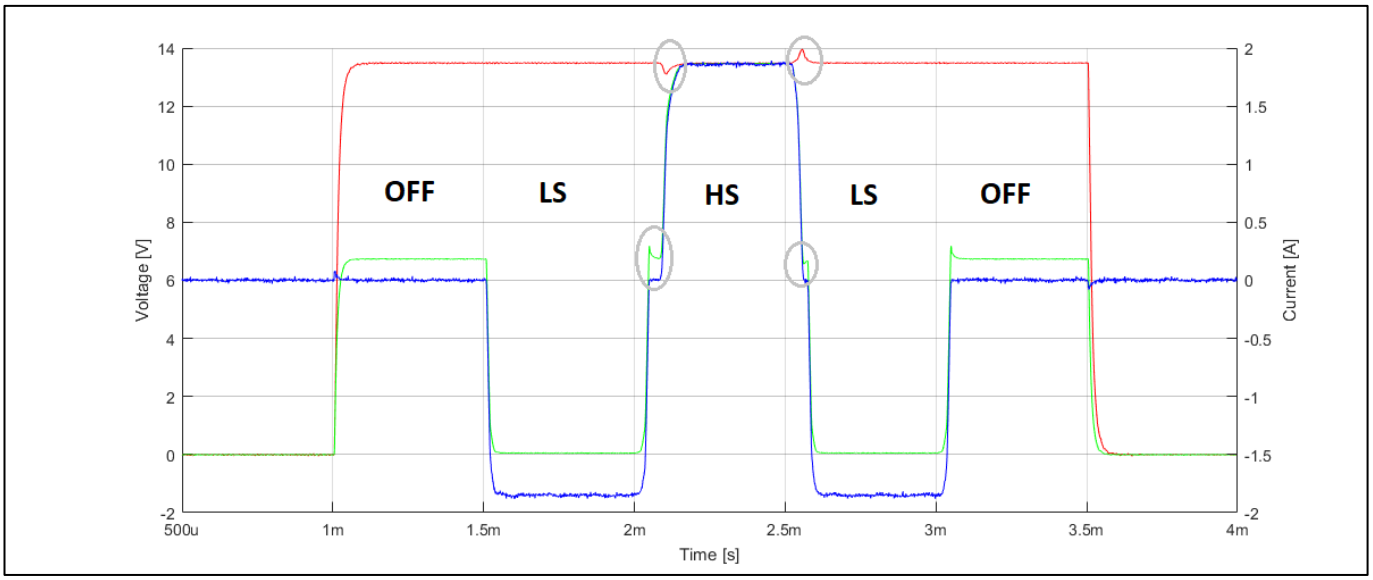

Figure 8 Passive freewheeling when switching from low-side to high-side to low-side stage

3.4 Overload protection

The BTN7030-1EPA is protected in case of overload, short circuit to battery (low-side output stage) or short circuit to ground (high-side output stage).

This device has an overcurrent detection, and shutdown protection feature. Value of the current, which when reached activates the protection mechanism is for the high-side switch dependent on the the junction temperature and drain to source voltage.

Figure 9 shows the situation where the OUT pin is shorted to GND which caused the setting of the internal latch to 1 and led to device switch OFF. In order to switch the device back ON internal latch has to be de-latched and this is described in Chapter **3.6 Inteligent latch strategy (INLAT)**.

Figure 9 OUT pin is connected to GND causing the device switch OFF

3.5 Open load detection

Open load is the situation in which there is no proper connection of the load to the output pin of the device. This can happen in both ON and OFF states. In both cases this situation is reflected on IS pin (if diagnosis is enabled). ***Figure 10*** shows the situation where open load is detected in ON state and marked with red rectangle it the value of the current on IS pin, $I_{IS} = I_{IS(EN)}$.

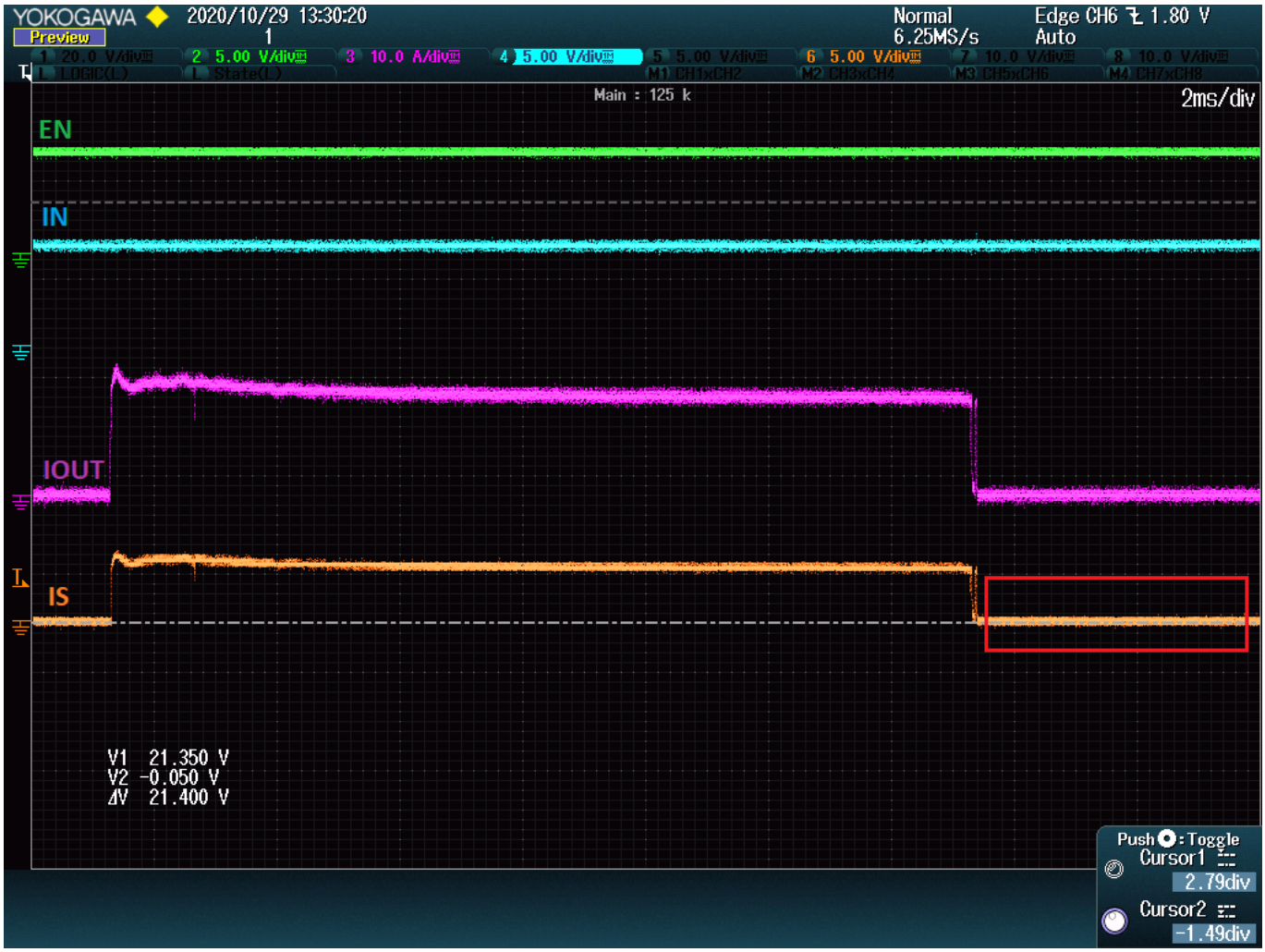

Figure 10 Open load detection in ON state $I_{IS} = I_{IS(EN)}$

Figure 11 shows the situation where open load is detected in OFF state and marked with red rectangle it the value of the current on IS pin, $I_{IS} = I_{IS(OLOFF)}$.

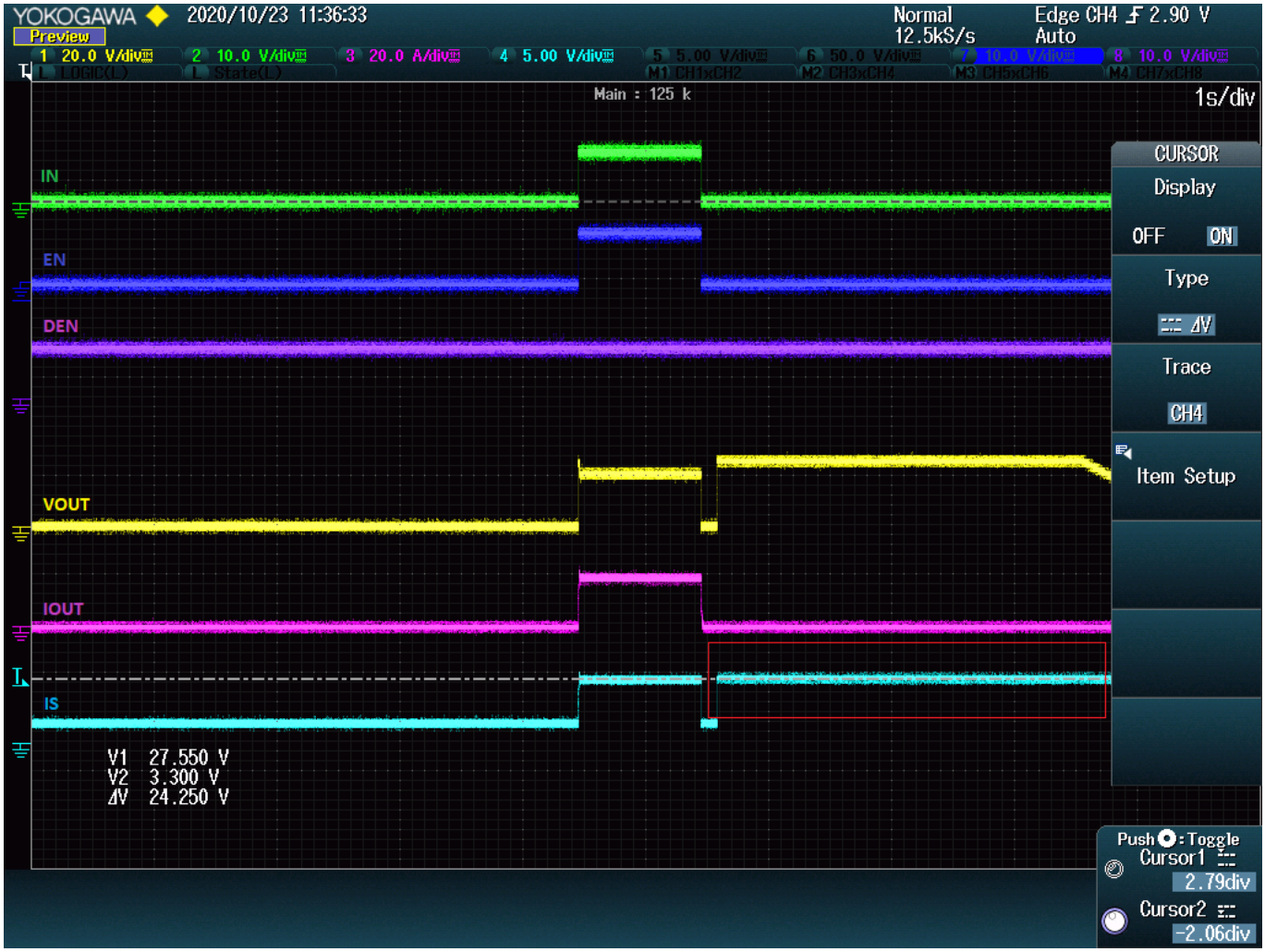

Figure 11 Open Load in OFF state detection $I_{IS} = I_{IS(OLOFF)}$

3.6 Inteligent latch strategy (INLAT)

It is possible to de-latch the internal latch either using EN or DEN pin.

With EN pin:

It is necessary to set the pin to LOW for a time longer than $t_{DELAY(LR)}$ ("latch reset delay" time) to de-latch the channel. This is independent from the state of the IN pin.

During the "latch reset delay" time, if the pin is set to HIGH the channel remains switched OFF and the timer $t_{DELAY(LR)}$) is reset and it is not started as long as the pin remains at HIGH. It restarts as soon as the pin is set to LOW again. This is shown in **Figure 12**.

With DEN pin:

It is possible to "force" a reset of the internal latch without waiting for $t_{DELAY(LR)}$ by applying a pulse (rising edge followed by a falling edge) to the DEN pin while EN pin is LOW. The pulse applied to DEN pin must have a duration longer than $t_{DEN(LR)}$ to ensure a reset of the internal latch. The timing is shown in **Figure 13**.

Figure 12 Intelligent latch timing diagram, with IN = HIGH and load to GND (de-latching with EN)

Figure 13 Intelligent latch timing diagram with forced reset, with IN = HIGH and load to GND (de-latching with DEN)

4 Revision History

Document version	Date of release	Description of changes
1.0	2020-10-29	First release

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