

OptiMOS™ P3 + Optimos™ 2 Small Signal Transistor

Features

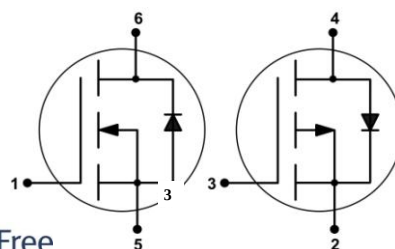
- Complementary P + N channel
- Enhancement mode
- Logic level (4.5V rated)
- Avalanche rated
- Qualified according to AEC Q101
- 100% Lead-free; RoHS compliant
- Halogen free according to IEC61249-2-21

Product Summary

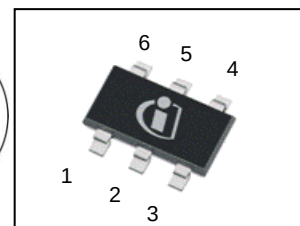
		P	N	
V_{DS}		-30	30	V
$R_{DS(on),max}$	$V_{GS}=\pm 10\text{ V}$	80	57	$m\Omega$
	$V_{GS}=\pm 4.5\text{ V}$	130	93	
I_D		-2.0	2.3	A



Halogen-Free



PG-TSOP-6



Type	Package	Tape and Reel Information	Marking	Lead Free	Packing
BSL308C	PG-TSOP6	H6327: 3000 pcs / reel	sPS	Yes	Non dry

Maximum ratings, at $T_j=25\text{ }^{\circ}\text{C}$, unless otherwise specified ¹⁾

Parameter	Symbol	Conditions	Value		Unit
			P	N	
Continuous drain current	I_D	$T_A=25\text{ }^{\circ}\text{C}$	-2.0	2.3	A
		$T_A=70\text{ }^{\circ}\text{C}$	-1.6	1.8	
Pulsed drain current	$I_{D,pulse}$	$T_A=25\text{ }^{\circ}\text{C}$	-8.0	9	
Avalanche energy, single pulse	E_{AS}	P: $I_D=-2.0\text{ A}$, N: $I_D=2.3\text{ A}$, $R_{GS}=25\text{ }\Omega$	10.7	10.8	mJ
Gate source voltage	V_{GS}		± 20		V
Power dissipation ²⁾	P_{tot}	$T_A=25\text{ }^{\circ}\text{C}$	0.5		W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150		$^{\circ}\text{C}$
ESD class		JESD22-A114-HBM	class 0 (<250V)		
Soldering temperature	T_{solder}		260		$^{\circ}\text{C}$
IEC climatic category; DIN IEC 68-1			55/150/56		

¹⁾ Remark: only one of both transistors active

Parameter		Symbol	Conditions	Values			Unit
				min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - ambient ¹⁾	P	R_{thJA}	minimal footprint ²⁾	-	-	250	K/W
	N						

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	P	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=-250\text{ }\mu\text{A}$	-	-	-30	V
	N		$V_{GS}=0\text{ V}, I_D=250\text{ }\mu\text{A}$	30	-	-	
Gate threshold voltage	P	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-11\text{ }\mu\text{A}$	-2	-1.5	-1	
	N		$V_{DS}=V_{GS}, I_D=11\text{ }\mu\text{A}$	1.2	1.6	2	
Zero gate voltage drain current	P	I_{DSS}	$V_{DS}=-30\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	-	-1	μA
	N		$V_{DS}=30\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	-	1	
	P		$V_{DS}=-30\text{ V}, V_{GS}=0\text{ V}, T_j=150\text{ °C}$	-	-	-100	
	N		$V_{DS}=30\text{ V}, V_{GS}=0\text{ V}, T_j=150\text{ °C}$	-	-	100	
Gate-source leakage current	P	I_{GSS}	$V_{GS}=\pm 20\text{ V}, V_{DS}=0\text{ V}$	-	-	± 100	nA
	N						
Drain-source on-state resistance	P	$R_{DS(on)}$	$V_{GS}=-4.5\text{ V}, I_D=-1.7\text{ A}$	-	88	130	m Ω
	N		$V_{GS}=4.5\text{ V}, I_D=1.85\text{ A}$	-	67	93	
	P		$V_{GS}=-10\text{ V}, I_D=-2.0\text{ A}$	-	62	80	
	N		$V_{GS}=10\text{ V}, I_D=2.3\text{ A}$	-	44	57	
Transconductance	P	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=-1.6\text{ A}$	-	4.6	-	S
	N		$ V_{DS} >2 I_D R_{DS(on)max}, I_D=1.8\text{ A}$	-	5	-	

²⁾ Performed on 40mm² FR4 PCB. The traces are 1mm wide, 70 μm thick and 20mm long; they are present on both sides of the PCB

Parameter		Symbol	Conditions	Values			Unit
				min.	typ.	max.	

Dynamic characteristics

Input capacitance	P	C_{iss}	$V_{GS}=0\text{ V}$, P: $V_{DS}=-15\text{ V}$, N: $V_{DS}=15\text{ V}$, $f=1\text{ MHz}$	-	376	500	pF
	N			-	207	275	
Output capacitance	P	C_{oss}		-	196	261	
	N			-	75	100	
Reverse transfer capacitance	P	C_{rss}		-	12	18	
	N			-	12	17	
Turn-on delay time	P	$t_{d(on)}$	P: $V_{DD}=-15\text{ V}$, $V_{GS}=-10\text{ V}$, $R_G=6\ \Omega$, $I_D=-2\text{ A}$ N: $V_{DD}=15\text{ V}$, $V_{GS}=10\text{ V}$, $R_G=6\ \Omega$, $I_D=2.3\text{ A}$	-	5.6	-	ns
	N			-	4.4	-	
Rise time	P	t_r		-	7.7	-	
	N			-	2.3	-	
Turn-off delay time	P	$t_{d(off)}$		-	15.3	-	
	N			-	8.3	-	
Fall time	P	t_f		-	2.8	-	
	N			-	1.4	-	

Gate Charge Characteristics

Gate to source charge	P	Q_{gs}	$V_{DD}=-15\text{ V}$, $I_D=-2\text{ A}$, $V_{GS}=0\text{ to}$ -10 V	-	-1.2	-	nC
Gate to drain charge		Q_{gd}		-	-0.6	-	
Switching charge		Q_g		-	-5.0	-	
Gate plateau voltage		$V_{plateau}$		-	-3.1	-	
Gate to source charge	N	Q_{gs}	$V_{DD}=15\text{ V}$, $I_D=2.3\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$	-	0.65	-	
Gate to drain charge		Q_{gd}		-	0.45	-	
Switching charge		Q_g			1.5	-	
Gate plateau voltage		$V_{plateau}$			3.1	-	

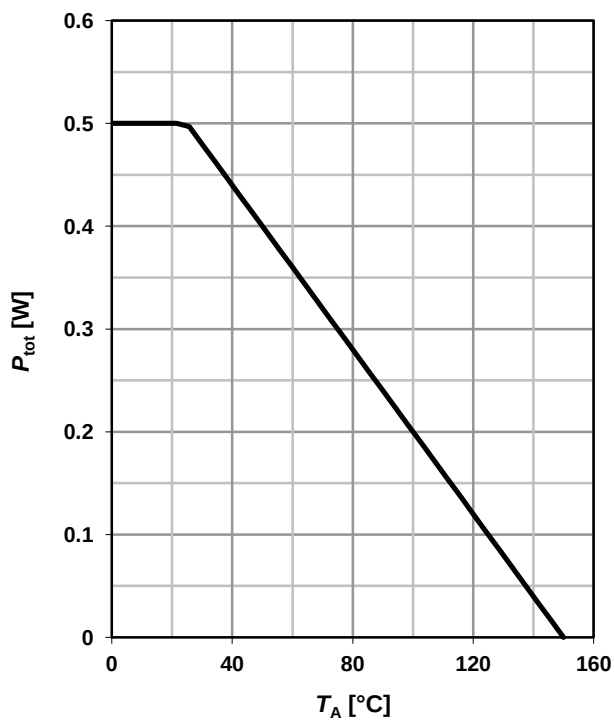
Parameter		Symbol	Conditions	Values			Unit
				min.	typ.	max.	

Reverse Diode

Diode continuous forward current	P	I_S	$T_C=25\text{ }^{\circ}\text{C}$	-	-	-0.4	A
	N			-	-	0.5	
Diode pulse current	P	$I_{S,pulse}$		-	-	-8.4	
	N			-	-	9	
Diode forward voltage	P	V_{SD}	$V_{GS}=0\text{ V}, I_F=-2\text{ A}, T_j=25\text{ }^{\circ}\text{C}$	-	-0.8	-1.1	V
	N		$V_{GS}=0\text{ V}, I_F=2.3\text{ A}, T_j=25\text{ }^{\circ}\text{C}$	-	0.83	1.1	
Reverse recovery time	P	t_{rr}	$V_R=-15\text{ V}, I_F=-2\text{ A}, di_F/dt=-100\text{ A}/\mu\text{s}$	-	14	-	ns
		Q_{rr}		-	-5.9	-	nC
Reverse recovery charge	N	t_{rr}	$V_R=15\text{ V}, I_F=2.3\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$	-	14.4	-	ns
		Q_{rr}		-	2.9	-	nC

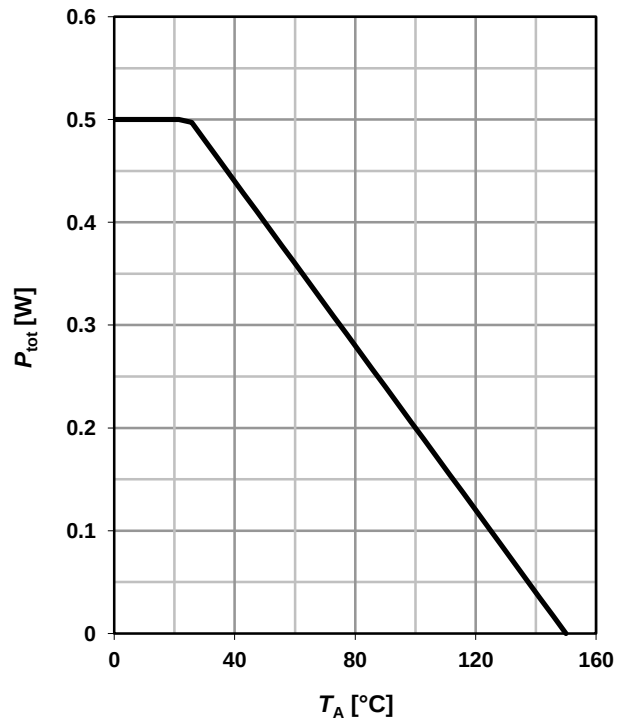
1 Power dissipation (P)

$$P_{\text{tot}} = f(T_A)$$



2 Power dissipation (N)

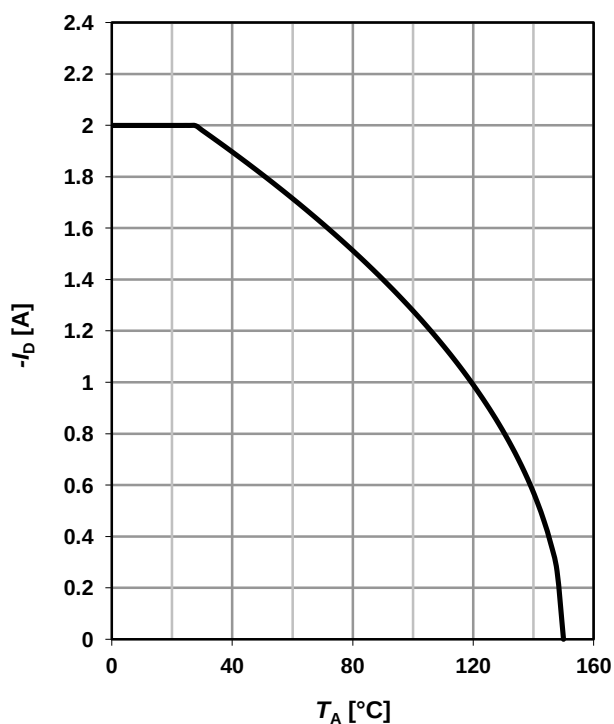
$$P_{\text{tot}} = f(T_A)$$



3 Drain current (P)

$$I_D = f(T_A)$$

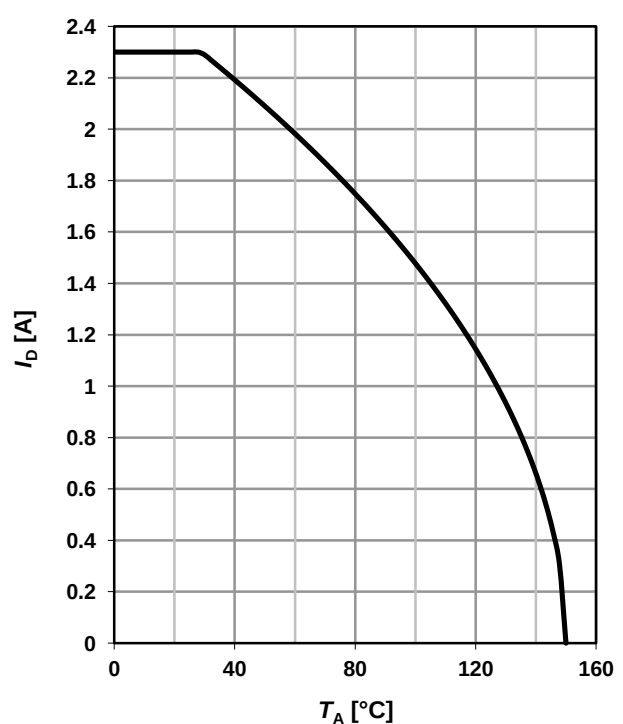
parameter: $V_{GS} \leq -10$ V



4 Drain current (N)

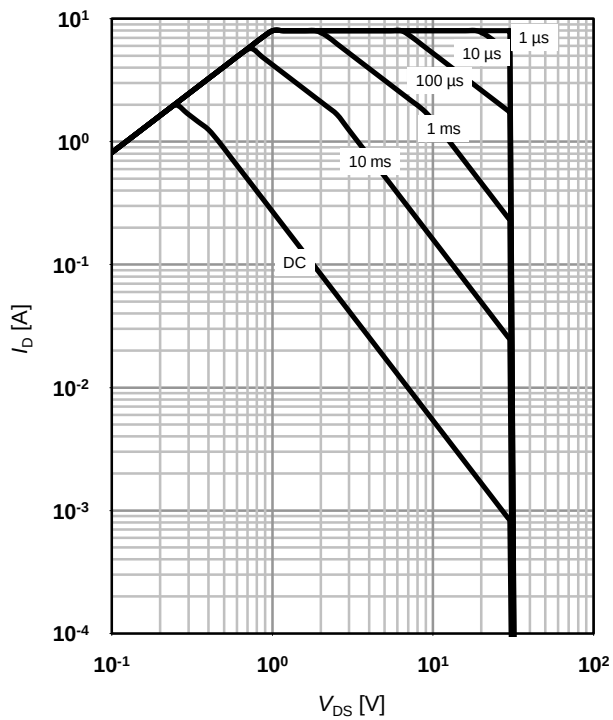
$$I_D = f(T_A)$$

parameter: $V_{GS} \geq 10$ V



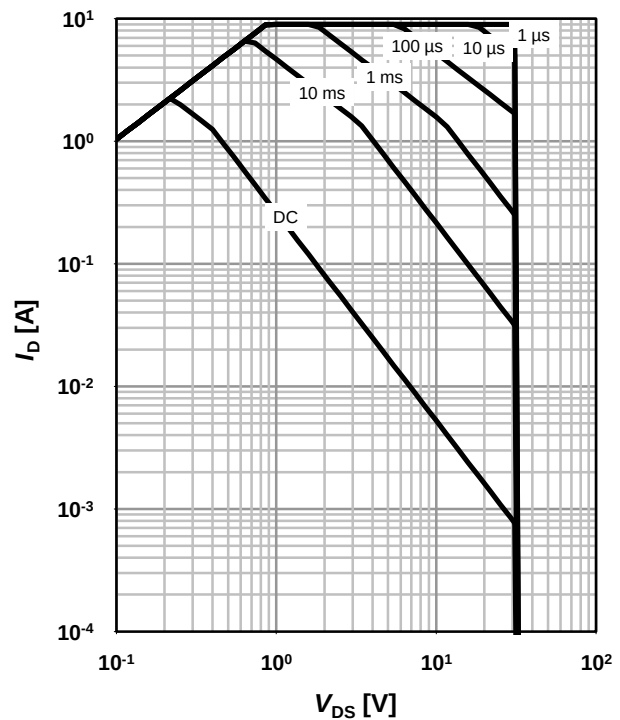
5 Safe operating area (P)

 $I_D = f(V_{DS}); T_A = 25^\circ\text{C}; D = 0$

parameter: t_p


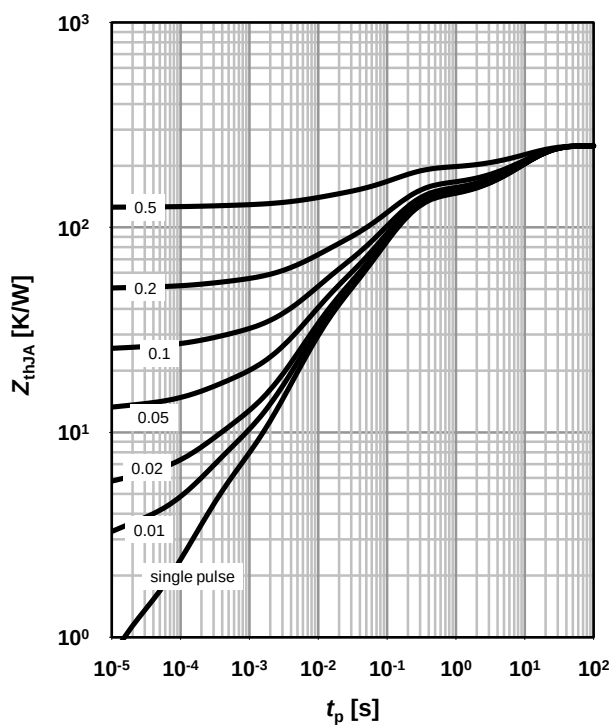
6 Safe operating area (N)

 $I_D = f(V_{DS}); T_A = 25^\circ\text{C}; D = 0$

parameter: t_p


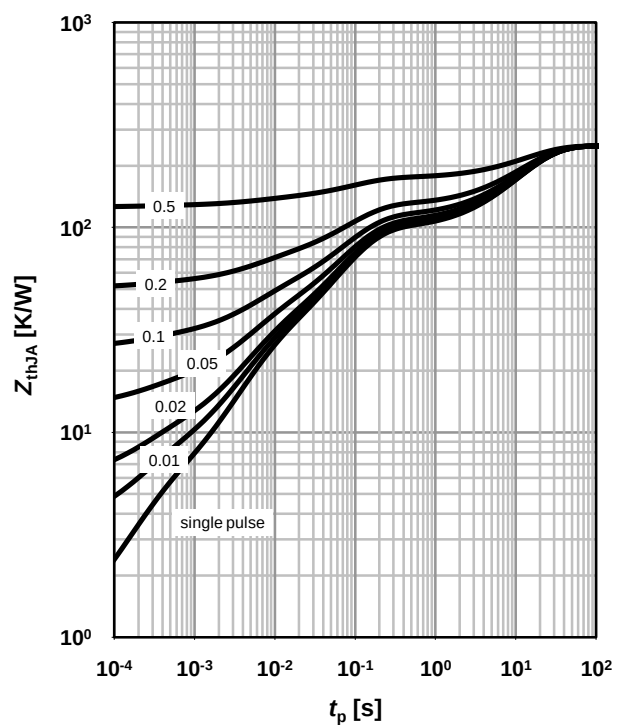
7 Max. transient thermal impedance (P)

 $Z_{thJA} = f(t_p)$

parameter: $D = t_p/T$


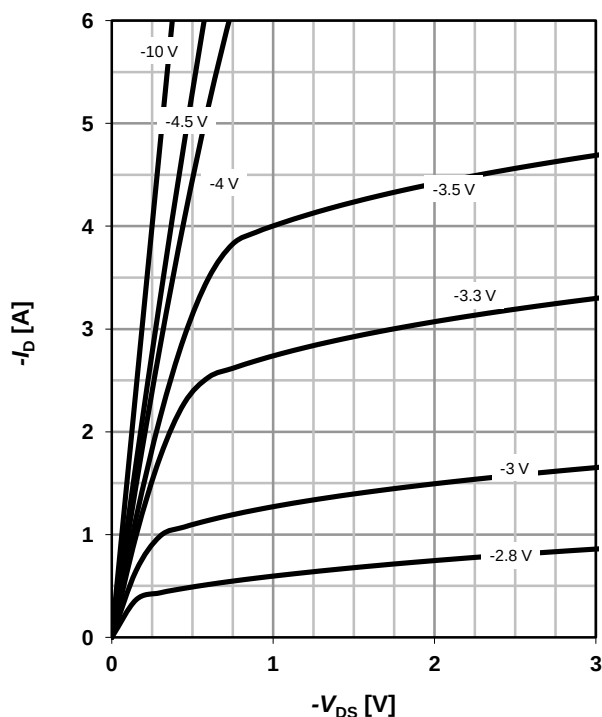
8 Max. transient thermal impedance (N)

 $Z_{thJA} = f(t_p)$

parameter: $D = t_p/T$


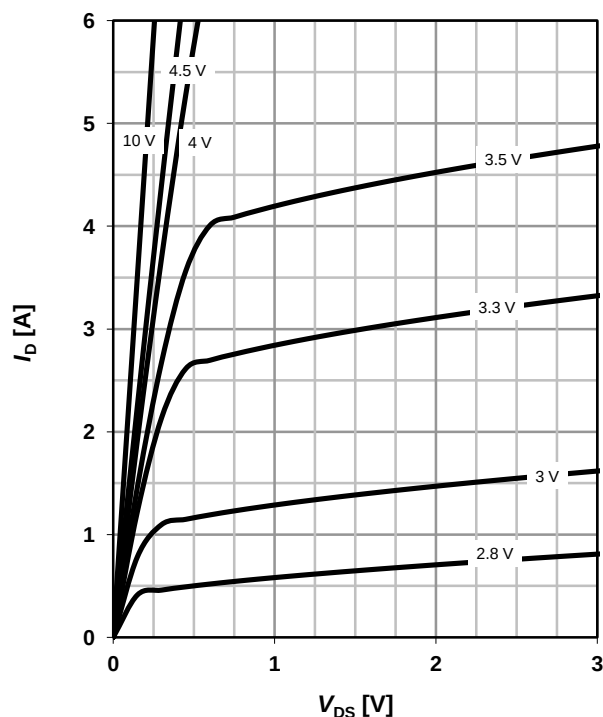
9 Typ. output characteristics (P)

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


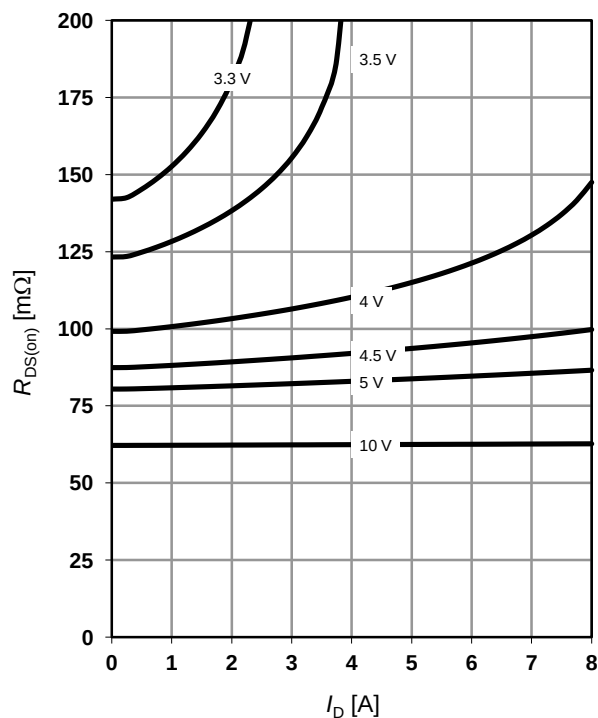
10 Typ. output characteristics (N)

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


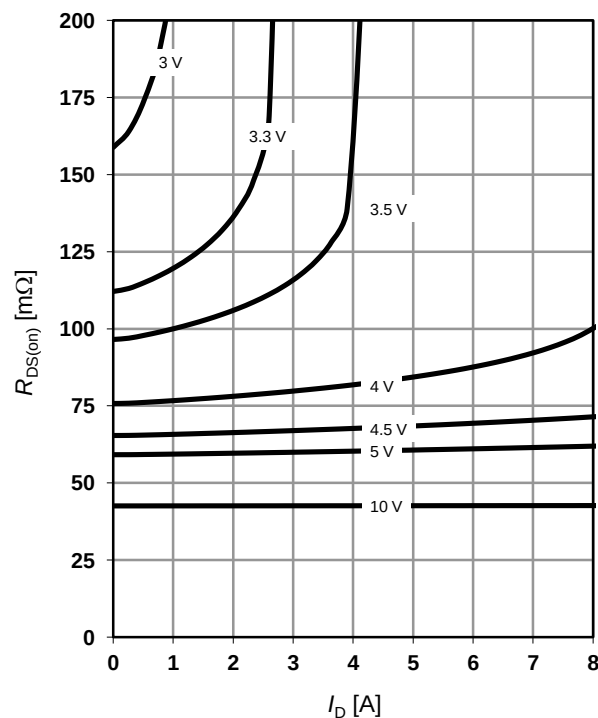
11 Typ. drain-source on resistance (P)

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

parameter: V_{GS}


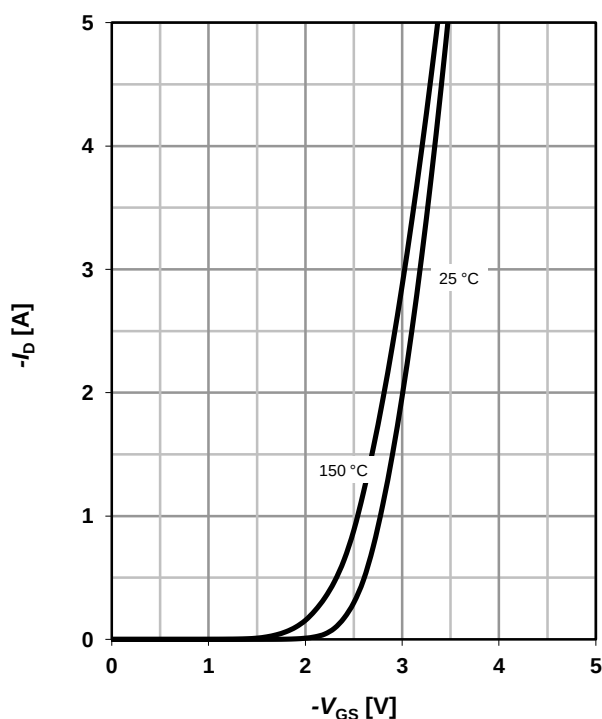
12 Typ. drain-source on resistance (N)

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

parameter: V_{GS}


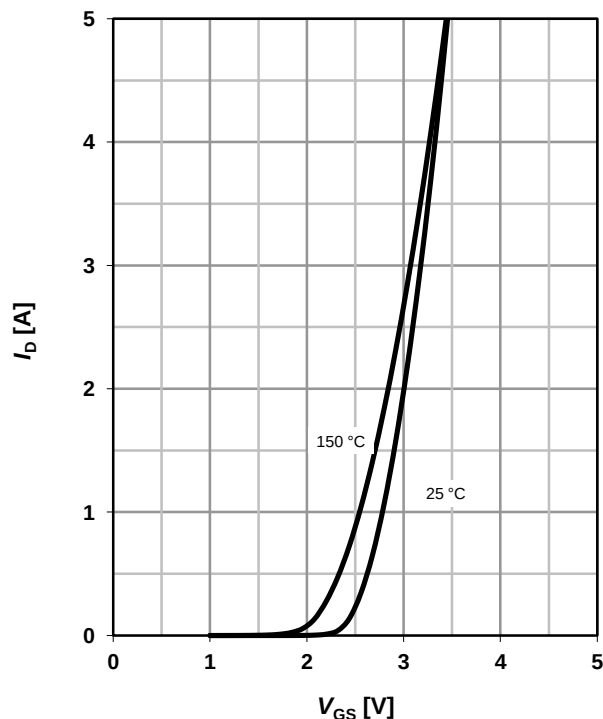
13 Typ. transfer characteristics (P)

 $I_D = f(V_{GS}); |V_{DS}| > 2 |I_D| R_{DS(on)max}$

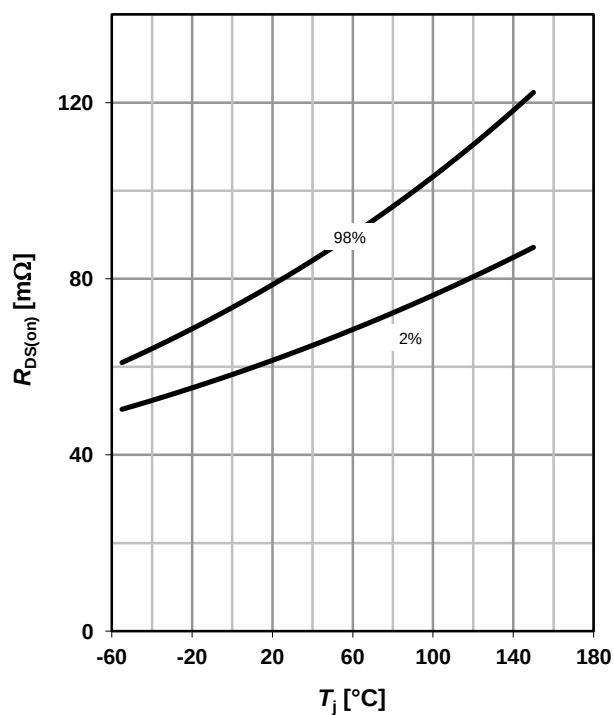
parameter: T_j


14 Typ. transfer characteristics (N)

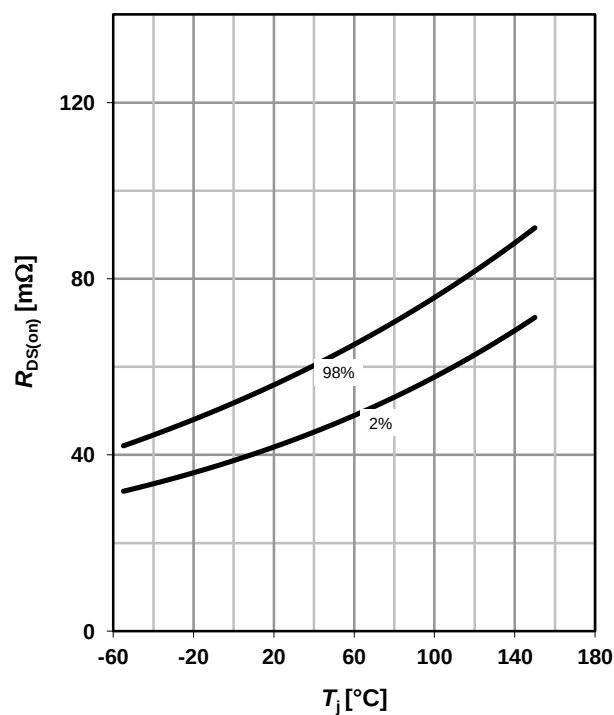
 $I_D = f(V_{GS}); |V_{DS}| > 2 |I_D| R_{DS(on)max}$

parameter: T_j


15 Drain-source on-state resistance (P)

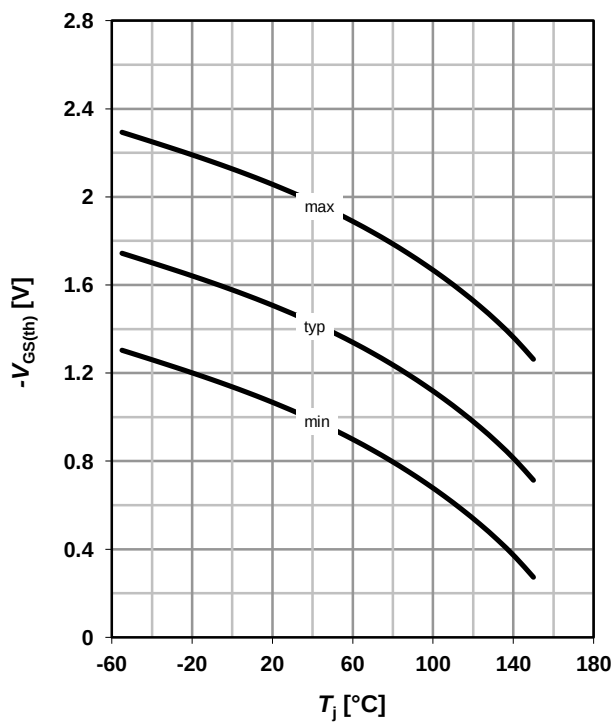
 $R_{DS(on)} = f(T_j); I_D = -2.0 \text{ A}; V_{GS} = -10 \text{ V}$


16 Drain-source on-state resistance (N)

 $R_{DS(on)} = f(T_j); I_D = 2.3 \text{ A}; V_{GS} = 10 \text{ V}$


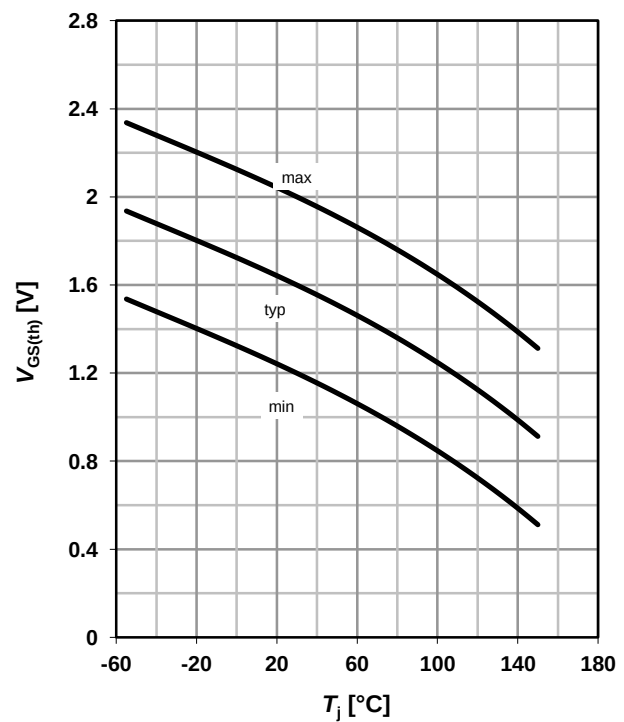
17 Typ. gate threshold voltage (P)

$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = -11 \mu A$$



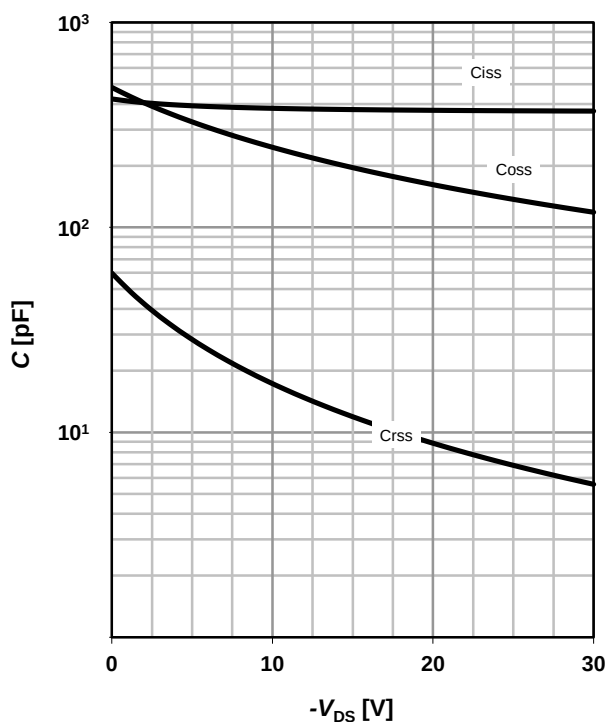
18 Typ. gate threshold voltage (N)

$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = 11 \mu A$$



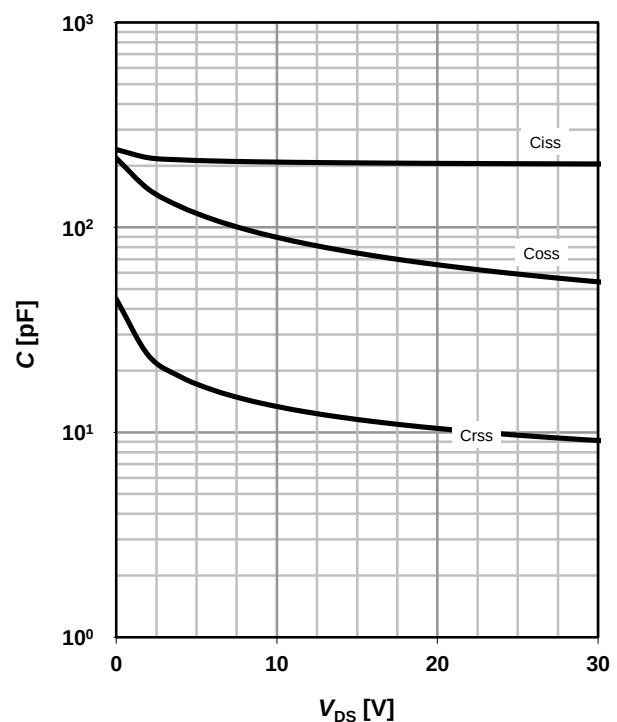
19 Typ. capacitances (P)

$$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$$



20 Typ. capacitances (N)

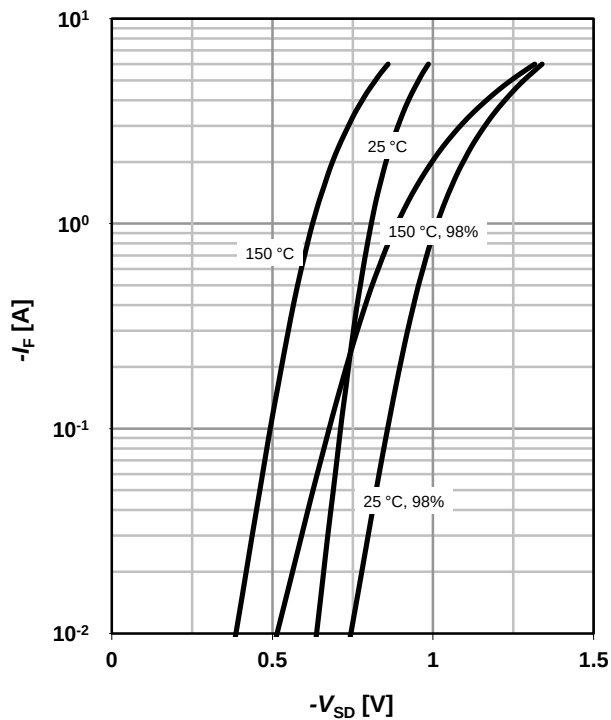
$$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$$



21 Forward characteristics of reverse diode (P)

$$I_F = f(V_{SD})$$

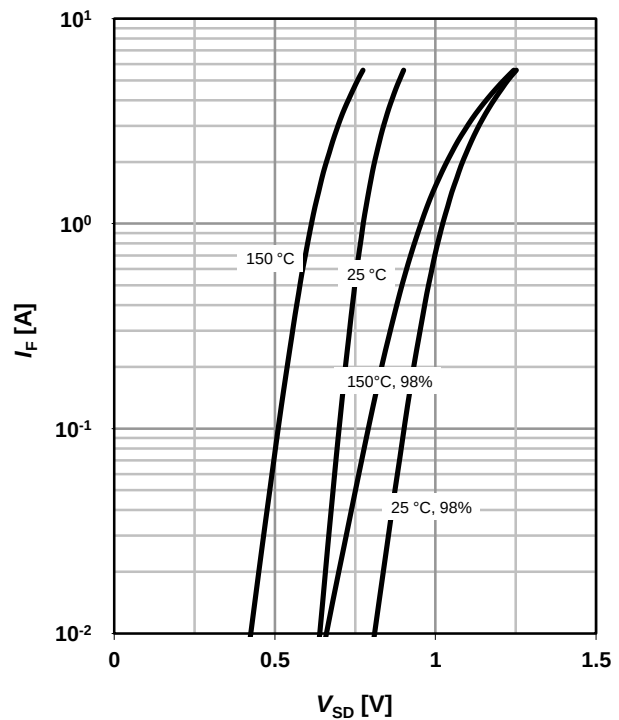
parameter: T_j



22 Forward characteristics of reverse diode (N)

$$I_F = f(V_{SD})$$

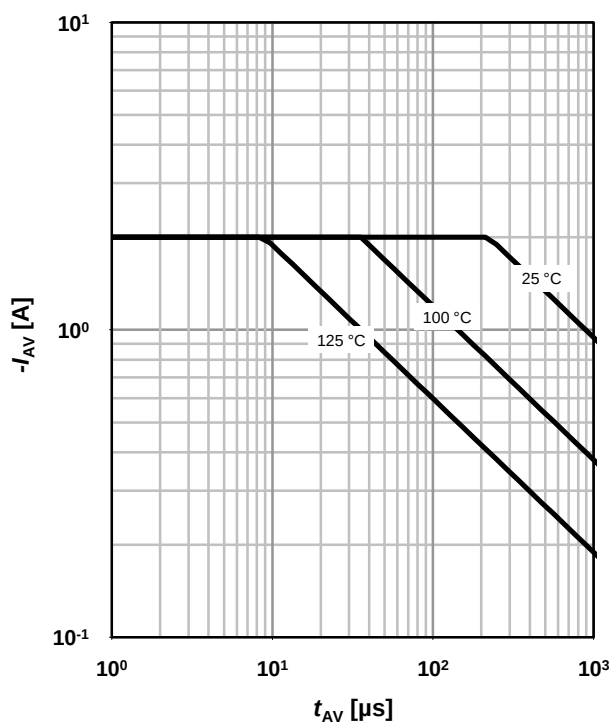
parameter: T_j



23 Avalanche characteristics (P)

$$I_{AS} = f(t_{AV}); R_{GS} = 25 \Omega$$

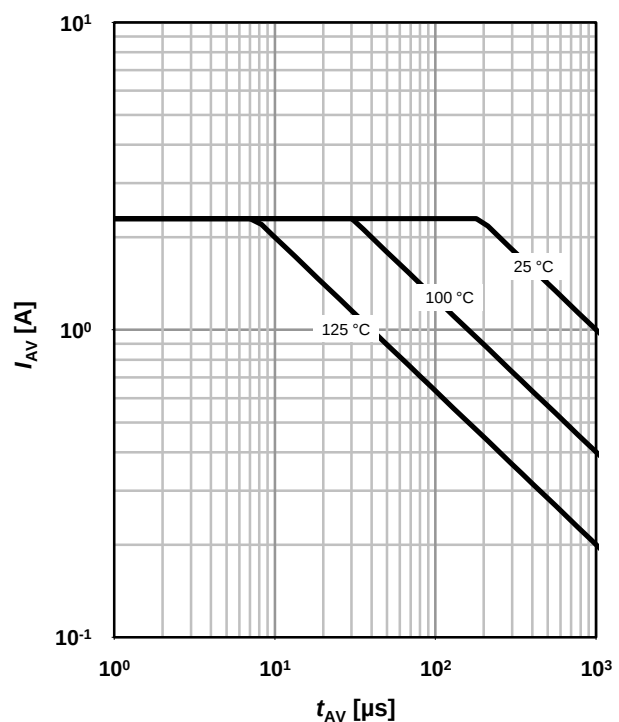
parameter: $T_{j(start)}$



24 Avalanche characteristics (N)

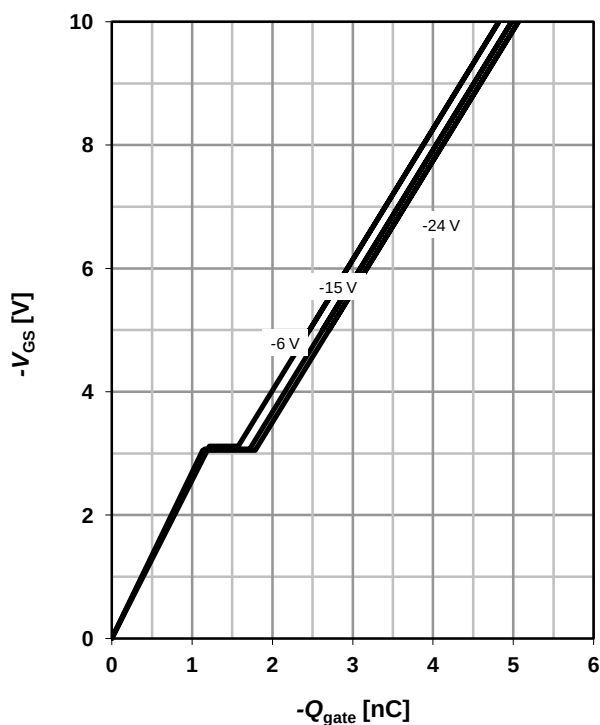
$$I_{AS} = f(t_{AV}); R_{GS} = 25 \Omega$$

parameter: $T_{j(start)}$



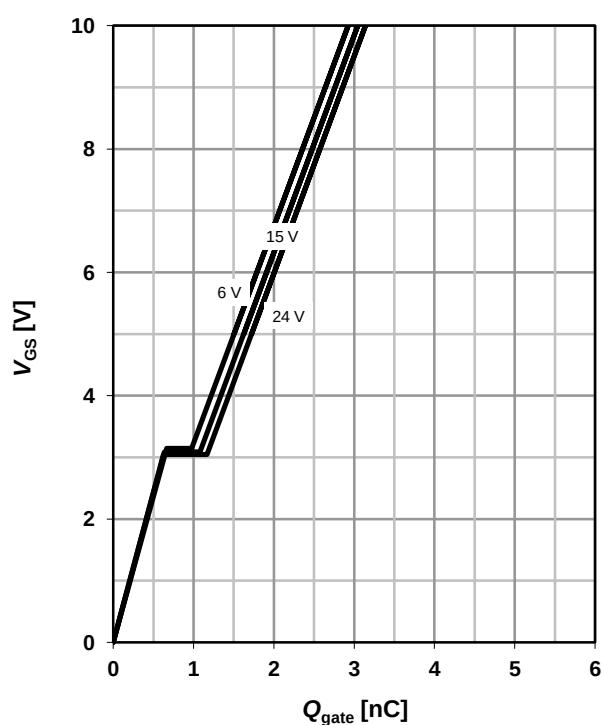
25 Typ. gate charge (P)

 $V_{GS}=f(Q_{gate}); I_D=-2.0\text{ A pulsed}$

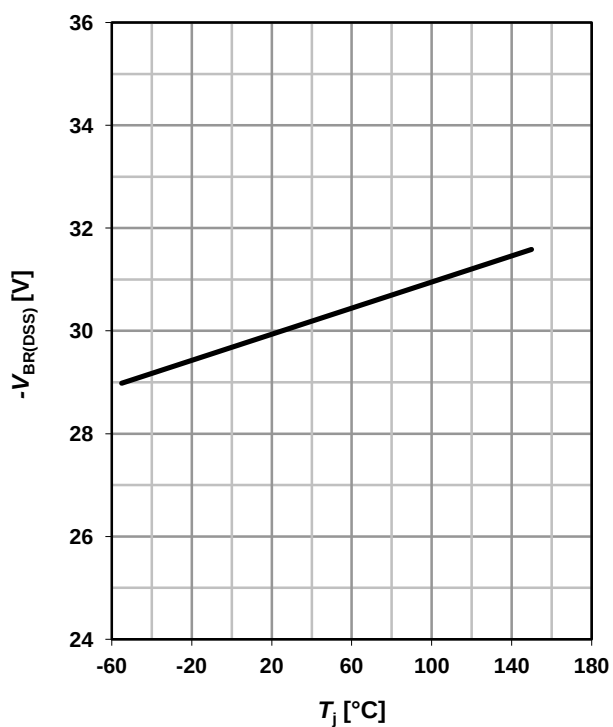
parameter: V_{DD}


26 Typ. gate charge (N)

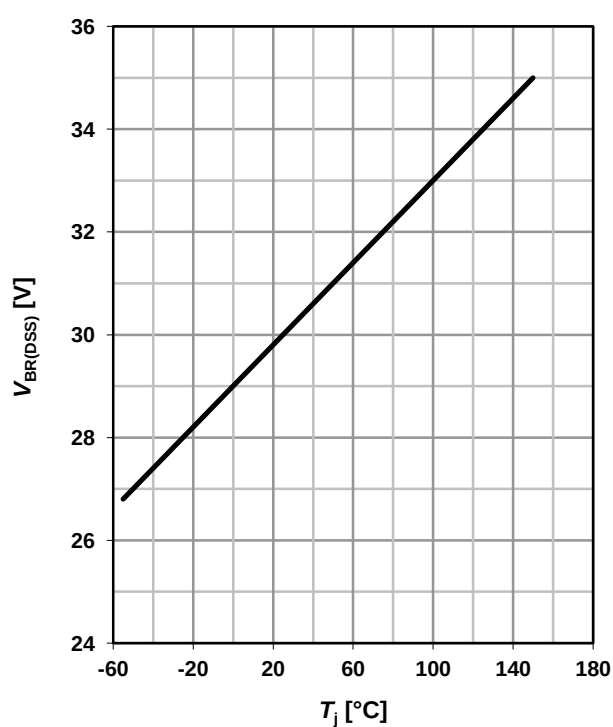
 $V_{GS}=f(Q_{gate}); I_D=2.3\text{ A pulsed}$

parameter: V_{DD}


27 Drain-source breakdown voltage (P)

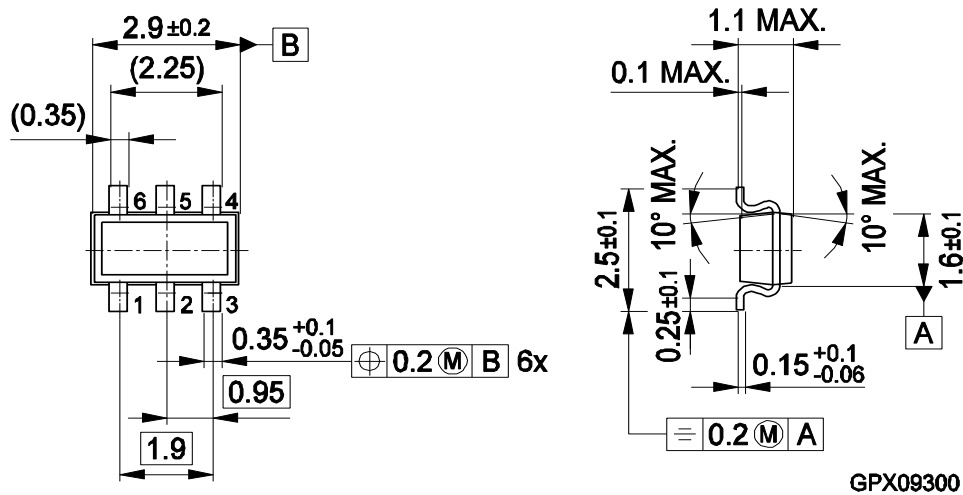
 $V_{BR(DSS)}=f(T_j); I_D=-250\text{ }\mu\text{A}$


28 Drain-source breakdown voltage (N)

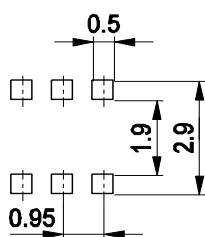
 $V_{BR(DSS)}=f(T_j); I_D=250\text{ }\mu\text{A}$


TSOP-6

Package Outline:



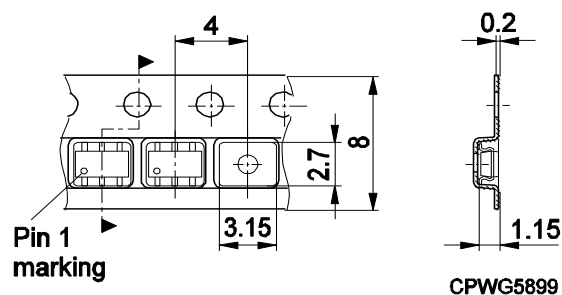
Footprint:



Remark: Wave soldering possible dep.
on customers process conditions

HLG09283

Packaging:



Dimensions in mm

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