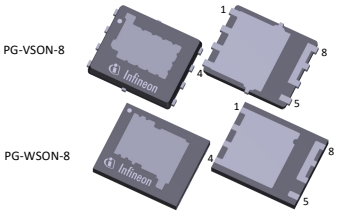
MOSFET

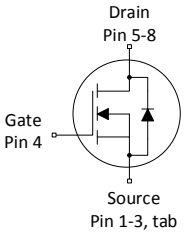
PG-VSON-8 / PG-WSON-8

OptiMOS™ 5 Power-Transistor, 100 V



Features

- Dual-side cooled package with lowest Junction-top thermal resistance
- 175°C rated
- Optimized for high performance SMPS, e.g. sync. rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	4.0	mΩ
I_D	140	A
Q_{oss}	75	nC
Q_G(0V..10V)	58	nC

Hal Pb RoHS

Part number	Package	Marking	Related links
BSC040N10NS5SC	PG-VSON-8 / PG-WSON-8	040N10SC	-

Table of contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	140	A	V_{GS}=10 V, T_C=25 °C
				99		V_{GS}=10 V, T_C=100 °C
				18		V_{GS}=10 V, T_C=25 °C, R_{thJA}=50K/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	560	A	T_C=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	268	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	167	W	T_C=25 °C
				3.0		T_A=25 °C, R_{thJA}=50 K/W [3]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.5	0.9	K/W	-
Thermal resistance, junction - case, top	R_{thJC}		0.4	0.86		
Device on PCB, 6 cm^2 cooling area [5]	R_{thJA}		-	50		

[5] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	V_{DS}=V_{GS}, I_D=95 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	1	µA	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C
			10	100		V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	3.4	4.0	mΩ	V_{GS}=10 V, I_D=50 A
			4.0	5.6		V_{GS}=6 V, I_D=25 A
Gate resistance	R_G	-	1.3	2.0	Ω	-
Transconductance	g_{fs}	60	120	-	S	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=50 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [6]	C_{iss}	-	4100	5300	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Output capacitance [6]	C_{oss}		630	820		
Reverse transfer capacitance [6]	C_{rss}		28	49		
Turn-on delay time	$t_{d(on)}$	-	13	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=3 Ω
Rise time	t_r		9			
Turn-off delay time	$t_{d(off)}$		32			
Fall time	t_f		10			

[6] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [7)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	19	-	nC	V_{DD}=50 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$		12	-	nC	
Gate to drain charge [8)]	Q_{gd}		12	18	nC	
Switching charge	Q_{sw}		18	-	nC	
Gate charge total [8)]	Q_g		58	72	nC	
Gate plateau voltage	$V_{plateau}$		4.6	-	V	
Gate charge total, sync. FET	$Q_{g(sync)}$	-	50	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge [8)]	Q_{oss}	-	75	100	nC	V_{DD}=50 V, V_{GS}=0 V

[7)] See "Gate charge waveforms" for parameter definition

[8)] Defined by design. Not subject to production test.

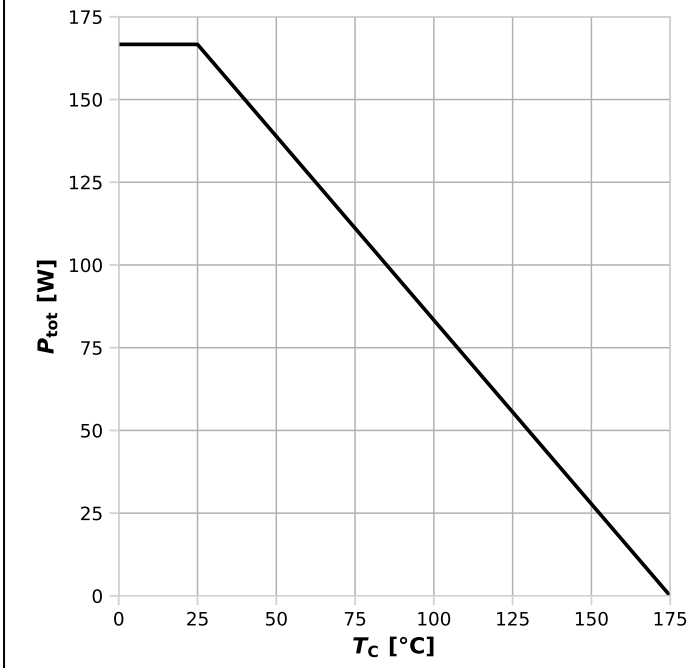
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	152	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$			560		
Diode forward voltage	V_{SD}	-	0.9	1.1	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery time [9)]	t_{rr}	-	54	108	ns	V_R=50 V, I_F=I_S, di_F/dt=100 A/µs
Reverse recovery charge [9)]	Q_{rr}		90	180	nC	

[9)] Defined by design. Not subject to production test.

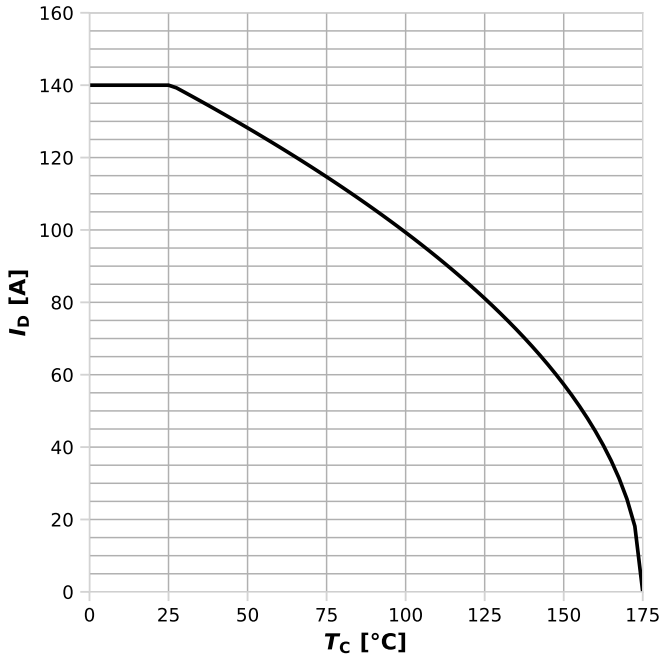
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



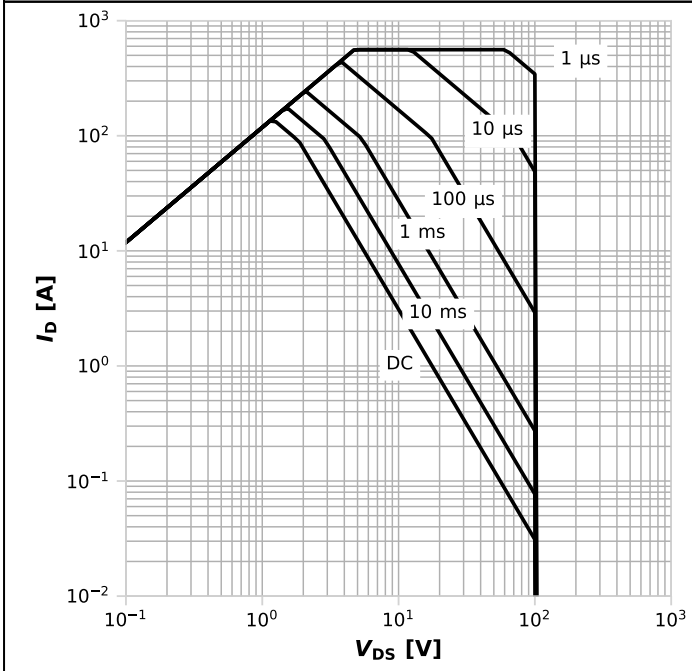
P_{tot}=f(T_C)

Diagram 2: Drain current



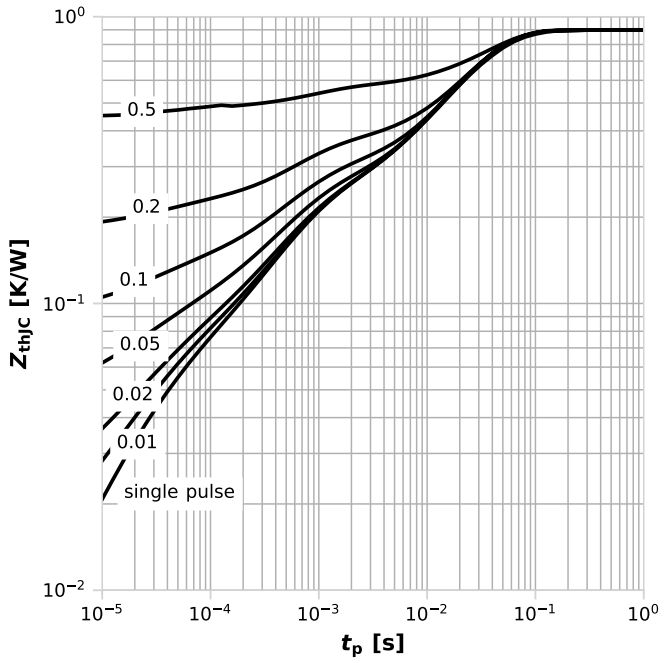
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



Z_{thJC}=f(t_p); parameter: D=t_p/T

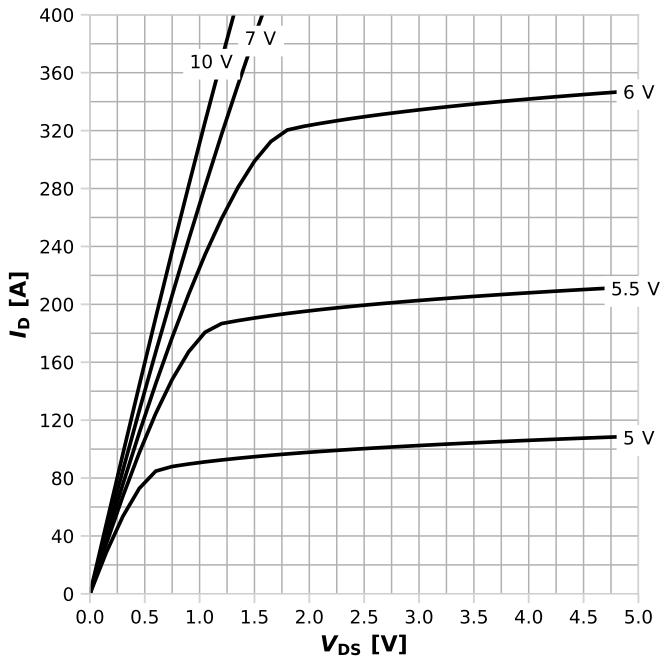
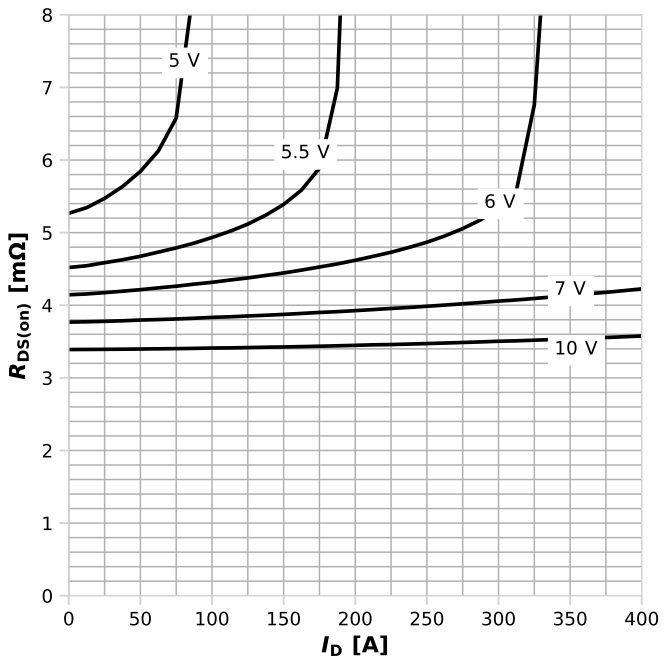
Diagram 5: Typ. output characteristics	Diagram 6: Typ. drain-source on resistance
	
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

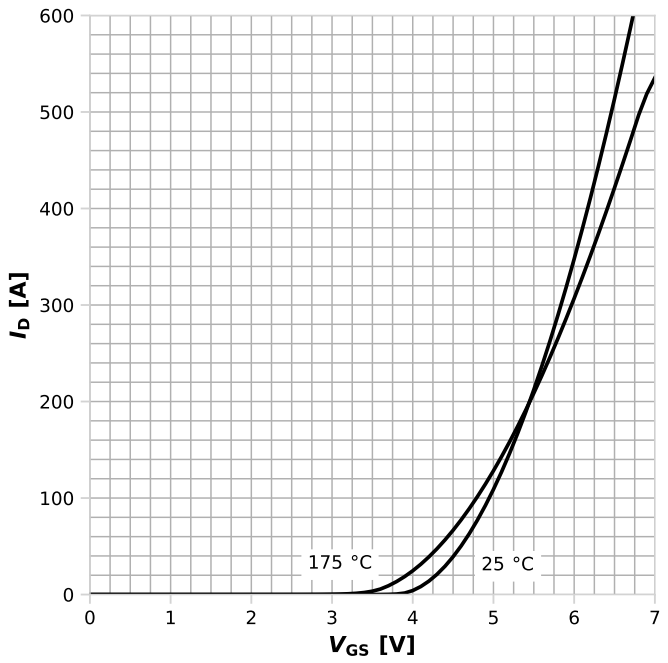
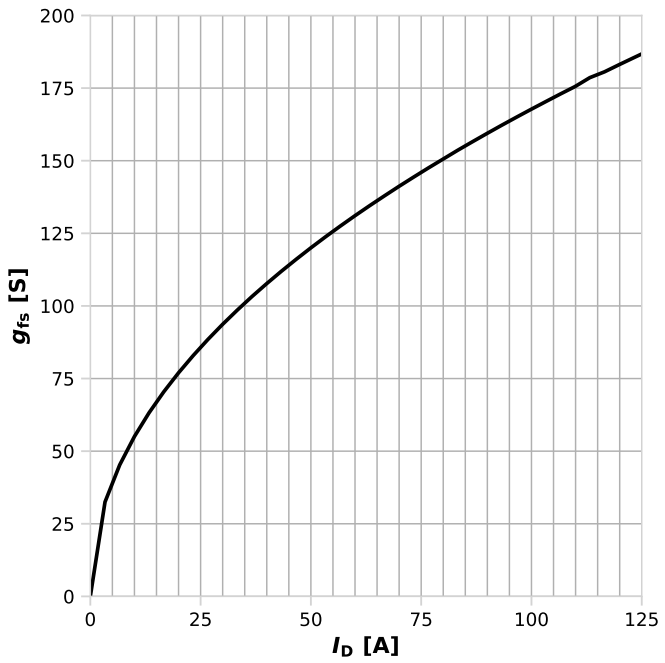
Diagram 7: Typ. transfer characteristics	Diagram 8: Typ. forward transconductance
	
I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j	g_{fs}=f(I_D), V_{DS}=5 V, T_j=25 °C

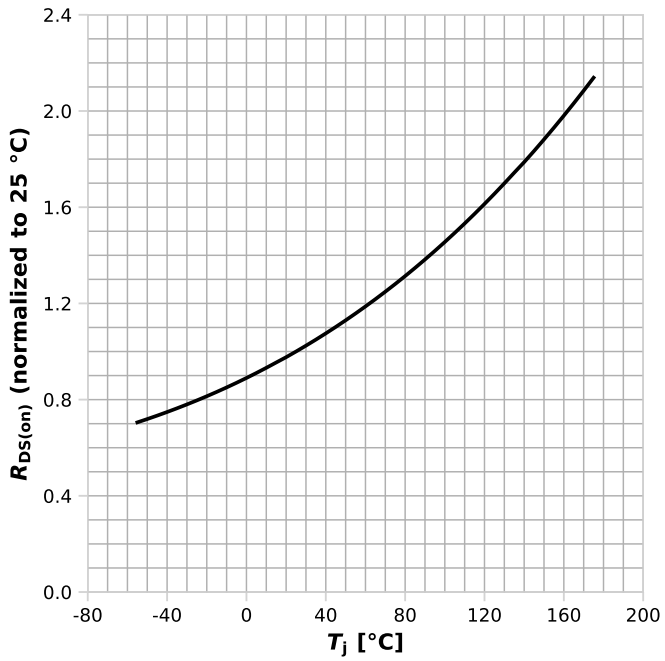
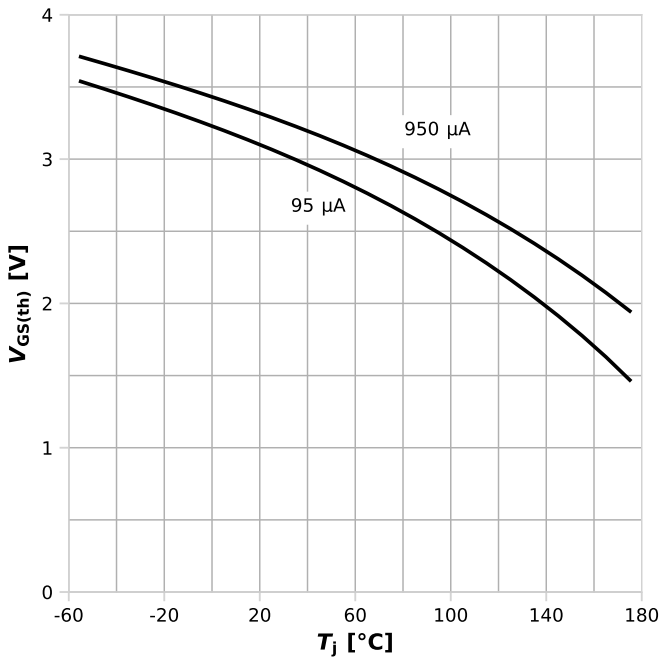
Diagram 9: Drain-source on-state resistance	Diagram 10: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j), I_D=50 A, V_{GS}=10 V	$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}

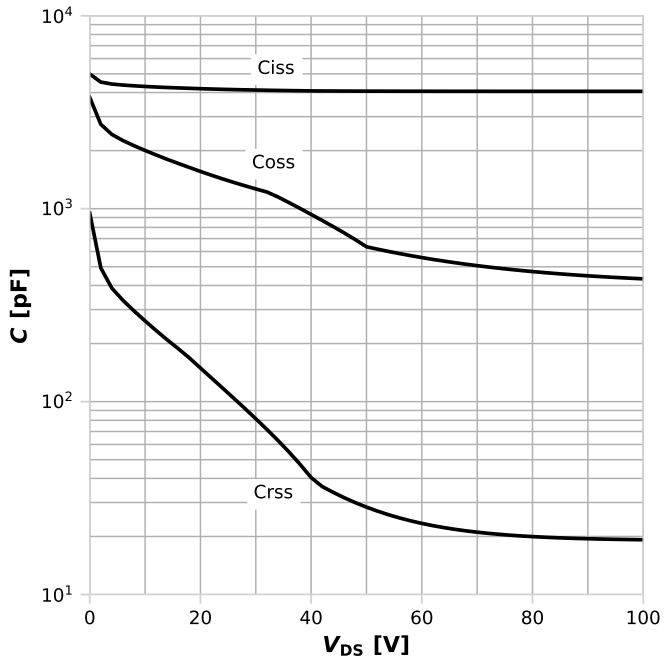
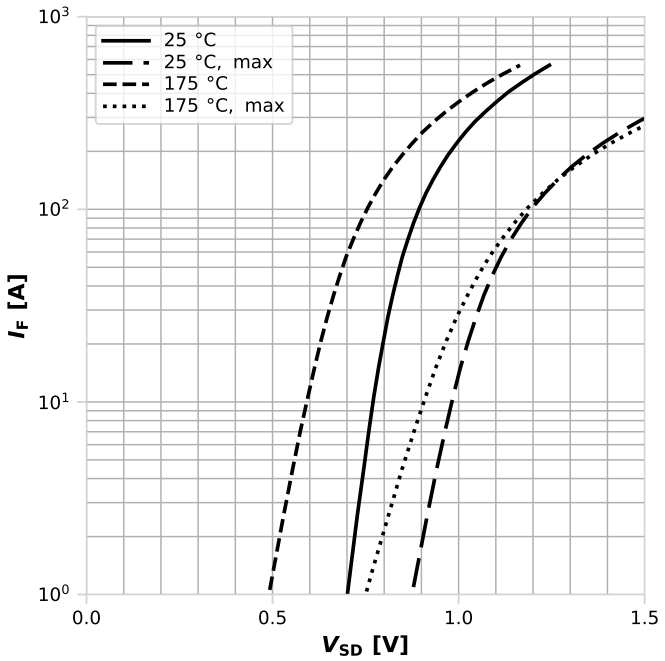
Diagram 11: Typ. capacitances	Diagram 12: Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	I_F=f(V_{SD}); parameter: T_j

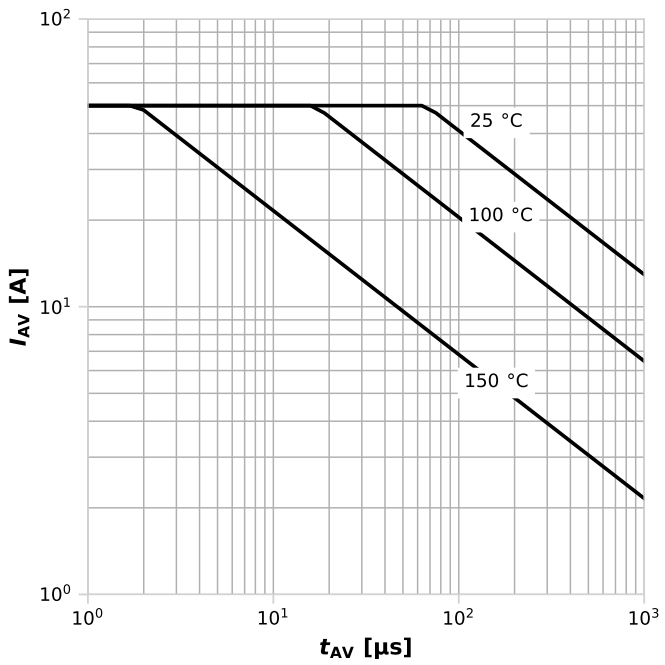
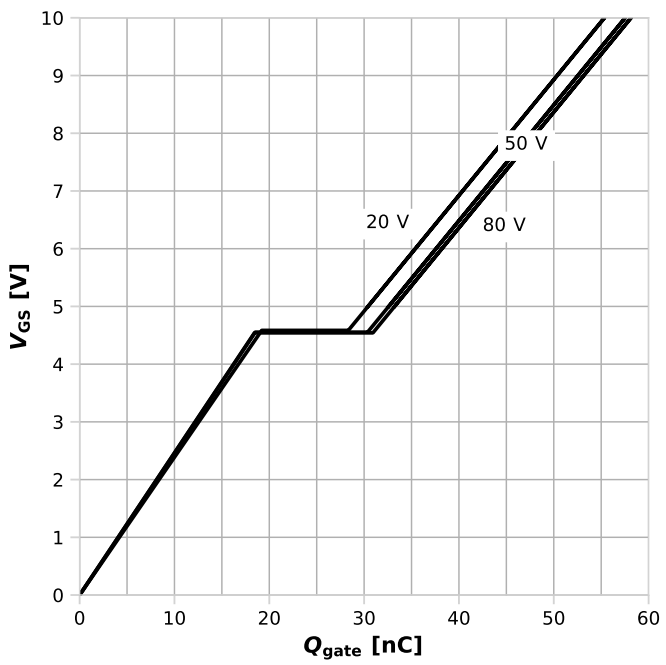
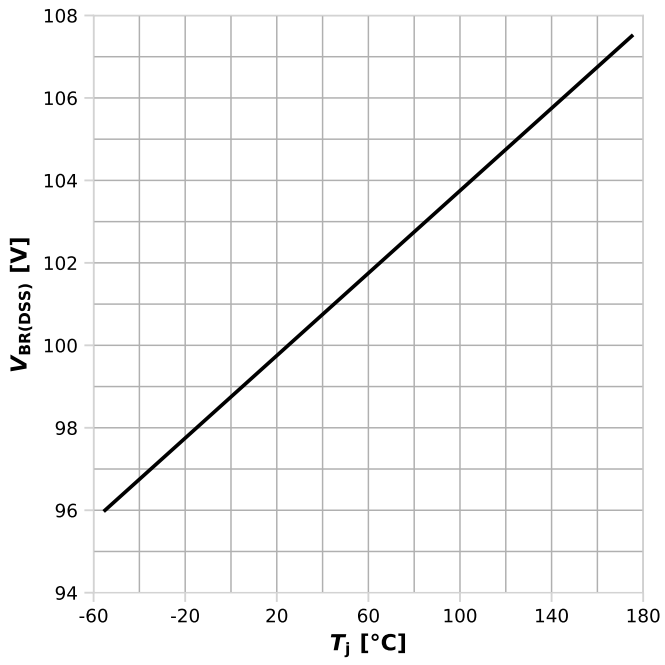
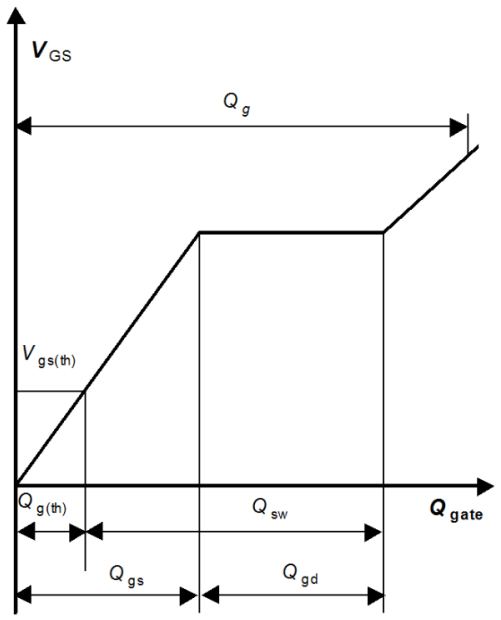
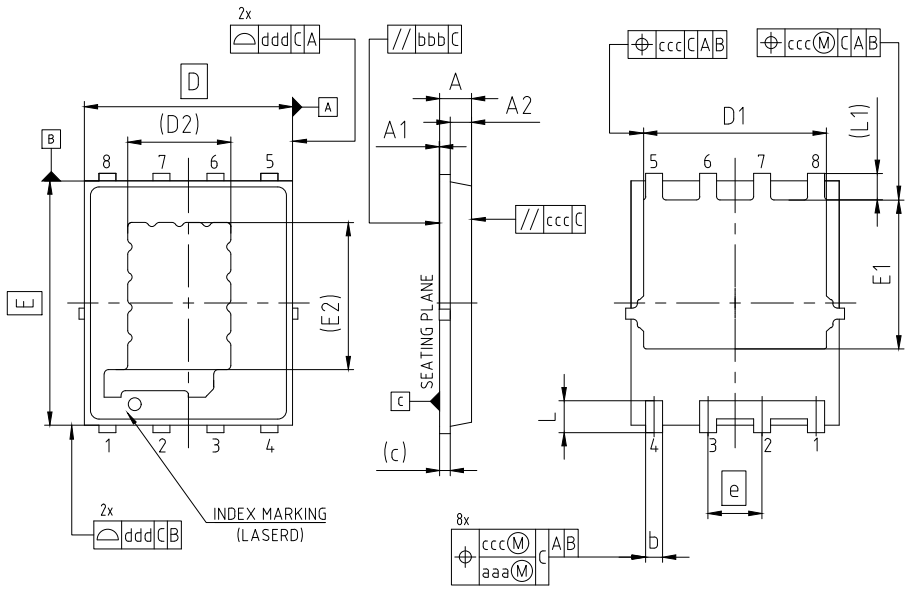
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$	V_{GS}=f(Q_{gate}); I_D=50 A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	-

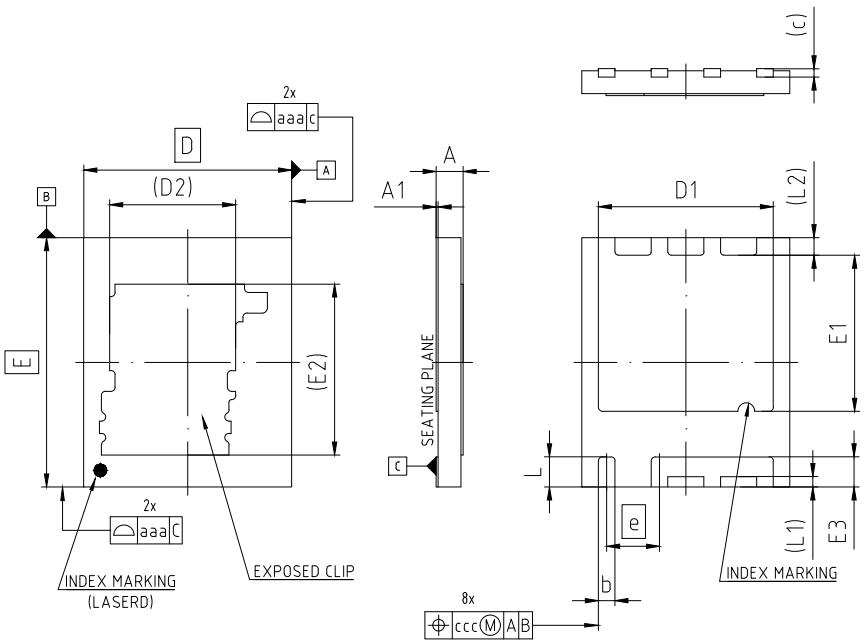
5 Package outlines



PACKAGE - GROUP NUMBER:	PG-VSON-8-U01				
DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.65	0.85	e	1.27	
A1	0.00	0.05	L	0.70	0.90
A2	0.45	0.55	L1	0.52	0.72
b	0.35	0.55	aaa	0.05	
c	0.25		bbb	0.08	
D	4.90		ccc	0.10	
D1	4.20	4.40	ddd	0.15	
D2	2.43				
E	5.75				
E1	3.40	3.60			
E2	3.46				

NOTE: DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-VSON-8 / PG-WSON-8, dimensions in mm



PACKAGE - GROUP NUMBER:	PG-WSON-8-U01					
DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS		
	MIN.	MAX.		MIN.	MAX.	
A	0.55	0.75	e	1.27		
A1	0.00	0.05	L	0.68	0.78	
b	0.35	0.45	L1	0.25		
c	0.20		L2	0.42		
D	5.00		aaa	0.05		
D1	4.11	4.31	ccc	0.10		
D2	3.03					
E	6.00					
E1	3.66	3.86				
E2	4.11					
E3	0.63	0.83				

NOTE: DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 2 PG-VSON-8 / PG-WSON-8, dimensions in mm

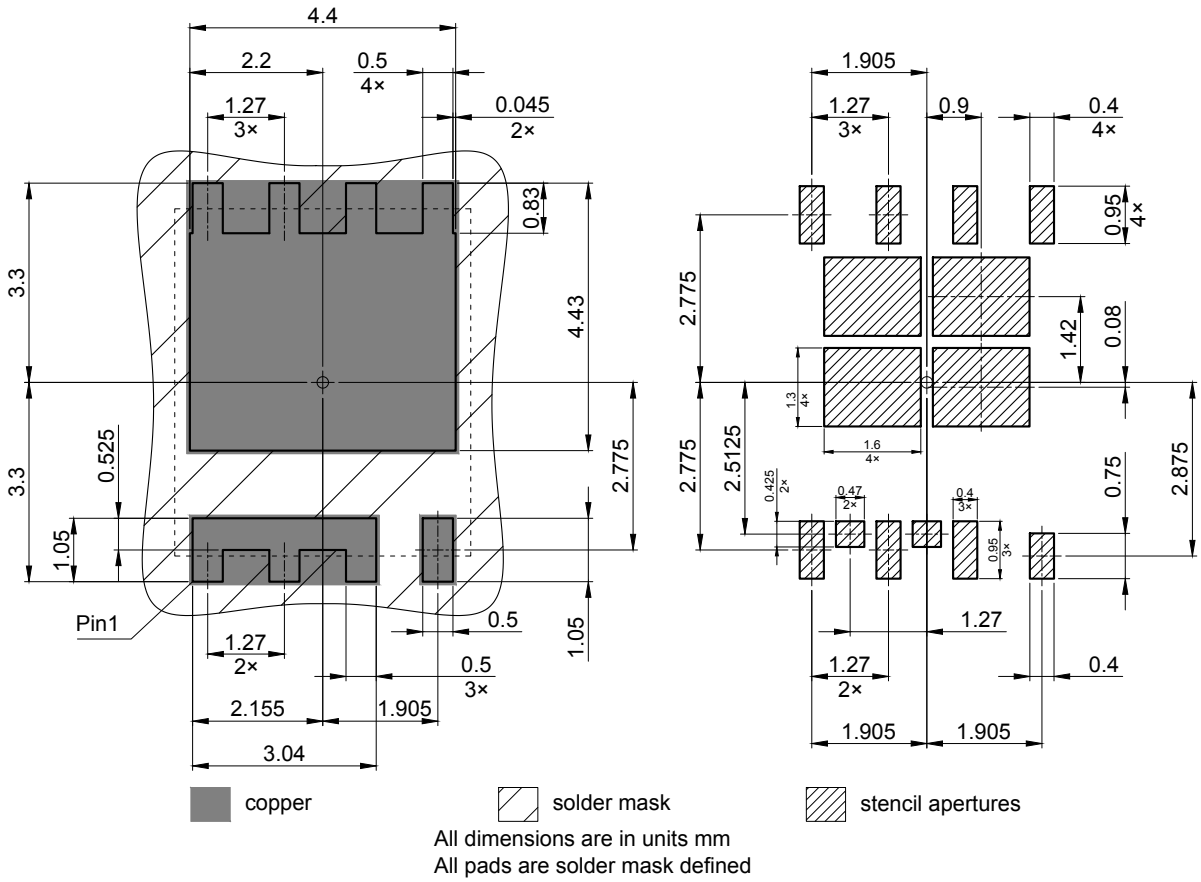


Figure 3 Bonding diagram PG-VSON-8 / PG-WSON-8, dimensions in mm

Revision history

BSC040N10NS5SC

Revision 2025-05-23, Rev. 2.2

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2019-11-19	Release of final version
2.1	2022-10-13	Update "Features
2.2	2025-05-23	Update package drawings

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