

PG-TDSON-8

MOSFET

OptiMOS™ Power-MOSFET, 40 V

Features

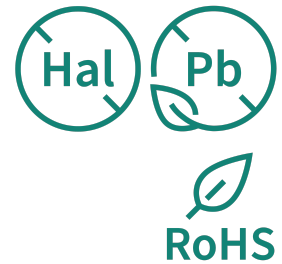
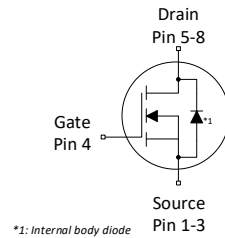
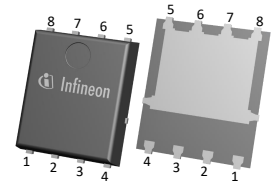
- Optimized for high performance SMPS, e.g. sync. rec.
- 175°C rated
- Very low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5\text{ V}$
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	40	V
$R_{DS(on),max}$	1.9	mΩ
I_D	161	A
Q_{OSS}	37	nC
$Q_G(0V..10V)$	41	nC



Type/Ordering Code	Package	Marking	Related Links
BSC019N04LS	PG-TDSON-8	019N04LS	-



Table of Contents

Description	1
Maximum ratings	3
Thermal characteristics	4
Electrical characteristics	5
Electrical characteristics diagrams	7
Package Outlines	11
Revision History	14
Trademarks	14
Disclaimer	14

1 Maximum ratings

unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	161	A	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$ $V_{GS}=10\text{ V}, T_C=100\text{ °C}$ $V_{GS}=4.5\text{ V}, T_C=25\text{ °C}$ $V_{GS}=4.5\text{ V}, T_C=100\text{ °C}$ $V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=50\text{ K/W}^2)$
				114		
				135		
				96		
				28		
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	644	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	90	mJ	$I_D=50\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage ⁵⁾	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	94	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}, R_{thJA}=50\text{ K/W}^2)$
				3.0		
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

⁵⁾ The negative rating is for low duty cycle pulse occurrence. No continuous rating is implied

2 Thermal characteristics

at $T_f=25\text{ °C}$, unless otherwise specified

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	1.0	1.6	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	K/W	-
Device on PCB, 6 cm ² cooling area ⁶⁾	R_{thJA}	-	-	50	K/W	-

⁶⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2	V	$V_{DS}=V_{GS}, I_D=250\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=40\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$ $V_{DS}=40\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.5 1.9	1.9 2.7	m Ω	$V_{GS}=10\text{ V}, I_D=50\text{ A}$ $V_{GS}=4.5\text{ V}, I_D=50\text{ A}$
Gate resistance	R_G	-	0.8	1.6	Ω	-
Transconductance	g_{fs}	95	190	-	S	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=50\text{ A}$

Table 5 Dynamic characteristics ⁷⁾

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2900	4060	pF	$V_{GS}=0\text{ V}, V_{DS}=20\text{ V}, f=1\text{ MHz}$
Output capacitance	C_{oss}	-	840	1180	pF	$V_{GS}=0\text{ V}, V_{DS}=20\text{ V}, f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	68	136	pF	$V_{GS}=0\text{ V}, V_{DS}=20\text{ V}, f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	6	-	ns	$V_{DD}=20\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A}, R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	4	-	ns	$V_{DD}=20\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A}, R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	26	-	ns	$V_{DD}=20\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A}, R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	4	-	ns	$V_{DD}=20\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A}, R_{G,ext}=1.6\text{ }\Omega$

⁷⁾ Defined by design. Not subject to production test

Table 6 Gate charge characteristics ⁸⁾

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	7.6	-	nC	$V_{DD}=20\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	6.2	-	nC	$V_{DD}=20\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	6.7	9.4	nC	$V_{DD}=20\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	8.1	-	nC	$V_{DD}=20\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	Q_g	-	41	57	nC	$V_{DD}=20\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$

Table 6 Gate charge characteristics ⁸⁾

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate plateau voltage	V_{plateau}	-	2.6	-	V	$V_{\text{DD}}=20\text{ V}$, $I_{\text{D}}=50\text{ A}$, $V_{\text{GS}}=0\text{ to }10\text{ V}$
Gate charge total	Q_{g}	-	21	29	nC	$V_{\text{DD}}=20\text{ V}$, $I_{\text{D}}=50\text{ A}$, $V_{\text{GS}}=0\text{ to }4.5\text{ V}$
Gate charge total, sync. FET	$Q_{\text{g(sync)}}$	-	16	-	nC	$V_{\text{DS}}=0.1\text{ V}$, $V_{\text{GS}}=0\text{ to }4.5\text{ V}$
Output charge	Q_{oss}	-	37	52	nC	$V_{\text{DD}}=20\text{ V}$, $V_{\text{GS}}=0\text{ V}$

⁸⁾ See "gate charge waveforms" for parameter definition. Defined by design. Not subject to production test

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_{S}	-	-	94	A	$T_{\text{C}}=25\text{ °C}$
Diode pulse current	$I_{\text{S,pulse}}$	-	-	644	A	$T_{\text{C}}=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.84	1	V	$V_{\text{GS}}=0\text{ V}$, $I_{\text{F}}=50\text{ A}$, $T_{\text{j}}=25\text{ °C}$
Reverse recovery time ⁹⁾	t_{rr}	-	70	140	ns	$V_{\text{R}}=20\text{ V}$, $I_{\text{F}}=50\text{ A}$, $di_{\text{F}}/dt=400\text{ A}/\mu\text{s}$
Reverse recovery charge ⁹⁾	Q_{rr}	-	27	-	nC	$V_{\text{R}}=20\text{ V}$, $I_{\text{F}}=50\text{ A}$, $di_{\text{F}}/dt=400\text{ A}/\mu\text{s}$

⁹⁾ Defined by design. Not subject to production test

4 Electrical characteristics diagrams

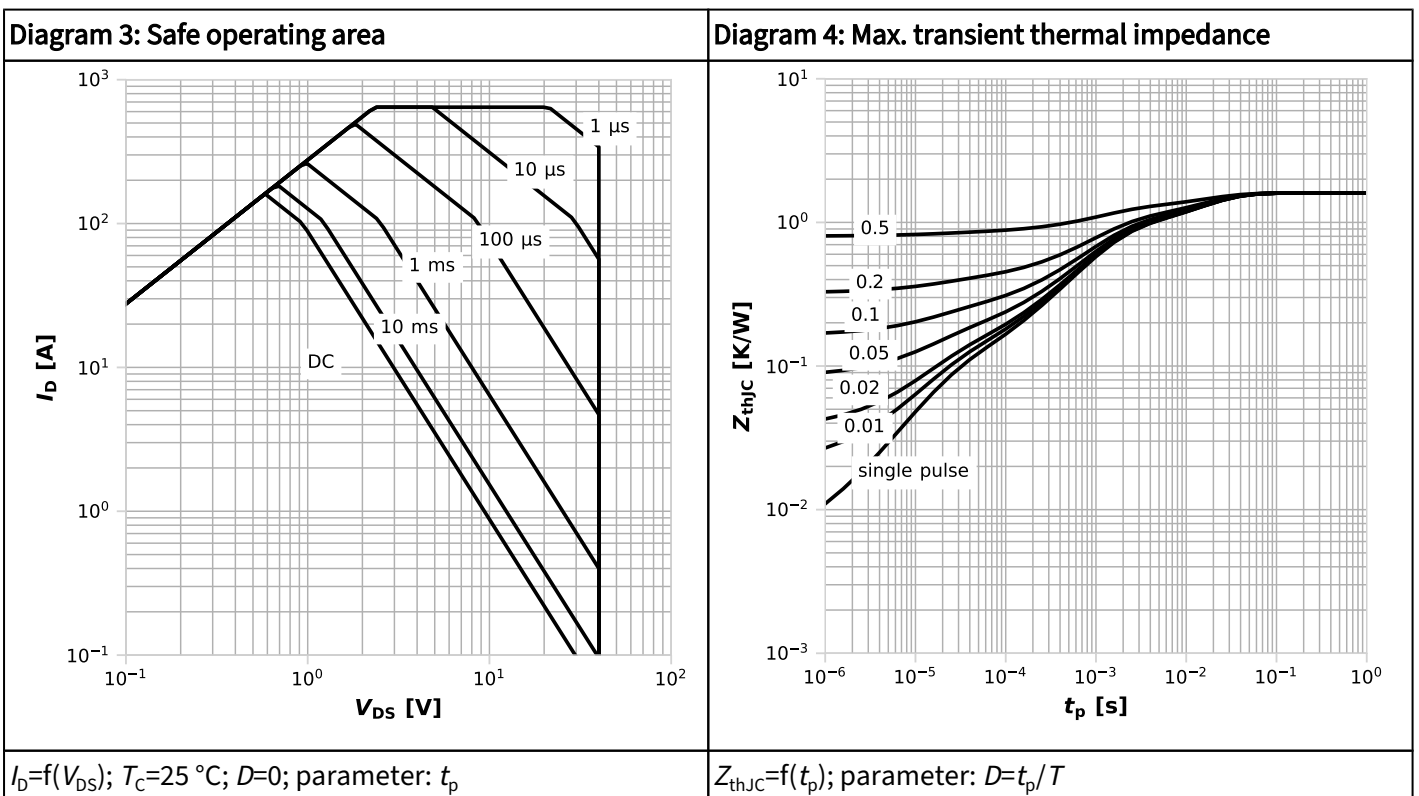
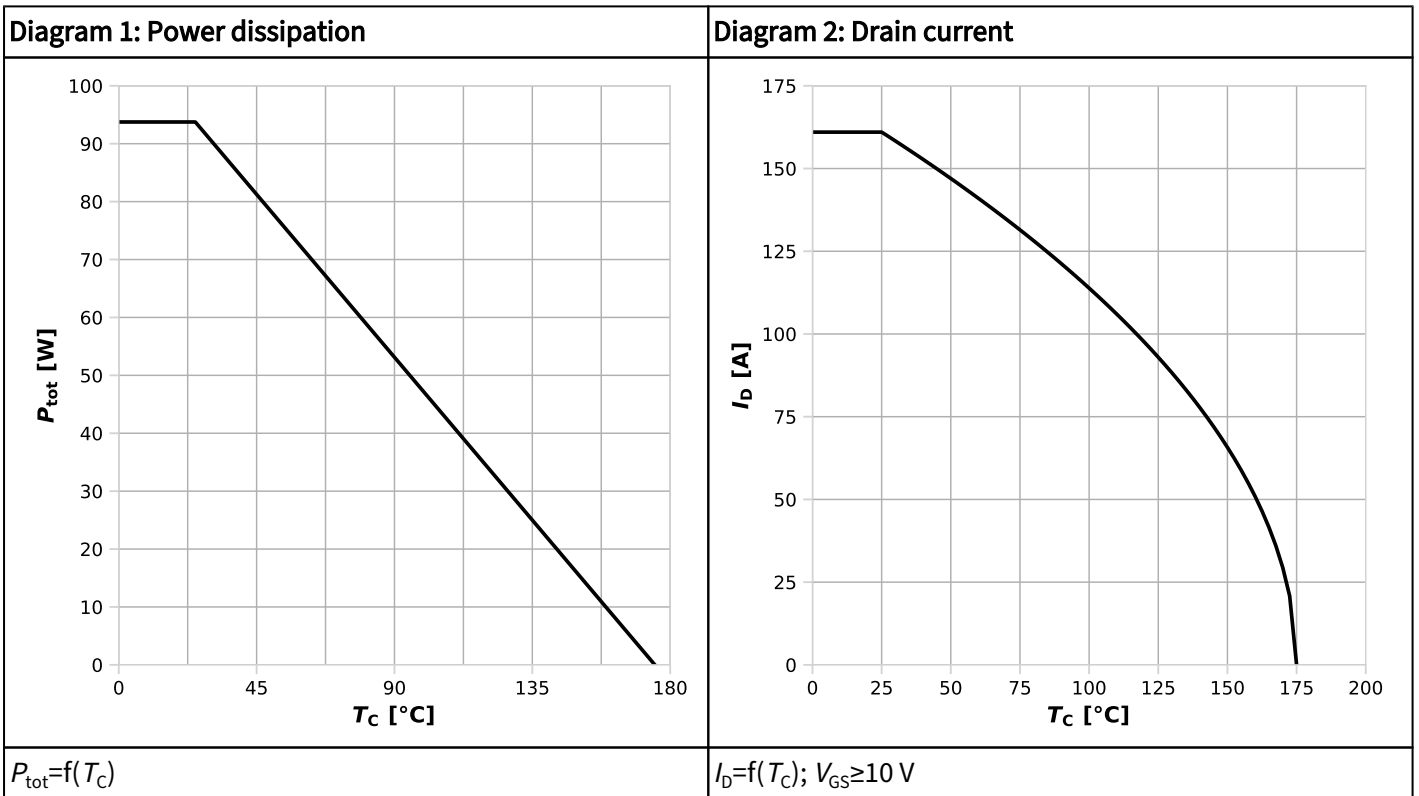
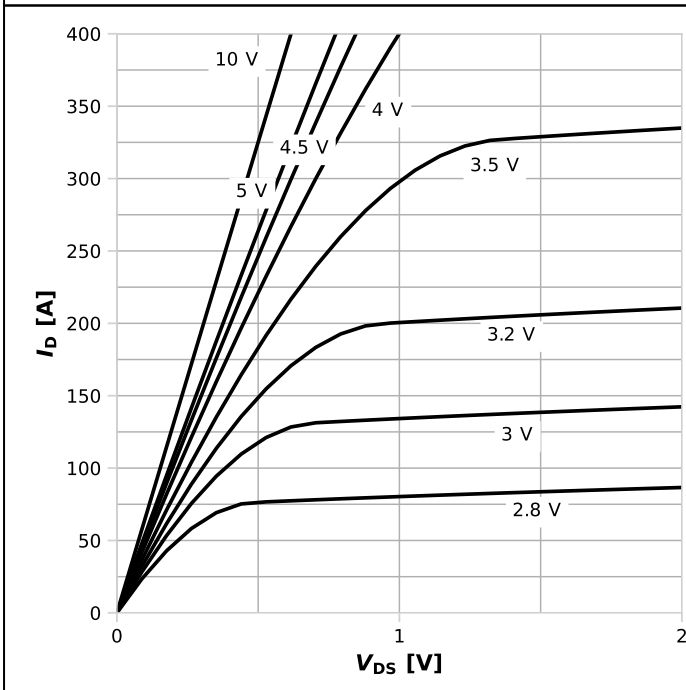
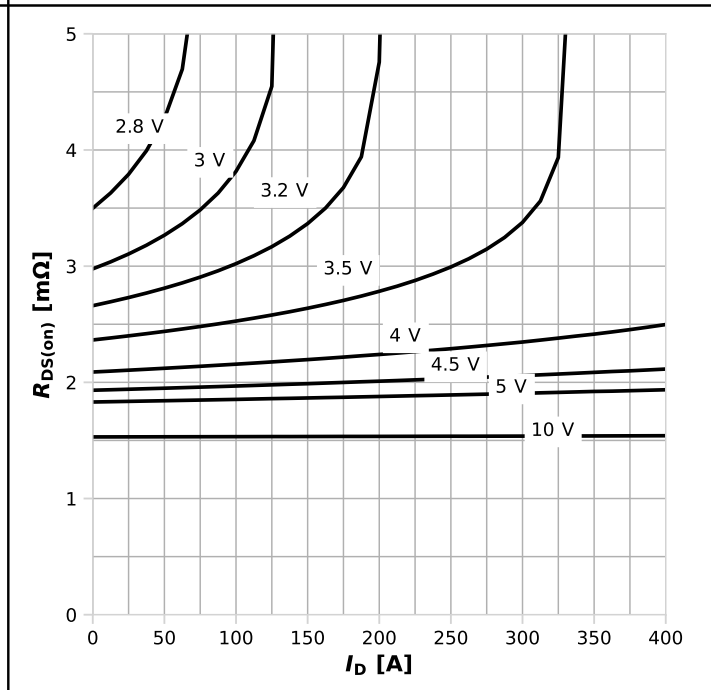


Diagram 5: Typ. output characteristics



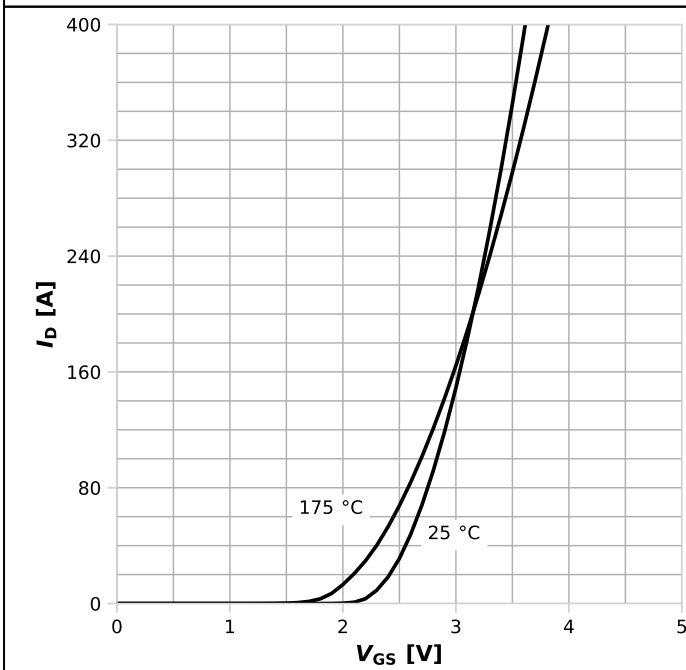
$I_D = f(V_{DS}); T_j = 25\text{ °C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. drain-source on resistance



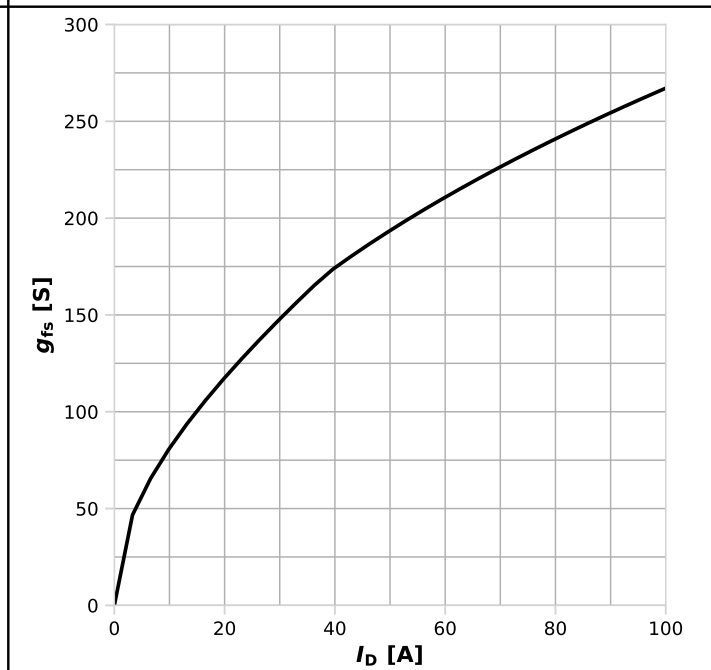
$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. transfer characteristics



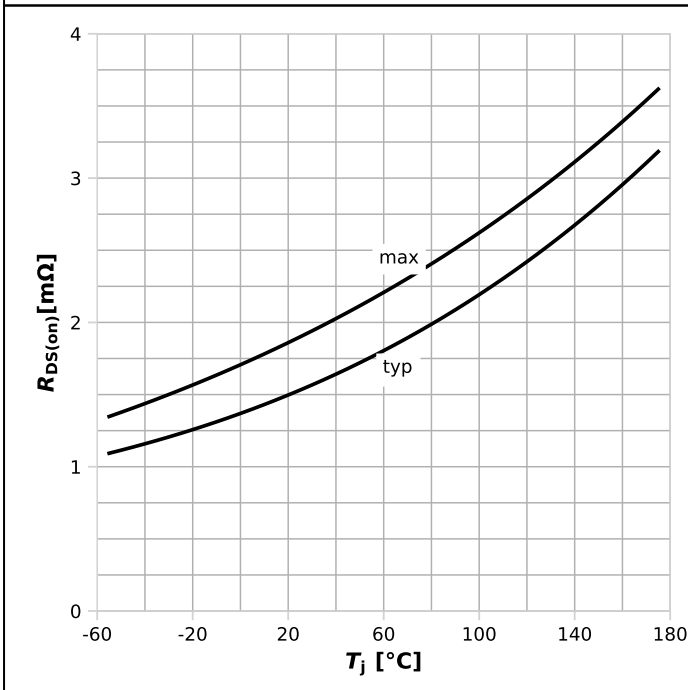
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}; \text{parameter: } T_j$

Diagram 8: Typ. forward transconductance



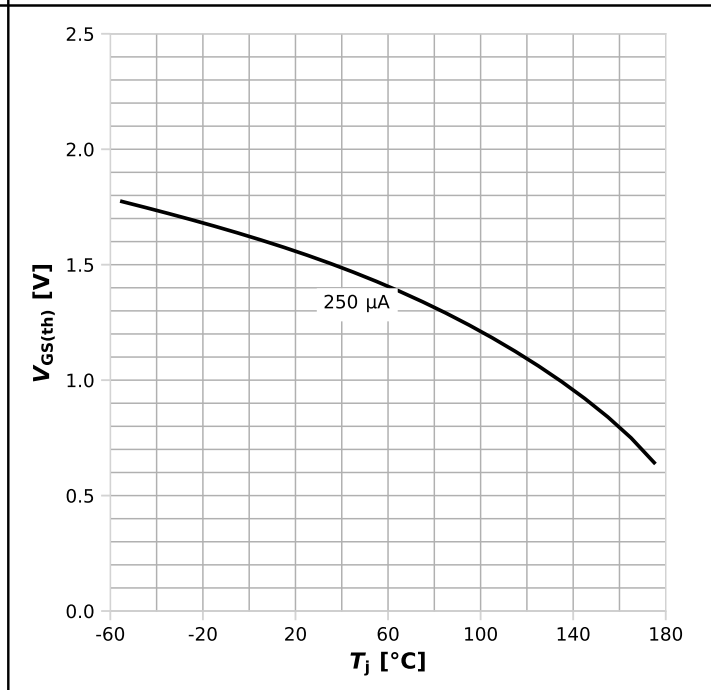
$g_{fs} = f(I_D); T_j = 25\text{ °C}$

Diagram 9: Drain-source on-state resistance



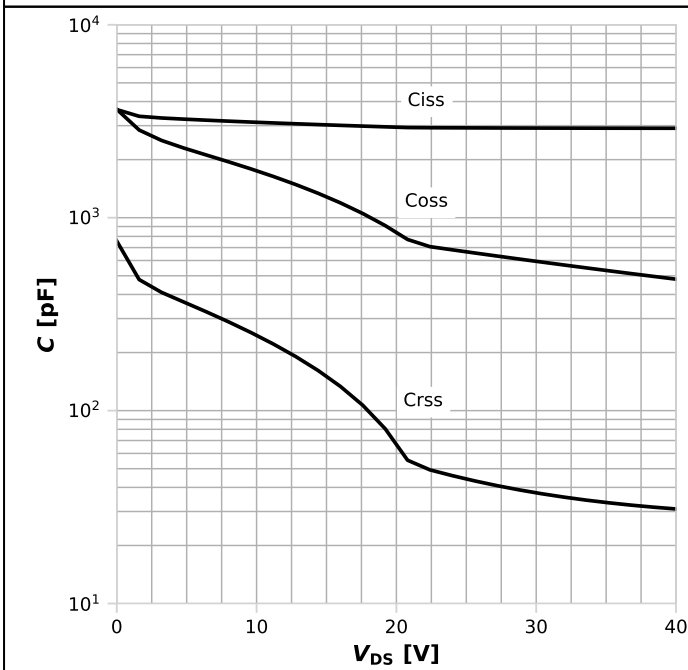
$R_{DS(on)} = f(T_j); I_D = 50 \text{ A}; V_{GS} = 10 \text{ V}$

Diagram 10: Typ. gate threshold voltage



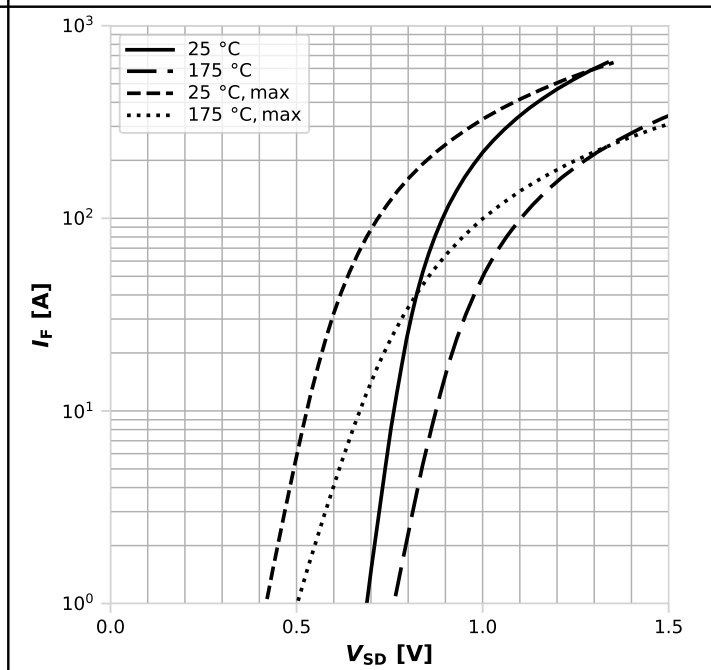
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = 250 \mu\text{A}$

Diagram 11: Typ. capacitances



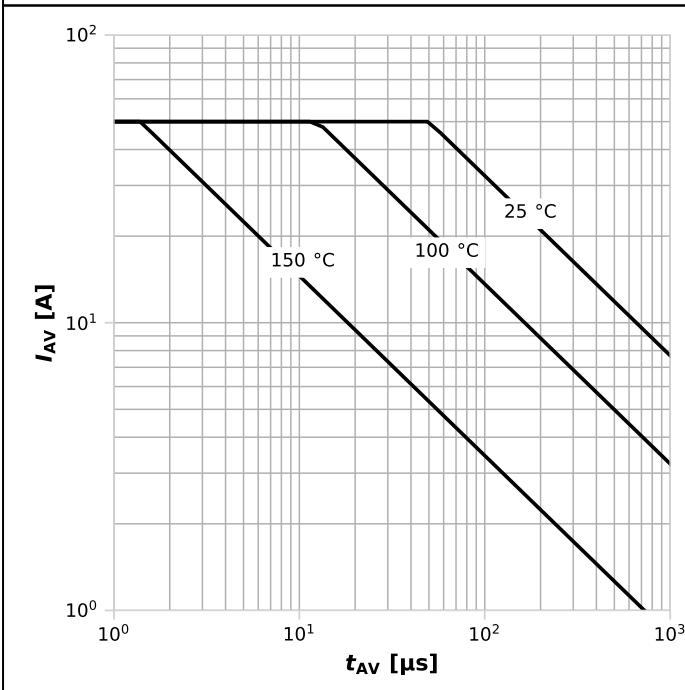
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



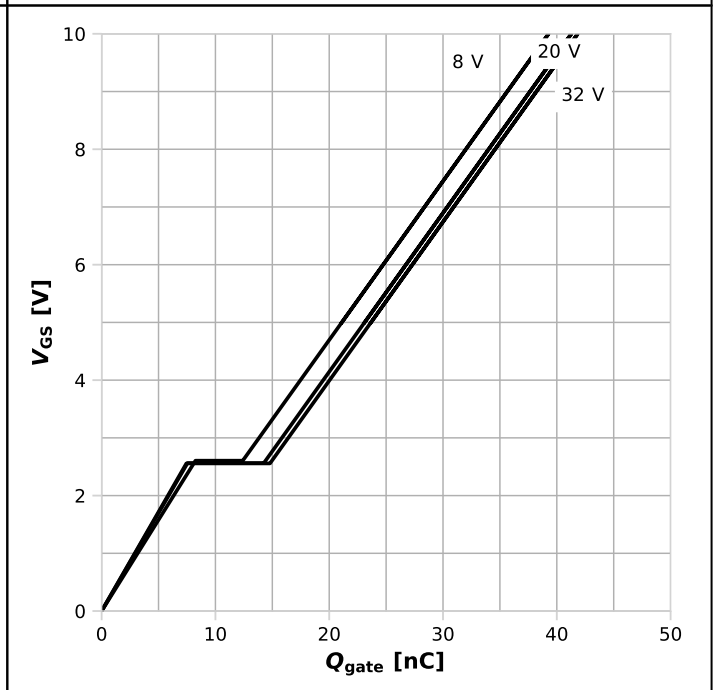
$I_F = f(V_{SD}); \text{parameter: } T_j$

Diagram 13: Avalanche characteristics



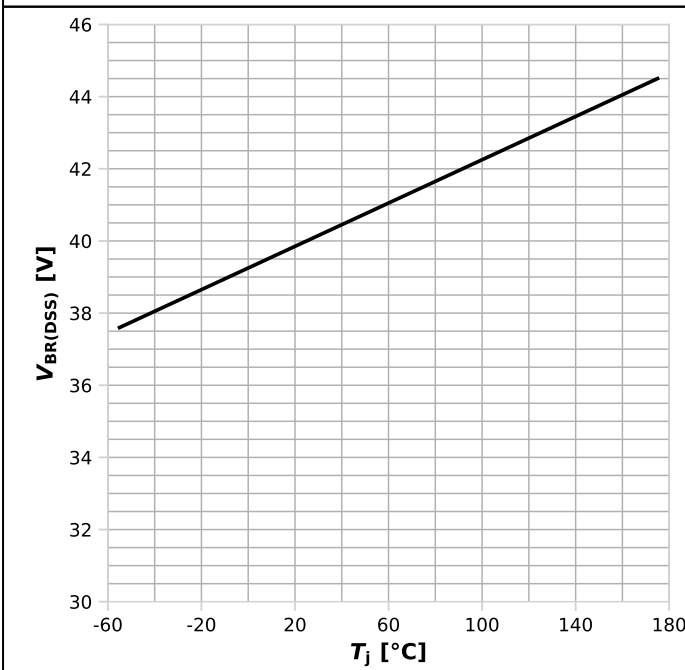
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



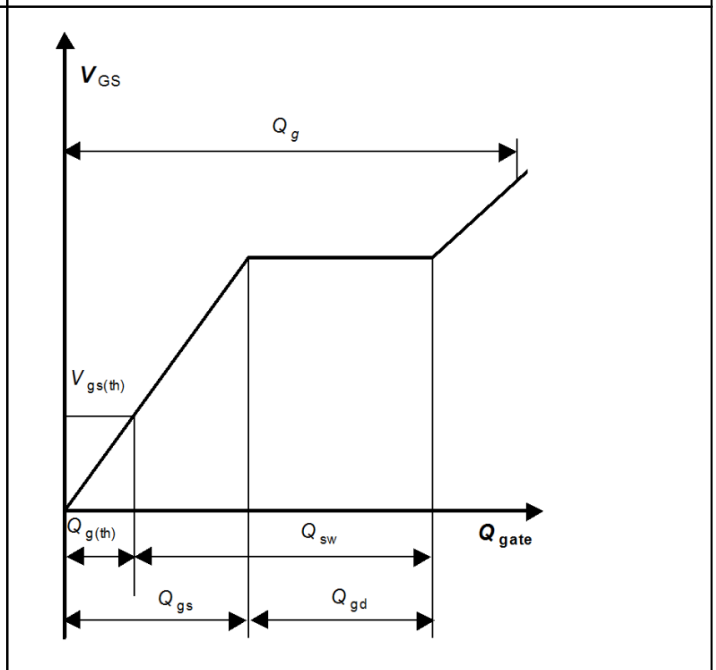
$V_{GS}=f(Q_{gate}); I_D=50 \text{ A pulsed}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



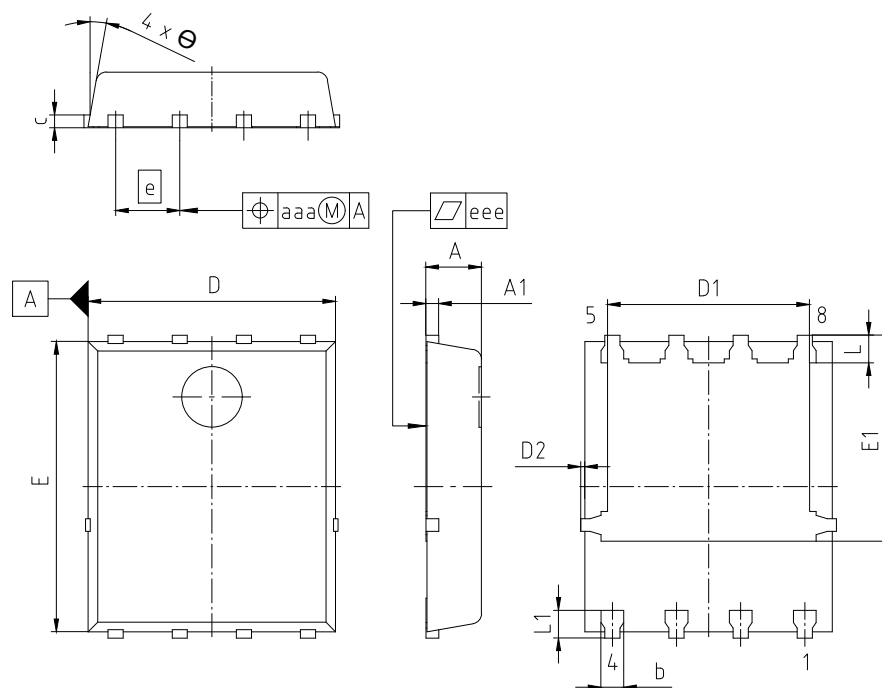
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Gate charge waveforms



-

5 Package Outlines



PACKAGE - GROUP NUMBER: PG-TDSON-8-U08		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.34	0.54
c	0.15	0.35
D	4.80	5.35
D1	3.90	4.40
D2	0.00	0.22
E	5.70	6.10
E1	4.03	4.25
e	1.27	
L	0.45	0.72
L1	0.45	0.71
aaa	0.25	
eee	0.05	
θ	8°	12°

- 1) EXCLUDING MOLD FLASH
- 2) REMOVAL ON MOLD GATE
INTRUSION 0.1 MM
PROTRUSION 0.1 MM
- 3) ALL METAL SURFACES ARE PLATED,
EXCEPT AREA OF CUT

Figure 1 Outline PG-TDSON-8, dimensions in mm

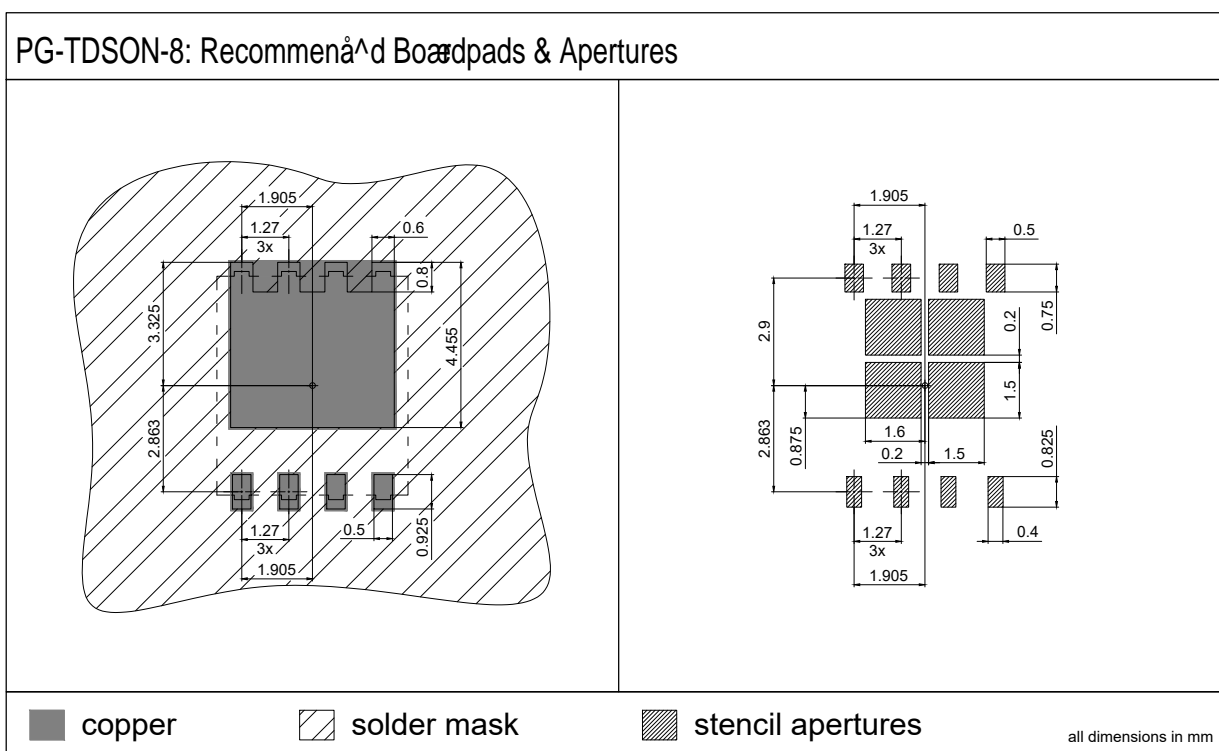
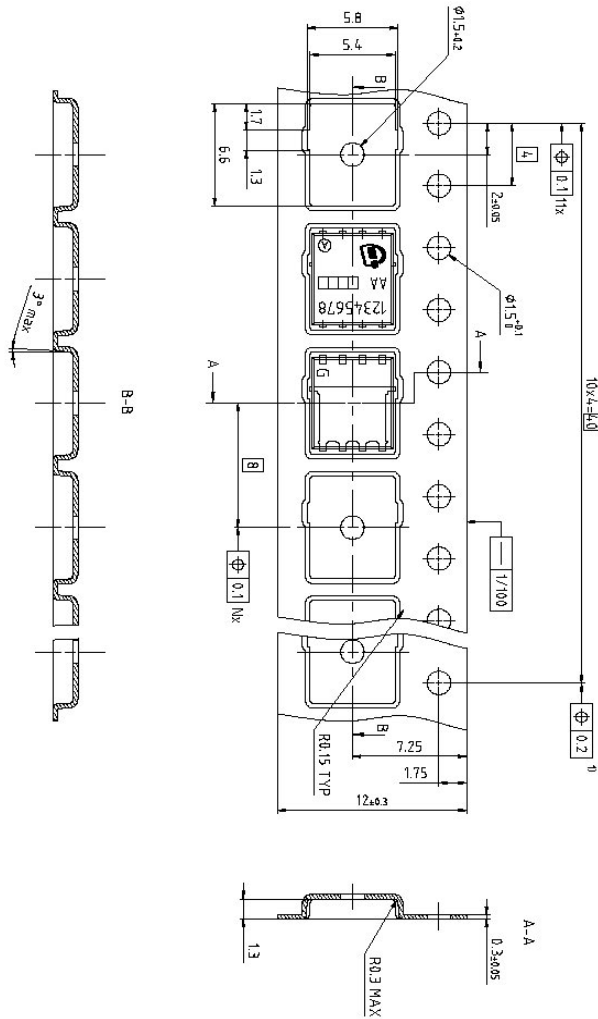


Figure 2 Outline PG-TDSON-8, dimensions in mm



Dimension in mm

Figure 3 Outline PG-TDSON-8, dimensions in mm

Revision History

BSC019N04LS

Revision 2024-06-11, Rev. 2.4

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.1	2016-05-24	Update footnotes and insert max values
2.2	2020-02-10	Update package drawings
2.3	2021-04-27	Update current rating
2.4	2024-06-11	Upgrade Operating and storage temperature max to 175°C . Update drawings in section 5 Package Outlines. Production validation added on page1

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

We Listen to Your Comments Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: erratum@infineon.com

Published by

Infineon Technologies AG
81726 München, Germany
© 2024 Infineon Technologies AG
All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie"). With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.