

MOSFET
OptiMOS™ 6 Power-Transistor, 40 V

Features

- Dual-side cooled package with lowest junction-top thermal resistance
- Optimized for synchronous application
- Very low on-resistance $R_{DS(on)}$
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- 175 °C rated

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	40	V
$R_{DS(on),max}$	0.7	mΩ
I_D	381	A
Q_{oss}	103	nC
$Q_G(0V..10V)$	94	nC
$Q_G(0V..4.5V)$	45	nC

Part number	Package	Marking	Related links
BSC007N04LS6SC	PG-VSON-8 / PG-WSN-8	007N04SC	-

PG-VSON-8 / PG-WSN-8

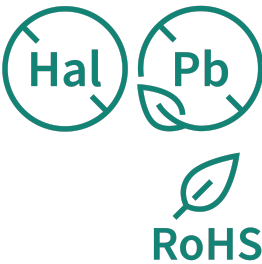
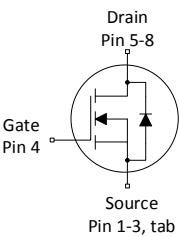
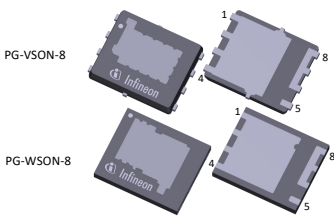




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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	381	A	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$
				269		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$
				319		$V_{GS}=4.5\text{ V}, T_C=25\text{ °C}$
				225		$V_{GS}=4.5\text{ V}, T_C=100\text{ °C}$
				48		$V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=50\text{ °C/W}^{2)}$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	1524	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	630	mJ	$I_D=50\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	188	W	$T_C=25\text{ °C}$
				3.0		$T_A=25\text{ °C}, R_{thJA}=50\text{ °C/W}^{2)}$
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	0.8	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}			0.72		
Device on PCB, 6 cm ² cooling area ⁵⁾	R_{thJA}			50		

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.3	-	2.3	V	$V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1	1	μA	$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$
			10	100		$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.57	0.7	m Ω	$V_{GS}=10\text{ V}$, $I_D=50\text{ A}$
			0.75	1.0		$V_{GS}=4.5\text{ V}$, $I_D=50\text{ A}$
Gate resistance	R_G	-	1	-	Ω	-
Transconductance	g_{fs}	-	300	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=50\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	6500	8400	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Output capacitance ⁶⁾	C_{oss}		2100	2700		
Reverse transfer capacitance ⁶⁾	C_{rss}		51	89		
Turn-on delay time	$t_{d(on)}$	-	8	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=20\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r		6			
Turn-off delay time	$t_{d(off)}$		40			
Fall time	t_f		13			

⁶⁾ Defined by design. Not subject to production test.

Table 6 Gate charge characteristics ⁷⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	17	-	nC	$V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$		10.3	-	nC	
Gate to drain charge ⁸⁾	Q_{gd}		11.2	17	nC	
Switching charge	Q_{sw}		18	-	nC	
Gate charge total ⁸⁾	Q_g		94	118	nC	
Gate plateau voltage	$V_{plateau}$		2.6	-	V	
Gate charge total	Q_g	-	45	-	nC	$V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	39	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Output charge ⁸⁾	Q_{oss}	-	103	137	nC	$V_{DD}=20\text{ V}$, $V_{GS}=0\text{ V}$

⁷⁾ See "Gate charge waveforms" for parameter definition

⁸⁾ Defined by design. Not subject to production test.

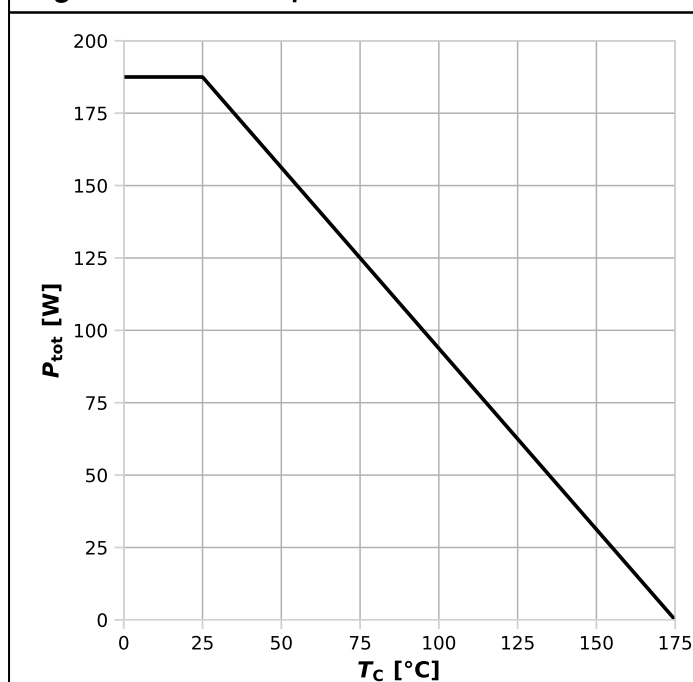
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	188	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$			1524		
Diode forward voltage	V_{SD}	-	0.78	1.0	V	$V_{GS}=0\text{ V}$, $I_F=50\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time ⁹⁾	t_{rr}	-	36	72	ns	$V_R=20\text{ V}$, $I_F=10\text{ A}$, $di_F/dt=400\text{ A}/\mu\text{s}$
Reverse recovery charge ⁹⁾	Q_{rr}		133	266	nC	

⁹⁾ Defined by design. Not subject to production test.

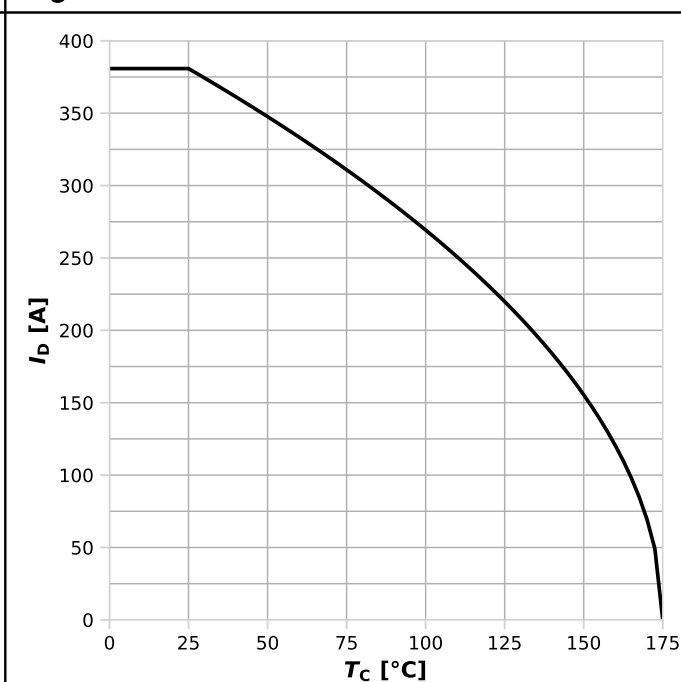
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



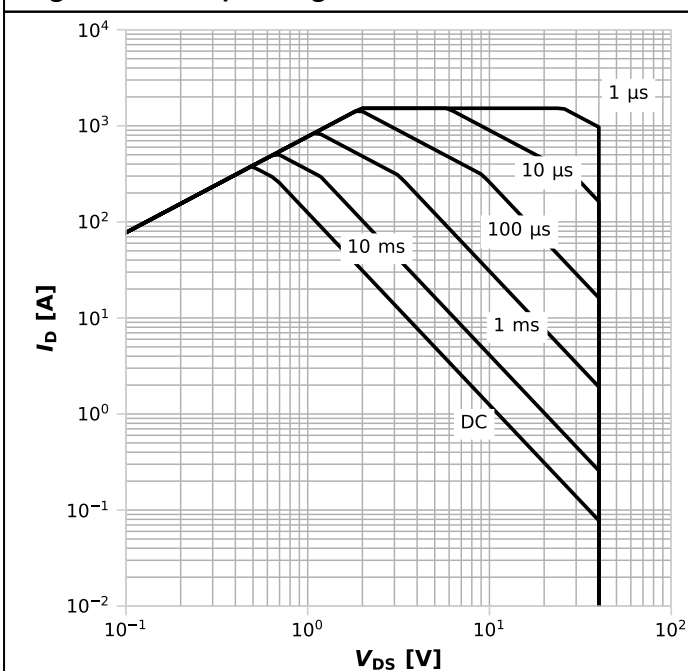
$$P_{tot}=f(T_c)$$

Diagram 2: Drain current



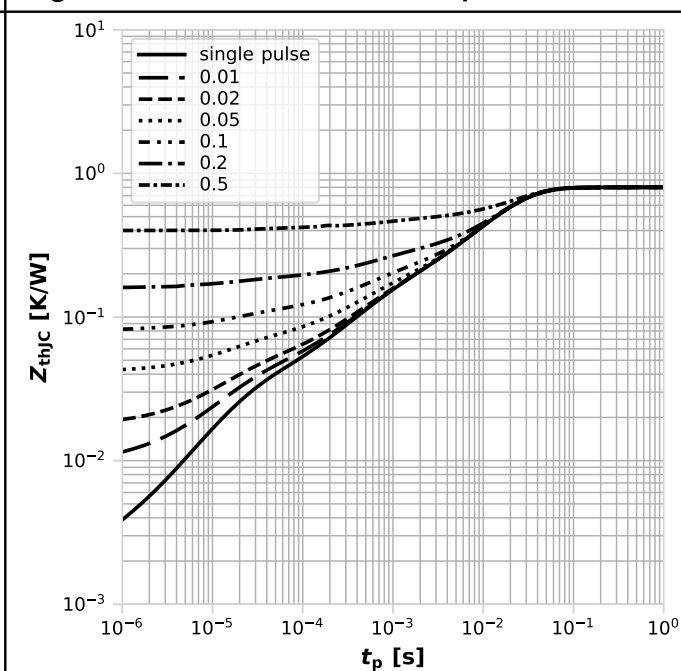
$$I_D=f(T_c); V_{GS}\geq 10\text{ V}$$

Diagram 3: Safe operating area



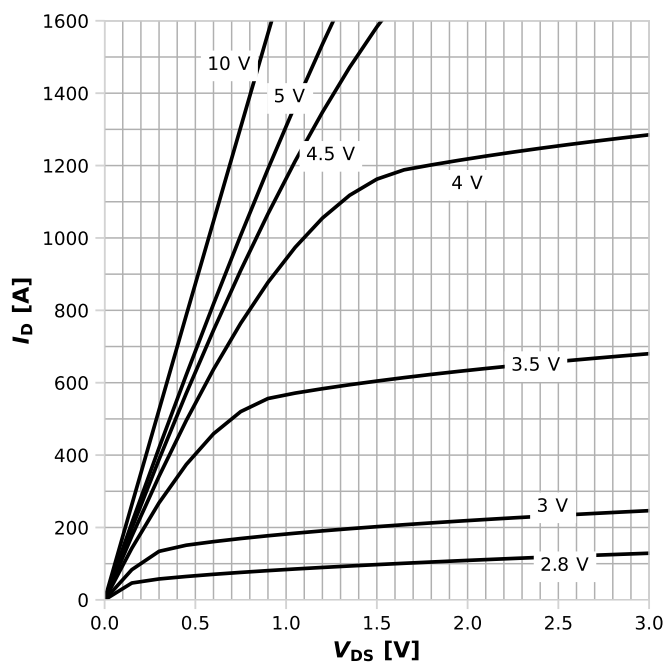
$$I_D=f(V_{DS}); T_c=25\text{ °C}; D=0; \text{parameter: } t_p$$

Diagram 4: Max. transient thermal impedance



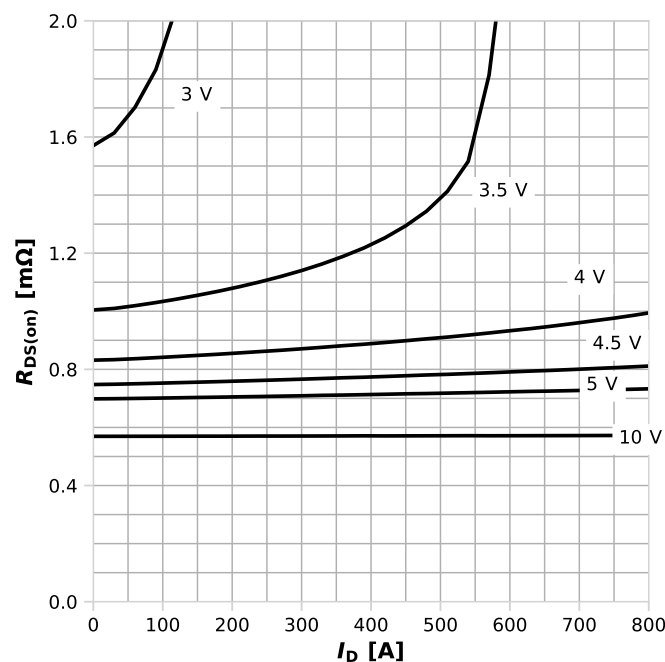
$$Z_{thJC}=f(t_p); \text{parameter: } D=t_p/T$$

Diagram 5: Typ. output characteristics



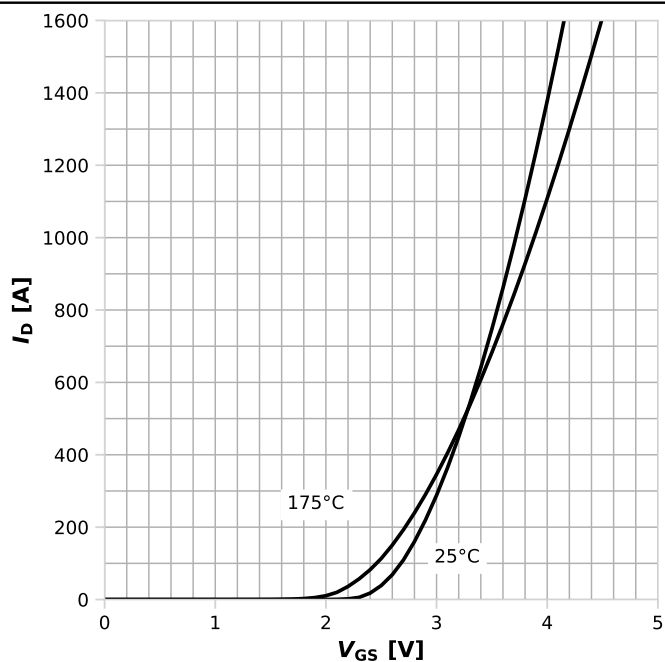
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



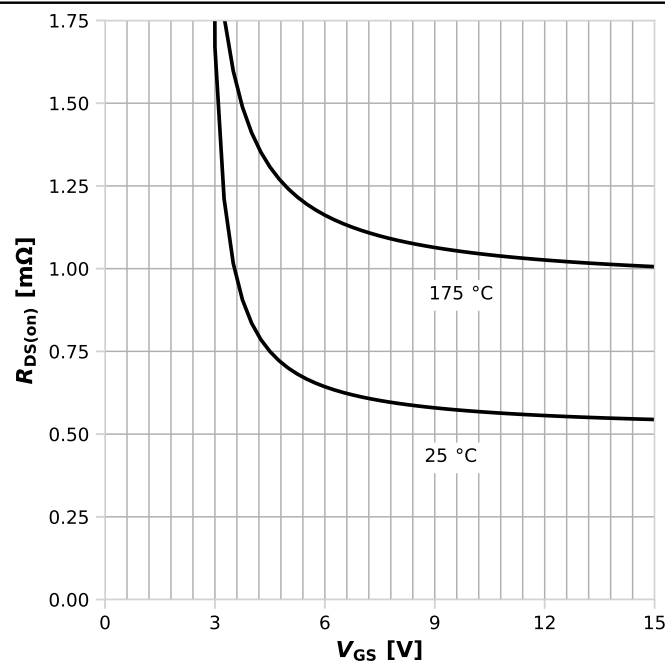
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



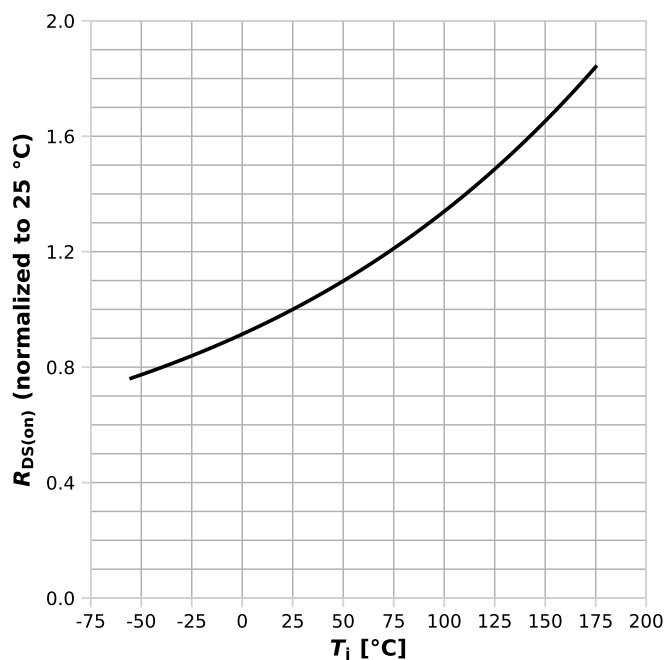
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



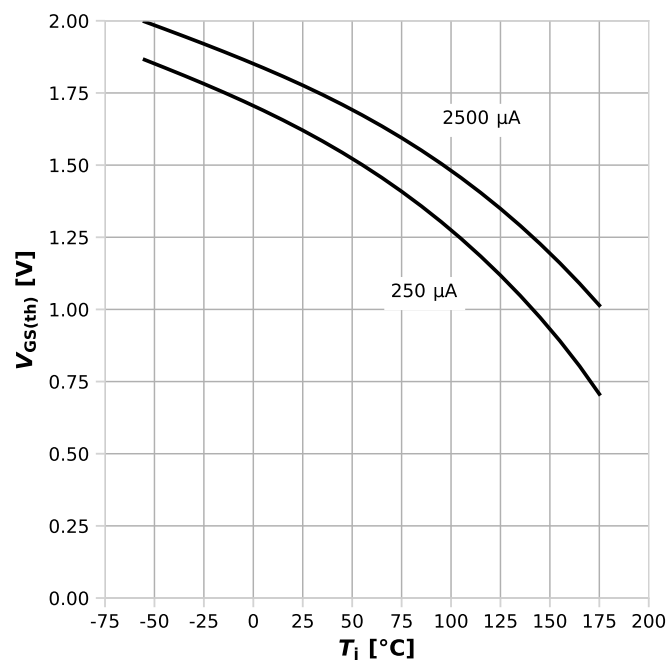
$R_{DS(on)} = f(V_{GS})$, $I_D = 50\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



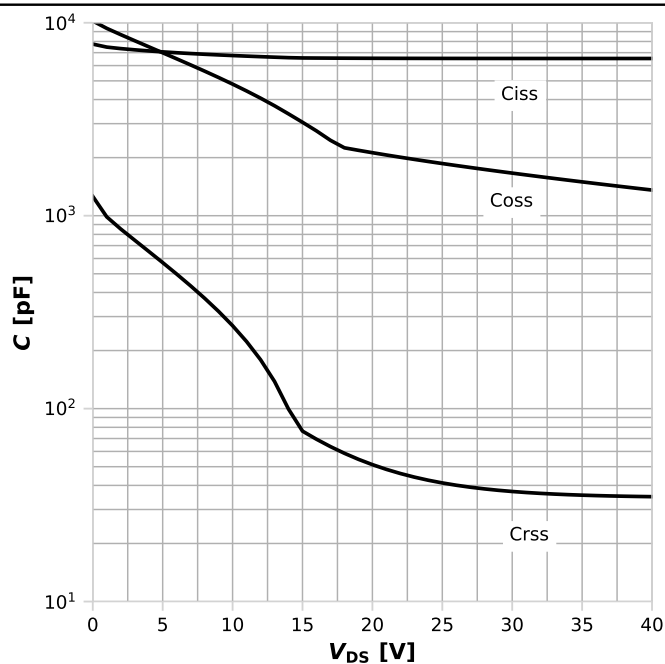
$$R_{DS(on)} = f(T_j), I_D = 50 \text{ A}, V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



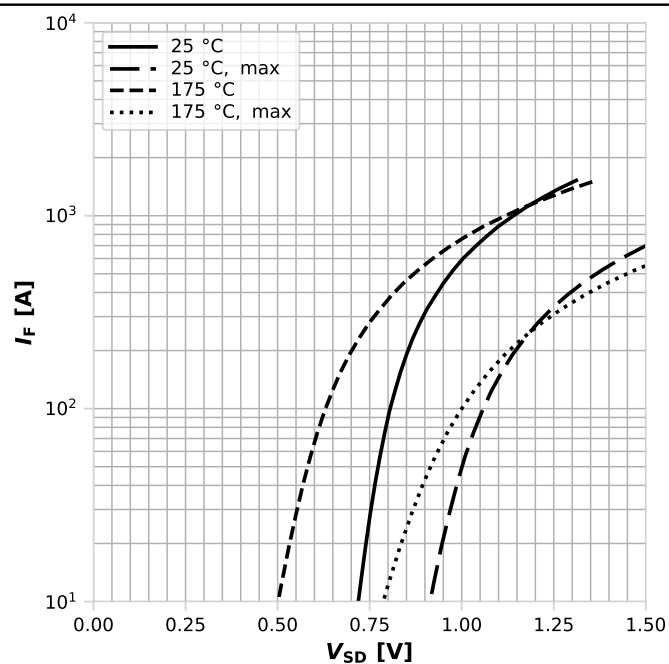
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{ parameter: } I_D$$

Diagram 11: Typ. capacitances



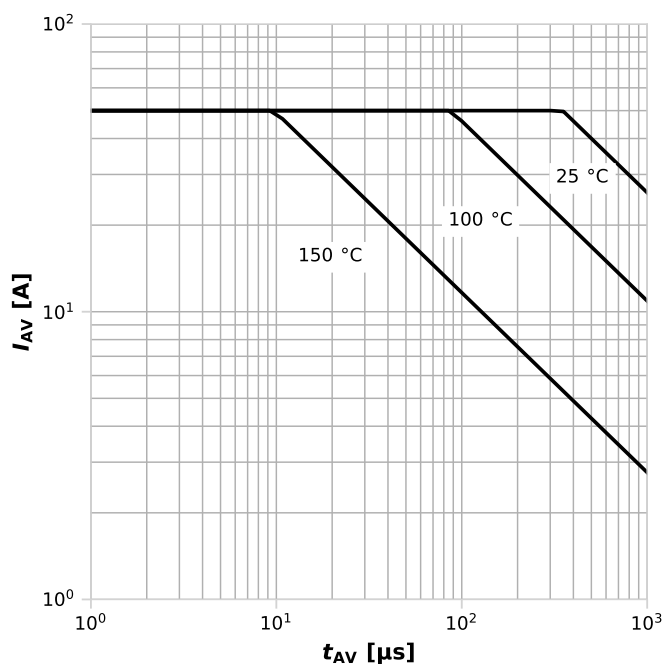
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 12: Forward characteristics of reverse diode



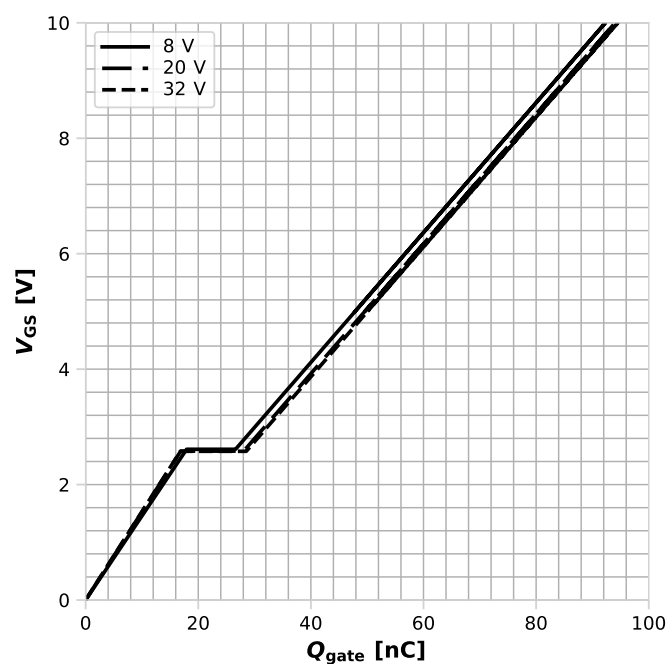
$$I_F = f(V_{SD}); \text{ parameter: } T_j$$

Diagram 13: Avalanche characteristics



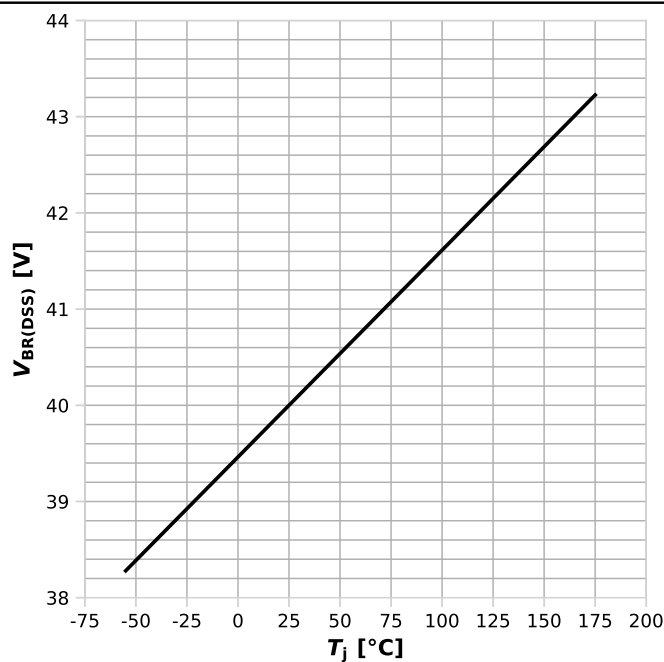
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



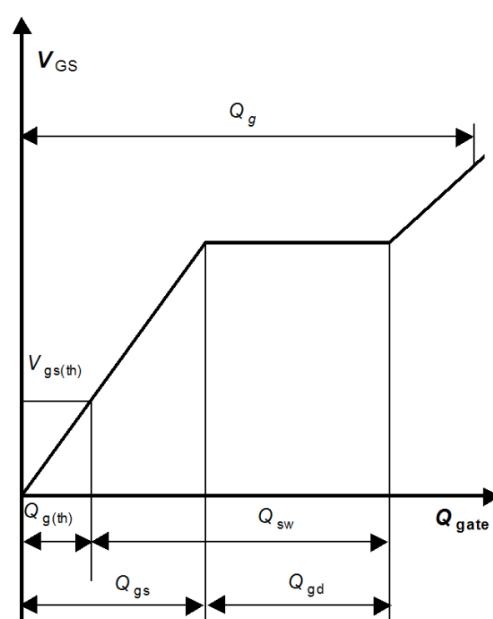
$V_{GS}=f(Q_{gate})$, $I_D=50\text{ A}$ pulsed, $T_j=25\text{ °C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



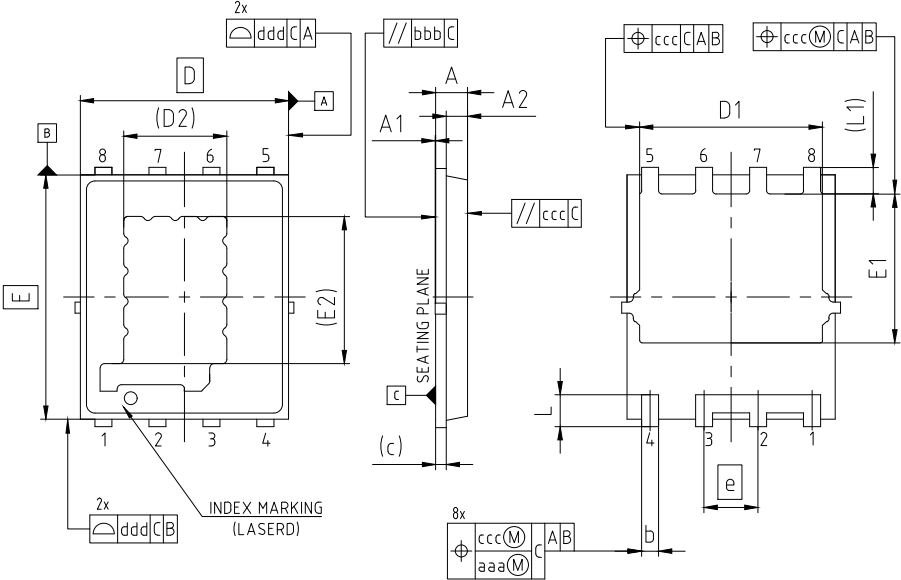
$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

Gate charge waveforms



-

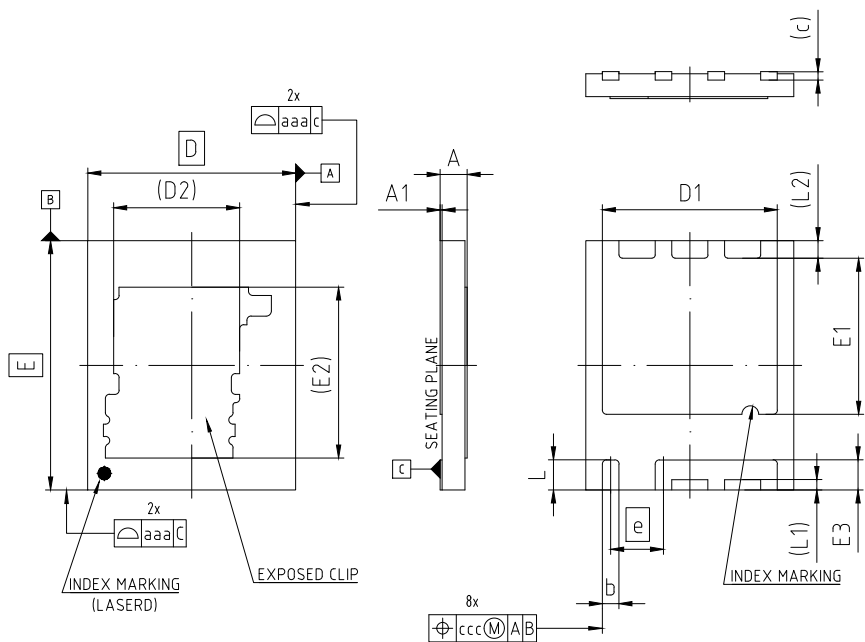
5 Package outlines



PACKAGE - GROUP NUMBER: PG-VSON-8-U01					
DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.65	0.85	e	1.27	
A1	0.00	0.05	L	0.70	0.90
A2	0.45	0.55	L1	0.52	0.72
b	0.35	0.55	aaa	0.05	
c	0.25		bbb	0.08	
D	4.90		ccc	0.10	
D1	4.20	4.40	ddd	0.15	
D2	2.43				
E	5.75				
E1	3.40	3.60			
E2	3.46				

NOTE: DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-VSON-8 / PG-WSO8-8, dimensions in mm



PACKAGE - GROUP NUMBER: PG-WSN-8-U01					
DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.55	0.75	e	1.27	
A1	0.00	0.05	L	0.68	0.78
b	0.35	0.45	L1	0.25	
c	0.20		L2	0.42	
D	5.00		aaa	0.05	
D1	4.11	4.31	ccc	0.10	
D2	3.03				
E	6.00				
E1	3.66	3.86			
E2	4.11				
E3	0.63	0.83			

NOTE: DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 2 PG-VSON-8 / PG-WSN-8, dimensions in mm

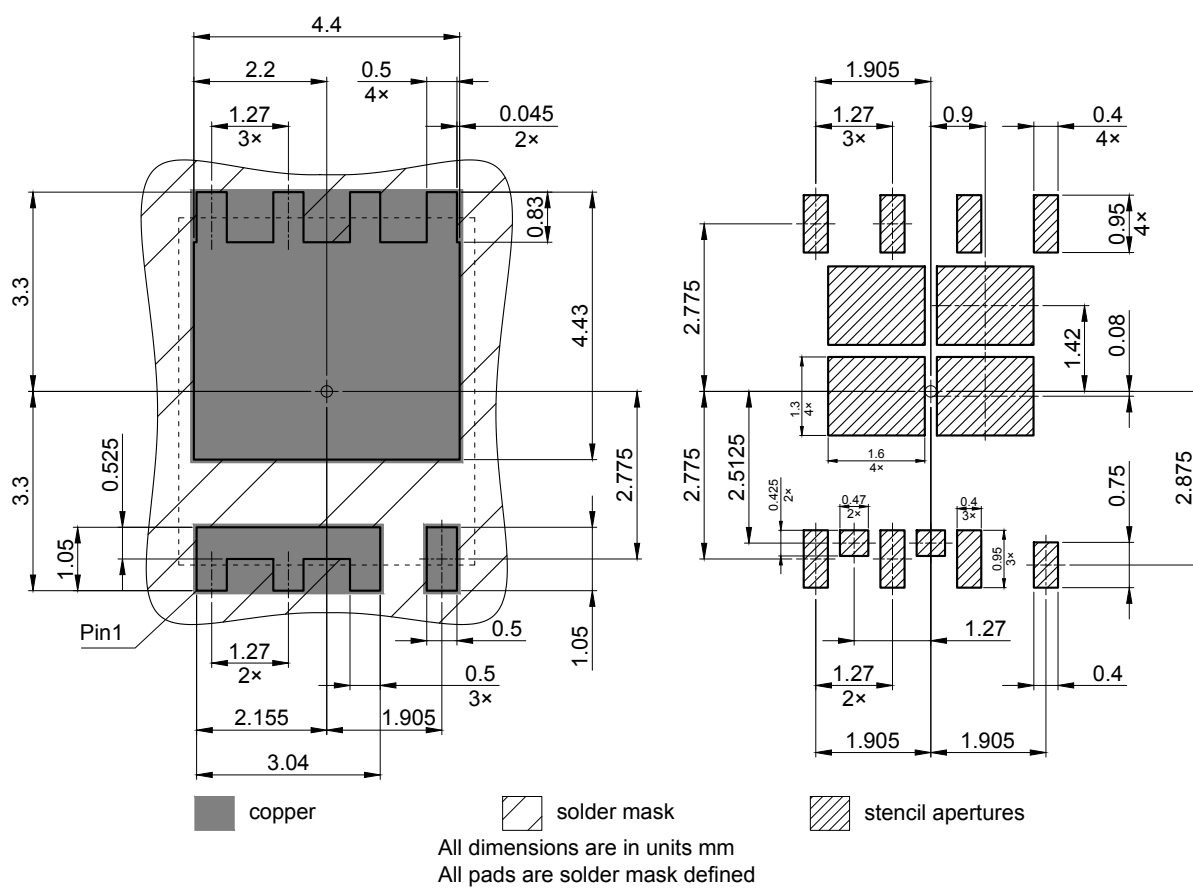


Figure 3 Bonding diagram PG-VSON-8 / PG-WSN-8, dimensions in mm

Revision history

BSC007N04LS6SC

Revision 2025-06-09, Rev. 2.2

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2022-09-17	Release of final version
2.1	2022-10-06	Update "Features" and Is
2.2	2025-06-09	Update package drawings

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