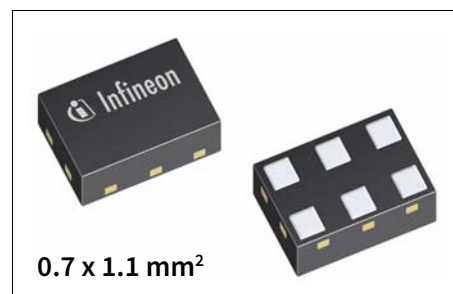


BGA5H1BN6

18dB High Gain Low Noise Amplifier for LTE Highband

Features

- Operating frequencies: 2300 - 2690 MHz
- Insertion power gain: 18.1 dB
- Insertion Loss in bypass mode: 5.2 dB
- Low noise figure: 0.7 dB
- Low current consumption: 8.5 mA
- Multi-state control: Bypass- and high gain-Mode
- Ultra small TSNP-6-10 leadless package
- RF output internally matched to 50 Ohm
- Low external component count



Application

The LTE data rate can be significantly improved by using the Low Noise Amplifier. The integrated bypass function increases the overall system dynamic range and leads to more flexibility in the RF front-end.

In high gain mode the LNA offers best Noise Figure to ensure high data rates even on the LTE cell edge. Closer to the basestation the bypass mode can be activated reducing current consumption.

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Block diagram

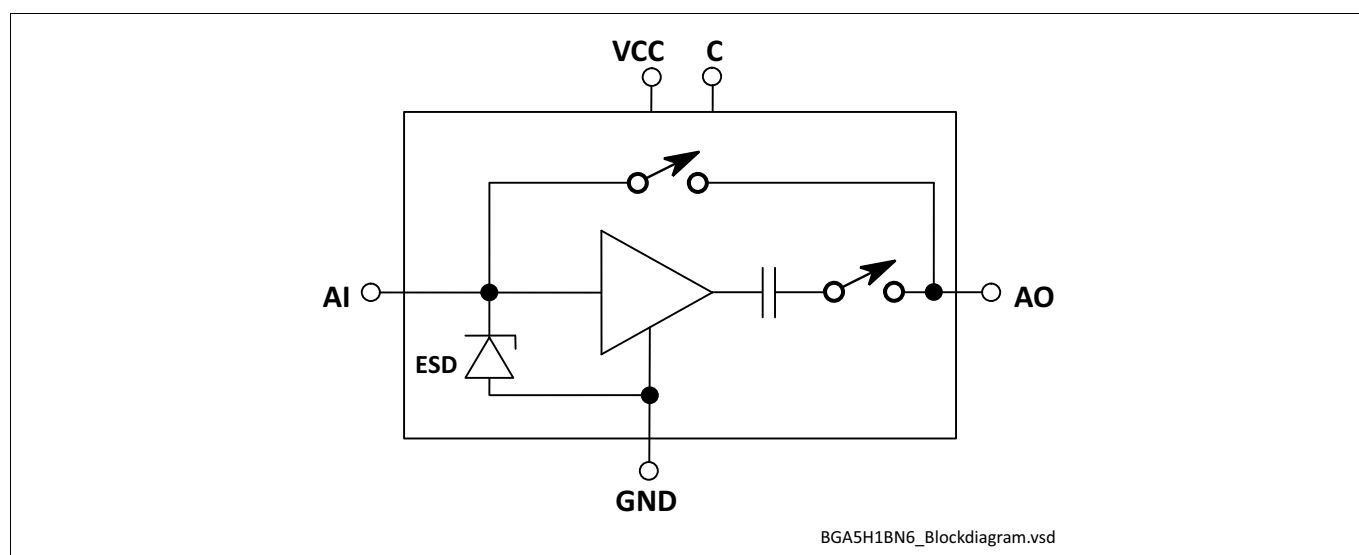


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Features

1 Features

- Insertion power gain: 18.1 dB
- Insertion Loss in bypass mode: 5.2 dB
- Low noise figure: 0.7 dB
- Low current consumption: 8.5 mA
- Operating frequencies: 2300 - 2690 MHz
- Multi-state control: Bypass- and High gain-Mode
- Supply voltage: 1.5 V to 3.6 V
- Ultra small TSNP-6-10 leadless package (footprint: 0.7 x 1.1 mm²)
- B9HF Silicon Germanium technology
- RF output internally matched to 50 Ohm
- Low external component count
- Pb-free (RoHS compliant) package

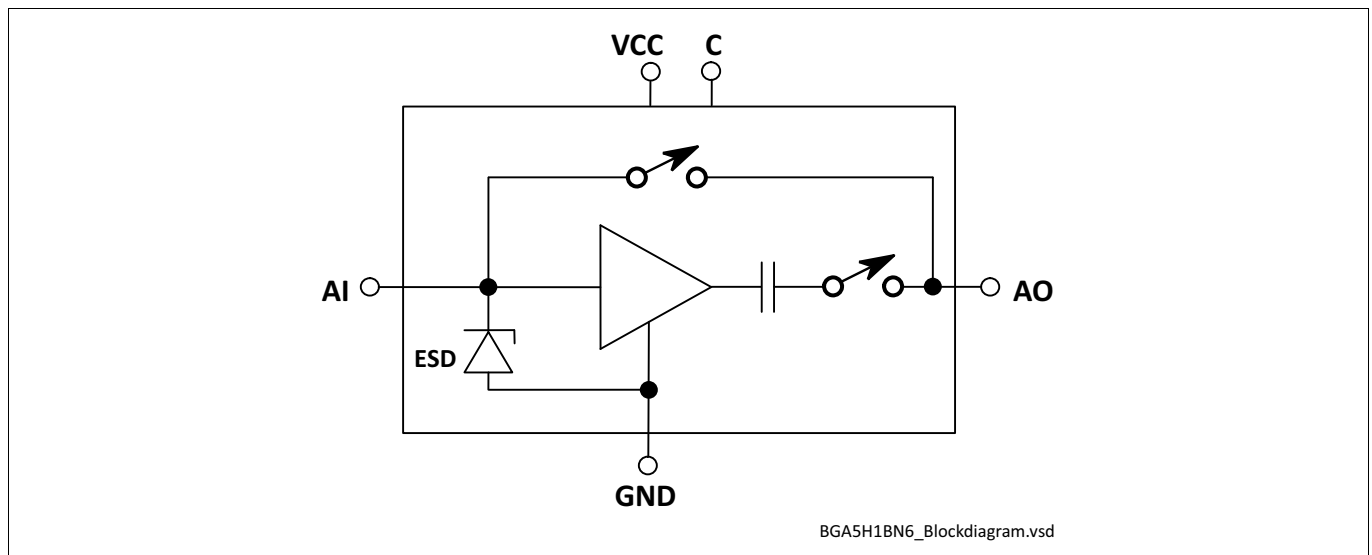


Figure 1 Block Diagram

Product Name	Marking	Package
BGA5H1BN6	4	TSNP-6-10

Features

Description

The BGA5H1BN6 is a front-end low noise amplifier for LTE which covers a wide frequency range from 2300 MHz to 2690 MHz. The LNA provides 18.1 dB gain and 0.7 dB noise figure at a current consumption of 8.5 mA in the application configuration described in [Chapter 4](#). In bypass mode the LNA provides an insertion loss of 5.2 dB. The BGA5H1BN6 is based upon Infineon Technologies' B9HF Silicon Germanium technology. It operates from 1.5 V to 3.6 V supply voltage. The device features a single-line two-state control (Bypass- and High gain-Mode). OFF-state can be enabled by powering down VCC.

Pin Definition and Function

Table 1 **Pin Definition and Function**

Pin No.	Name	Function
1	GND	Ground
2	VCC	DC supply
3	AO	LNA output
4	GND	Ground
5	AI	LNA input
6	C	Control

Maximum Ratings

2 Maximum Ratings

Table 2 Maximum Ratings

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Voltage at pin VCC	V_{CC}	-0.3	–	3.6	V	1)
Voltage at pin AI	V_{AI}	-0.3	–	0.9	V	–
Voltage at pin AO	V_{AO}	-0.3	–	$V_{CC} + 0.3$	V	–
Voltage at pin C	V_C	-0.3	–	$V_{CC} + 0.3$	V	–
Voltage at pin GND	V_{GND}	-0.3	–	0.3	V	–
Current into pin VCC	I_{CC}	–	–	16	mA	–
RF input power	P_{IN}	–	–	+25	dBm	–
Total power dissipation, $T_S < 148\text{ °C}^{2)}$	P_{tot}	–	–	60	mW	–
Junction temperature	T_J	–	–	150	°C	–
Ambient temperature range	T_A	-40	–	85	°C	–
Storage temperature range	T_{STG}	-55	–	150	°C	–

1) All voltages refer to GND-Node unless otherwise noted

2) T_S is measured on the ground lead at the soldering point

Attention: *Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.*

Electrical Characteristics

3 Electrical Characteristics

Table 3 Electrical Characteristics $V_{CC} = 1.8V^{1)}$

$T_A = 25^\circ C$, $V_{CC} = 1.8 V$, $V_{C,BP} = 1.8 V$, $V_{C,OFF} = 0 V$, $f = 2300 - 2690 MHz$

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	1.5	1.8	3.6	V	–
Control voltages	V_C	1.0	–	V_{CC}	V	High gain mode
		0	–	0.4	V	Bypass mode
Supply current	I_{CC}	–	8.5	10.3	mA	High gain mode
		–	85	120	μA	Bypass mode
Insertion power gain $f = 2500 MHz$	$ S_{21} ^2$	16.4	18.1	19.8	dB	High gain mode
		-6.5	-5.2	-3.9	dB	Bypass mode
Noise figure ²⁾ $f = 2500 MHz$, $Z_S = 50 \Omega$	NF	–	0.7	1.2	dB	High gain mode
		–	5.2	6.5	dB	Bypass mode
Input return loss ³⁾ $f = 2500 MHz$	RL_{IN}	7	10	–	dB	High gain mode
		5	8	–	dB	Bypass mode
Output return loss ³⁾ $f = 2500 MHz$	RL_{OUT}	10	20	–	dB	High gain mode
		3	5	–	dB	Bypass mode
Reverse isolation ³⁾ $f = 2500 MHz$	$1/ S_{12} ^2$	25	36	–	dB	High gain mode
		3.9	5.2	–	dB	Bypass mode
Power on time ⁴⁾⁶⁾	t_S	–	3	7	μs	OFF to High gain mode
Inband input 1dB-compression point, $f = 2500 MHz^{3)}$	IP_{1dB}	-21	-17	–	dBm	High gain mode
		-7	-3	–	dBm	Bypass mode
Inband input 3 rd -order intercept point ³⁾⁵⁾ $f_1 = 2500 MHz$, $f_2 = f_1 \pm 1 MHz$	IIP_3	-12	-7	–	dBm	High gain mode
		1	6	–	dBm	Bypass mode
Stability ⁶⁾	k	> 1	–	–		$f = 20 MHz \dots 10 GHz$

1) Based on the application described in [Chapter 4](#)

2) PCB losses are subtracted

3) Verification based on AQL; not 100% tested in production

4) Gain changed to >90% of gain difference (in dB)

5) Input power HG = -30 dBm for each tone; input power BP = -10 dBm for each tone

6) Guaranteed by device design; not tested in production

Electrical Characteristics

Table 4 Electrical Characteristics $V_{CC} = 2.8V^{1)}$

$T_A = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 2.8\text{ V}$, $V_{C,BP} = 2.8\text{ V}$, $V_{C,OFF} = 0\text{ V}$, $f = 2300 - 2690\text{ MHz}$

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	1.5	2.8	3.6	V	–
Control voltages	V_C	1.0	–	V_{CC}	V	High gain mode
		0	–	0.4	V	Bypass mode
Supply current	I_{CC}	–	9.8	11.6	mA	High gain mode
		–	87	120	μA	Bypass mode
Insertion power gain $f = 2500\text{ MHz}$	$ S_{21} ^2$	16.6	18.3	20.0	dB	High gain mode
		-6.5	-5.2	-3.9	dB	Bypass mode
Noise figure ²⁾ $f = 2500\text{ MHz}$, $Z_S = 50\text{ }\Omega$	NF	–	0.7	1.2	dB	High gain mode
		–	5.2	6.5	dB	Bypass mode
Input return loss ³⁾ $f = 2500\text{ MHz}$	RL_{IN}	7	10	–	dB	High gain mode
		5	8	–	dB	Bypass mode
Output return loss ³⁾ $f = 2500\text{ MHz}$	RL_{OUT}	10	19	–	dB	High gain mode
		3	5	–	dB	Bypass mode
Reverse isolation ³⁾ $f = 2500\text{ MHz}$	$1/ S_{12} ^2$	25	36	–	dB	High gain mode
		3.9	5.2	–	dB	Bypass mode
Power on time ⁴⁾⁶⁾	t_s	–	3	7	μs	OFF to High gain mode
Inband input 1dB-compression point, $f = 2500\text{ MHz}^{3)}$	IP_{1dB}	-20	-16	–	dBm	High gain mode
		-6	-2	–	dBm	Bypass mode
Inband input 3 rd -order intercept point ³⁾⁵⁾ $f_1 = 2500\text{ MHz}$, $f_2 = f_1 \pm 1\text{ MHz}$	IIP_3	-11	-6	–	dBm	High gain mode
		1	6	–	dBm	Bypass mode
Stability ⁶⁾	k	> 1	–	–		$f = 20\text{ MHz} \dots 10\text{ GHz}$

1) Based on the application described in [Chapter 4](#)

2) PCB losses are subtracted

3) Verification based on AQL; not 100% tested in production

4) Gain changed to >90% of gain difference (in dB)

5) Input power HG = -30 dBm for each tone; input power BP = -10 dBm for each tone

6) Guaranteed by device design; not tested in production

4 Application Information

Application Board Configuration

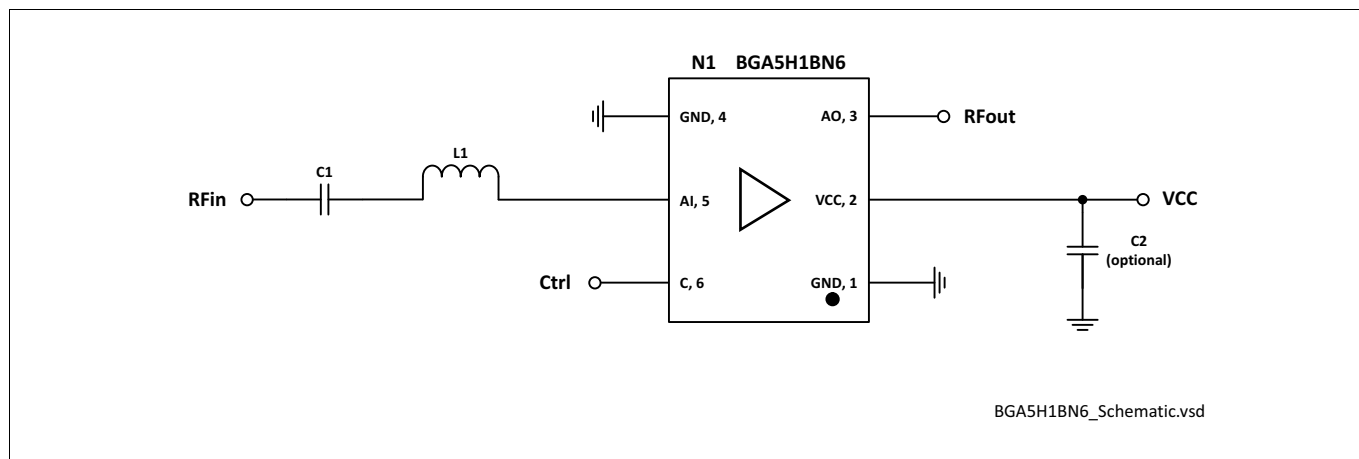


Figure 2 Application Schematic BGA5H1BN6

Table 5 Bill of Materials

Name	Value	Package	Manufacturer	Function
C1	1nF	0402	Various	Input matching
C2 (optional)	$\geq 1\text{nF}$	0402	Various	RF bypass ¹⁾
L1	3.6nH	0402	Murata LQW15 type	Input matching
N1	BGA5H1BN6	TSNP-6-10	Infineon	SiGe LNA

1) RF bypass recommended to mitigate power supply noise

A list of all application notes is available at <http://www.infineon.com/ltelna>

5 Package Information

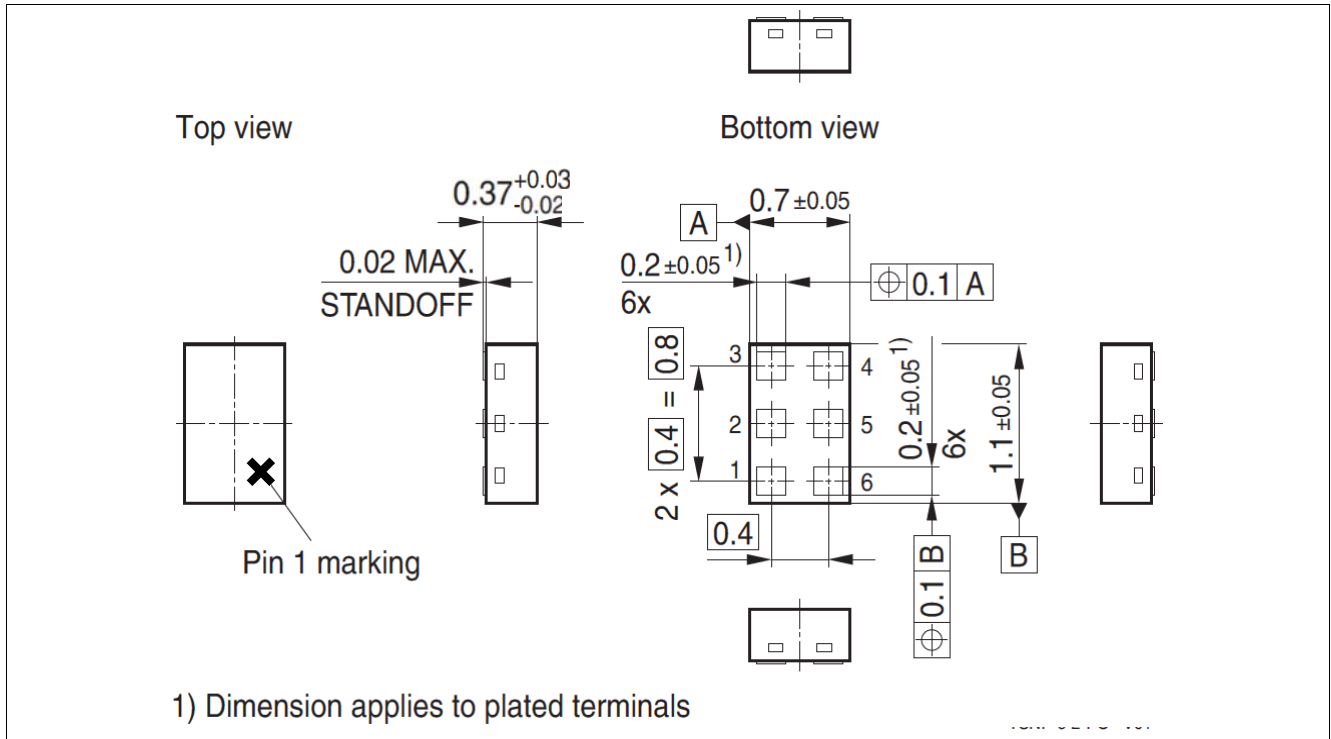


Figure 3 TSNP-6-10 Package Outline (top, side and bottom views)

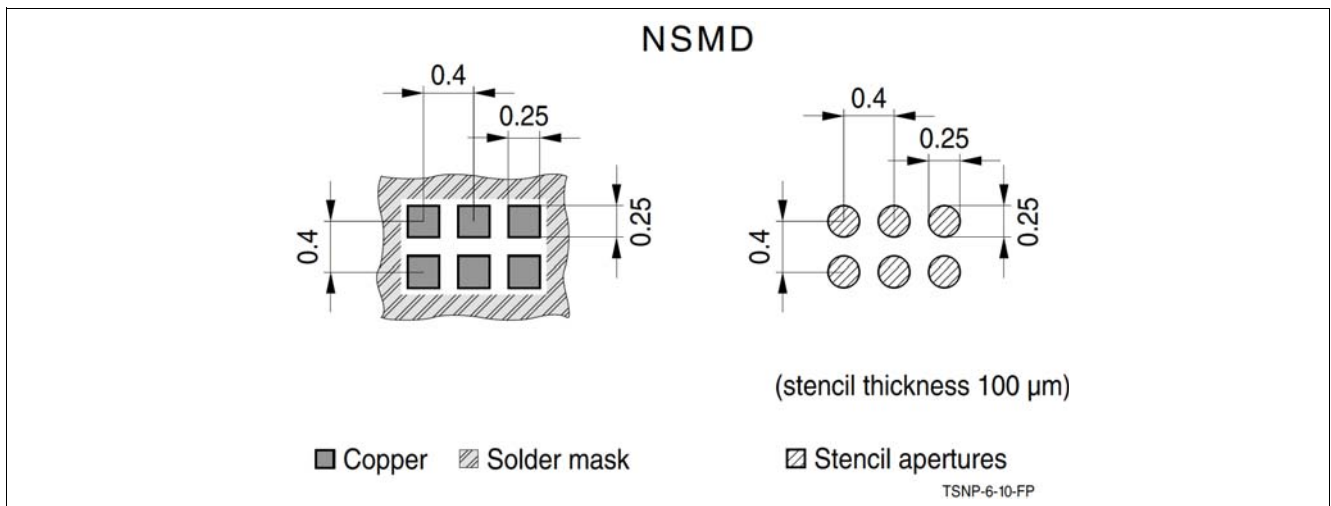


Figure 4 Footprint Recommendation TSNP-6-10

The diagram shows a 16-pin DIP package with pins numbered 1 to 16. A box highlights the pin 1 marking area, which includes a type code (a stylized 'L' shape), a monthly data code (a small square), and a pin 1 marking (an 'X').

- Type code
- Monthly data code
- Pin 1 marking

Month	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
01	a	p	A	P	a	p	A	P	a	p	A	P
02	b	q	B	Q	b	q	B	Q	b	q	B	Q
03	c	r	C	R	c	r	C	R	c	r	C	R
04	d	s	D	S	d	s	D	S	d	s	D	S
05	e	t	E	T	e	t	E	T	e	t	E	T
06	f	u	F	U	f	u	F	U	f	u	F	U
07	g	v	G	V	g	v	G	V	g	v	G	V
08	h	x	H	X	h	x	H	X	h	x	H	X
09	j	y	J	Y	j	y	J	Y	j	y	J	Y
10	k	z	K	Z	k	z	K	Z	k	z	K	Z
11	l	2	L	4	l	2	L	4	l	2	L	4
12	n	3	N	5	n	3	N	5	n	3	N	5

[illegible]

Revision History

Page or Item	Subjects (major changes since previous revision)
Revision 2.2, 2018-03-15	
5	Update Maximum Ratings

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