Automotive MOSFETs Current-Handling in Power-Applications

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Table of Contents

1 Introduction – Background and Motivation

In order to respond to the increased current requirements in high power applications, a lower package resistance is of high interest. The total MOSFET resistance is a consequence of the Si-chip resistance (depending on the technology and total die size) and package resistance (influenced by the bond-wire or Cu-clip, pins and tab-thickness). Therefore, the transition from bond-wire (Figure 1 a) to Cu-clip (Figure 1 b) has been proposed in some of the packages. By using Cu-clip a significant reduction in package resistance (with a factor of 3 times) can be reached compared to the bond-wire based packages.

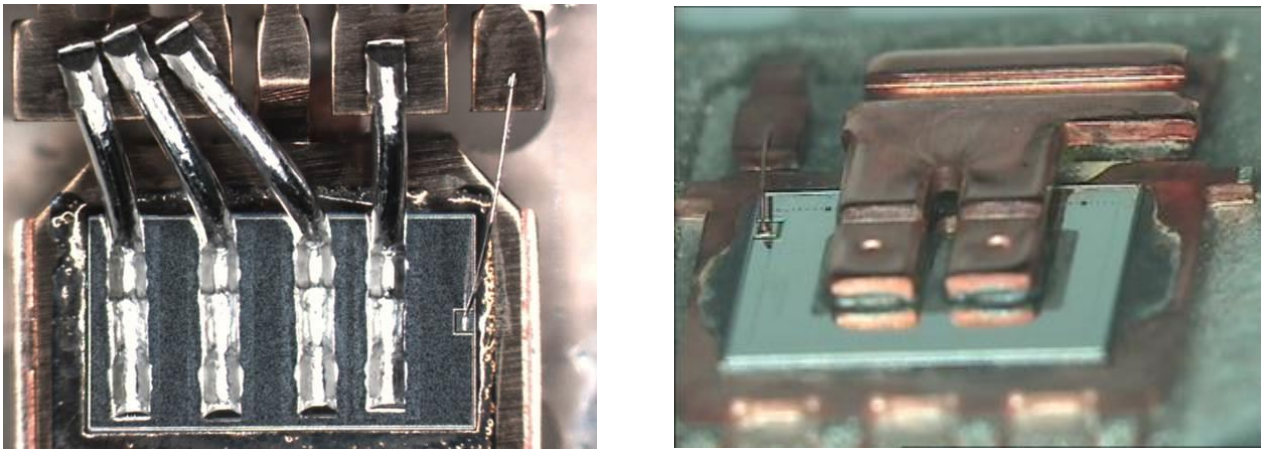
As shown to the AN2008-01 “Power Bond Technology for High-Current Automotive Power MOSFETs”, in the past the device current capability limitation was due to the bond-wire current ratings.

Due to the fact that modern packaging technologies moved from bond-wires to Cu-clips (in order to decrease the package-resistance), the device current capability limitation has switched from bond-wire limitations to the device interface areas and electromigration. This is especially important for the new power MOSFET technologies.

Presently, there are many device-producers companies and each of them has their own way on defining the device current ratings. The definition of the device current-capability is a very sensitive topic which is mainly depending on the company-standards.

Unfortunately, many companies are intentionally overrating their devices by not considering the whole current limitation chain when defining the device current capability. Therefore a difference of up to 3.5 times higher can exist in the current ratings when considering definition-standard of some competitors compared to Infineon approach.

In order to support customers during selection of the proper device (according to their requirements), it is very important to have a common and realistic approach on defining the device current ratings. This application note is proposed to understand and to be aware of the details regarding the current limitation chain from device-level and application-level standpoint.



(a) Bond-Wire based package **(b) Cu-Clip based package**

Figure 1: The device internal structure for a package based on (a) bond-wires and (b) Cu-clip

2 Device Current Capability

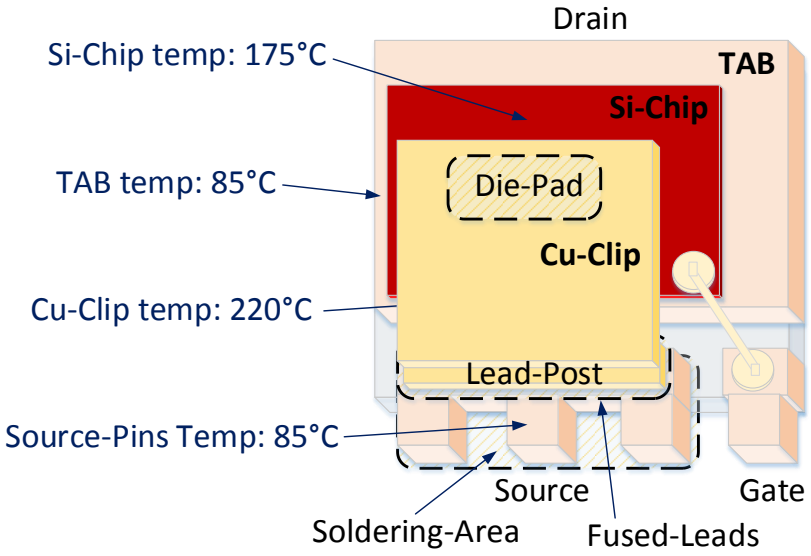


Figure 2: The internal structure of the power MOSFET device and the main parts responsible for device current capability

The device-level current capability depends on the following main factors:

- Si-Chip current limitation
- Cu-Clip current limitation
- Die-Pad, Lead-Post and Soldering area current limitation
- Current density and Electro-Migration

The internal structure of the automotive MOSFET (based on leadless-package) is presented in Figure 2 where it can be clearly seen the main components which define the device current limitations.

It is worth mentioning that the fused-leads concept introduced by Infineon improves the device current ratings.

A short description of the main current limiting factors is presented below.

2.1 The silicon (Si) chip current limitation

The Si-chip current rating (I_{D_Chip}) is defined by the MOSFET dissipated power via the thermal path (1) which leads to a junction temperature rise from the case temperature of T_C=25°C (kept constant) to the maximum allowed junction temperature of T_{J_max}=175°C. Therefore, considering the device maximum allowed power losses dissipation and the on-state resistance, the Si-chip maximum allowed current is defined in (2).

$$P_{Loss\_tot} = \frac{T_{J\_max} - T_c}{R_{thJC}} \quad (1)$$

$$I_{D\_Chip} = \sqrt{\frac{P_{Loss\_tot}}{R_{DSon\_175℃}}} = \sqrt{\frac{T_{J\_max} - T_C}{R_{thJC} * R_{DSon\_175℃}}} \quad (2)$$

Where:
P_{Loss_tot} – device power loss dissipation,
T_C – device case temperature,
T_{J_max} – device junction temperature,
R_{thJC} – junction-to-case thermal resistance,
R_{DSon_175C} – device on-state resistance at an operating temperature of 175°C,
I_{D_Chip} – maximum allowed device Si-chip current.

Comparing the Competitor X and IFX devices, the Si-chip current limitation for a junction temperature of 175°C is presented in Table 1. In case of the Competitor X it can be clearly seen that the Continuous Drain Current (I_D) stated in the datasheet is equal with the obtained Si-chip current limitation ($I_{D\_Chip175°C}$). This means that the Competitor X is not considering the main limitations in terms of Cu-clip and electromigration. In the following sections the impact of these limitations in the device current capability is explained.

Table 1: The IFX versus Competitor X Si-Chip current limitation

Parameters	Product name	
	IFX S308	Competitor X
Junction-to-case thermal resistance R_{thJC}	2.1 K/W	2.2 K/W
Device on-resistance $R_{DSon\_175°C}$	5.1 mΩ	6.48 mΩ
Device power loss dissipation P_{Loss_tot}	72 W	68 W
Maximum allowed Si-chip current $I_{D\_Chip175°C}$	120 A	102 A
Continuous Drain Current I_D	40 A	102 A

2.2 Device Copper-Clip current limitations

The Cu-clip current limitation has been determined by a model which considers the lead-frame geometry, the Cu-clip geometry (the cross-section area and the distance from the die-pad to the lead-post) and the maximum allowed temperature of the Cu-clip (which is limited by the influence on the molding compound material decomposition if the Cu-clip temperature exceeds 220°C). The temperature target (Figure 2) for the Si-chip, Cu-clip, Tab and source pins are also considered in the model for the calculation. All this defines the current capability of the Cu-clip of the power MOSFET.

As a final result, in order to decrease the package resistance, the Cu-clip current capability is higher than the Si-chip. Therefore the Cu-clip das not represent a limitation in device current capability.

2.3 Die-Pad, Lead-Post and Solderable area current limitations

According to IFX standards, the current density limitations (in order to avoid electro-migration issues at high current and high temperature operation) are defined up to be 50 [A/mm^2]. Therefore this value will be considered for further calculations according to the connection areas. The current limitation of the device is therefore defined as follows:

- Die-Pad – connection area of the Cu-clip to the Si-chip.
- Lead-Post – connection area of the Cu-clip to the Source-Pins.
- Soldarable area – represents the common connection area of the source pins to the PCB pad.

The total die-pad area of the device will introduce a first current limitation lower than the Si-chip limit.

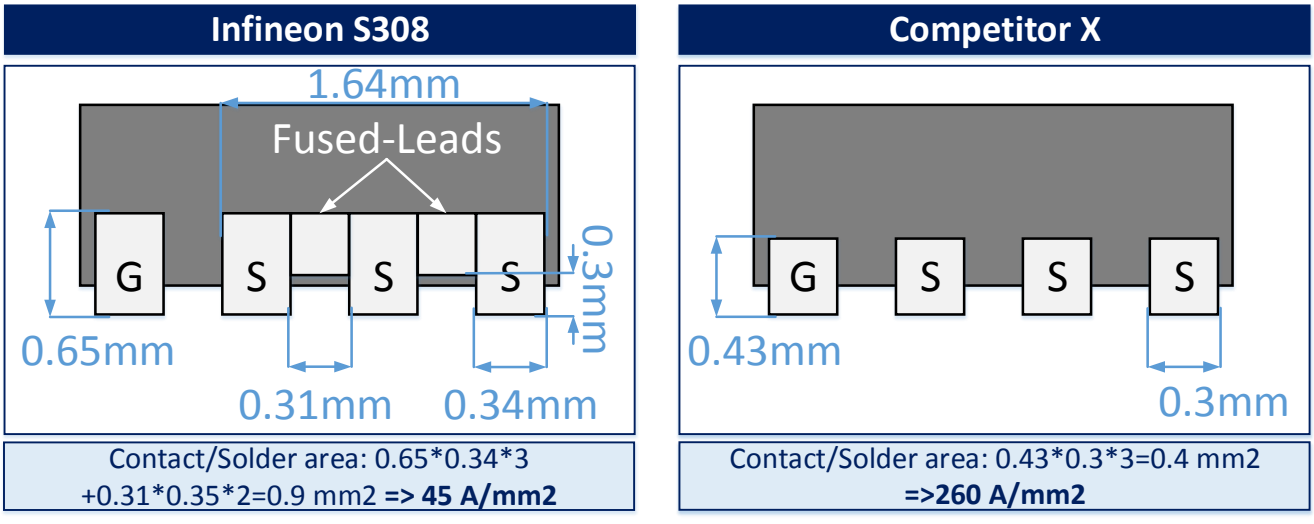
Furthermore, due to the fused-leads concept (Figure 2) introduced by Infineon, the IFX-devices offers a contact area of the Lead-Post (Cu-Clip to the Source-pins) and a Source-Soldarable area (of the Source-Pins to the PCB-pad Figure 3) of >2 times higher than the Competitor X device, which will have a positive impact increasing the IFX-device current capability.

By considering the whole chain of limitations, the IFX-device has a current capability of 2 times higher than the Competitor X device.

Moreover the Competitor X is stating a 2.5 times higher current ratings (Table 2) than the IFX-device but with one half (50 % lower) Source-Connection area. By considering the stated device current capability and the Source-Connection area, the Competitor X device (260 [A/mm2]) will end-up with a current density of 6 times higher than the IFX device (45 [A/mm^2]). All this determines a higher current density, increasing the risk of electro-migration at high current and high temperature operation for the Competitor X device.

Table 2: Main parameters comparison of the S308 IFX versus Competitor X device

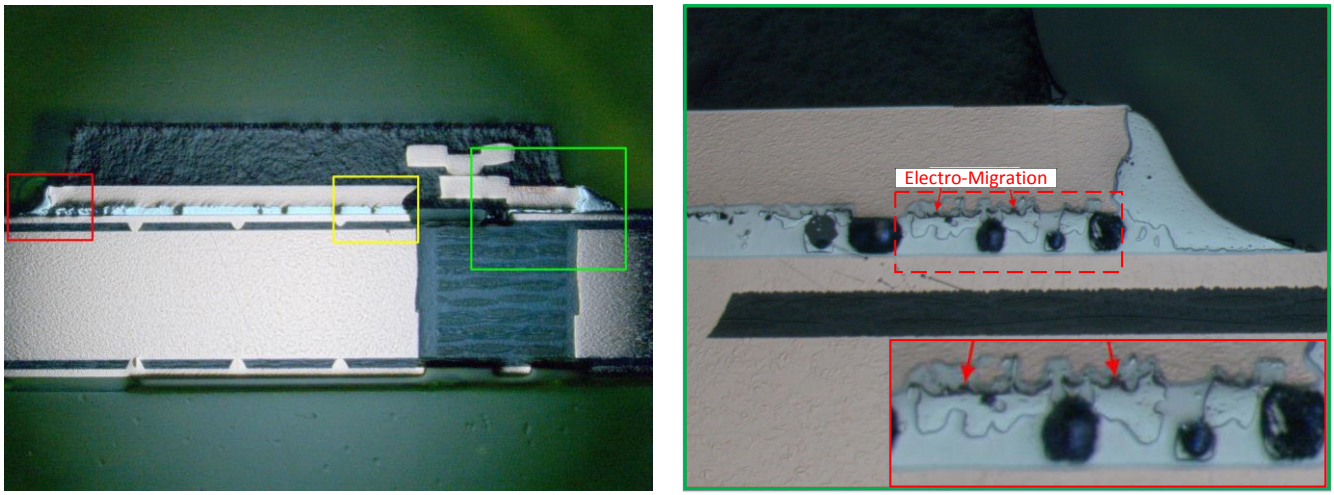
Product name		IFX S308	Competitor X	Improvement
Continuous Drain Current I_D		40 A	102 A	2.5 X
ON-resistance	V_G= 10V	2.8 mΩ	3.6 mΩ	30%
	V_G= 4.5V	3.8 mΩ	5.1 mΩ	
Thermal resistance		2.1 K/W	2.2 K/W	-
Solderable area		0.9 mm^2	0.4 mm^2	2.3 X
Current Density		45 A/mm^2	260 A/mm^2	6 X



(a) Soldering area of IFX device **(b) Soldering area of Competitor X device**

Figure 3: Total Source-Soldering area of the IFX versus Competitor X device

2.4 Current density and Electro-Migration



(a) Cross-section area of the device

(b) Zoom with the area affected by Electro-Migration

Figure 4: The Electro-Migration impact in MOSFET source-pins connection

In order to emphasize the actual effect of electro-migration when having high temperature and high current operation, a test at high-current (2 times higher current density than the maximum allowed by the IFX standards) and high-temperature operation has been performed with an IFX device. The main objective is to emphasize the impact of electro-migration in the source pins to PCB connection interface due to the high-current operation.

After performing the test, the device was analyzed. A cross-section area of the device is shown in Figure 4 (a) and a zoom to the source-to-PCB connection interface is presented in Figure 4(b). According to the obtained results it can clearly be seen that due to 2 times higher-current density and high temperature operation, the copper-electrons are migrating through the soldering-material (Figure 4). This will have a negative impact on solder joint reliability and could result in soldering-cracking and voids. With continued exposure to the described conditions, contact loss between the device-pins and PCB can result leading to failure of the device to PCB interface.

Therefore, special attention has to be paid to the electro-migration impact when defining the device current capability of the device.

2.5 Device current capability definition according to IFX-standards

According to the obtained results, the IFX way to define the device current capability is to consider the whole limitation-chain encountered by the current flow through the device as shown in Figure 5 (a): Si-Chip -> Die-Pad -> Cu-Clip -> Lead-Post -> and Soldering area. The Competitor X way of defining the device current capability is to consider only the Si-Chip current limitation (Figure 5 (b)), without considering the main limitation in the chain. In Table 3 the device current capability is presented according to IFX and Competitor X definition standards.

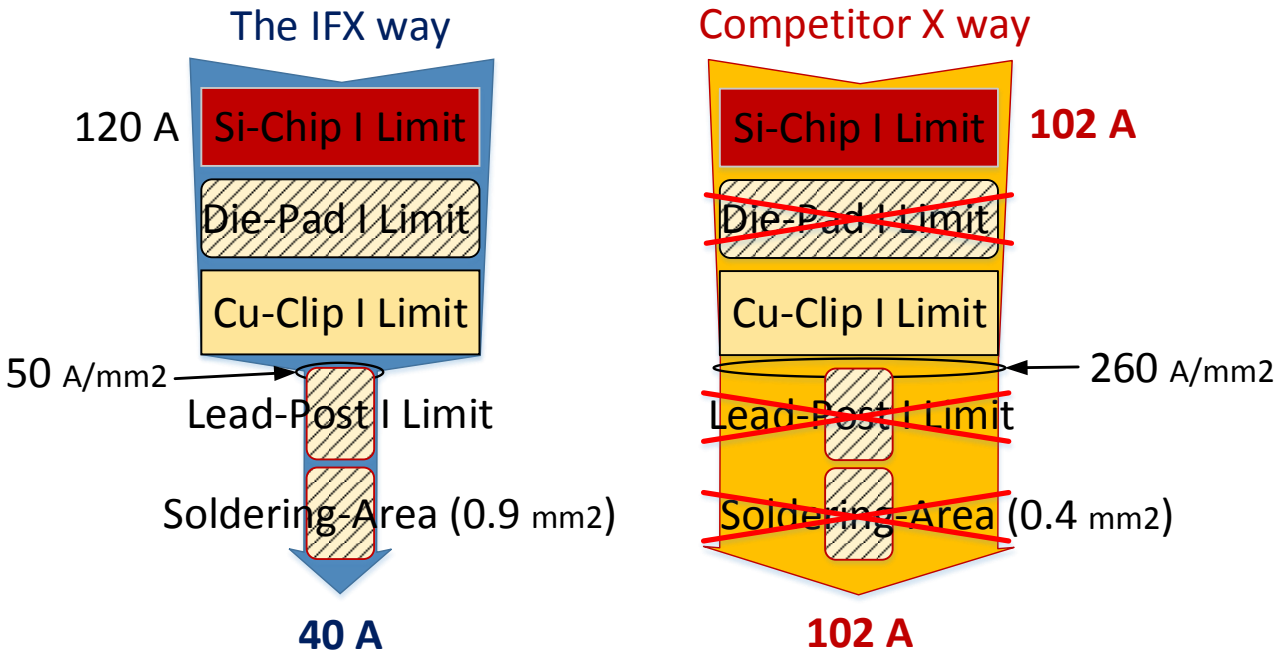
According to IFX definition standard (considering the whole current limitation chain) the Competitor X device would have a continuous drain current of 20 A.

Finally, by considering the obtained results it may be concluded that the Competitor X Continuous Drain Current (I_D) stated in the datasheet is equal to the Si-chip current limitation ($I_{D\_Chip175°C}$). Some competitors are over-rating their device current ratings, requiring special attention in analyzing the

MOSFET-device before selecting it in order to avoid electro-migration problems due to high-current and high-temperature operation.

Table 3: The device current capability according to IFX and Competitor X definition standards

Product	Device Current Capability		Improvement
	S308	Competitor X	
Competitor X definition standard	120 A	102 A	-
IFX definition standard	40 A	20 A	2X



(a) IFX current capability definition **(b) Competitor X current capability definition**

Figure 5: Device current capability limitation-chain definition according to IFX (a) and Competitor X (b) standards

3 Device current limitations in automotive-power applications

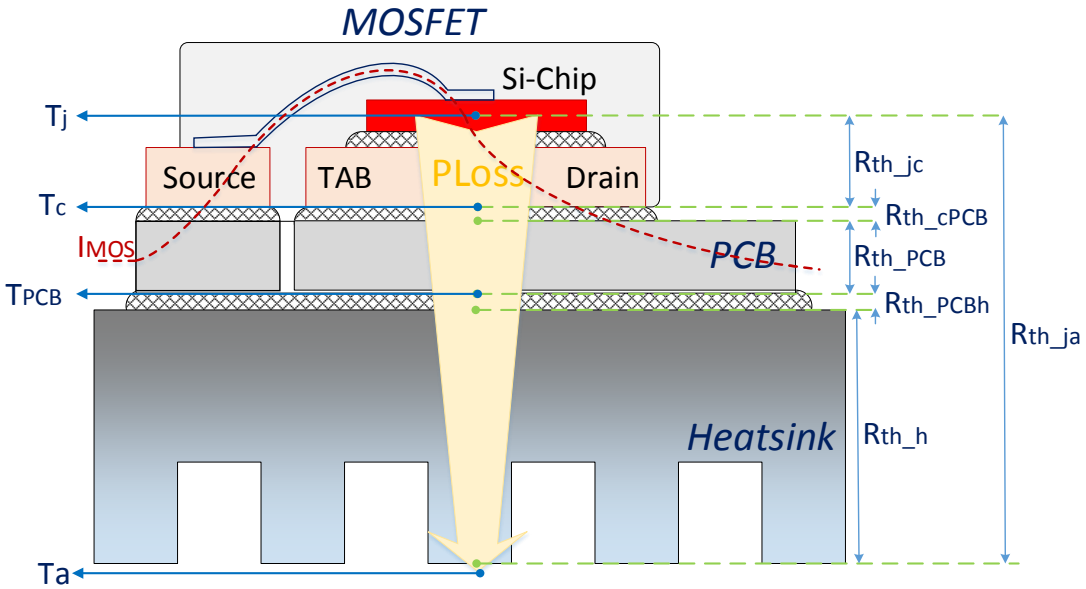


Figure 6: Power device thermal chain from junction to ambient in automotive application

In normal operation the device current level is limited by the junction temperature which is increasing with the power losses and thermal resistance as shown in (3). If the junction-to-ambient thermal resistance has a lower value, higher power losses are allowed to reach the same junction temperature (the device current may be increased).

$$P_{Loss} = \frac{T_J - T_a}{R_{thJa}} \tag{3}$$

The device current capability in automotive power-applications is depending on the following main factors:

- Device power losses – the device total power losses are composed of the conduction losses and switching losses. For Electric Power Steering (EPS) application the typical switching losses have a contribution of 30 % to the total power losses. Therefore, the main focus in this specific case is on the device conduction losses. The conduction losses are directly related to the device on-state resistance R_{DS_on} which is mainly depending on the Si-chip resistance and on the device-package resistance.
- Junction-to-ambient thermal resistance – as shown in Figure 6, the junction to ambient thermal resistance is depending on the junction-to-case R_{thJC} and on the case-to-ambient thermal resistance R_{thCA}. The junction-to-case thermal resistance R_{thJC} (defined by the Si-chip size) has a low contribution in the total thermal resistance chain (Figure 6) from the junction-to-ambient. The R_{thCA} has a large variation and mainly depends on the device packaging tab size and the cooling concept.

In order to understand the impact of the above mentioned parameters, an example on how to calculate the device current capability in Electric Power Steering (EPS) applications (Figure 7) is further presented.

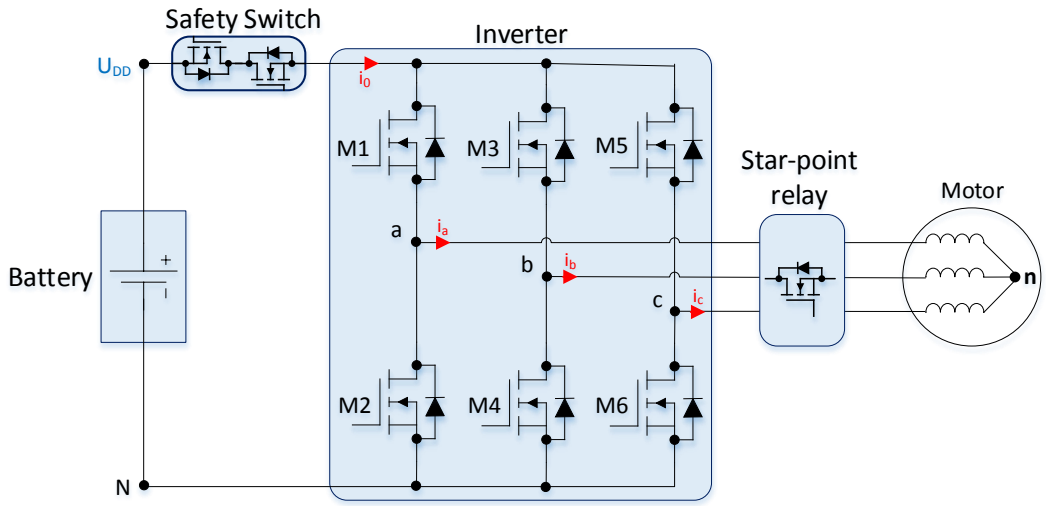


Figure 7: Schematic of the Electric Power Steering application

The schematic of the EPS-application is shown in Figure 7 and the main system specifications are given in Table 4.

Table 4: Electric Power Steering (EPS) system specifications

System parameters	Symbol	Value
Inverter Power	P [kW]	0 to 1.8
DC-link voltage	VDD [V]	14
RMS output current	I [A]	0 to 70
Switching frequency	fSW [KHz]	20

As shown in Table 5, according to the device-packaging it is possible to reach a device ON-state resistance R_{DS_on} which may vary from 2.8 mΩ in S308 package, to 0.7 mΩ in TOLL package for 40V IFX portfolio.

Table 5: The IFX best-in-class RDS_on according to device packaging for automotive products

Device Packaging Type			$R_{DSon\ min}$ [mΩ]
Leads-Less	1	S308 (TSDSON 8)	2.8
	2	SS08 (TDSON 8)	2
	3	TOLL (H-PSOF)	0.7
Leads	4	DPAK (TO252-3/5)	2
	5	D2PAK (TO263-3/5/7)	0.87

The junction-to-ambient thermal resistance and the package tab-size play a key role on dissipating the power losses from the device. This value also varies according to the device packaging (Table 6) from 20 [K/W] in S308 to 3 [K/W] in TOLL package. These are typical values which may be found in applications which are using devices with these packages.

Table 6: The device junction-to-ambient thermal resistance in automotive-applications according to device packaging

Device Packaging Type			Thermal resistance RthJA [K/W]	Tab Size of the Package [mm^2]	Tab Thickness of the Package [mm^2]
Leads-Less	1	S308 (TSDSON 8)	20	4	0.2
	2	SS08 (TDSON 8)	10	18	0.25
	3	TOLL (H-PSOF)	3	50	0.5
Leads	4	DPAK (TO252-3/5)	5	29	0.9
	5	D2PAK (TO263-3/5/7)	3.5	64	1.3

All the above mentioned parameters were considered in order to calculate the required R_{DS_on} according to the application power and device packaging.
A short explanation on how to calculate the required R_{DS_on} according to device operating conditions and device packaging is given in the following.
In order to calculate the device current capability for the EPS application the eq. 4 will be used:

$$P_{Loss} = \frac{T_J - T_a}{R_{thJa}} \Rightarrow R_{DSon} \cdot I^2 \cdot Ct \cdot fP_{SW} = \frac{T_J - T_a}{R_{thJa}}$$
$$R_{DSon25°C} = \frac{T_J - T_a}{R_{th\_Ja} \cdot I^2 \cdot Ct \cdot 1.3} \quad (4)$$

Where:

$$R_{DSon}(T_J) = R_{DSon25°C} \cdot \left(1 + \frac{\propto}{100}\right)^{T_J - 25°C} \Rightarrow Ct = \left(1 + \frac{\propto}{100}\right)^{T_J - 25°C} \quad (5)$$

α=0.4 is the technology related constant for power MOSFETs,
Ct- is the temperature coefficient when converting the R_{DSon} from 25°C to the Tj value.
fP_{SW} – the impact of switching losses in the total power losses

The ambient temperature of 125°C and the junction temperature of 150°C are considered as a worst case scenario for the calculations.
The power (current) is increased until the required MOSFET R_{DS_on} reaches the minimum allowed value according to the device-packaging technology. In this way the maximum allowed power (current) may be determined according to the device packaging and the device R_{DS_ON}.
Figure 8 shows the R_{DS_on} requirements according to device-package and application power ratings by considering the best in class 40V devices from IFX portfolio. The same idea is presented in Figure 9 according to the device current capability.

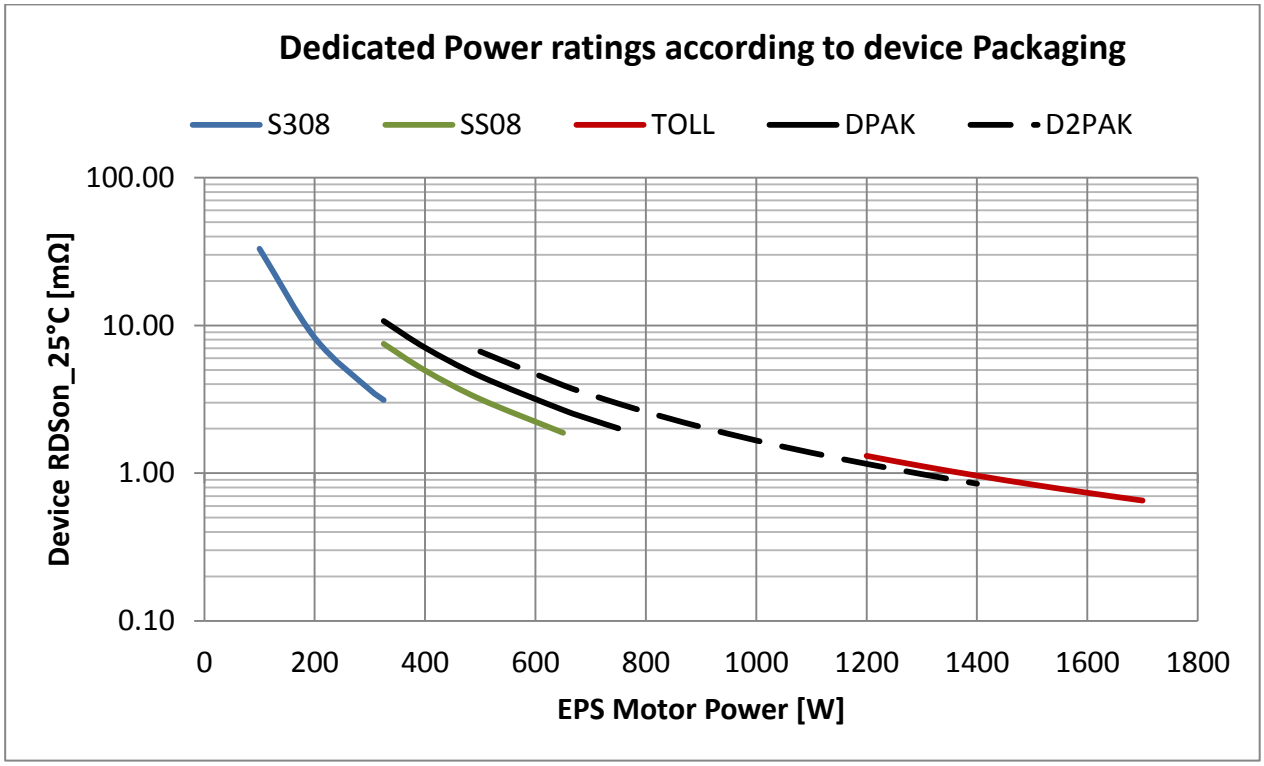


Figure 8: The device R_{DS_on} requirements according to package and application power ratings by considering the best in class 40V IFX portfolio

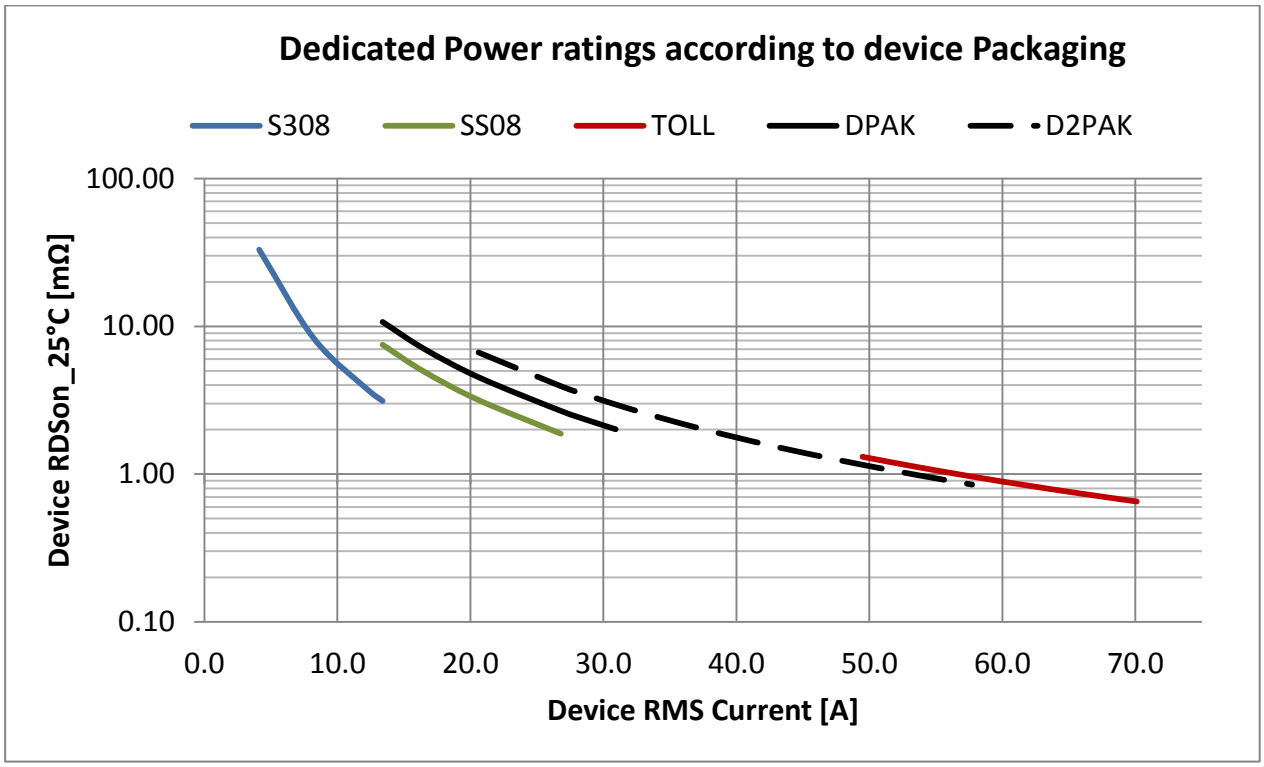


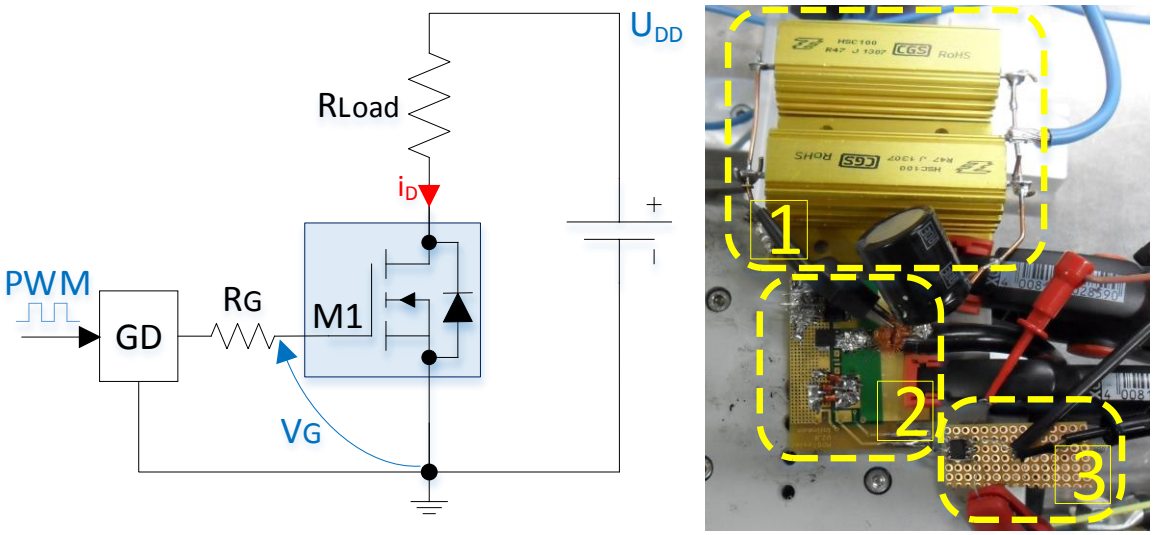
Figure 9: The device R_{DS_on} requirements according to package and application current ratings by considering the best in class 40V IFX portfolio

According to the device packaging and the best in class R_{DS_on}, the maximum current capability of the IFX devices is presented in Table 7 for EPS application.
This approach may be used in selecting the devices according to the application power ratings and device-packaging.
It is worth to mention that IFX portfolio is based on two type of packages, the leaded (e.g. D2PAK) and lead-less devices (e.g. TOLL). The new generation of lead-less devices offers a larger portfolio of optimized-for-power packages. Therefore the customer has many options on selecting the proper device according to their specifications.

Table 7: Device current ratings according to device packaging for the IFX products in EPS application

Device Packaging Type			Device current capability
Lead-Less	1	S308 (TSDSON 8)	15 A
	2	SS08 (TDSON 8)	28 A
	3	TOLL (H-PSOF)	70 A
Lead-Based	4	DPAK (TO252-3/5)	30 A
	5	D2PAK (TO263-3/5/7)	60 A

4 Device current capability – Laboratory Measurements



(a) Test-board schematic (b) Hardware implementation

Figure 10: Test board schematic (a) and hardware implementation (b): 1 – Load resistors, 2 – Test-board with the MOSFET device, 3 – Gate-Driver.

A test setup has been developed in order to compare the current capability of the IFX versus Competitor X device. The devices used in this study case are different than the ones presented in the Section 2 of the application note. The test-board schematic (a) and the hardware implementation (b) are presented in Figure 10.

The target of the experiment is to measure the length of time it takes for the device to heat-up to a certain case temperature. Therefore, as shown to Figure 10, the test setup consists of the test-board and the Infra-Red (IR) thermal camera. The IR-Camera is used to measure and record the device temperature at different operating conditions.

The laboratory test conditions for the devices are presented in Table 8. There are two main test conditions which are performed, first one at 20 kHz operation (typical EPS-applications) and the second one at 100 kHz operation (typical DC/DC converter application).

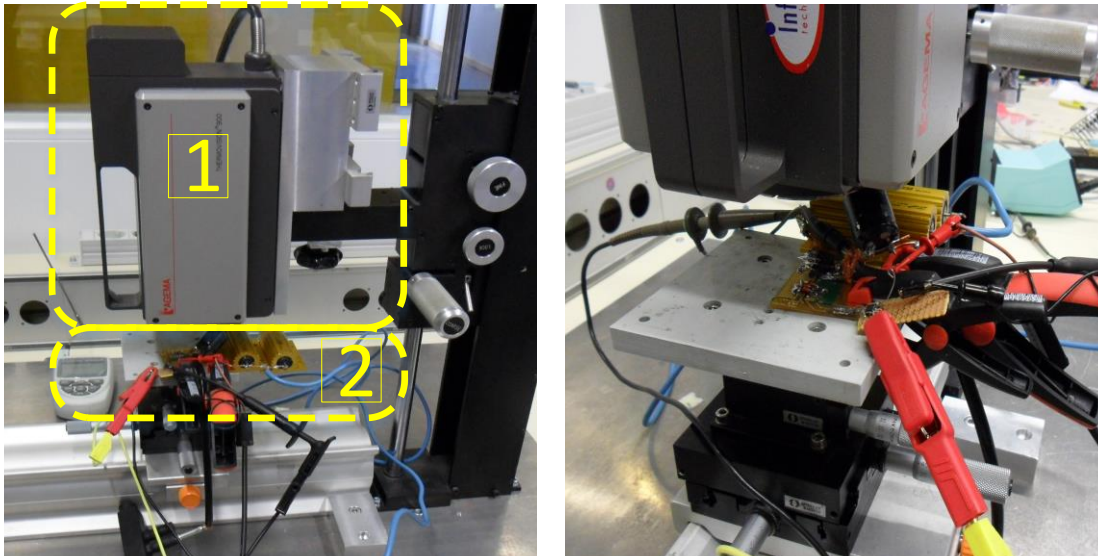


Figure 11: Test-setup laboratory implementation: 1 – Thermal camera, 2 – Test-board

Table 8: Test conditions for IFX versus Competitor X devices

Test No.		Devices	Test Conditions				App.
			DC-Voltage	Load Current	Duty Cycle	Switching frequency	
Test 1	1.1	IFX	VDD=12V	IL=67A	50%	20 kHz	EPS
	1.2	Competitor X					
Test 2	2.1	IFX				100 kHz	DC/DC
	2.2	Competitor X					

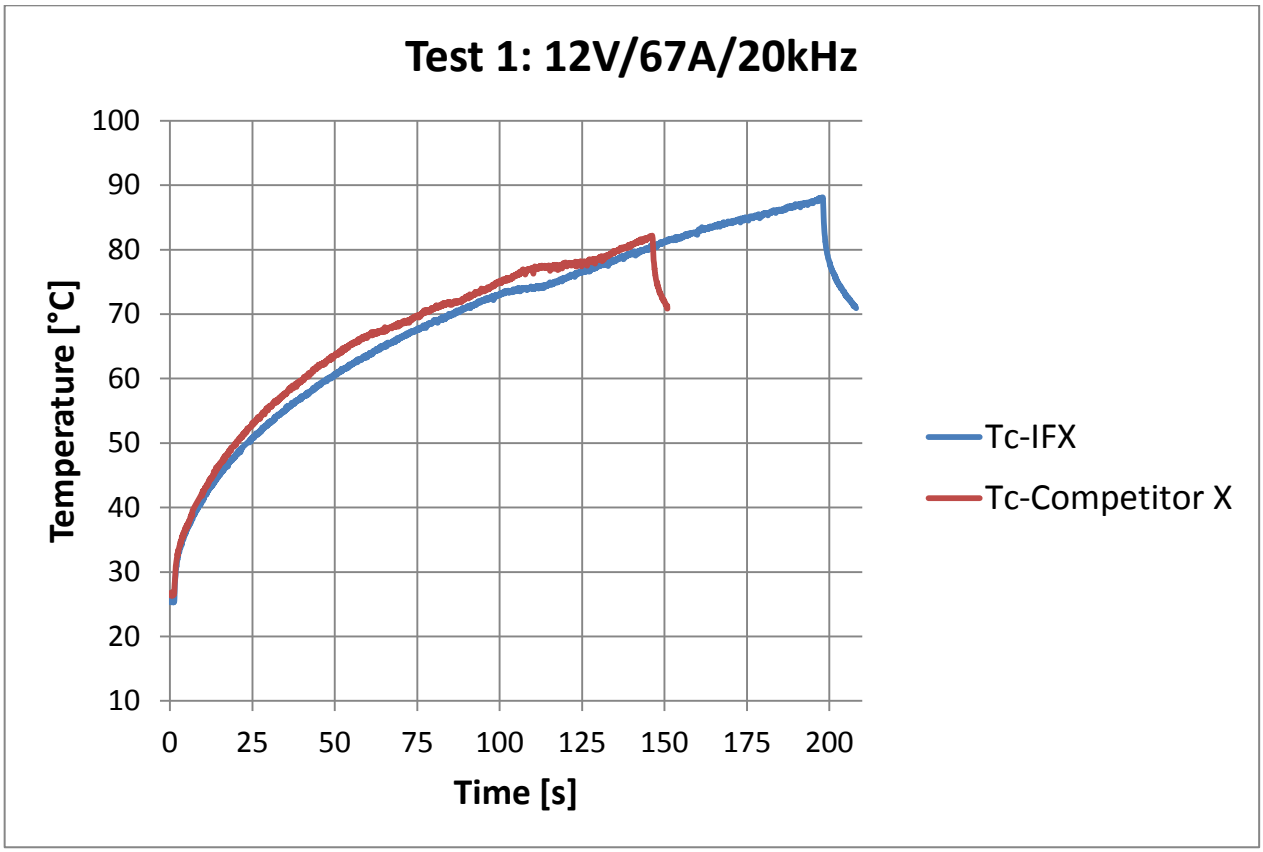


Figure 12: Thermal-camera measured temperature for IFX versus Competitor X device by considering the Test 1 operating conditions

The only difference in the test conditions is the switching frequency which is changed from 20 kHz (Test 1) to 100 kHz (Test 2). The used gate-driver parameters are: gate resistance R_G=3 Ω and gate voltage V_G=10V.

According to the obtained results from Test 1 (Figure 13) it can be stated that even though Competitor X device has a 30 % lower R_{DS_on} (due to a 40% larger chip-area), the switching losses are much higher than the IFX device. Therefore in the Test 1 operating conditions for 20 kHz, the higher switching losses are compensating the difference in terms of R_{DS_on} between the devices. The temperature trend of both devices is similar with a slightly advantage for IFX device (Figure 12). Based on the obtained results it can be stated that both devices have a similar current rating capability for the EPS-applications (Test 1).

If the switching frequency is further increased to 100 kHz according to Test 2, the IFX device temperature rising is much slower than the Competitor X device. In Figure 13 it can be seen a 60% difference between temperature rising time of IFX and Competitor X device. This it means that the IFX device has lower power-loss dissipation, thus it can operate at a higher current capability than the Competitor X device in DC/DC-converter applications (Test 2 - 100 kHz switching frequency). It is worth to mention that the Competitor X device has a double current density therefore this device is prone to electromigration issues at high-current and high-temperature operation.

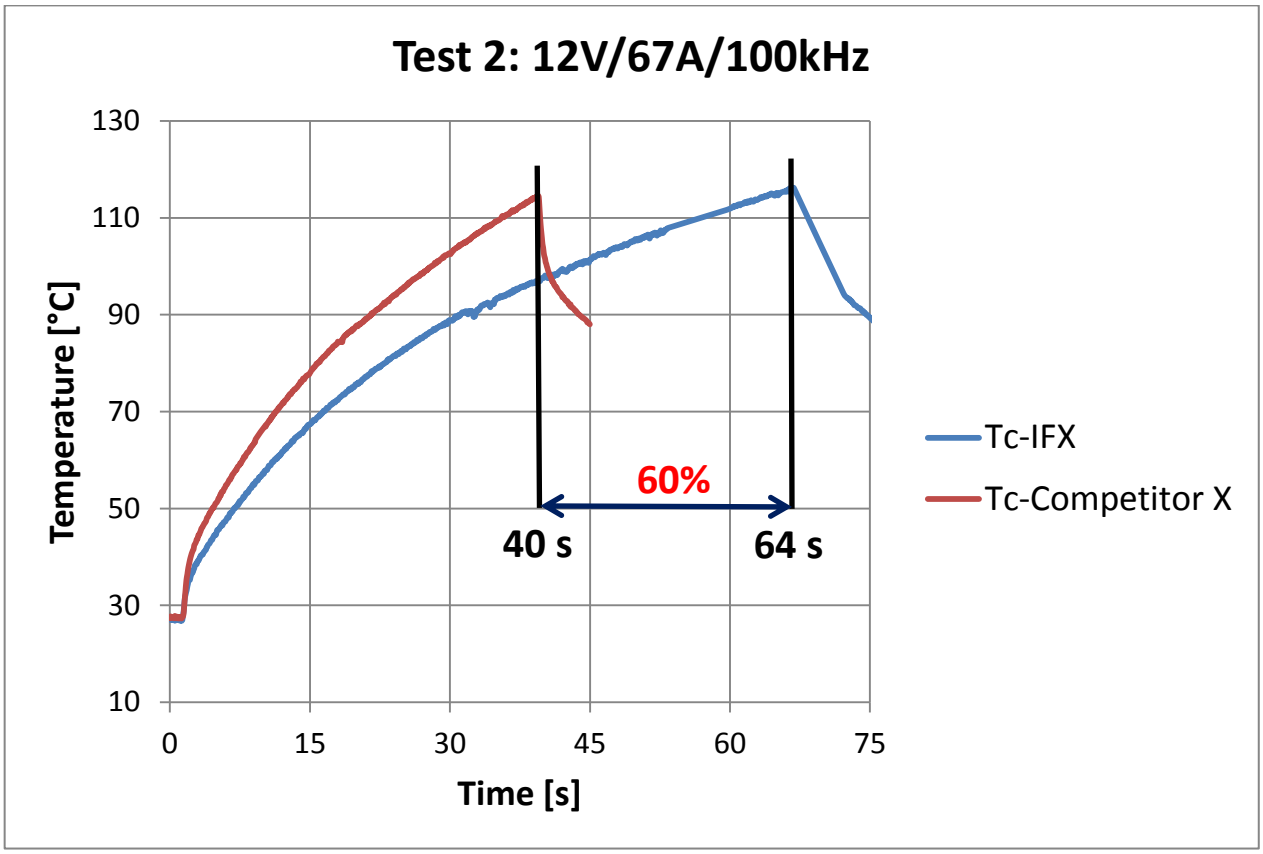


Figure 13: Thermal-camera measured temperature for IFX versus Competitor X device by considering the Test 2 operating conditions

An example of the thermal IR-camera measured device case temperature is presented in Figure 14.

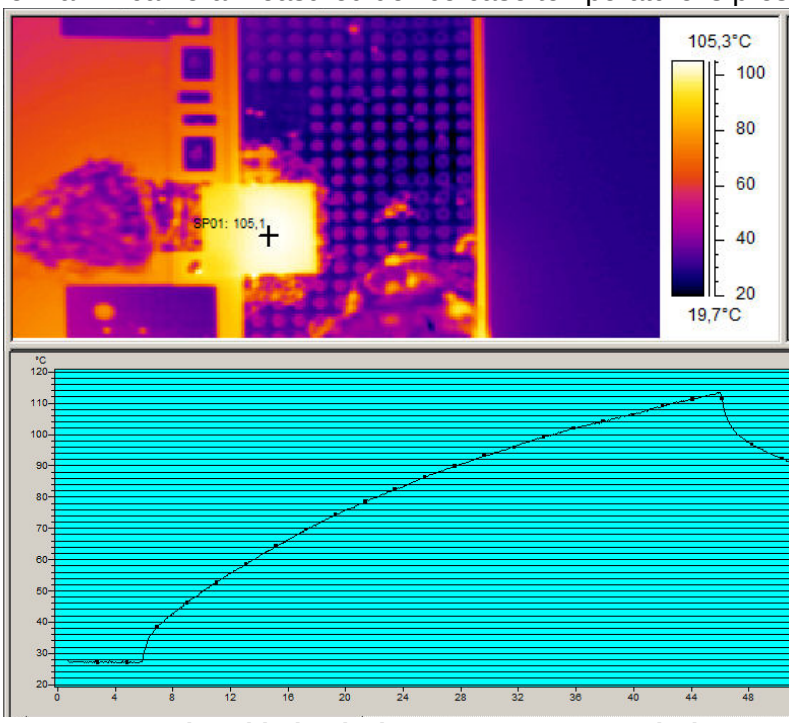


Figure 14: Thermal IR-camera results with the device-case temperature (Tc) measurements

5 Conclusions

This application note is proposed in order to explain the current limitation chain for power MOSFETs from device-level and application-level standpoint.

Based on the obtained results it may be stated that some competitors are overrating their devices by not considering the entire current limitation chain (encountered by the current flow through the device) when defining the device current capability. Therefore a difference is evident of up to 3.5 times higher current ratings when considering the definition-standard of some competitors compared to Infineon approach.

In Table 3 the device current capability is presented according to IFX and Competitor X definition standards. According to IFX definition standard (considering the whole current limitation chain) the Competitor X device would have a continuous drain current (20 A) equal to half of the IFX device.

Furthermore, a method for calculating the device current capability in automotive applications for IFX power MOSFETs by considering the device packaging is also introduced. According to the device packaging and the best in class R_{DS_on}, the maximum current capability of the IFX devices is presented in Table 7 for EPS application.

In order to determine the Competitor X device current capability, a comparison with the IFX best in class device has been done. By knowing the IFX-device thermal limitations, a test setup has been developed in order to compare the IFX device with the Competitor X device.

Two main test conditions were performed according to Table 8. Based on the obtained results, it can be stated that the Competitor X device has similar power ratings to IFX device for 20 kHz based applications (eg. EPS). For the applications which requires a higher switching frequency operation (eg. DC/DC converter), the IFX device has a higher current capability than the Competitor X device.

It is worth mentioning that the Competitor X device has a double current density therefore this device is prone to electro-migration issues at high-current and high-temperature operations.

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