IR43xx MERUS™ MCM Class D amplifier IC

Functional description

About this document

Scope and purpose

The purpose of his document is to provide a functional description and design guide to the IR43xx series MERUS™ MCM Class D ICs.

Intended audience

Audio amplifier design engineers

Table of Contents

1 General description

The IR43xx is a Class D amplifier IC integrating a PWM controller and digital audio MOSFETs. Thanks to application optimized MOSFETs co-packed with a controller IC, the IR43xx operates without a mechanical heatsink attached in typical music playback applications. High voltage ratings and noise immunity in the controller IC ensure reliable operation over various environmental conditions. A small 5x6mm (IR43x1) or 7x7 mm (IR43x2) PQFN package enhances the benefit of smaller size realized by the Class D topology.

The internal protections monitor the status of the power supplies and load current in each MOSFET. All of the protection features are internally programmed.

For the convenience of a half bridge configuration, the differential input analog PWM modulator and protection logic interface are floated from the main power supplies.

The IR43xx implements click noise reduction to suppress unwanted audible noise during PWM start-up and shutdown.

The dual channel IR43x2 features status output reporting for clipping detection and fault output detection.

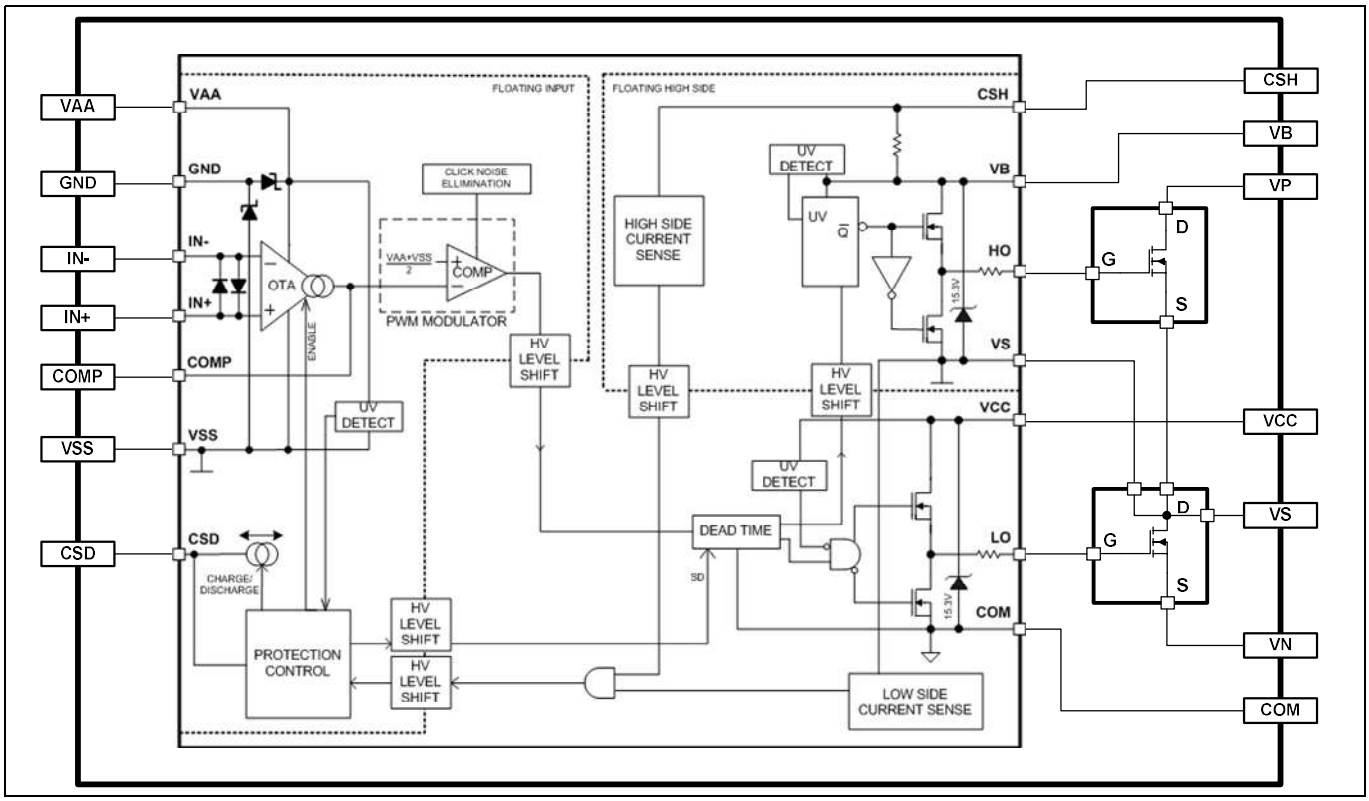


Figure 1 Functional block diagram of single channel IR43x1

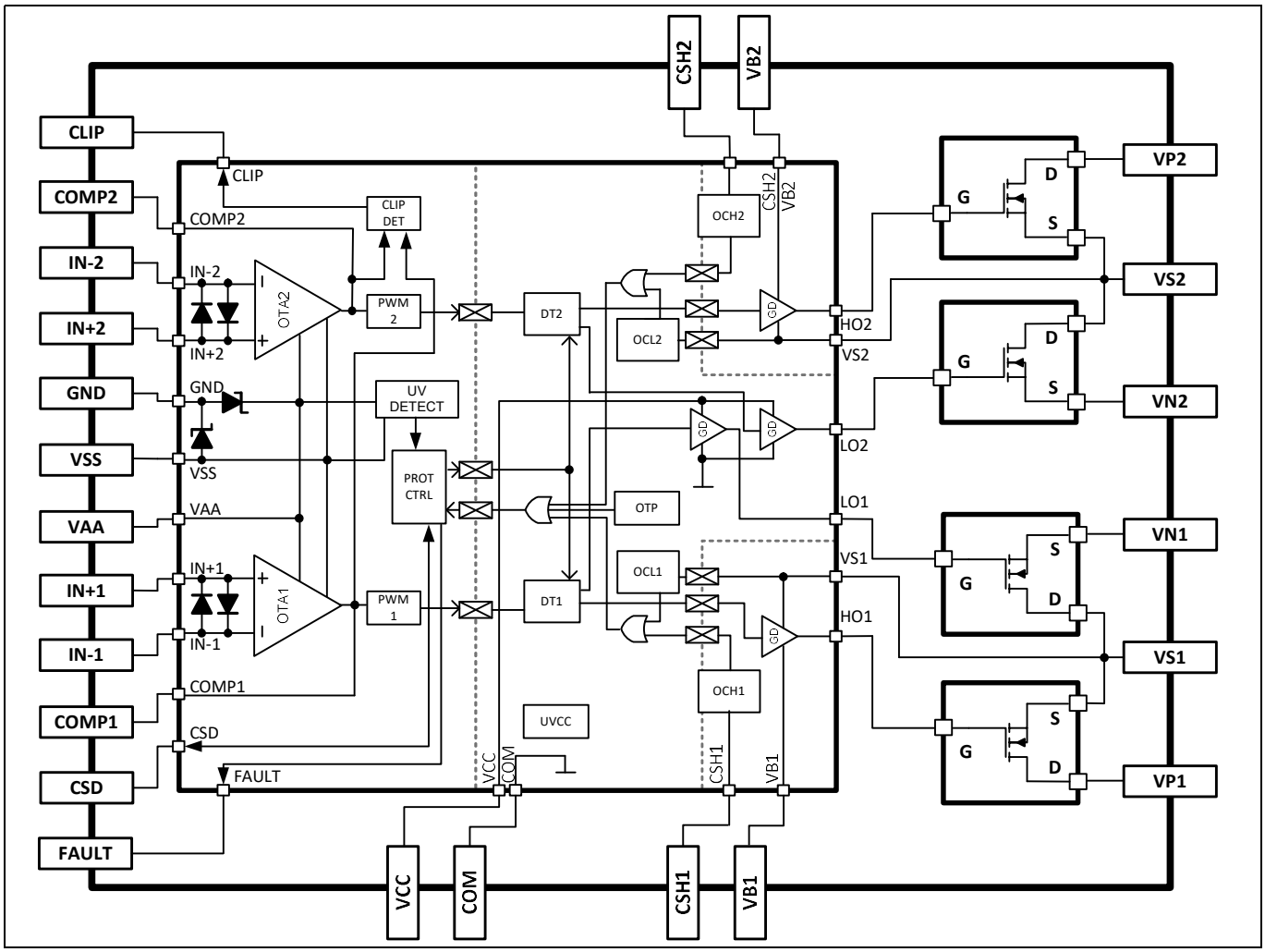


Figure 2 Functional block diagram of dual channel IR43x2

2 Typical implementation

The IR43xx can be designed as single ended or BTL output, using single or split power supply. Here are examples of typical configurations.

A configuration for single ended input with split power supply sets the base example. The front end section refers to GND which is common to speaker output GND.

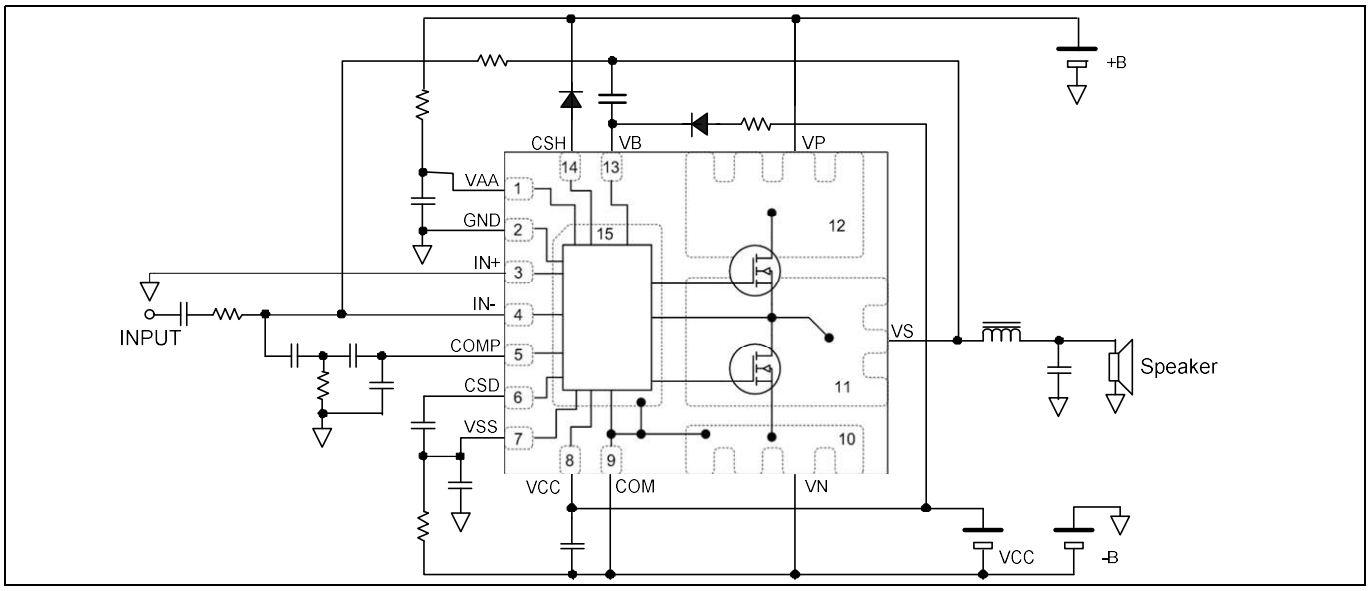


Figure 3 Typical application circuit with split power supply

The single supply configuration uses a virtual GND which sits in the middle of the power supply rail. The front-end section of the amplifier refers to the virtual GND as a reference. This medthod uses differential input to receive a input signal from a different voltage potential. It is recommended to allow input capacitors to fully settle to steady state values before releasing the CSD pin to start PWM oscillation. The load current and inductor ripple current flows through bus splitting capacitor.

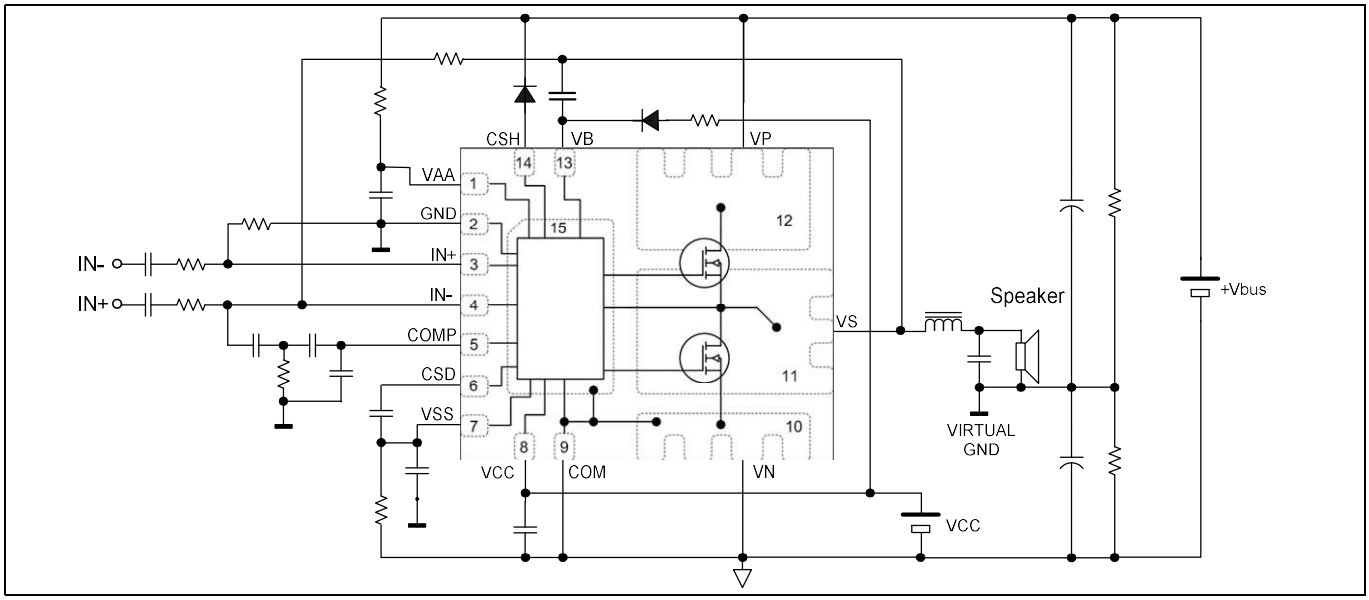


Figure 4 Typical application circuit with single power supply

Ballanced Tied Load (BTL) output takes two output legs for a speaker output. It doubles output power with double load impedance. Any load current does not flow through supply dividing capacitor; therefore BTL configuration is free from GND fluctuations. Also the bus splitting capacitor can be much smaller. Higher output power and absence of GND fluctuation make BTL suitable for subwoofer applications.

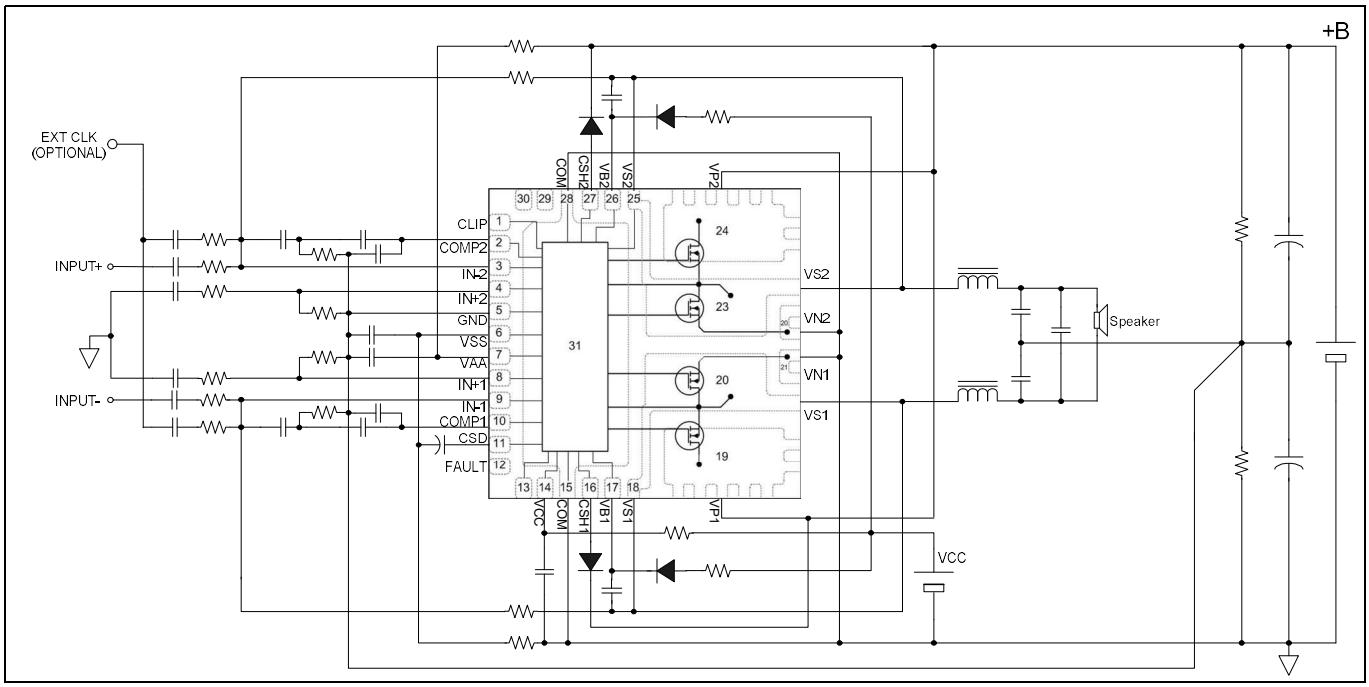


Figure 5 Typical application circuit with Bridged Tied Load (BTL) output with single power supply

3 PWM modulator design

The following explanations refer to a typical application circuit with self-oscillating PWM topology shown in Figure 3.

The open access front-end configurationof IR43xx enables many ways to implement a PWM modulator. This section explains how PWM modulation works based on an example of a self-oscillating PWM modulator in a typical application.

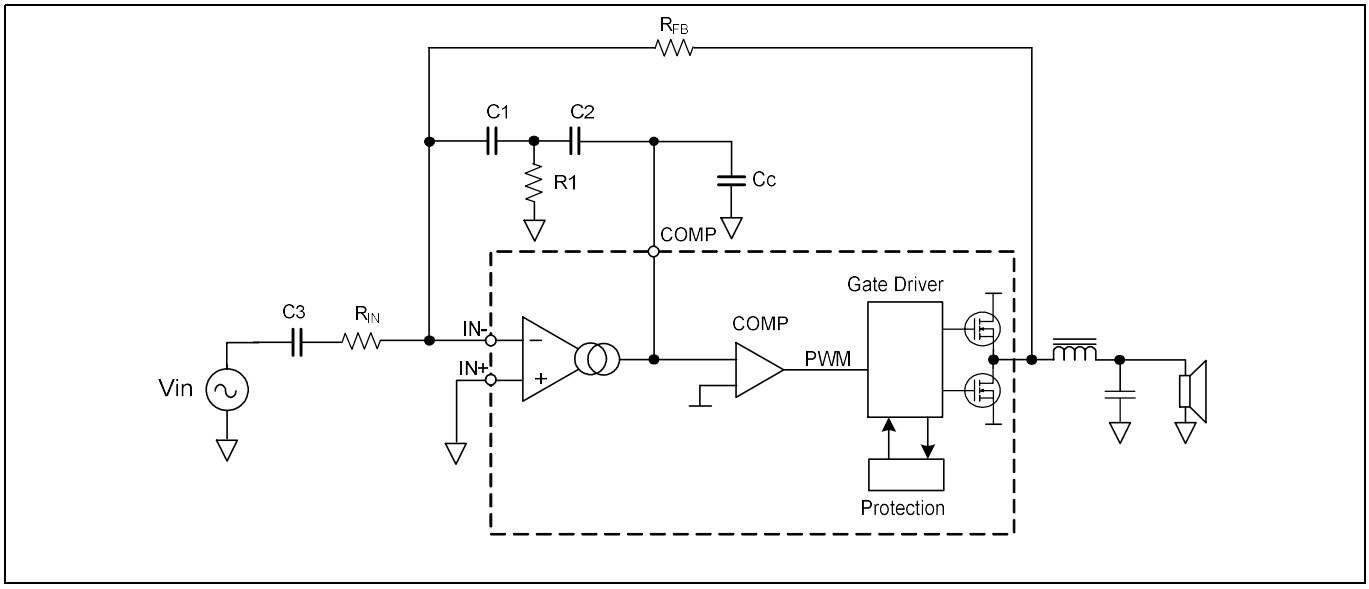


Figure 6 IR43xx typical control loop design

3.1 Input section

The audio input stage of IR43xx forms an inverting error amplifier. The voltage gain of the amplifier, G_V, is determined by the ratio between input resistor R_{IN} and feedback resistor R_{FB}.

$$G_V = \frac{R_{FB}}{R_{IN}}$$

Since the feedback resistor R_{FB} is part of an integrator time constant, which determines switching frequency, changing the overall voltage gain by R_{IN} is simpler and therefore recommended. Note that the input impedance of the amplifier is equal to the input resistor R_{IN}.

A DC blocking capacitor C3 should be connected in series with R_{IN} to minimize the DC offset voltage on the output. Due to potential distortion, a ceramic capacitor is not recommended. Minimizing the DC offset is essential to minimize the audible noise during power-ON and -OFF.

The connection of the non-inverting input IN+ is a reference for the error amplifier, and thus is crucial for audio performance. Connect IN+ to the signal reference ground in the system, which has the same potential as the negative terminal of the speaker output.

3.2 Control loop design

The IR43xx allows the user to choose from numerous methods of PWM modulator implementations. In this section, all the explanations are based on a typical application circuit of a self-oscillating

3.3 PWM frequency

Choosing the switching frequency entails making a trade off between many aspects. At lower switching frequency, conduction losses in the MOSFET stage increases due to higher inductor ripple current. The output carrier leakage in the speaker output increases. At higher switching frequency, the efficiency degrades due to higher switching losses. Higher switching frequency supports wider audio bandwidth. The inductor ripple decreases yet core loss might increase. For these reasons, 400kHz is chosen for a typical design example.

Self-oscillating frequency is determined mainly by the following items in Figure 6.

- Integration capacitors, C1 and C2
- Integration resistor, R1
- Propagation delay in the gate driver
- Feedback resistor, R_{FB}
- Duty cycle

Self-oscillating frequency has little influence from the bus voltage and input resistance RIN. Note that the nature of a self-oscillating PWM is for the switching frequency to decrease as PWM modulation deviates from idling.

Table 1 summarizes suggested values of components for a given target self-oscillating frequency. The front-end operational transconductance amplifier (OTA) output has limited voltage and current compliances. This set of component values ensures that OTA operates within its linear region for optimal THD+N performance. In case the target frequency is somewhere in between the frequencies listed in Table 1, simply adjust the frequency by tweaking R1.

Table 1 External component values vs. self-oscillation frequency

Target self-oscillation frequency (kHz)	C1=C2 (nF)	R1 (ohms)
500	2.2	200
450	2.2	165
400	2.2	141
350	2.2	124
300	2.2	115
250	2.2	102
200	4.7	41.2
150	10	20.0
100	10	14.0
70	22	4.42

3.4 Clock synchronization

In the PWM control loop design example, the self-oscillating frequency can be set and synchronized to an external clock. Through a set of resistors and a capacitor, the external clock injects periodic pulsating charges into the integrator, forcing oscillation to lock up to the external clock frequency. A typical setup with 5 Vp-p 50% duty clock signal uses R_{CK}=22 kΩ and C_{CK}=100 pF in Figure 7. To maximize audio performance, the self-running frequency without clock injection should be 20 to 30% higher than the external clock frequency.

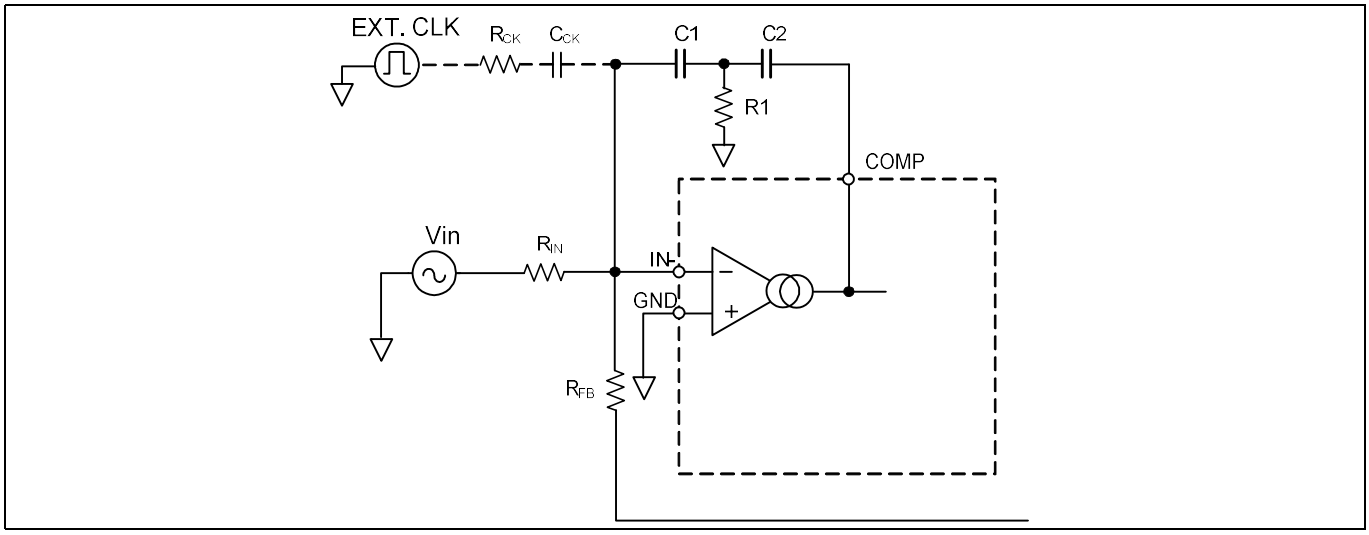


Figure 7 External clock synchronization

Figure 8 shows how a self-oscillating frequency locks up to an external clock frequency. A design of a 400 kHz self-oscillating frequency synchronizes to an external clock whose frequency is within the red boarder lines.

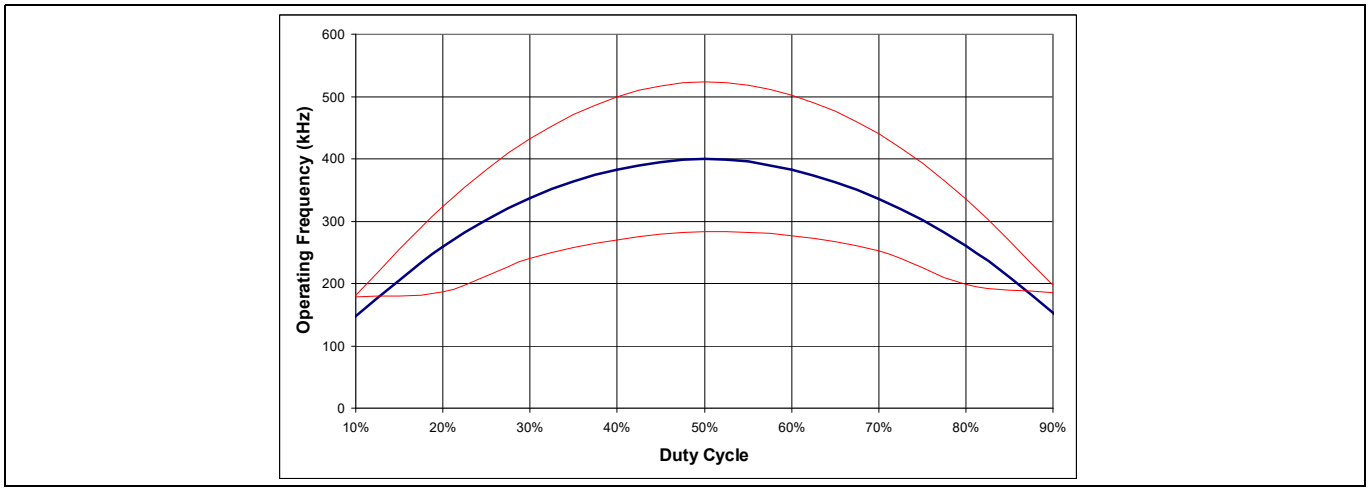


Figure 8 Typical lock range to external clock

3.5 Click noise elimination

The IR43xx has a unique feature that minimizes power-ON and -OFF audible click noise. When CSD is in between Vth1 and Vth2 during start up, an internal closed loop around the OTA enables an oscillation that generates voltages at COMP and IN-, bringing them to steady state values. It runs at around 1 MHz, independent from the switching oscillation.

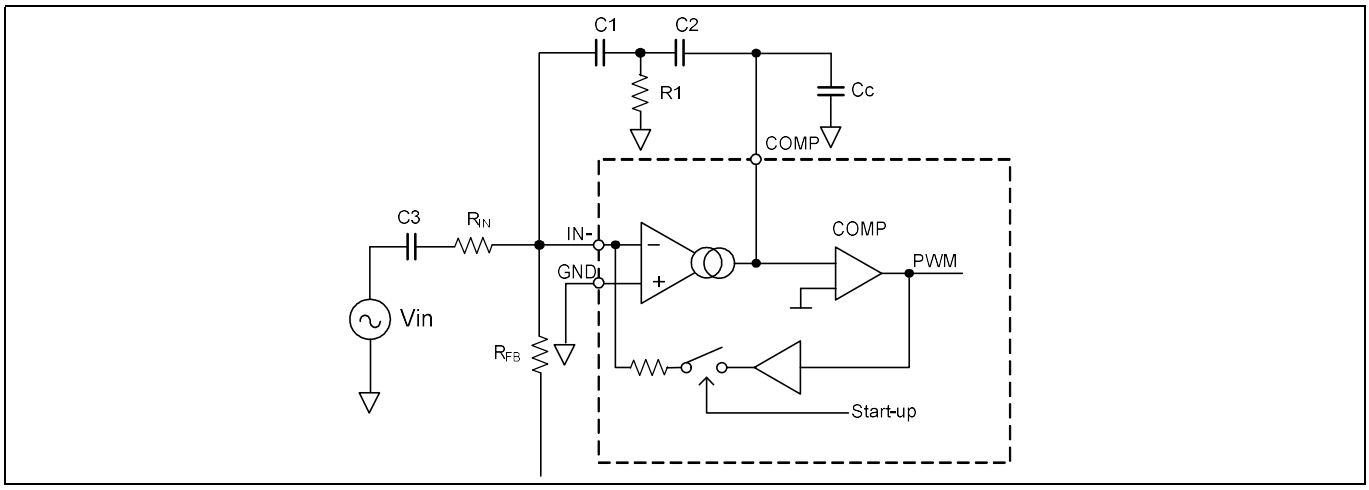


Figure 9 Audible click noise elimination

As a result, all capacitive components connected to COMP and IN- pins, such as C1, C2, C3 and Cc in Figure 9, are pre-charged to their steady state values during the start up sequence. This allows instant settling of closed –loop PWM operation.

To utilize the click noise reduction function, the following conditions must be met.

1. CSD pin has slow enough ramp up from Vth1 to Vth2 such that the voltages in the capacitors can settle to their target values.
2. High-side bootstrap power supply needs to be charged up prior to starting oscillation.
3. Audio input has to be zero.
4. For internal local loop to override external feedback during the startup period, DC offset at speaker output prior to shutdown release has to satisfy the following condition.

$$DCoffset < 30\mu A \cdot R_{FB}$$

3.6 Differential input

Figure 10 shows an example of a differential input configuration. This design is useful in single supply configuration. Use R_{IN1}=R_{IN2}, R_{FB1}=R_{FB2}, C3=C4.

Voltage gain is given by a ratio between R_{IN} and R_{FB}.

$$G_V = \frac{R_{FB}}{R_{IN}}$$

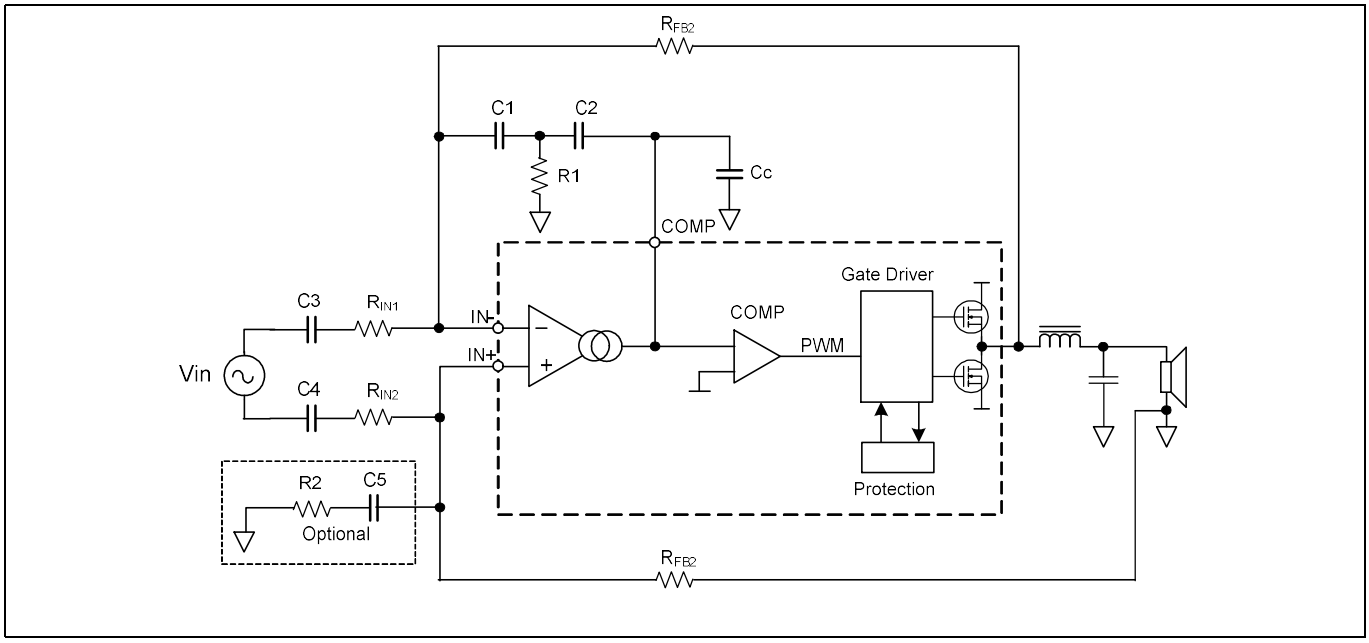


Figure 10 Differential input

Although component values in feedback network are balanced between inverting and non-inverting inputs, the integration capacitor path in the non-inverting input creates unbalance at high frequencies, causing slightly higher distortion compared to an unbalanced input configuration. To improve the THD degradations, place optional RC network R2=R1 and C5=C1.

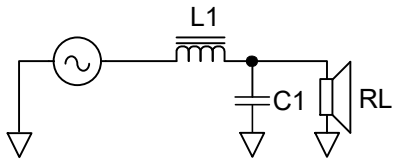
3.7 Output LPF

The output low pass filter (LPF) demodulates the amplified audio signal. It is also necessary for efficienct operation of a Class D amplifier; therefore selecting the right component is critical for both audio performance and system efficiency.

A typical ouput LPF uses a second order Butterworth LC filter designed to acheive maximum flat frequency response up to a corner frequency with nominal load impedance. Figure 11 explains how to calculate component values for a load impedance. Set the corner frequency according to the bandwidth requirement. A corner frequency of 40 kHz would be a good tradeoff point between 20 kHz bandwidth, inductor ripple current, and inductance in other words, the size of the inductor and PWM carrier leak amplitude in the output. Note that the higher the corner frequency, the higher the switching carrier leakage, and the lower the corner frequency the bigger the inductor size.

Inductance of the inductor changes with load current bias, which causes distortion in audio output. Core saturation increases inductor ripple significantly that could trigger over current protection immediately. Use an inductor with a saturation point that is higher than the peak load current. Consider I_{RMS} rating of an inductor for temperature rise condition with 1/8 rated power and peak current for maximum load current.

Use a capacitor which meets AC voltage ratings at highest audio frequency output. Use a film capacitor with lower series inductance structure type. Ceramic capacitors could add audio distortion from the strong bias voltage dependency in capacitance, this is especially demonstrated in high dielectric coefficient ceramic capacitors such as Y5V.



$$L_n = \frac{1.414 \cdot R_L}{2 \cdot \pi \cdot f_C}$$

$$C_n = \frac{0.707}{2 \cdot \pi \cdot f_C \cdot R_L}$$

Figure 11 Output LPF design

4 Operational mode

The CSD pin determines the operational mode of the IR43xx as shown in Figure 12. The OTA has three operational modes: shutdown, pop-less startup and normal operation; while the gate driver section has two modes: shutdown and normal opreration.

When V_{CSD} < Vth2, the IC is in shutdown mode and the input OTA is cut off. When Vth2< V_{CSD} < Vth1, the output MOSFETs are still in shutdown mode. The OTA is activated and starts local oscillation for pop-less start-up which pre-biases all the capacitive components in the error amplifier. When V_{CSD}>Vth1, the IR43xx enters normal operation mode and PWM operation starts.

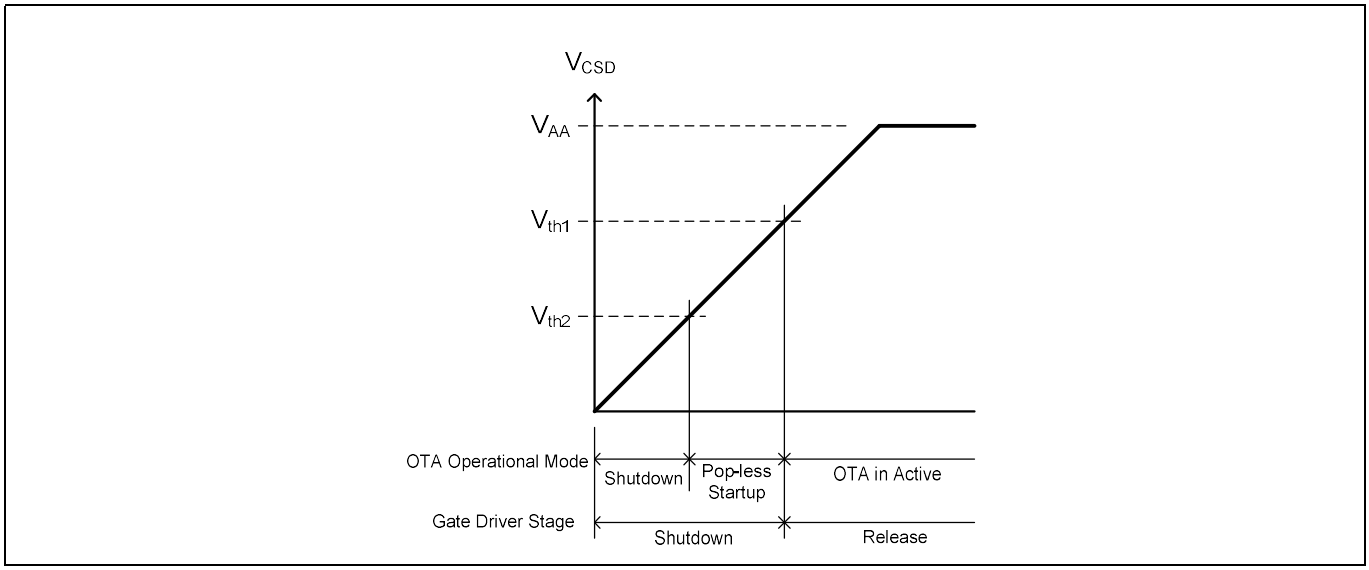


Figure 12 V_{CSD} and operational mode

4.1 Self-oscillation start-up condition

The IR43xx requires the following conditions in order for pop-less startup to work properly.

- All the control power supplies, VAA, VSS, VCC and VBS are above the under voltage lockout thresholds.
- CSD pin voltage is over Vth1 threshold.
- $|i_{IN}| < |i_{FB}|$

  Where $i_{IN} = \frac{V_{IN}}{R_{IN}}$, $i_{FB} = \frac{V_{+B}}{R_{FB}}$.
- The duration CSD voltage transitioning from Vth2 to Vth1 is long enough to pre-charge input and integration capacitors around OTA section.

5 Protections

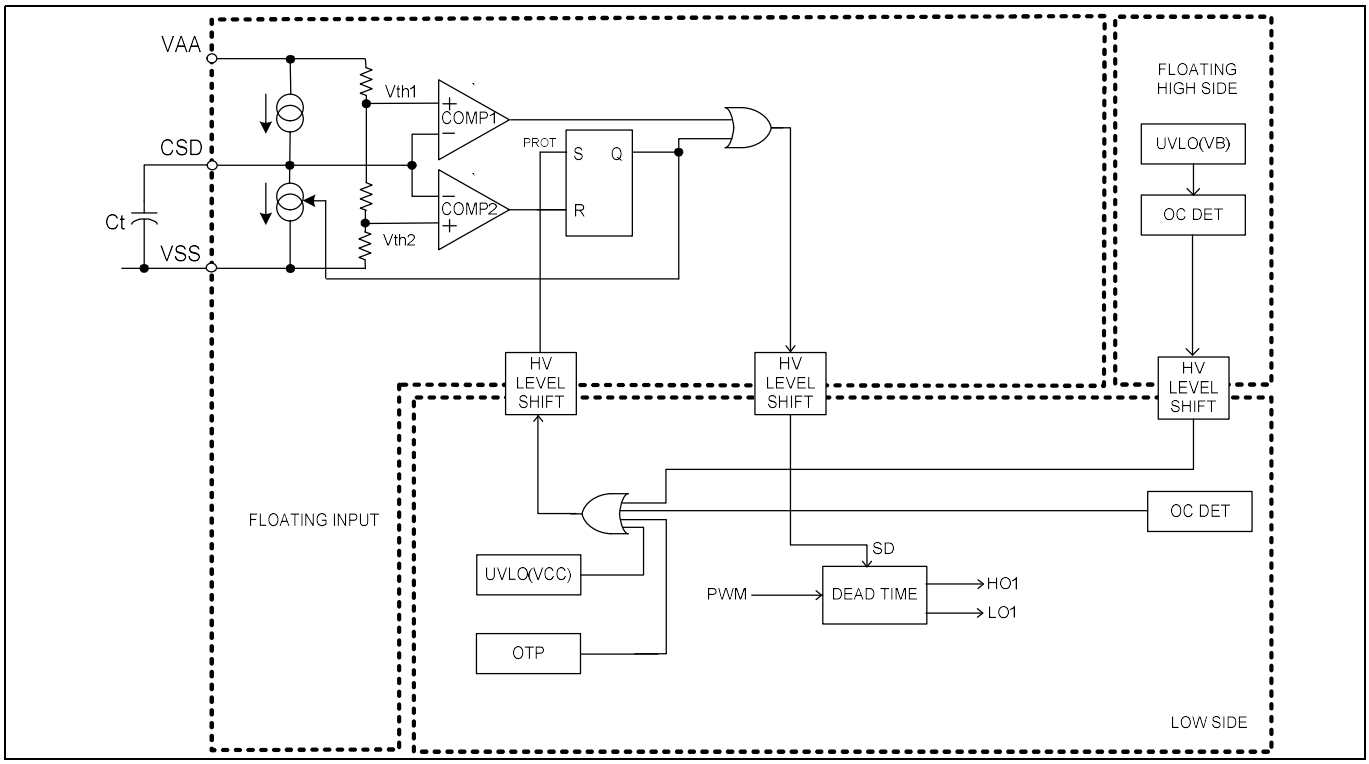


Figure 13 Protection functional block diagram (IR43x1)

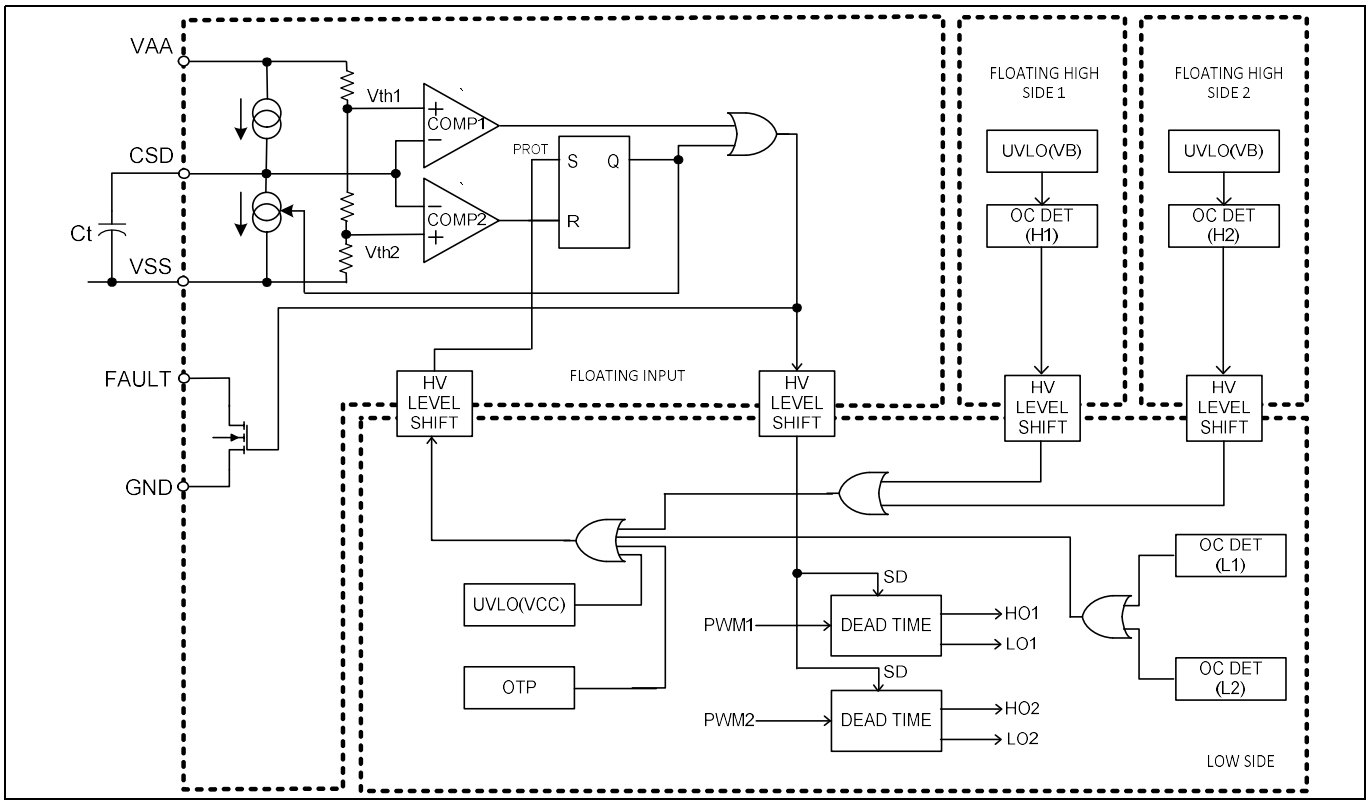


Figure 14 Protection functional block diagram (IR43x2)

The internal protection control block dictates the operational modes, normal or shutdown, using the input of the CSD pin. In shutdown mode, the controller IC turns off internal power MOSFETs.

The CSD pin provides five functions.

1. Power up delay timer
2. Self-reset timer
3. Shutdown input
4. Latched protection configuration
5. Shutdown status output (host I/F)

The CSD pin cannot be paralleled with another IR43xx directly.

The operating statuses of the protection features are shown in Table 2.

Table 2 Events and actions of CSD and FAULT

Event	CSD	FAULT
UVCC, rising edge	Recycle	L until CSD>Vth1
UVCC, falling edge	n/a	n/a
UVAA, rising edge	n/a	L at VAA<UVAA
UVAA, falling edge	n/a	L at VAA<UVAA
UVBS, rising edge	n/a	n/a
UVBS, falling edge	n/a	n/a
Over Current Protection	Keep recycling until OCP is reset	Held L until OCP is reset
DC Protection	Held L until DCP is reset	Held L until DCP is reset
Clip Detection	n/a	n/a
OTP1-3 Inputs	Keep recycling until OTP is reset	Held L until OTP is reset

*CSD recycle: CSD pin voltage discharges down to Vth2 and charges back to VAA, if CSD pin is configured as self reset protection.

5.1.1 Self-reset protection

Attaching a capacitor between CSD and V_{SS} configures the IR43xx self-reset protection mode.

Upon an OCP event, the CSD pin discharges the external capacitor voltage V_{CSD} down to the lower threshold V_{th2} to reset the internal shutdown latch. Then, the CSD pin begins to charge the external capacitor, Ct, in an attempt to resume operation. Once the voltage of the CSD pin rises above the upper threshold, V_{th1}, the IC resumes normal operation.

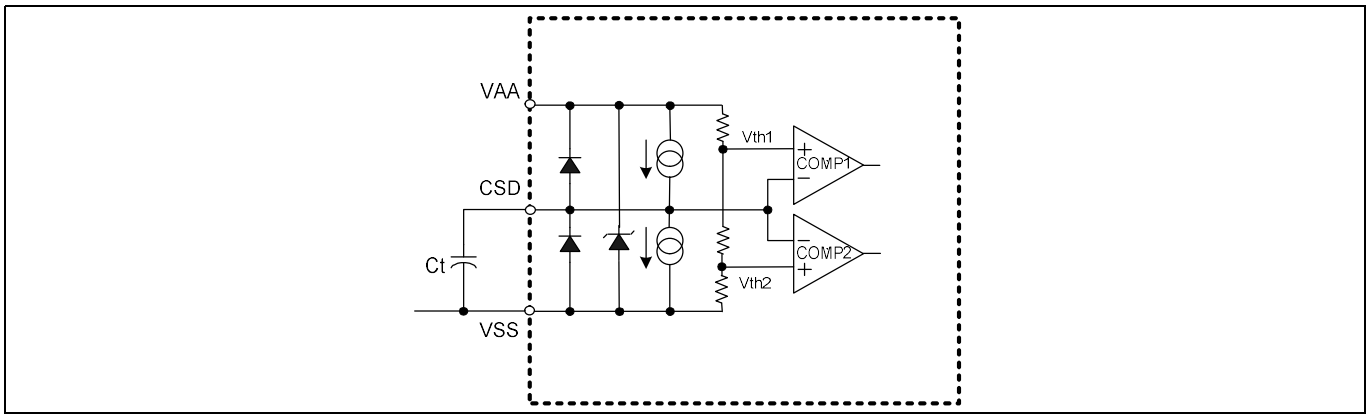


Figure 15 Self-reset protection configuration

5.1.2 Designing Ct

The external timing capacitor, Ct, programs self-reset timings: t_{RESET} and t_{SU}.

- t_{RESET} is the time that elapses from when the IC enters the shutdown mode to the time when the IC resumes operation. t_{RESET} should be long enough to avoid over heating the MOSFETs from the repetitive sequence of shutting down and resuming operation during over-current conditions. In most applications, the minimum recommended time for t_{RESET} is 0.1 seconds.
- t_{SU} is the time between powering up the IC in shutdown mode to the moment the IC releases shutdown to begin normal operation.

The Ct determines t_{RESET} and t_{SU} as following equations:

$$t_{RESET} = \frac{Ct \cdot V_{AA}}{1.1 \cdot I_{CSD}} \quad [s]$$

$$t_{SU} = \frac{Ct \cdot V_{AA}}{0.7 \cdot I_{CSD}} \quad [s]$$

where I_{CSD}: the charge/discharge current at the CSD pin
V_{AA}: the floating input supply voltage with respect to V_{SS}.

5.1.3 Shutdown input

During normal operation, pulling the CSD pin below the upper threshold Vth1 forces the IC into shutdown mode. Figure 16 shows how to add an external discharging path to shutdown the PWM.

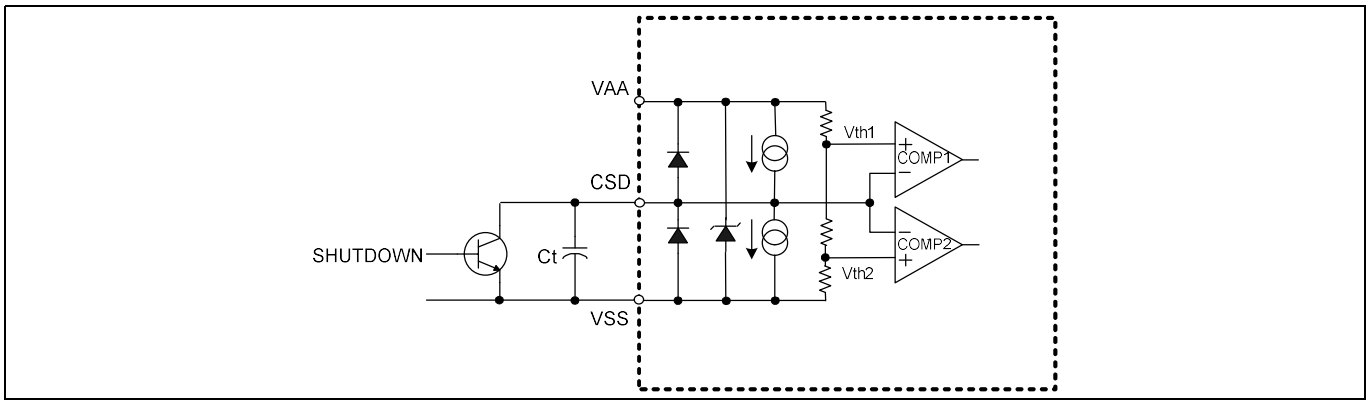


Figure 16 Shutdown input

5.1.4 Latched protection

Connecting CSD to V_{AA} through a 10 kΩ or less resistor configures latched protection mode. The internal shutdown latch stays in shutdown mode after over current is detected. An external reset switch brings CSD below the lower threshold Vth2 for a minimum of 200 ns and resets the latch. At first power up, a reset signal to the CSD pin is required to release the IC from shutdown mode.

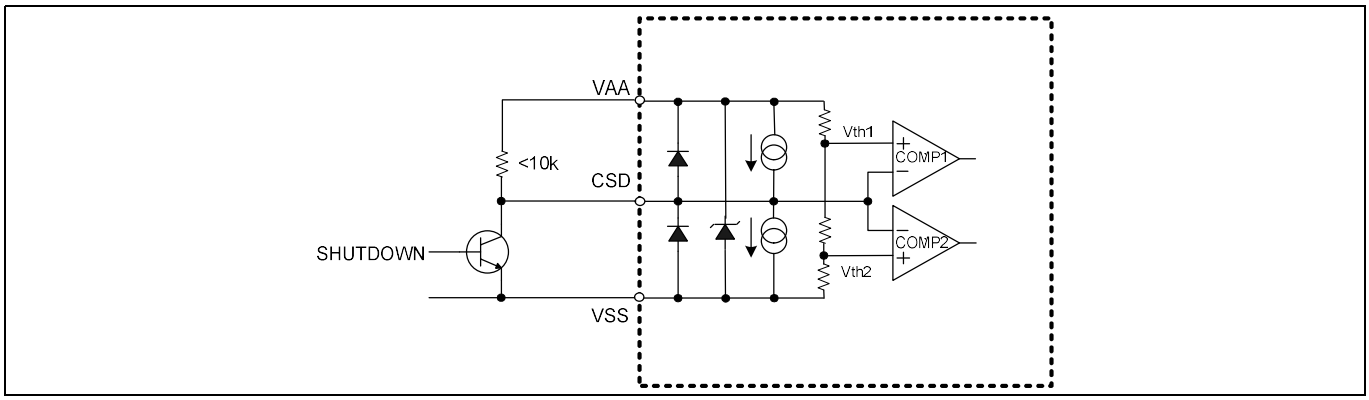


Figure 17 Latched protection with reset input

5.1.5 Interfacing with system controller

The IR43xx can communicate with an external system controller through a simple interfacing circuit shown in Figure 18. A generic PNP transistor, U1, detects the sink current at the CSD pin during protection event and outputs a shutdown flag signal to an external system controller. Another generic NPN transistor, U2, can then reset the internal protection logic by pulling the CSD voltage below the lower threshold Vth2. After the first power up sequence, a reset signal to the CSD pin is required to release the IC from shutdown mode.

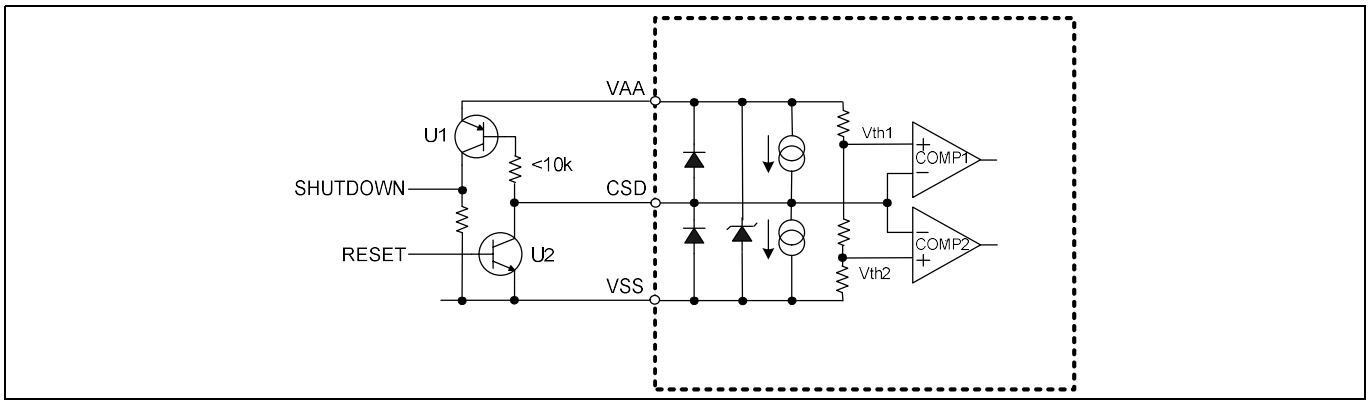


Figure 18 Interfacing CSD with system controller

5.2 Over Current Protection (OCP)

The IR43xx features over current protection to protect the internal power MOSFETs during abnormal load conditions. The control logic diagrams are in Figure 13 and 14. As soon as either the high-side or low-side current sensing block detects over current, the following sequence will occur.

1. The shutdown latch flips its logic states from normal operational mode to shutdown mode.
2. Low-side and high-side MOSFETs go into an off state condition.
3. The CSD pin starts discharging the external capacitor Ct.
4. When voltage across Ct falls below the lower threshold Vth2, COMP2 resets the shutdown latch to normal mode.
5. The CSD pin starts charging the external capacitor Ct.
6. When V_{CSD} goes above the upper threshold Vth1, the logic on COMP1 toggles and the IC resumes operation.

Figure 19 summarizes the above. As long as the over current condition exists, the IC will repeat the over current protection sequence at a repetitive rate set by the CSD capacitor.

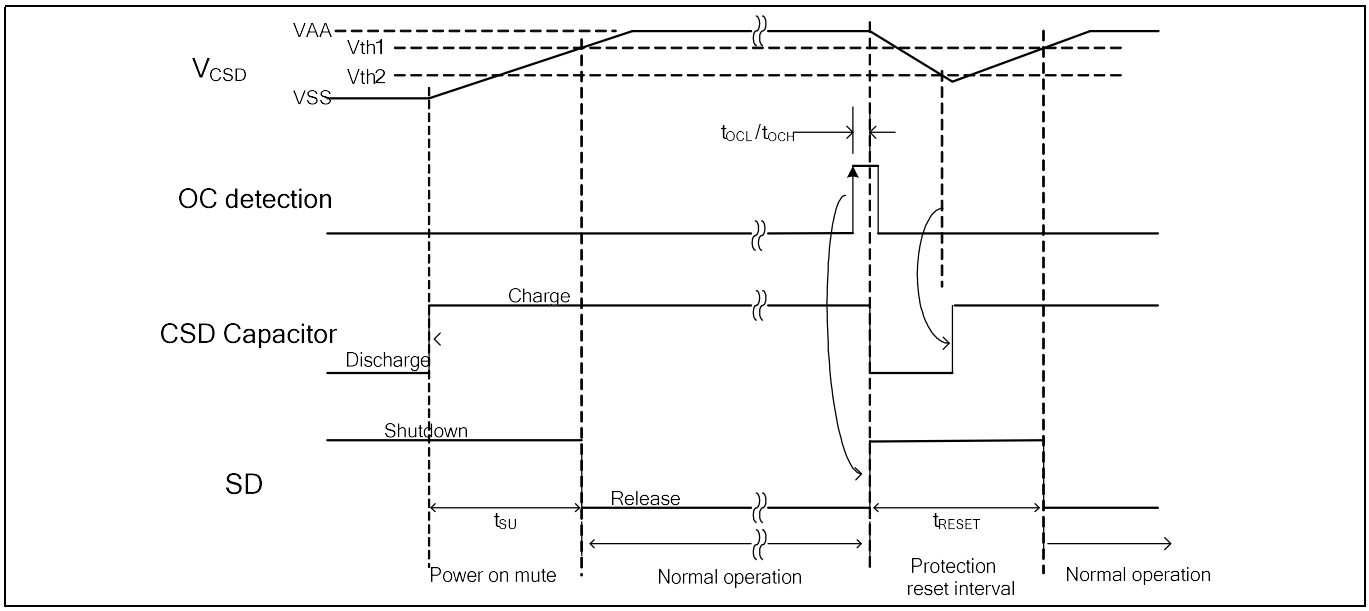


Figure 19 Overcurrent protection timing chart

5.3 Over Temperature Protection (OTP)

If the junction temperature T_J of the controller IC exceeds the on-chip thermal shutdown threshold, T_{SD}, the on-chip over temperature protection shuts down the PWM.

5.4 Under Voltage Protection (UVP)

In order to prevent a partial on-state of the internal MOSFET, under-voltage protection monitors the low side and high side gate bias supplies, VCC and VB. When VCC is below UVLO, both high and low side MOSFETs are turned off. When the high side supply V_{BS} is below the UVLO threshold, the high side output is disabled, while the low side works normaly.

5.5 Over Voltage Protection (OVP)

When the supply voltage in VP exceeds the internal MOSFET's rating, PWM stops in order to protect the MOSFET.

6 Status output (IR43x2 only)

6.1 Fault output

FAULT output is an open drain output referenced to GND to report whether the IR43x2 is in shutdown mode or in normal operating mode. If the FAULT pin is open, the IR43x2 is in normal operation mode, i.e. the output MOSFETs are active. The following conditions trigger shutdown internally and pulls the FAULT pin down to GND.

- Over Current Protection
- Over Temperature Protection
- Shutdown mode from CSD pin voltage

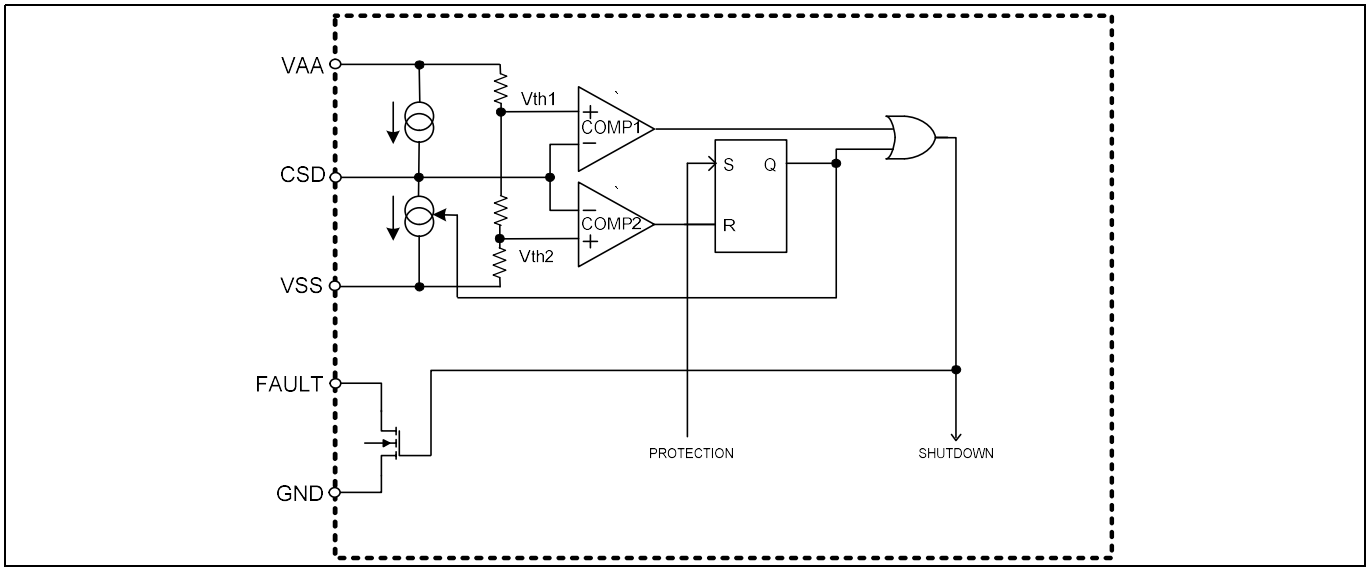


Figure 20 Fault output

6.2 CLIP output

When the output of the amplifier loses track of an expected target value, the amplifier enters into clipping condition.
The CLIP detection block monitors the COMP pin voltage with a window comparator. The CLIP pin is pulled to GND when a clipping condition is detected. The detection thresholds in the COMP pin are at 10% and 90% of VAA-VSS. The CLIP outputs are disabled in shutdown mode.

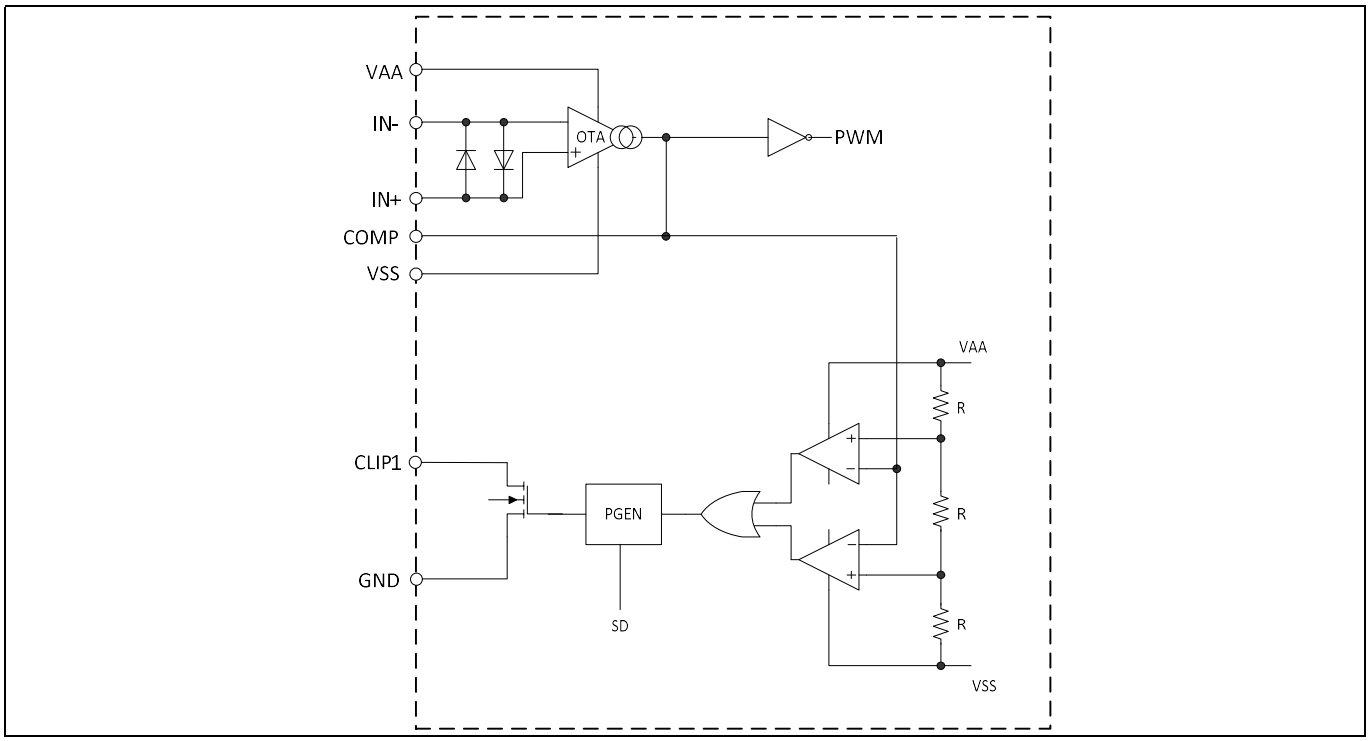


Figure 21 CLIP detection

7 Power supply design

7.1 Supplying VAA and VSS

VAA and VSS are supply voltages to the front-end of the analog section, hence are noise sensitive. For best audio performance, use regulated power supplies for VAA and VSS.

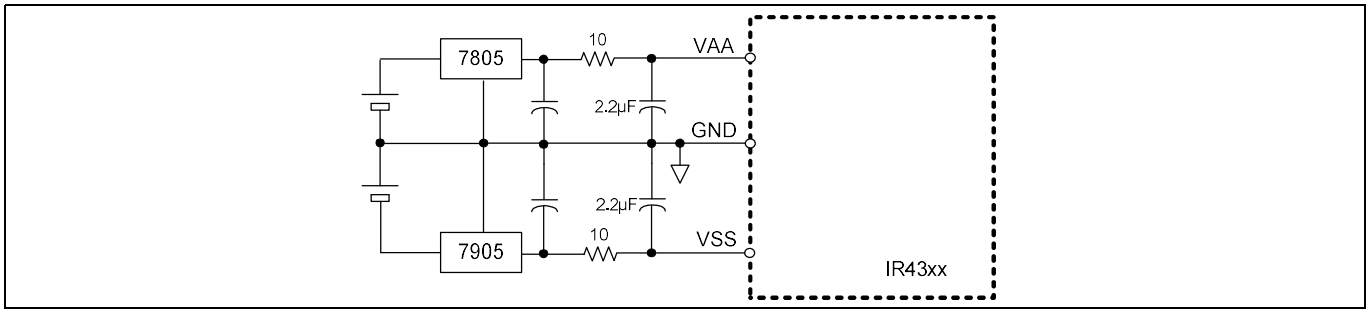


Figure 22 Supplying VAA and VSS with external voltage regulators

When switched mode regulators are used as supply voltages for VAA and VSS, place a two-stage R-C noise filter in the supply lines as shown in Figure 23.

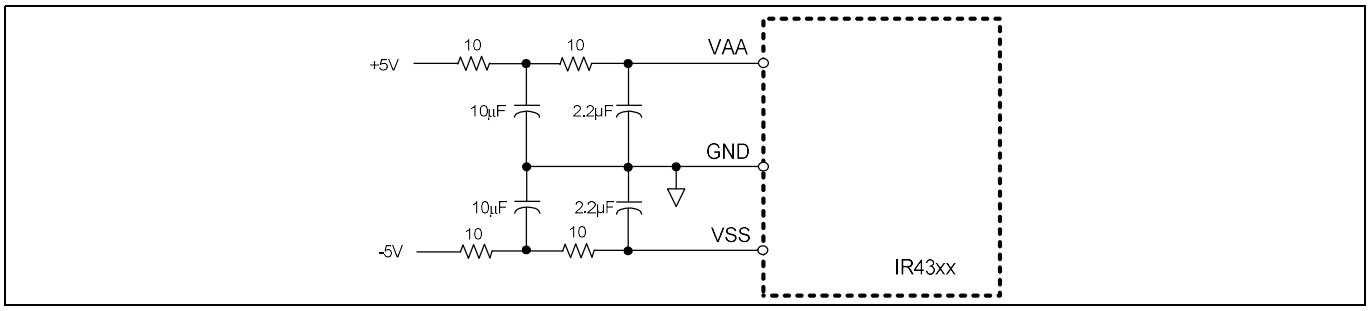


Figure 23 Supplying VAA and VSS from Switched Mode Power Supply (SMPS)

7.2 Supplying VCC and VB

Figure 24 shows the recommended power supply configuration for gate driver power supplies. The gate driver stage has three power supply inputs:

1. VCC-COM: low side gate drive supply
2. VB1-VS1: CH1 high side gate drive supply
3. VB2-VS2: CH2 high side gate drive supply (IR43x2 only)

The low-side power supply, VCC, feeds the internal gate drive logic and low side gate driver. In order to protect VCC from switching noise generated by the VS node, it is recommended to insert a few ohms of R_{VBS} in the bootstrap charging path.

The high-side driver requires a floating supply VBn referenced to the respective switching node VSn where the source of the output MOSFET is connected. A charge pump method (floating bootstrap power supply) eliminates the need for a floating power supply and thus is used in the typical application circuit. The floating bootstrap power supply charges the bootstrap capacitor C_{BS} from the low-side power supply VCC during the

low-side MOSFET ON period. When the high-side MOSFET is ON, the diode cuts off and floats the VBS supply. C_{BS} retains its VB supply voltage for the rest of the high-side ON duration.

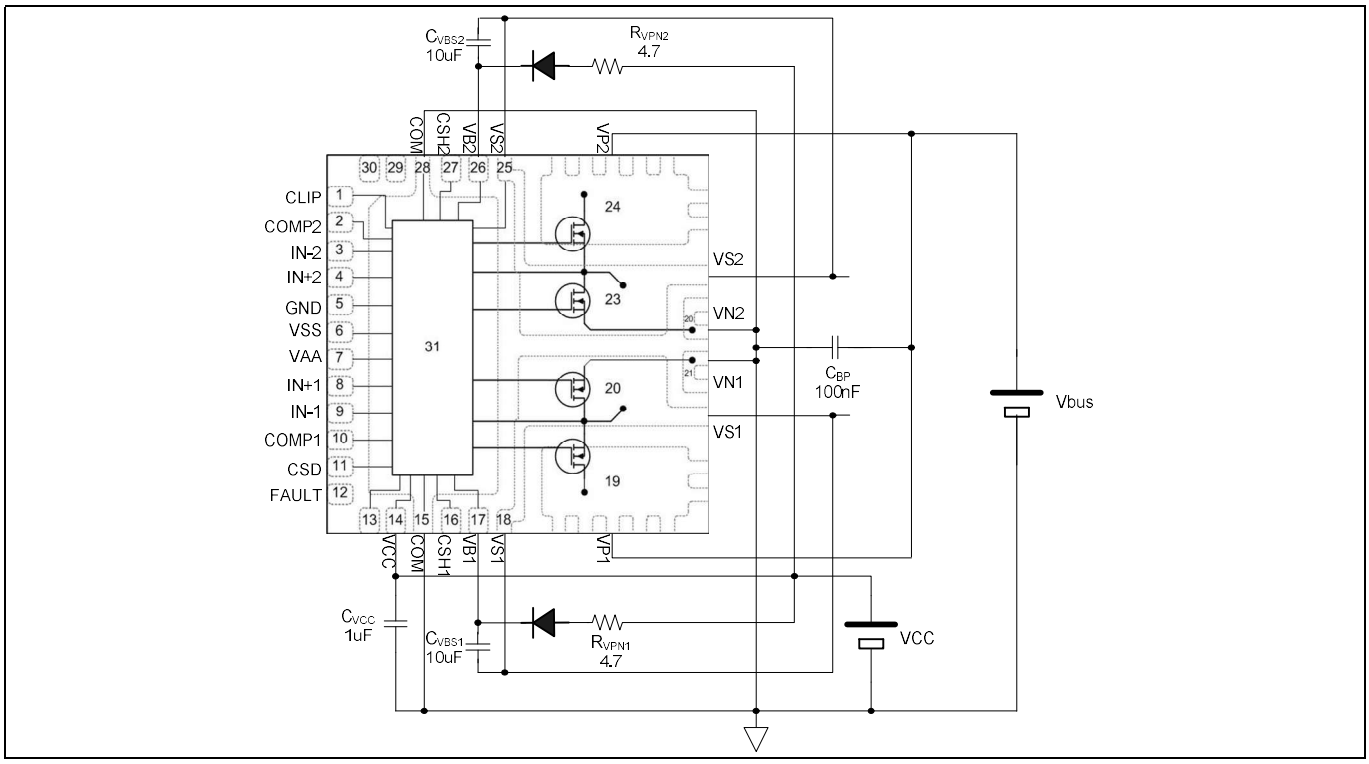


Figure 24 Recommended power supply configurations for output stage

7.2.1 Choosing bootstrap capacitance

The minimum bootstrap capacitance is determined as follows:

$$C_{BS} >> \frac{(I_{QBS} + I_{R1}) \cdot t_{ON}}{VCC - 1.5 - UVBS}$$

Where C_{BS}: floating bootstrap capacitance [F]
I_{QBS}: high-side quiescent current [A]
I_{R1}: high-side current sensing bias current [A]
t_{ON}: longest high-side MOSFET conduction time [s]
VCC: low-side power supply voltage [V]
UVBS: high-side under voltage lockout threshold [V]
1.5: voltage drop in the bootstrap charging diode D_{BS}

Often IR43xx uses hard clipping condition. The continuous high-side ON duration could continue as long as half of the lowest audio frequency, tens of miliseconds. A typical application uses a 22 uF C_{BS} to support low audio frequency clipping. A ceramic capacitor (X7R, X5R or X5S type) or aluminium electrolytic capacitor with 25 V or higher voltage rating is recommended.

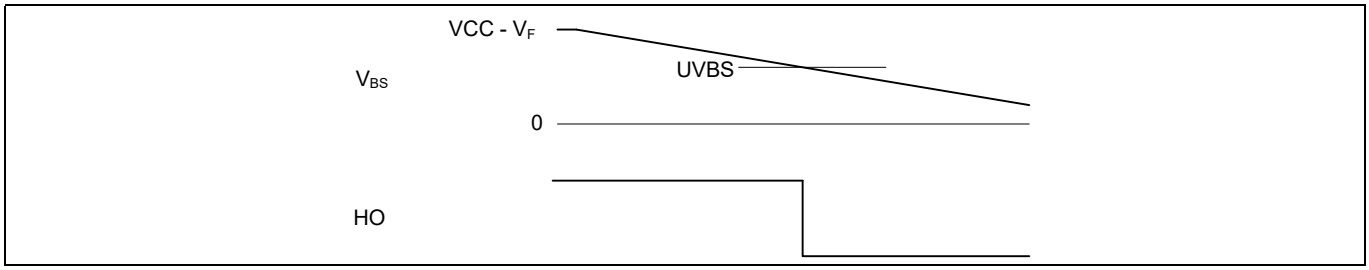


Figure 25 V_{BS} discharging

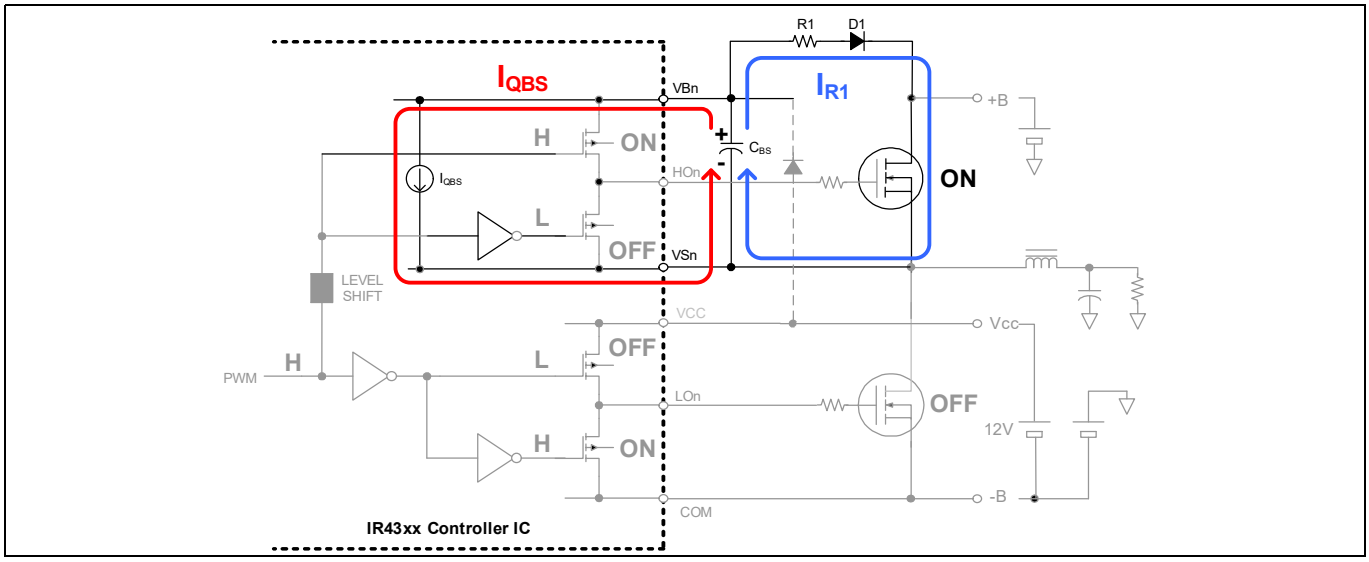


Figure 26 V_{BS} discharging during high-side ON

7.2.2 Choosing bootstrap diode

Use a bootstrap charging diode with voltage rating of 1.5 x the maximum bus voltage. In order to charge the bootstrap capacitor in a very short low-side ON period with a high PWM modulation ratio, a fast recovery diode type (trr<50ns) is recommended.

7.2.3 Charging V_{BS} prior to start

For proper start-up, precharging the bootstrap supply V_{BS} prior to PWM start-up is necessary in self-oscillating PWM modulator topologies. A charging resistor, R_{CHARGE}, inserted between the positive supply bus and V_B, charges C_{BS} prior to switching start as shown in Figure 27. The minimum resistance of R_{CHARGE} is limited by the maximum PWM modulation index of the system. When the high-side MOSFET is on, R_{CHARGE} drains the bootstrap power supply together with the quiescent current, I_{QBS}, so it reduces the holding time, resulting in maximum continuous high-side on time.

- The maximum resistance of R_{CHARGE} is limited by the current charge capability of the resistor during startup:

  $I_{CHARGE} > I_{QBS}$

  Where,

  I_{CHARGE} = the current through R_{CHARGE}

  I_{QBS} = the high side supply quiescent current, 1mA

Pre-charging current flows into the speaker load. In order to startup without the load connected, a dummy load R_{dummy} in parallel with the speaker output provides a pre-charging current path.

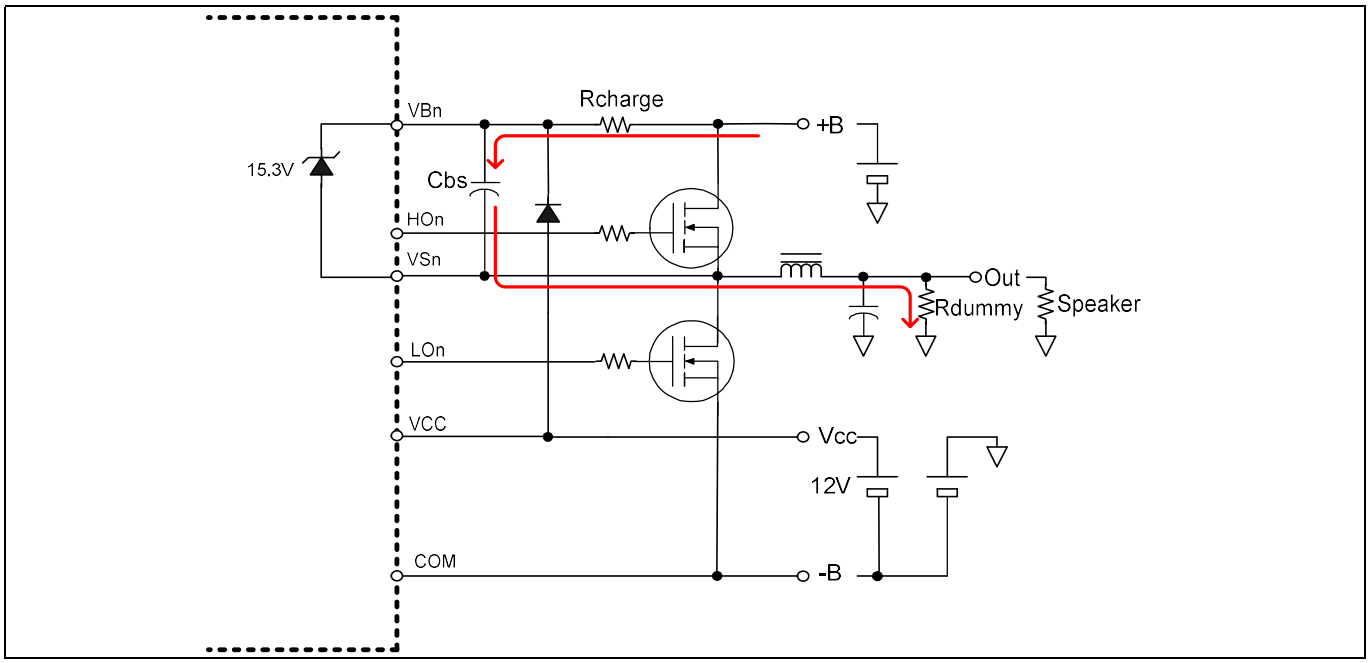


Figure 27 Bootstrap supply pre-charging

7.3 Snubber in VP and VN

VP and VN are supply voltages to the output MOSFET section where the high frequency peak current flows. Placing optional RC snubber, R_{VPN} and C_{VPN}, could help reduce the high frequency ringing due to reverse recovery charge in the output MOSFET. Optimal component value depends on parasitic inductance and PCB layout, R_{VPN} =1 ohm and C_{VPN} =100 nF is a good starting point with a typical PCB layout.

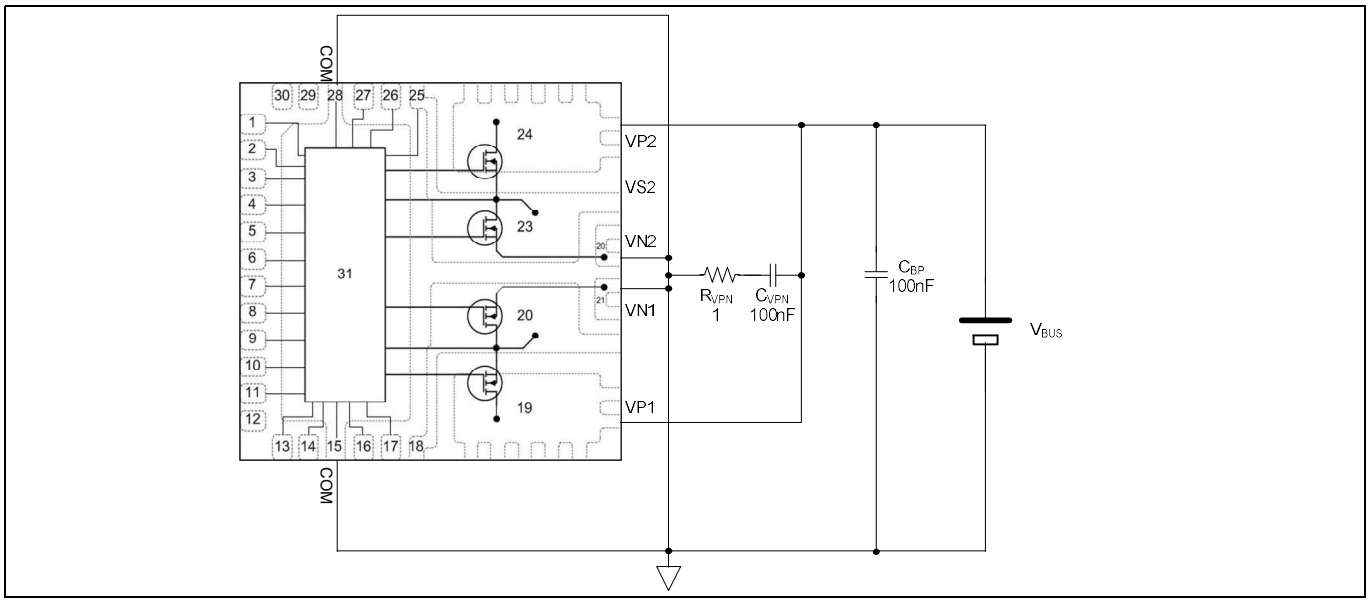


Figure 28 Snubber in VP and VN

7.4 Power supply sequence

The protection control block in the IR43xx monitors the status of V_{AA} and V_{CC} to ensure that both voltage supplies are above their respective UVLO (under voltage lockout) thresholds before starting normal operation. If either V_{AA} or V_{CC} is below the under voltage threshold, the outout MOSFETs are disabled in shutdown mode until both V_{AA} and V_{CC} rise above their voltage thresholds. As soon as V_{AA} or V_{CC} falls below its UVLO threshold, protection logic in the IR43xx turns off high-side and low-side.

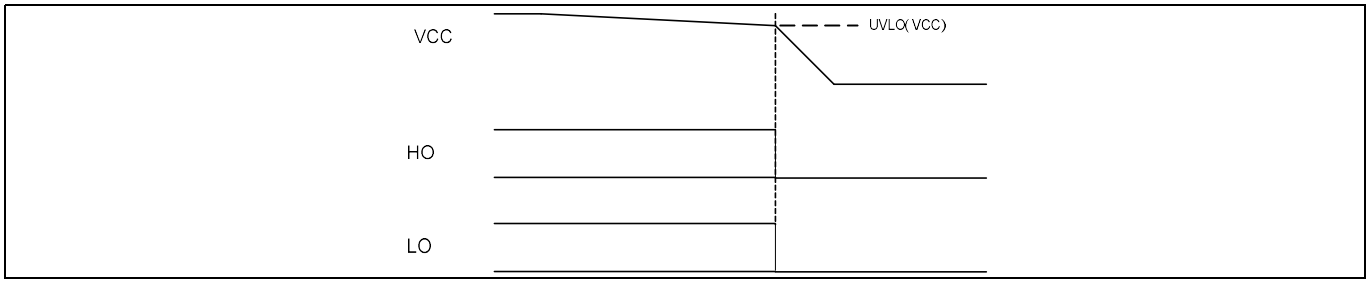


Figure 29 IR43xx UVLO timing chart

8 Board layout considerations

Reliability of products in PQFN package is subject to board mounting process. The soldering process is critical. Refer to Application Note AN-1170 Audio Power Quad Flat No-Lead (PQFN) Board Mounting Application Note for specific footprint design and soldering methods.

8.1 Basic layout plan

There are functional blocks that generate noise and there are functional blocks that are sensitive to noise. The PCB designer should identify them and find out the best component placement based on these facts as well as the mechanical and thermal requirements.
Noise sensitive functions:

- The audio input circuitry, especially IN+ and IN-

Noise generating functions:

- The gate driver stage, especially VB, CSH and VS
- The MOSFET stage

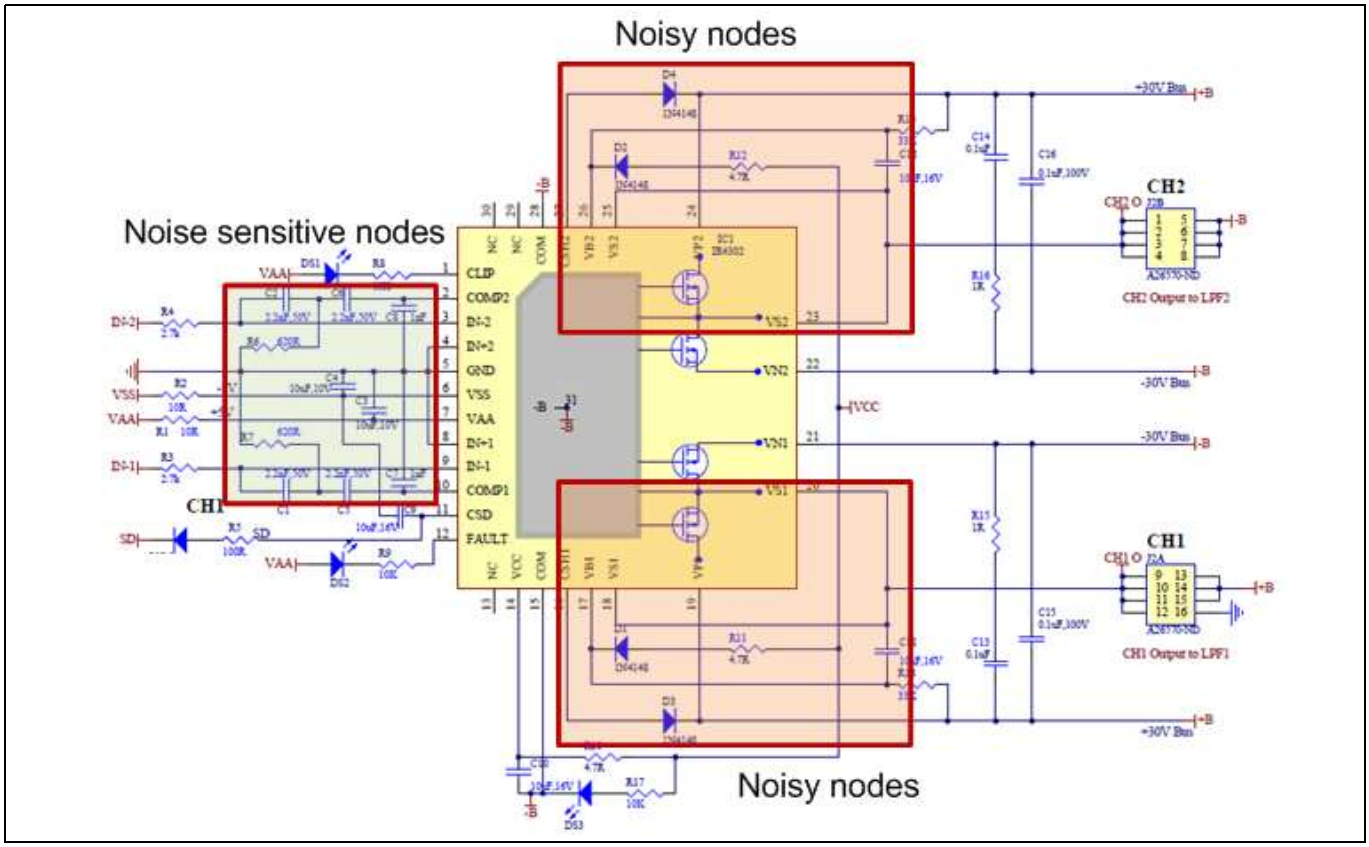


Figure 30 Noise mapping of IR43x2

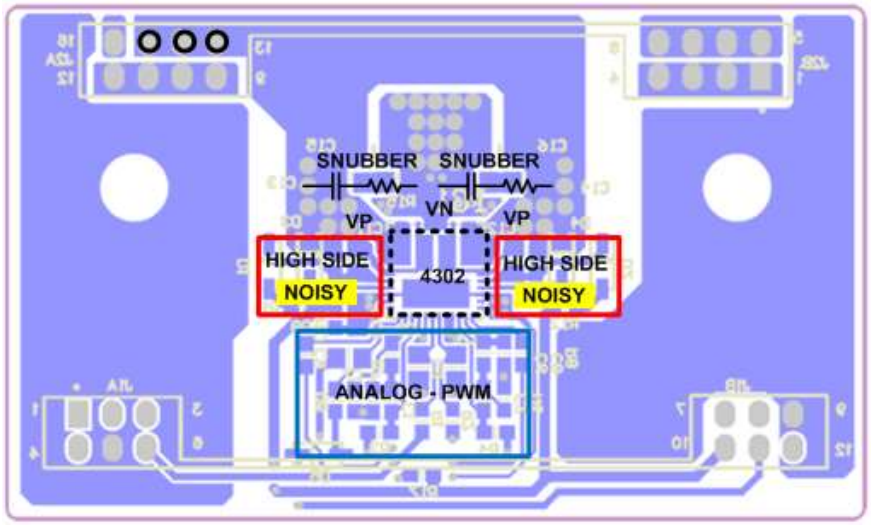


Figure 31 Noise mapping of IR43x2 (component side)

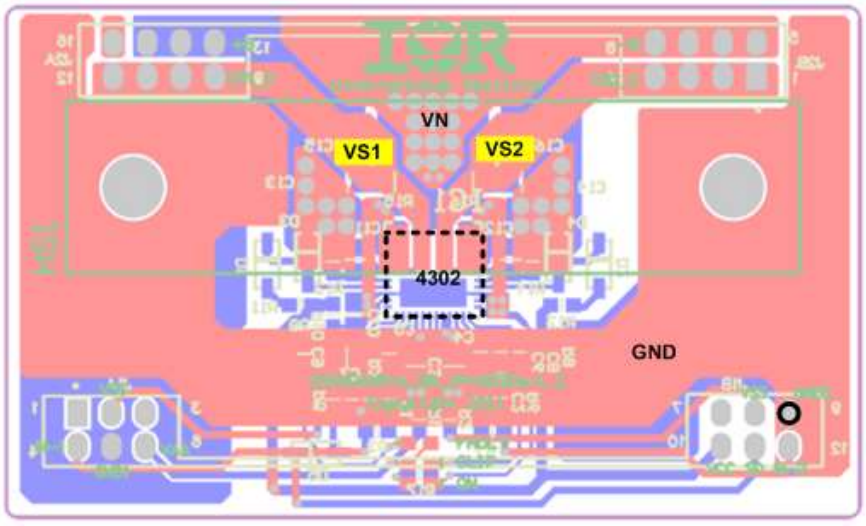


Figure 32 Noise mapping of IR43x2 (bottom side)

It is important to properly locate the ground planes to obtain good audio performance. Since each functional block within the IR43xx refers to different potentials, it is recommended to apply three reference potentials: analog, gate drive and power grounds.

Figures 31 and 32 are examples of a PCB layout used with the IRAUDAMP16 reference design. Note that there is no overlap between the input GND plane and the noisy switching nodes: VS1, VS2 and high side components. Stray inductance in the VS connection is less influential than VP and VN so prioritize these power supply traces.

8.1.1 Analog ground

The Input analog section is referenced to the signal ground, or GND, which should be a quiet reference node for the audio input signal. The peripheral circuits in the floating input section, such as CSD and COM pins refer to this ground. These nodes should all be separated from the switching stages of the system. In order to prevent potential capacitive coupling to the switching nodes, use a ground plane only in this part of the circuit. Do not share the signal ground plane with gate driver or power stages unless there is a dedicated layer for GND plane.

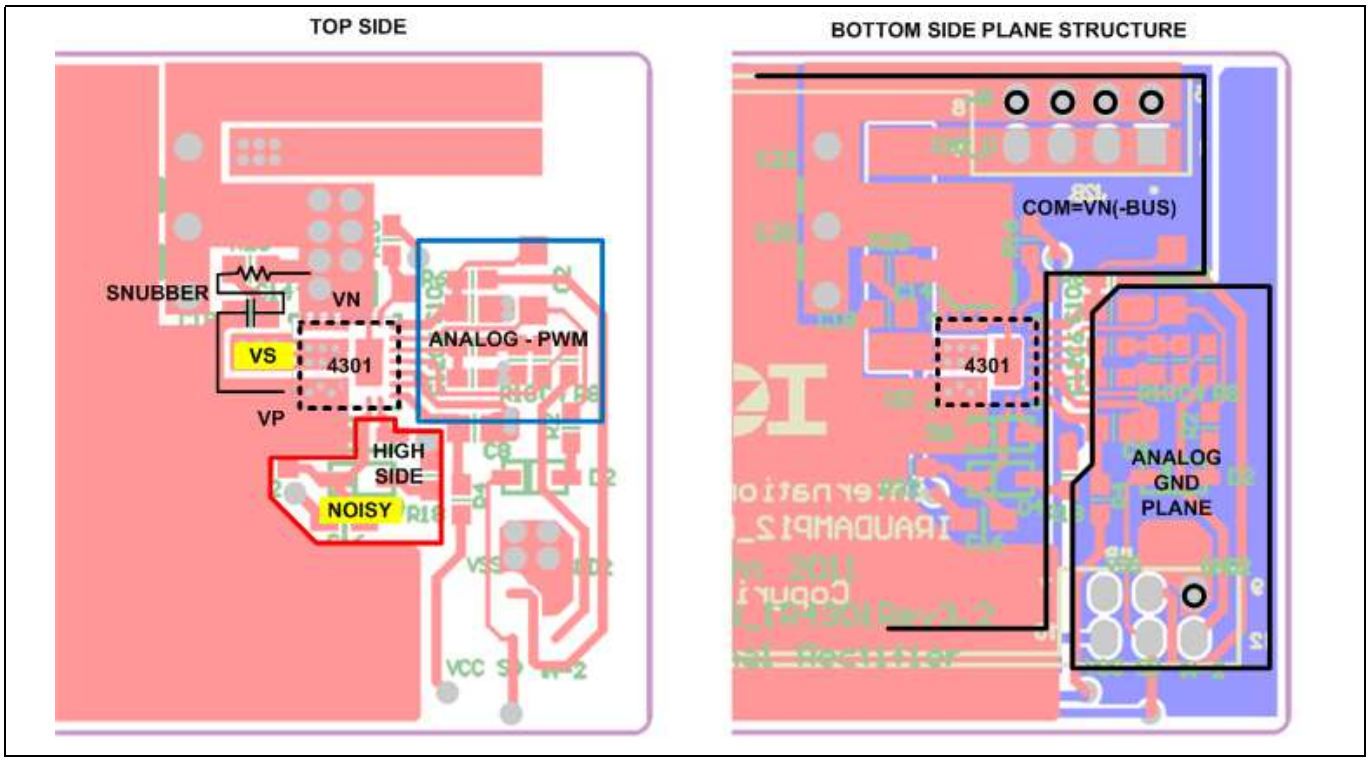


Figure 33 Ground separation of IR43x1

8.1.2 Gate driver reference

The gate driver stage of the IR43xx is located between pins 7 and 30 and is referenced to the negative bus voltage, COM and COM2. This is the substrate of the IC and acts as ground. Although the negative bus is a noisy node in the system, both of the gate drivers refer to this node. Therefore, it is important to shield the gate drive stages with the negative bus voltage so that all the noise currents due to stray capacitances flow back to the power supply without degrading signal ground.

8.1.3 Power ground

Power ground is the ground connection that closes the loops of the bus capacitors and inductor ripple current circuits. Separate the power ground and input signal grounds from each other as much as possible to avoid common stray impedances.

Figure 34 illustrates how to layout reference planes. The power GND plane should include a negative bus cap. The power reference plane should include Vcc.

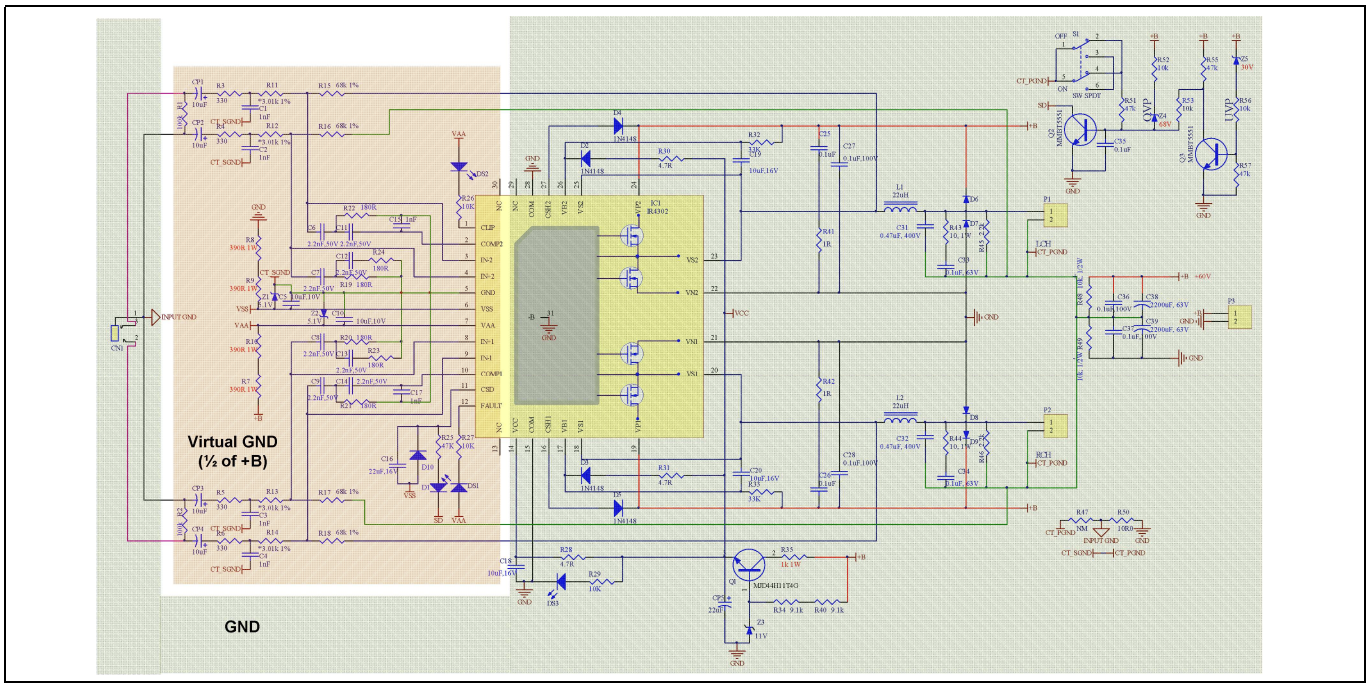


Figure 34 Applying ground planes in single power supply design

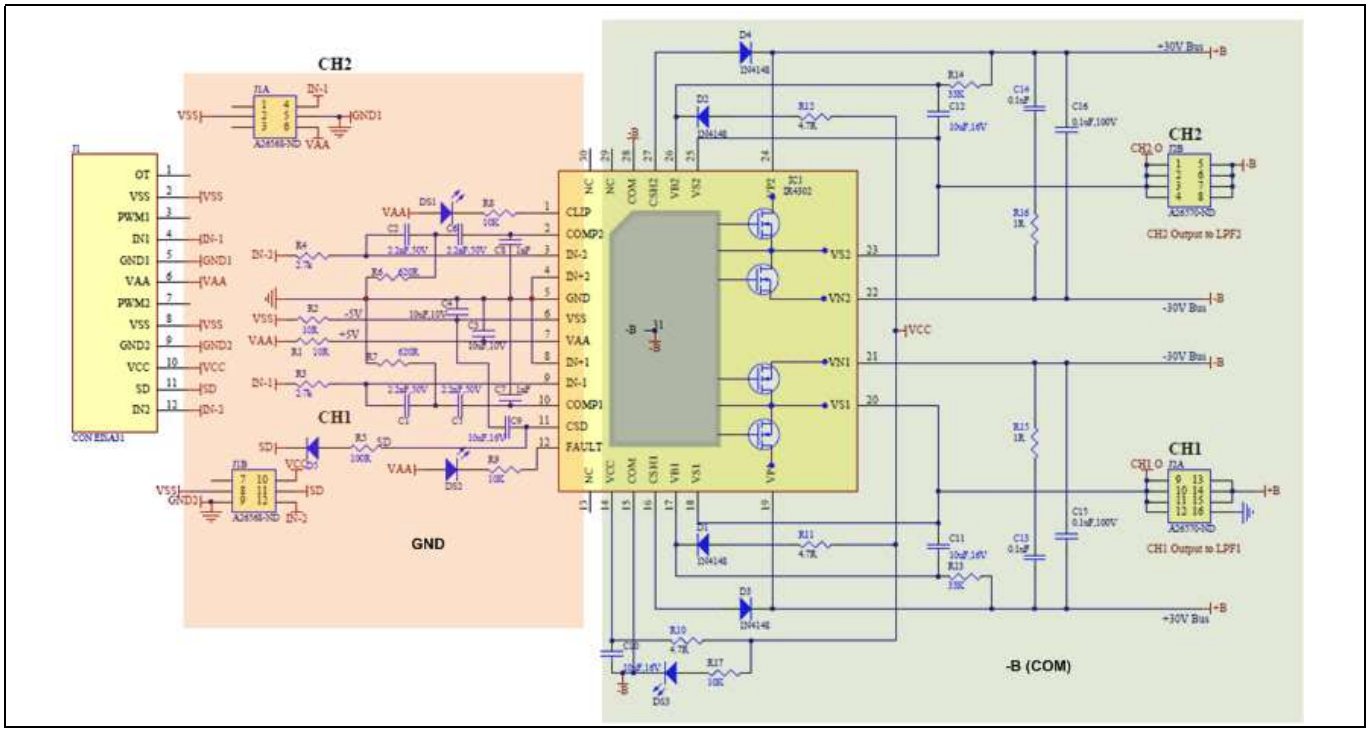


Figure 35 Applying ground planes in split power supply design

8.2 Thermal design

Continuous output power of IR43xx depends on thermal design while instantaneous peak power is determined by bus voltage.

8.2.1 Using the PCB as a heatsink

The Power Quad Flat No-lead Package (PQFN) uses the PCB as a heatsink. Heat sources from the package are VS and VP exposed pads where the MOSFET die is placed. Vias placed underneath the device spreads the heat from the component side to the bottom side of the PCB. Use wide traces to enhance heat spread on the component side. Use vias to propagate heat to the bottom side in order to maximize heat spread.

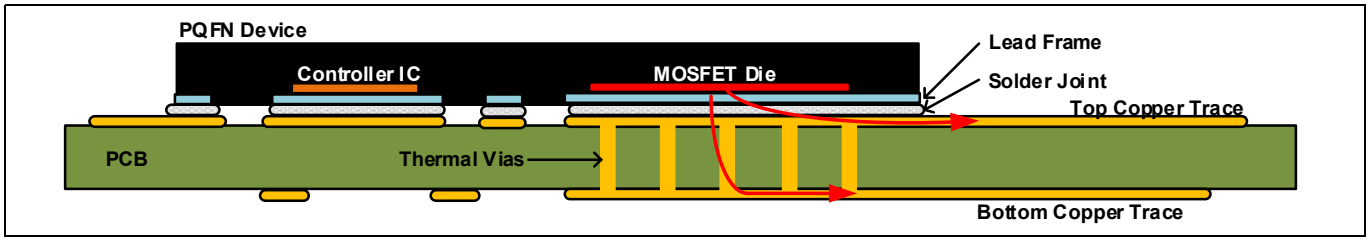


Figure 36 Heat dissipation path ssing PCB vias

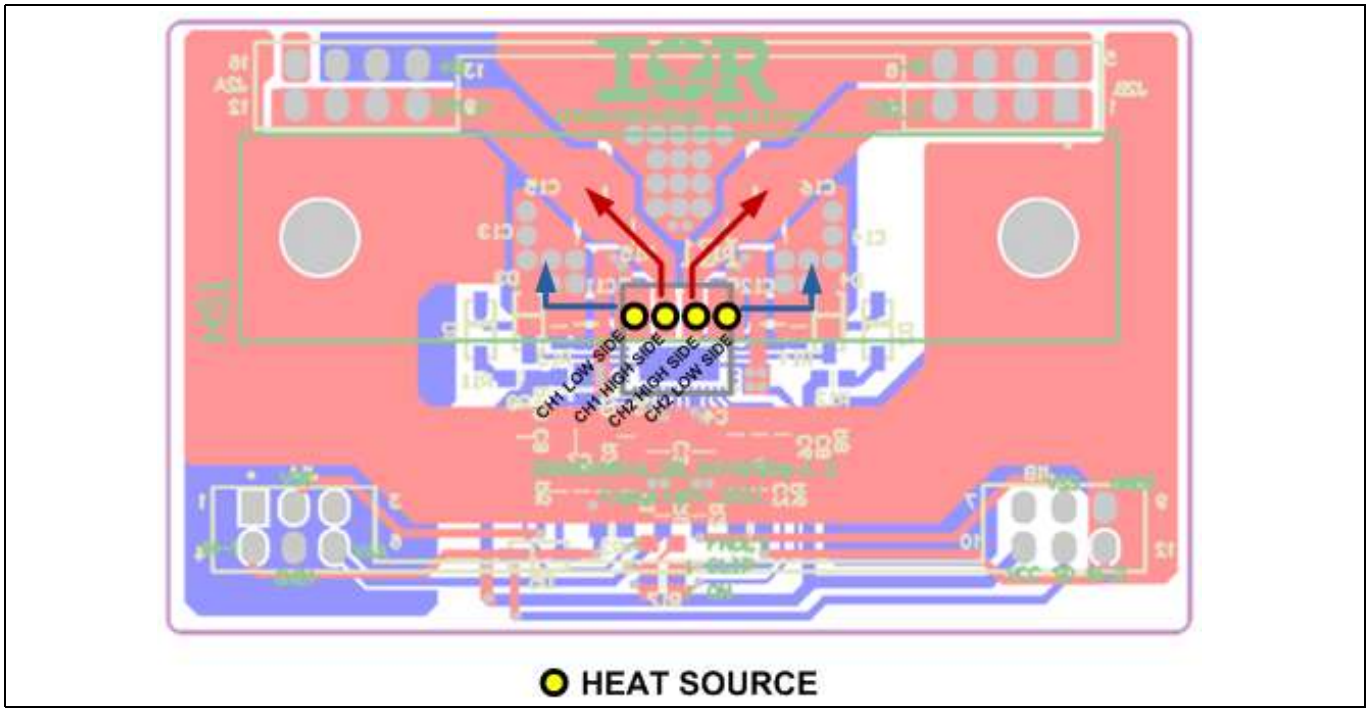


Figure 37 Heat source in IR43x2

8.2.2 Attaching heatsink

To achieve extended continuous peak power duration, attach a heatsink from the bottom of the PCB. Use a thick thermal interface material such as AAVID 4880G between the PCB and the heatsink to electrically isolate and thermally connect the heatsink. The effectiveness of attaching a heatsink is demonstrated in Table 3.

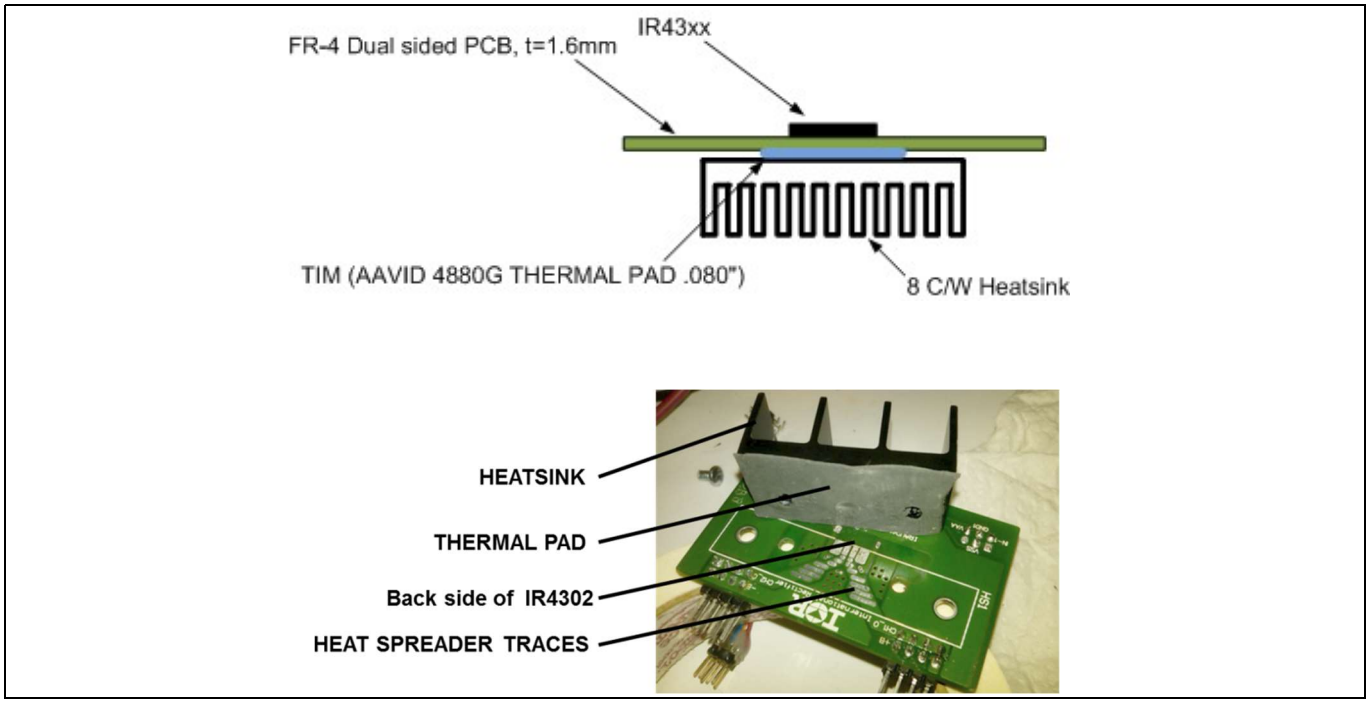


Figure 38 Example of heatsink

Table 3 IR4302 peak power duration (4 ohms load, +/-33.5 V, IRAUDAMP16)

Peak power	No heatsink	With heatsink
10 W	500 s	>500 s
20 W	80 s	>500 s
50 W	20 s	>500 s
100 W	10 s	200 s
150 W	5 s	50 s

Attention:

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Page or Reference	Description of change

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