Improving power density and efficiency in servers and telecom

The right MOSFET often makes all the difference

By: Milko Paolucci, Application Engineer, Infineon Technologies

The explosion of Internet applications and data usage has put a great deal of pressure on servers and their related infrastructures. This massive growth of resources poses questions on energy demand to the major Internet providers and server makers, increasing the demand for more efficient energy utilization.

Every wasted watt affects not only the electricity bill, but also thermal management efforts to keep the ambient temperature in the facility low. As a consequence, the need to reduce the cost of energy is independent of which server farm architecture is selected. In a server there might be several places where power losses occur, but in many cases the power supplies for the CPUs and memories are the most stressed components due to the high power requirements. Moreover, in some cases like blade servers, the possibility of cooling in the inner case is minimal due to the small form factor.

In the end, achieving an efficient server requires an efficient DC/DC converter, which is ultimately influenced by the selection of the power switches used in the step down converter. Manufacturers like Infineon Technologies are creating such products to enable engineers to create more efficient and compact servers, in this case their latest Power Block family of devices. Currently consisting of two switches in a 5.0 x 6.0 mm² footprint, the solution presents advantages versus the standard discrete solutions.

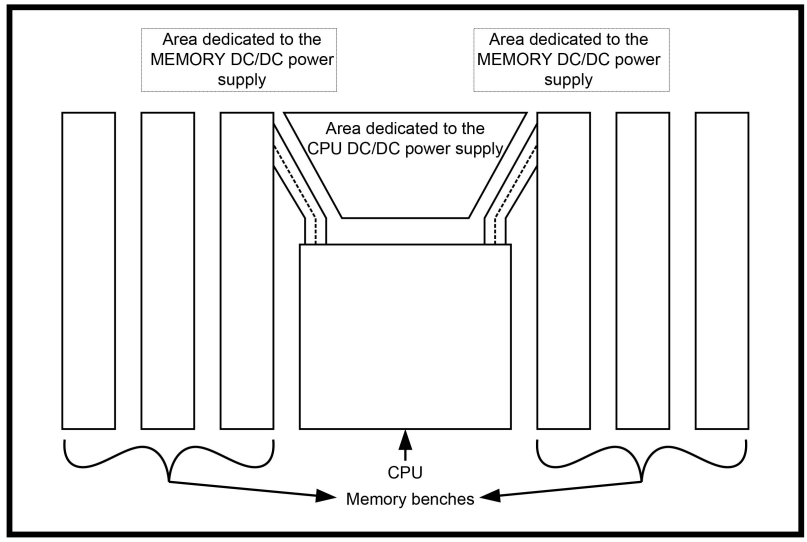

Figure 1: Simplified customer set-up

Before starting the design phase, it is important to fully understand the application requirements and their own priorities. The most important technical requirements for power converters in server and telecom applications come from the system and load specification.

Load profile and temperature

The load profile depends on the processor utilization, and thus on the kind of tasks required by the server. In many cases, the load can vary from several hundred amperes down to a few amperes. Since the load distribution is for most of the time at a medium-low load, it is important to maximize the efficiency in this range, without compromising too much at full load.

The ambient temperature inside a

Application requirements	Reference value	Condition
Efficiency and thermals	Increased T_J not above ~50°C Efficiency higher than ~90°C	At full load load range between 20% and 80% of full load
Area consumption	~ 1000 mm²	For a 5-to-6 phase solution
Transition time	~ns	Full load

Table 1: Summary of requirements for applications

case of the server is in the range of 50°C. Assuming a maximum temperature on PCB of around 100 °C permits a temperature increase of only 50°C to 60°C for the power stage due to power dissipation at full load. The maximum temperature on PCB depends on the material, construction and required lifetime of the PCB. 100°C is normally accepted as limitation for FR4 material.

Application real estate and switching time

The typical simplified set up in a server board is outlined in **Figure 1.** The area dedicated to the power supply for the CPU is basically trapezoidal shaped, defined mainly by the routing of the data connections between the CPU and server and the socket size of the server.

This shape determines the area for the power converter for the CPU, which generally consists of a multiphase buck converter with 4 – 6 phases. The number of phases depends on the power requirements; the area needed for the power converter is in the range of 1000 mm².

This area is also indirectly influenced by the switching frequency fsw: The higher the switching frequency is, the smaller is the area necessary for the passives used as a filter in the output. In order to have high fsw, it is important to have transition times in the range of a few ns; in today's designs the fsw is in the range of 500 kHz and the transition times are in the range of ns. The requirements for applications are summed up in **Table 1**.

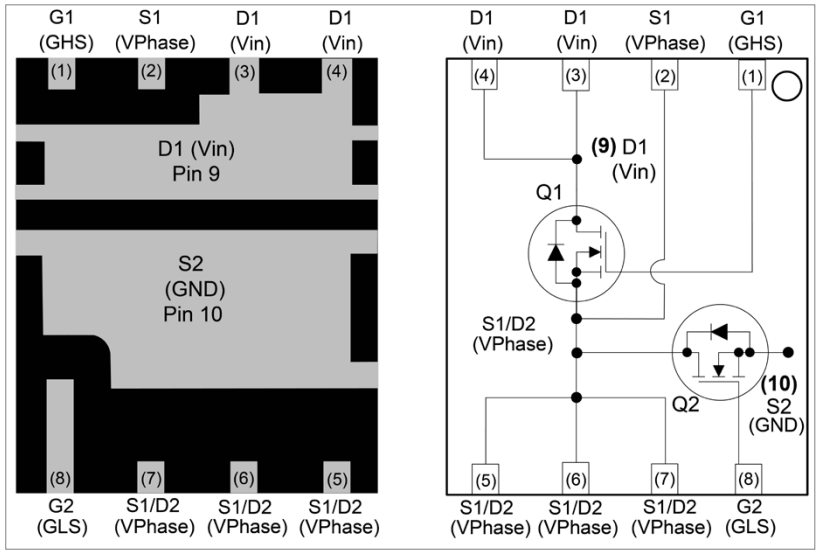

Figure 2: Pinout (left) and electrical connection (right)

These three requirements are interdependent. For instance, aiming at low power dissipation requires low resistances in the power MOSFETs. This might require increased area consumption, depending on the silicon and package technology. Vice versa, aiming at a small package might aggravate the conduction of the heat to the outside of the power stage.

Shrinking packages

In the past, the two MOSFETs used in buck converter topology were generally packaged in two different packages, e.g. SuperSO8 or S3O8, which measure 5.0 x 6.0 mm² and 3.0 x 3.0 mm², respectively. As silicon technology progresses, the die size is shrinking, allowing for smaller packages. With regard to these two MOSFETs, they can now be integrated in a single 5.0 x 6.0 mm² package, reducing the area consumption by 50% compared to the SuperSO8 solution.

The Power Block family is composed of three devices that are all sharing the same footprint with low side MOSFETs featuring different on-state resistance $R_{DS(on)}$ to better accommodate different load profiles. All products are housed in a 5.0 x 6.0 x 1.0 mm³ asymmetric dual-molded package with a pitch for

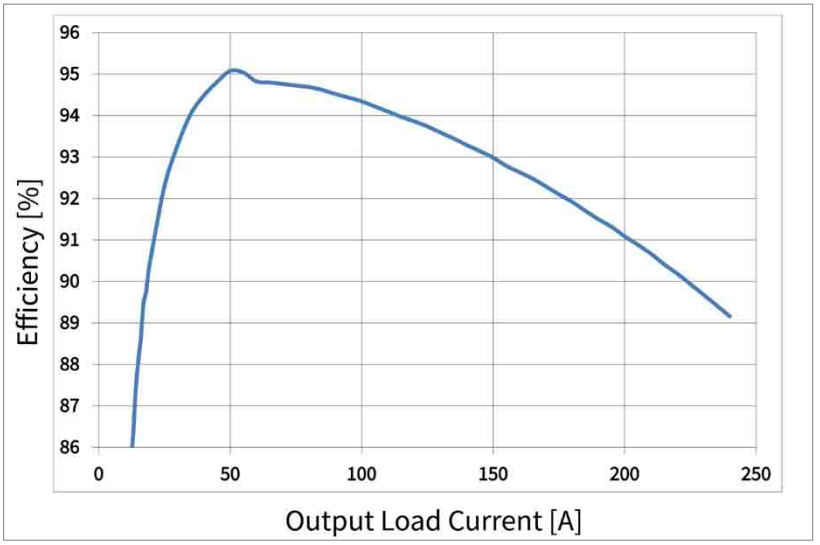

Figure 3: Efficiency curve of the 5-phase board

the pins of 1.27 mm.

Devices with a monolithic integrated Schottky-like diode improve the efficiency peak in the case of a driver with long dead time control (20ns).

Pinout and package size

Figure 2 depicts the pinout of the devices and the electrical connections. It can be clearly seen that the device is divided into two areas: the upper area is dedicated to the high side MOSFET. Pin 1 is dedicated to the gate connection. Pin 2 is used for the Kelvin connection to the driver. Whereas pins 3, 4 and 9 are dedicated to the drain of the high side MOSFET, which is connected to the input voltage, pin 9 delivers a good thermal connection to the PCB.

The bottom area of the device is dedicated to the low side MOSFET. Pins 5, 6 and 7 connect the middle point of the bridge (VPhase) to the inductor. Pin 8 is the gate connection for the low side MOSFET. Pin 10 is the source of the low side MOSFET and is generally connected to the ground of the PCB. This connection is intentionally increased in size, like for the high side MOSFET, in order to keep a very good thermal connection to the board. A reduced footprint for the power stage also leads to less parasitic inductance, improving the efficiency of the system at high switching frequencies.

Efficiency and thermal performance

The Power Block is optimized for server applications. It is in this regard that the efficiency and thermal performance of the device are described for the standard server conditions V_{IN} = 12 V, V_{OUT} = 1.8 V, f_{SW} = 430 kHz.

As shown in **Figures 3 and 4** the peak efficiency is approximately 95%, whereas the efficiency is around 91% in the range between 10% and 90% of the load. The junction temperature is measured at 62°C, with an increase of approximately 40°C. Adding the information about efficiency and temperature, thermal resistance Rth(j-a) can be calculated to be in the range of 5-10 K/W.

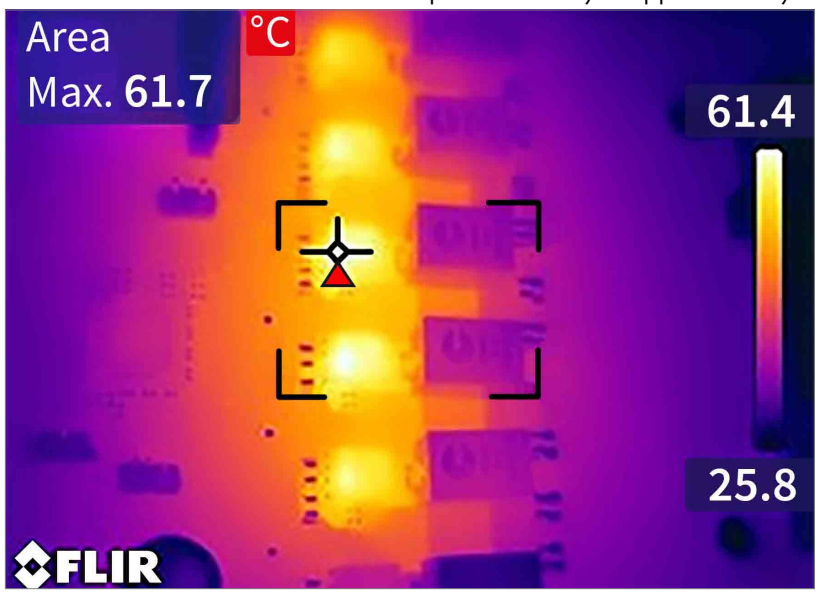

Figure 4: Thermal infrared picture of the 5-phase board at IOUT = 200 A

Application requirements	Reference value	Power Block
Efficiency and thermals	Increased T_j not above 50°C Efficiency higher than 90%	**40°C** **91%**
Transition time	~ns	4ns
Area consumption	No more than 1000mm²	1000-1200mm²

Table 2: Comparison between application requirements and Power Block performance

Obviously, the thermal resistance is not only product related, but also depending on the board and airflow conditions. Nevertheless, a very good thermal resistance is also associated with the fact that a device like the Power Block enables designers to realize a layout with very good GND connection and the Kelvin connection to the driver.

Layout area consumption and switching time

The area consumption is relevant for applications, which require high power density. The overall area consumption of the Power Block together with input and output capacitance and the power choke is in the range of 200 mm², which results in roughly 1000 – 1200 mm² consumption for 5 – 6 phases.

The Kelvin connection for the driver to the high side enables a fast transition between the ON and OFF state. For the Power Block, the rise time of the high side during turn-on has been measured as 4ns.This also helps to increase the switching frequency without losing too much efficiency. As an example **Table 2** compares the application requirements listed at the beginning and the results obtained by the tests performed.

In conclusion, devices such as the Power Block product family fit very well with most of the criteria listed, providing a very good solution in terms of power density, performance, flexibility, and easy design-in.

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