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# News



CoolMOS™

**Enabling faster charging  
in smaller form factors**



# Impact of $C_{oss}$ hysteresis losses in high-density adapter applications

## Why do we need fast charging hence high power density?

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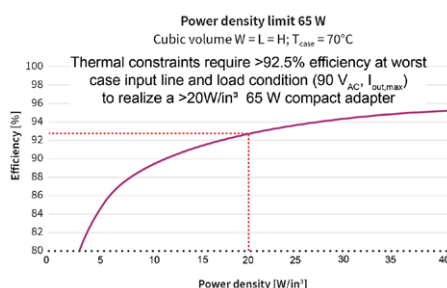
**N**owadays, more than ever in history, people rely on their devices. As they'd become portable, devices such as smartphones, tablets, and laptops conquer more and more space and time in our everyday life. Constant, limit- and borderless communication, connection and tasking due to the seamless and instantaneous access to other people and content around the globe became a living standard. But what impact does it have on the power semiconductor industry? These portable devices run on batteries, therefore, the fundamental prerequisite to be able to use them is to have a charger or adapter (depending on the power rating) to charge them. And this is where power microelectronics come into play. After establishing above that a charger/adapter is required to charge the battery of our (smart) devices, the next question is: how much time are we willing to spend on charging? The answer is pretty obvious: as little as possible. This is exactly the reason why fast charging is gaining more traction. But fast charging is only possible by increasing the power-delivery capability of a charger/adapter. In addition to the charging time, the weight of the charger is also a key consideration (the lighter the better it is simply because we usually have to carry them with ourselves). This is the reason why chargers/adapters with higher power density are required that can deliver more power without increasing their physical dimensions or weight.

### Enabling higher power density in chargers and adapters

In a completely enclosed adapter, any size-reduction through high switching frequency or package innovation must go hand in hand with efficiency improvements to maintain low component and adapter case temperatures. Figure 1 shows the relationship between power density and the minimum efficiency required to keep the adapter case temperature below 70°C for a 65 W adapter. It is evident that to increase the power density above 20 W/in<sup>3</sup>, the converter efficiency must be above 92.5 percent. Typically, for chargers and adapters with universal input range (90 V<sub>ac</sub> - 264 V<sub>ac</sub>) the most critical operating point to meet the minimum efficiency requirement is at:

- Maximum continuous output power
- Minimum input voltage (typically 90 V<sub>ac</sub>)

The reason for this is that at this operating point the conduction losses reach the maximum, resulting in a poorer overall efficiency compared to high input-line conditions.



**Figure 1**  
Correlation between power density and minimum efficiency required to keep the adapter case temperature below 70°C for a 65 W adapter

The single-switch QR flyback has been widely adopted in power adapter applications: it is operated in discontinuous conduction mode (DCM), achieving zero-voltage switching (ZVS) at low-line and partial hard switching at high-line. However, the hard-switching operation occurring at high-line together with the lack of recovery of the transformer leakage energy limits the maximum switching frequency at which the adapter can be operated.

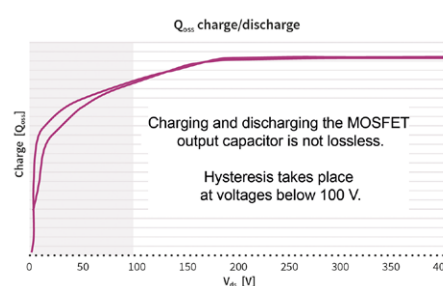
In order to overcome these limitations designers are moving toward topologies embedding the following features:

- Soft-switching (ZVS) operation, regardless of the input-line voltage and loading conditions
- Recovery of the transformer leakage energy

A well-known example of a topology satisfying both requirements above is the active clamp flyback (ACF). Soft-switching operation enables the elimination of turn-on losses and moving to relatively high switching frequencies (typically more than 120 kHz). At this point, the remaining main loss mechanisms affecting the MOSFET are turn-off losses, conduction losses and the so-called " $C_{oss}$  hysteresis losses", which will be described in the next section.

### $C_{oss}$ hysteresis losses

As already explained, in order to operate efficiently at the relatively high switching frequencies typically utilized in high-density adapters, soft-switching techniques are a must. Soft-switching techniques enable the operation of the device in ZVS, meaning that the MOSFET is turned on only after its drain-source voltage has reached 0 V (or a value close to 0 V). This strategy eliminates the turn-on losses of the device, which are typically the dominant contribution to the overall switching losses. Unfortunately, all High Voltage Superjunction (SJ) MOSFETs suffer from an additional type of losses due to the "non-lossless" behavior of the output capacitance. This means that when the MOSFET output capacitance ( $C_{oss}$ ) is charged and subsequently discharged some energy is lost, so even when operating in ZVS conditions, the entire energy stored in the output capacitance ( $E_{oss}$ ) is not recovered. This phenomenon is related to the hysteretic behavior of the  $C_{oss}$ , which can be observed between 0 V and 100 V performing a  $C_{oss}$  charge/discharge cycle with a large signal measurement, as shown in Figure 2. This is the reason why these losses are commonly known as  $C_{oss}$  hysteresis losses, in short  $E_{oss,hys}$ .



**Figure 2**  
Hysteretic behavior of the  $C_{oss}$

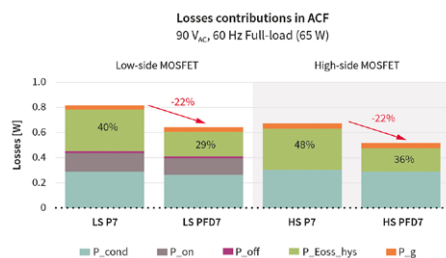
The power dissipation originated by the loss mechanism depends on:

- **Technology:** For the same chip size, thus  $R_{DS(on)}$ , different technologies show different  $E_{oss,hys}$ , as for instance CoolMOS™ PFD7 and CoolMOS™ P7.
- **Breakdown voltage:** For the same technology  $E_{oss,hys}$  increases with the voltage class, meaning that typically a 650 V device shows higher  $E_{oss,hys}$  than a 600 V device based on the same technology.
- **Switching frequency  $f_{sw}$ :** Since the charge and discharge cycle of the  $C_{oss}$  happens one time per switching cycle, the power dissipation originated by this loss mechanism is proportional to the switching frequency ( $f_{sw}$ ).
- **$R_{DS(on)}$  class:** Affecting the  $C_{oss}$  of the device, this loss is also dependent on the chip size, meaning that, for the same technology, MOSFETs with lower  $R_{DS(on)}$  will show higher  $E_{oss,hys}$  losses.

The 600 V CoolMOS™ PFD7 features 41 percent less  $C_{oss}$  hysteresis losses with respect to CoolMOS™ P7, offering a significant efficiency improvement in soft-switching applications.

## Dominant MOSFET losses contribution

In order to better estimate the impact of the  $C_{oss}$  hysteresis losses in the final application, a breakdown loss has been worked out by means of simulations and calculations. Figure 3 shows the impact of the different loss mechanisms to the overall losses of the high-side (HS) and low-side (LS) MOSFET in a 65 W adapter based on the ACF topology at low-line, full load, which, as already mentioned, is the most critical operating point for adapters from the thermal standpoint. The ZVS has been optimized to reduce the overall system losses, turning on the LS MOSFET at 25 V (partial ZVS), while the high-side operates in full ZVS.



**Figure 3**  
The impact of the different loss mechanisms to the overall losses of the high-side (HS) and low-side (LS) MOSFET in a 65 W adapter

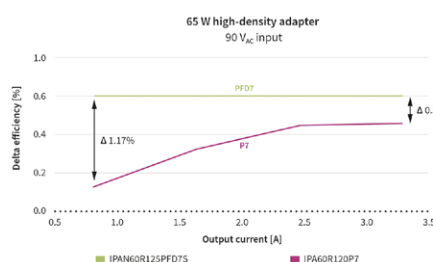
It can be observed that, when using a 120 mΩ 600 V CoolMOS™ P7 (IPA60R120P7) SJ MOSFET for both high HS and LS switches, the  $C_{oss}$  hysteresis losses account for 44% of the total MOSFET loss (HS + LS), while the second most significant contribution comes from the conduction losses which account for 40 percent. All the other loss mechanisms as gate driving losses, turn-on and turn-off losses account only for less than 20 percent of the overall loss.

Having established that the  $C_{oss}$  hysteresis losses have a major impact on the full-load efficiency at low line and being the 600 V CoolMOS™ PFD7 specifically optimized in respect to such losses, the natural consequence is to replace the CoolMOS™ P7 part (IPA60R120P7) with the new CoolMOS™ PFD7 (IPAN60R125PFD7S) counterpart in order to quantify the actual loss reduction in the application.

As shown in Figure 3, by replacing the CoolMOS™ P7 with the PFD7 the overall device losses are reduced by 22% (0.33 W), positively impacting the final efficiency of the adapter.

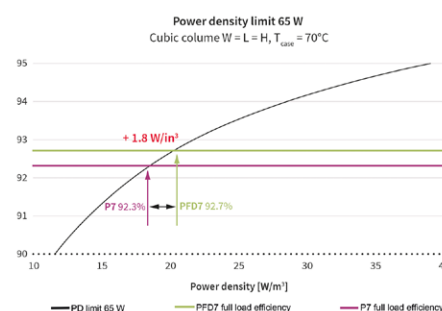
## Experimental results

In order to experimentally confirm the MOSFET loss reduction achievable replacing CoolMOS™ P7 with CoolMOS™ PFD7, extensive measurements have been performed on an ACF test board, operating at a switching frequency of around 155 kHz at low-line. Figure 4 shows the efficiency difference between CoolMOS™ P7 and CoolMOS™ PFD7: it can be observed that CoolMOS™ PFD7 provides a significant efficiency advantage across the entire load range. The efficiency gap between the two parts gets wider at light load and it decreases as the current increases. This is due to the fact that, while the contribution to the overall MOSFET losses of the  $C_{oss}$  hysteresis loss does not depend on the load, the conduction losses do. Therefore the impact on the efficiency of a MOSFET featuring lower  $C_{oss}$  hysteresis loss is even more evident under light load conditions.



**Figure 4**  
Efficiency difference between CoolMOS™ P7 and CoolMOS™ PFD7

Now considering the most critical operating point from the thermal standpoint which, as mentioned, is full-load low-line (90 V<sub>ac</sub>), CoolMOS™ PFD7 offers an efficiency improvement of 0.34 percent, which results in a MOSFET case temperature 5°C lower, reducing the risk of a hotspot on the adapter case. Another consequence of the improved efficiency is detailed out in Figure 5 where the power density limits enabled by the CoolMOS™ PFD7 and P7, assuming a maximum adapter case temperature of 70°C are shown. Thanks to the improved efficiency, PFD7 pushes the maximum power density limit above 20 W/in<sup>3</sup>, increasing it by 1.8 W/in<sup>3</sup> compared to P7.



**Figure 5**  
Power density improvement enabled by CoolMOS™ PFD7

## 600 V CoolMOS™ PFD7

In the previous paragraphs, we have seen that the  $C_{oss}$  hysteresis losses have a significant impact on the efficiency and subsequent power density of adapter applications. The 600 V CoolMOS™ PFD7 features reduced  $C_{oss}$  hysteresis losses, offering improved efficiency. Additionally, since it addresses the consumer segment its pricing has been tailored to this market.

## Infineon Technologies AG

For more information, please visit [www.infineon.com/PFD7-600V](http://www.infineon.com/PFD7-600V)