The Promise of GaN in Light of Future Requirements for Power Electronics

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Abstract

This paper will discuss the benefits of e-mode GaN HEMTs in low power and high power applications such as USB-PD adapter and server power supplies. In comparison to the next best silicon alternative, this paper will show quantitatively how much better systems being built with GaN devices will be. It will also provide further insight into corresponding topologies, choice of magnetics and switching frequencies to take the full benefit of the next generation of power devices.

1 Introduction

The commercial availability of wide band-gap power semiconductors with their significantly better figures of merit raises some fundamental questions on the agenda of many customers: How much better are system solutions based on these wide band-gap components in terms of density and efficiency? To what extent can silicon based solutions follow at the potential expense of more complex topologies and control schemes?

This paper tries to give answers to these questions for two major application fields, server power supplies for datacenter and compact chargers.

GaN HEMTs as lateral power devices have an order of magnitude lower gate charge and output charge compared to their silicon counterparts. Combined with virtually zero reverse recovery charge it enables hard commutation of reverse conducting devices. Thus, GaN supports simpler topologies and an optimization of control methods seamlessly changing between soft switching and (partial) hard switching. Even though hard commutation is acceptable for silicon based power devices in low and medium voltage classes, Superjunction devices as prominent technology in the 600V class prevent any such operation due to losses and voltage overshoots. The designer of AC/DC applications has three choices as next best alternatives to the use of wide bandgap devices: single ended topologies such as boost converter as a power factor correction stage, strict avoidance of hard commutation through corresponding control methods such as triangular current mode (TCM) operation in totem pole PFC, or the use of cascaded converter architecture where the voltage stress is distributed to several series connected converter stages.

While single ended topologies may not comply with efficiency targets, alternative solutions such as the dual boost may not comply with space or cost targets. Even though cascaded solutions have demonstrated their ability to reach both efficiency and density targets [1], control efforts remain challenging and may limit the use of this concept to the high power segment only.

The design options for highly efficient and compact server power supplies are narrowing down to silicon based TCM operation of interleaved totem pole legs versus a CCM/TCM GaN based totem pole stage followed by a DC/DC converter, typically being based on an LLC converter.

Vice versa the design options for compact chargers are significantly narrowing down when trying to overcome density targets of 20 W/in³ for a 65 W adapter. The need to recuperate the energy in the leakage inductance and to provide zero voltage switching in most or all operation conditions rules out much of the single ended topology choices.

In both examples being as diverse as a 65 W adapter or a 3 kW power supply this paper explores the value of GaN HEMTs in comparison to next best silicon alternatives.

2 Device concepts

As the race is set between GaN HEMTs versus their silicon counterpart, Superjunction devices being evidently the best alternative, let's start with a brief review of the latest technology achievements.

Superjunction devices have pushed for more than a decade towards ever lower on-state resistance [2], which in turn reduces the device capacitances and makes the devices inherently faster switching. **Figure 1** shows the output capacitance characteristics of three subsequent generations of Superjunction transistors versus an e-mode GaN HEMT. **Figure 2** shows the energy stored in the output capacitance.

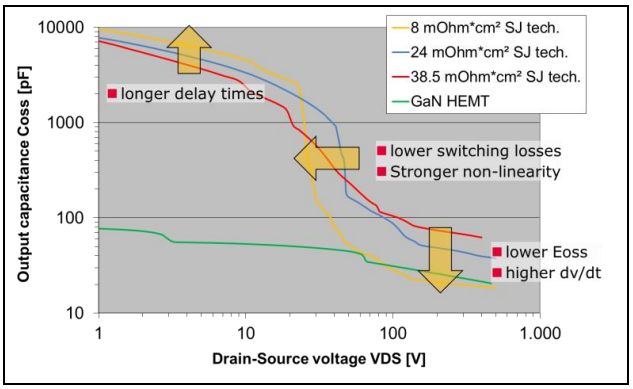

Figure 1 Development of the characteristic output capacitance of three consecutive technology nodes of Superjunction device in comparison to an e-mode GaN HEMT.

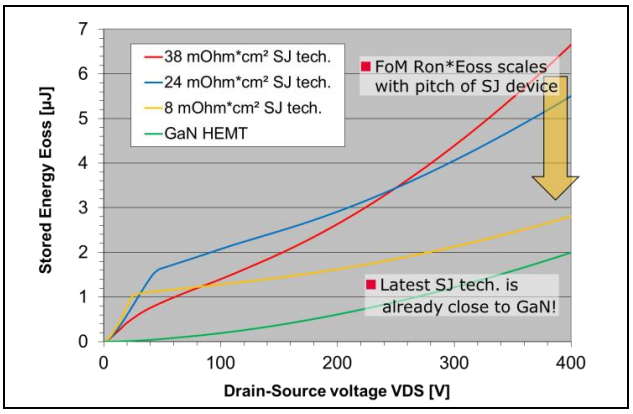

Figure 2 Trend for the energy stored in the output capacitance across three consecutive generations of Superjunction devices in comparison to GaN HEMTs.

Even though the output capacitance of GaN is significantly lower in the low voltage range, the energy stored in the output capacitance is comparatively close to the values achieved by Superjunction devices. Since this energy is dissipated as heat in every switching cycle during hard switching transients, it is already obvious from this graph that the true value of GaN will be in half bridge based circuits and will be limited in single ended topologies.

Figure 3 shows a comparison of the charge stored in the output capacitance as one of the key parameter for soft switching transitions.

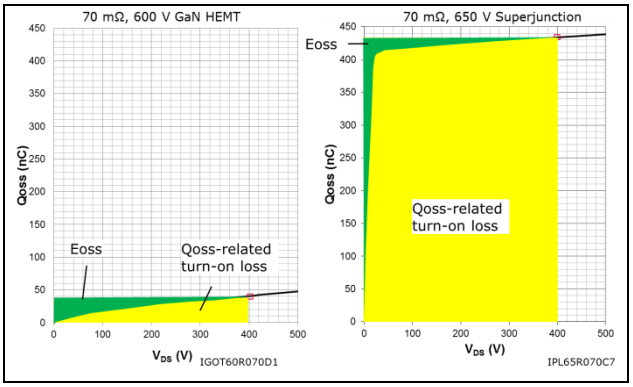

Figure 3 Comparison of Qoss versus voltage for an e-mode GaN HEMT (left) to an advanced Superjunction device (right).

Whereas in single ended topologies the E_{oss} parameter is governing loss mechanisms, in half bridge based circuits the charge stored in the output capacitance [3] and the reverse recovery charge is commanding the losses. While Superjunction devices are optimized for an extremely low E_{oss} figure of merit, GaN HEMTs offer a much more favorable Q_{oss} figure of merit, with the first generation already being one order of magnitude better than their silicon counterparts.

3 Application examples

To evaluate, quantitatively, the performance improvements offered by wide band-gap power devices, multi-objective optimizations were performed for each application. This method allows us to consider all available degrees of freedom in the converter design such as various topologies, interleaving of stages, switching frequencies, and semiconductor usage, and yields as a result for each potential design efficiency and power density. Such an analysis reveals an envelope function with all Pareto optimal designs and allows an assessment of the trade-off between efficiency and density for an entire application [4].

3.1 Server power supplies

The emergence of cloud based internet services, artificial intelligence, and cryptocurrency has initiated a strong growth of processing power in data centers around the world. Since the data centers are also facing rising electricity and real estate prices, there is a clear trend towards highly efficient and compact server supplies. These new power supplies do not only lead to a lower power consumption of the server, but also to a lower heat dissipation reducing secondary costs such as the cooling of the servers.

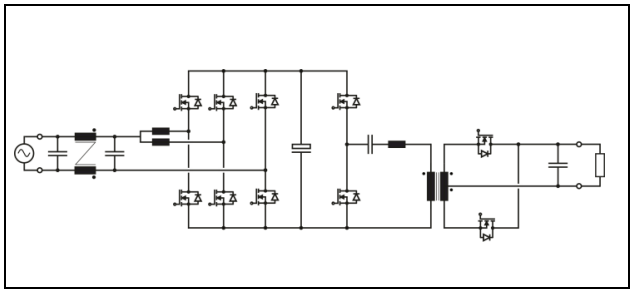

Figure 4 Server supply comprising a totem-pole AC/DC rectifier with two interleaved high-frequency bridge legs and an LLC DC/DC converter with center-tapped transformer.

Typically, state-of-the-art high efficiency power supplies are comprised of a bridgeless PFC stage such as a totem-pole stage and a resonant DC/DC stage such as an LLC converter (see **Figure 4**). For an output voltage of 12 V typically a center tapped transformer is used, while for 48 V systems a full bridge rectification should be considered. The specifications of a server supply are given in **Table 1**.

Table 1 Specifications of server supplies

Parameter	Variable	Value
Input voltage	V_{in}	180 V – 270 V
Output voltage	V_{out}	12 V / 48 V
Rated power	P_{out}	3 kW
Hold-up time	T_{hold}	10 ms

3.1.1 12 V server supplies

Currently, a majority of data center operators are running their server boards on 12 V DC input. In the legacy architecture, Uninterruptible Power Supplies (UPS) will provide back-up power to two independent AC distribution schemes throughout the datacenter. In a classic server board two AC/DC power supplies provide redundancy to each other, each power supply being sufficient to cover the full power demand of the server board.

The need for lower operational cost and more payload per rack to save on capital expenditure will drive two major transitions: first, local energy storage on rack level to cut out the UPS from the power flow, second, the transition from server based power supplies to rack based power supplies to cut redundancy from 1+1 to n+1, thus saving cost. Both trends favor higher output power in a given form factor. Hence, the focus of this study is to analyze benefits of GaN HEMTs towards power density.

A bridgeless topology is used, in this case the totem pole configuration, both for silicon switches and GaN HEMTs. Using silicon devices mandates operation in TCM at all times, whereas, different modulation schemes can be selected for GaN HEMTs. The capability to operate the GaN switches in both hard and soft-switching allows the totem pole rectifier to operate in continuous conduction mode (CCM), triangular conduction mode (TCM), or optimal frequency modulation (OFM). The OFM is a seamless transition between hard and soft-switching over a grid period depending on the power level and/or grid voltage [5].

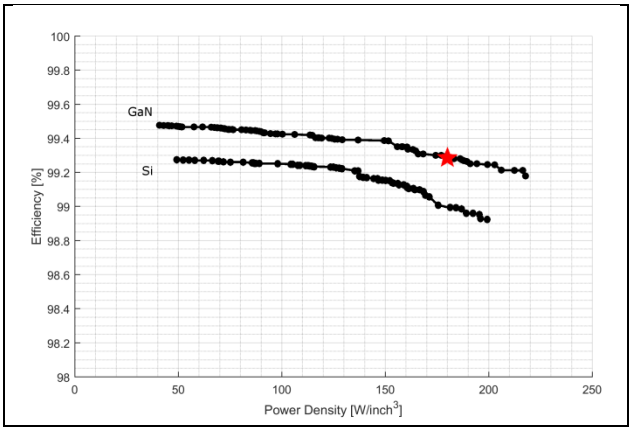

Figure 5 Optimization results for the totem pole PFC stage, including the EMI filter, with GaN or Si.

A comparison of the optimization results for a Si totem-pole rectifier stage (including the EMI filter) operated in TCM and a GaN totem pole stage operated in TCM or CCM is shown in **Figure 5**. Both systems are optimized for 50 percent of the rated power and evaluated at nominal operating voltages. In the results, the volume of the power electronics including the PCB and additional air between the components is considered, excluding the case. The results clearly indicate the improved performance of the GaN designs, especially in the area of high power density. An analysis of the designs using GaN transistors reveals that the TCM modulation offers a benefit compared to CCM specifically in the region of highest power density.

In a similar manner, the LLC stage has been optimized for Si and GaN semiconductors. The results are shown in **Figure 6**. As can be seen, GaN provides a simultaneous improvement of efficiency and power density.

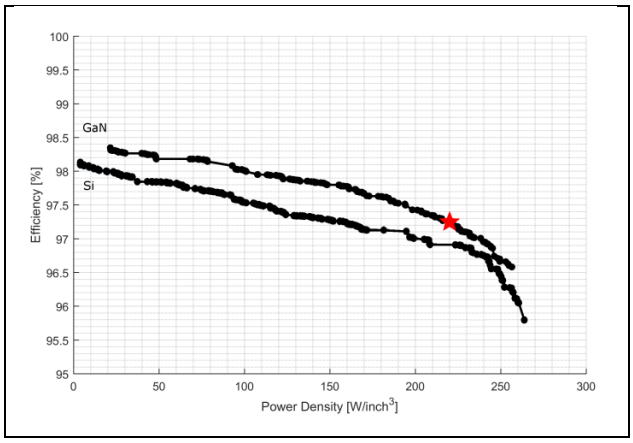

Figure 6 Optimization results for the LLC stage with GaN or Si.

Finally, the optimization results of the entire systems are shown in **Figure 7**. The results include all power electronic components, auxiliary electronics, PCB and 20 percent of additional volume which was added to account for non-ideal placement of the components. The connectors and the casing with standoff are not included.

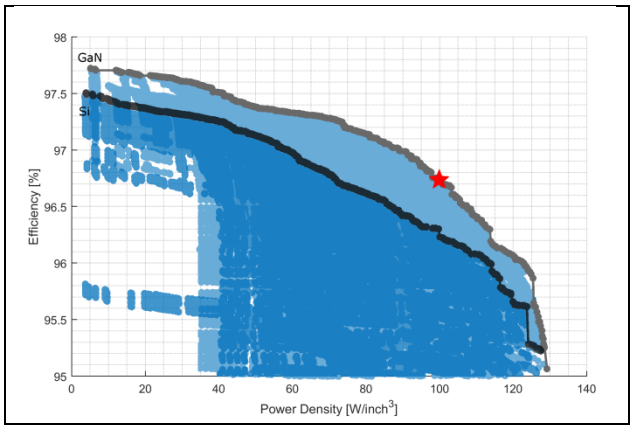

Figure 7 Optimization results of the entire 12 V server supply for either GaN or Si semiconductors.

The result clearly indicates a path towards 3 kW in a given form factor such as the 68 mm × 41 mm × 184 mm flex slot size, thus nearly doubling the output power in this box size. Comparing to off the shelf solutions delivering 1600 W in this form factor, we not only nearly double the power but increase efficiency in average by 4 percent without increasing dissipated heat within the power supply (see **Figure 8**).

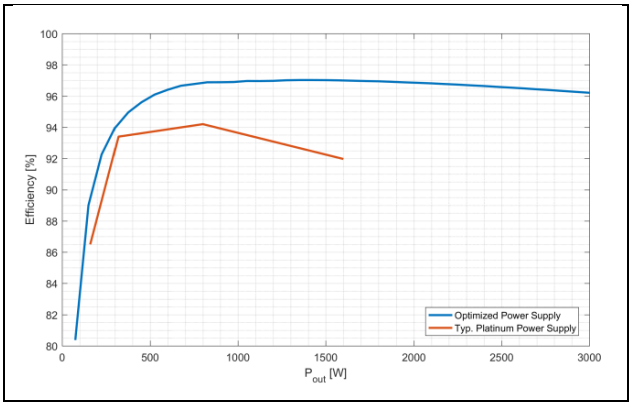

Figure 8 Evaluation of the 12 V GaN server supply with a power density of 100 W/in^3 in dependence of the output power.

3.1.2 48 V server supplies

The emerging use of artificial intelligence in computer science and the training of the corresponding neural networks has shifted the computational architectures from pure CPU-based servers to more specialized platforms with a very high degree of parallel data processing, e.g. employing GPUs. As a result of this trend, the power consumption per rack has roughly tripled now, pushing the power per rack to 20 kW and above. This power level can no longer be economically handled by classic 12 V distribution rails. As a solution, power distribution within the rack on 48 V level instead of 12 V will be more widespread in the future.

Since the 48 V server supplies are mainly targeting applications, being optimized for total cost of ownership (TCO), the performance of GaN in these systems is evaluated purely from an efficiency perspective.

As a basis for the comparison an industrial 48 V Si power supply with P_{rat} = 3 kW is taken as reference. This power supply features a peak efficiency of 97.1 percent at half of the rated power and a power density of around 33 W/in^3. Power supplies like these typically comprise a dual boost AC/DC rectification stage followed by an LLC.

As a first step of improvement, the AC/DC stage can be changed into a totem pole rectifier with one high frequency bridge leg. This is enabled by the use of GaN switches ($R_{DS(on)25,max}$ = 70 mΩ) in the high frequency bridge leg, and Superjunction MOSFETs with very low on-state resistance in the low frequency bridge leg. As addressed before, GaN HEMTs offer a choice of different modulation schemes.

The achievable Pareto front for CCM operation at nominal operating voltages (V_{in} = 230 V, V_{out}= 48 V) and 50 percent power level is shown in **Figure 9**.

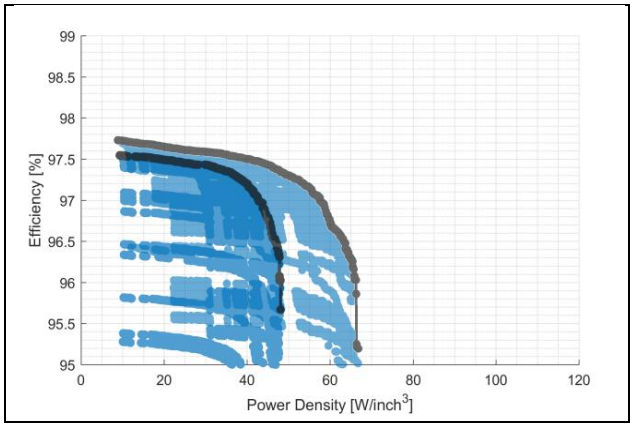

Figure 9 Pareto-front of the state-of-the-art 48 V power supply at 50 percent load and nominal operating voltage. The performance improvement offered by interleaving two GaN HF bridge-legs is overlaid.

As a second step of improving the efficiency of the AC/DC stage, several possibilities exist:

- Using two interleaved HF bridge-legs in the totem pole
- Increasing the chip area of the HF and LF switches
- Operating the totem-pole in TCM

A cost analysis of the different options reveals that the most cost effective performance improvement is achieved by interleaving two HF bridge legs using CCM control. This cuts the average current in each HF bridge leg by a factor of 2, which has two major benefits:

- The reduced RMS current significantly lowers the conduction losses in each HF branch (i.e. inductor and GaN switches).
- Natural ZVS can be achieved more easily when the HF current ripple (peak-peak) is larger than twice the average current, thereby reducing the switching losses.

The performance improvement is shown in **Figure 9** by the overlaid opaque Pareto front. The introduction of TCM to achieve ZVS over the whole grid period, would allow the chip area to be increased for a further reduction of conduction losses. This is a rather costly implementation, however, since the additional chip area and the optimization of the boost inductors for larger ripple currents with thin strands adds significant cost and control complexity with an improvement potential of only around 0.1 percent at the considered level of power density. Hence, CCM control is the option of choice for efficiency driven converter designs.

In the LLC stage, there are also several improvement options. Similarly, the optimization flow is based on an industrial design using 31 mΩ fast body diode-type Superjunction devices at a relatively low switching frequency.

As a first measure, the primary side half-bridge is equipped with 35 mΩ GaN switches. The system efficiency can be increased by around 0.3 percent by optimizing the resonant tank with one order of magnitude lower Q_{oss} charge on the switches, which includes adjustments of the resonant frequency and the magnetizing inductance.

On top of this, efficiency can be further improved by another 0.3 percent by changing the transformer setup to a matrix structure using two cores with series connected primary windings and parallel connected secondary side windings. This approach offers several advantages for the conversion efficiency:

- The high output current of the single transformer configuration is split among the two outputs. Under the assumption, that both configurations have comparable termination resistances, the total termination losses can be significantly lowered with the matrix transformer setup.
- Due to lower currents in each transformer, also the electrical fields that cause proximity effect losses are reduced in each transformer.
- The use of two synchronous rectification stages leads to a spatial distribution of the losses of the synchronous rectification MOSFETs which is beneficial especially from a thermal perspective.

The input series-output parallel connection of the matrix transformer setup is inherently stable as it guarantees equal splitting of the primary voltage among the series connected primary terminals, and equal output current splitting among the secondary terminals of the transformers. Caution has to be taken to reduce the leakage inductance of each transformer such that it does not affect the resonance behavior of the LLC. The total systems cost will only marginally increase through this step.

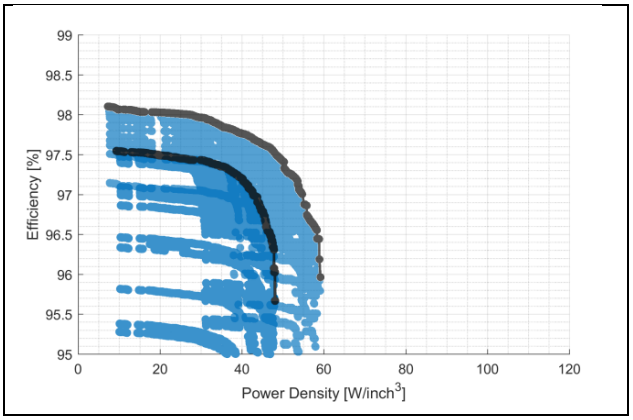

Figure 10 Performance improvements of the 48 V server supply provided by utilizing 35 mΩ GaN as primary switches in the LLC and a matrix transformer configuration.

As a further measure for performance improvements, the secondary side of the transformers can be changed from center-tapped into full-bridge rectification circuits. On the one hand, this leads to a better copper utilization in the transformers, and on the other allows to use synchronous rectification MOSFETs with a lower voltage rating and thus with a better figure-of-merit. With this configuration, the transformer and synchronous rectification losses can be further reduced, but at the expense of increased system cost.

By combining the most cost effective performance improvement options of the PFC (i.e. two interleaved HF bridge legs with 70 mΩ GaN HEMTs in CCM operation) and of the LLC stage (i.e. 35 mΩ GaN HEMTs on the primary side and matrix transformer configuration), the total system peak efficiency can be increased by 0.8 to 0.9 percent to a level of around 98.2 - 98.3 percent. Using the full potential of all available performance improvement methods allows the efficiency of the entire system to increase up to 98.5 percent, giving a power density around 30 to 35 W/in^3.

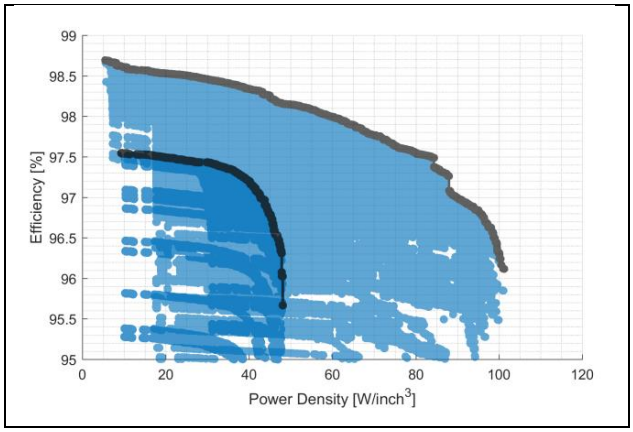

Figure 11 Achievable Pareto-front of the entire 48 V server power supply with all improvement options of the PFC and LLC incorporated.

3.2 Universal mobile device charger

The growing popularity of mobile electronics devices such as laptop, mobile phones, tablets, e-book readers and smart watches has led to a wide range of different charger types. In order to reduce electronic waste and to simplify the user experience, the need for a universal adapter with high efficiency and high power density has become evident. For this purpose the USB-PD standard has been introduced which supports a wide range of output voltages (5 V to 20 V) with power levels up to 65 W.

To identify the most suitable topology for a high density USB-PD adapter, several topology options have been evaluated by means of multi-objective optimizations. The considered topologies include: PFC flyback with secondary side power pulsation buffer, flyback converter with a fixed (high) output voltage and subsequent buck converter, flyback converter with wide output voltage range, cascaded asymmetrical PWM flyback where the primary side consists of two cascaded half-bridges, and asymmetrical PWM flyback. The optimization results are shown in **Figure 12** for full load operation at worst case input voltage (V_{in} = 90 V) and highest output current (I_{out} = 4 A). In

addition, the thermal limit line is shown, which defines the minimum efficiency required for a given power density in order to keep the surface temperature of the adaptor below 70 °C. Only designs above this line possess the necessary efficiency required to dissipate the generated heat passively (i.e. natural convection and radiation) without exceeding the thermal limit of the case. This clearly shows that the target of highest power density is inevitably linked to highest conversion efficiency, underlining the necessity of a comprehensive multi-objective optimization approach.

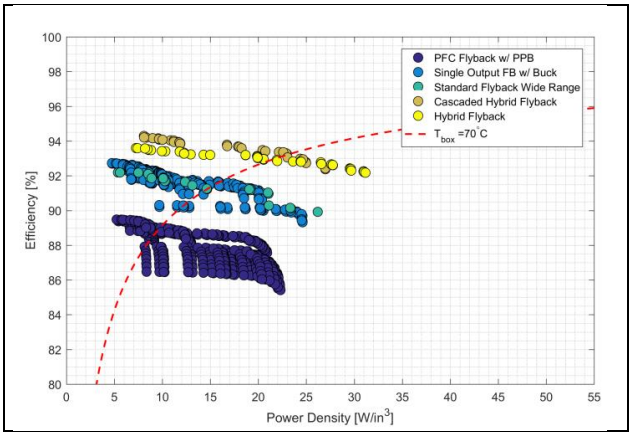

Figure 12 Multi-objective optimization results of several different adaptor concepts for full load (P_{out} = 65 W), V_{out} = 20 V and low line (V_{in} = 90 V) operation.

The optimization results reveal the asymmetrical flyback (see **Figure 12**) is the best suited topology among the considered candidates for highly compact chargers since it offers the highest efficiency. This topology features ZVS of the primary side half-bridge by utilizing the magnetization current, and ZCS of the synchronous rectification switch, laying the foundation for highest conversion efficiency. The converter is operated with a fixed ON-time of the low-side switch of the primary half-bridge, which is determined by the resonance frequency, and a varying ON-time of the high-side switch, which depends on the output voltage [6]. This results in a varying switching frequency.

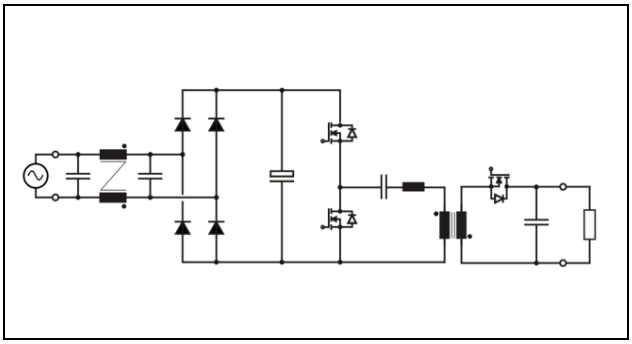

Figure 13 Asymmetrical PWM flyback with synchronous rectification.

Based on the optimization results, a 65W prototype employing 500 V/140 mΩ MOSFETs has been developed (see **Figure 13**) [7]. It supports USB-PD with different output voltage profiles ranging from 5 V / 3 A to 20 V/ 3.25 A. The operation frequency varies from 100 kHz to 220 kHz depending on the input and output voltages. The prototype achieves a maximum efficiency of 94.8 percent, while the lowest full-load efficiency at V_{in} = 90 V is 93 percent as shown in **Figure 15**.

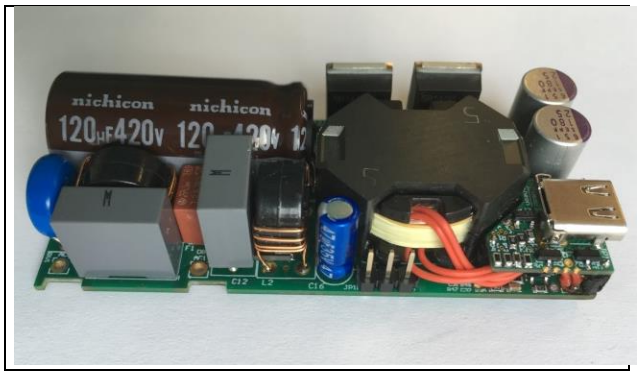

Figure 14 Prototype of the 65 W USB-PD adapter based on the asymmetrical PWM flyback topology. The prototype features a power density of 27 W/in^3 (cased: 20 W/in^3).

To push the power density to even higher levels, the use of GaN HEMTs becomes mandatory, as they allow the efficiency of the converter to be increased and thus to move away from the thermal limit. The first advantage of GaN is given by the greatly reduced Q_{oss} charge, which enables ZVS with lower magnetizing current. Thus, the conduction losses in the switches as well as the transformer can be reduced. Furthermore, due to the lower gate charge the gate driving losses are reduced. Last but not least, the losses associated with the charging/discharging of C_{oss} capacitance of the switches during ZVS are also lower in GaN HEMTs than in Superjunction MOSFETs [8]. As a result, the efficiency of the entire system can be increased by around 0.4 percent at full load over the entire input voltage range, as depicted in **Figure 15**.

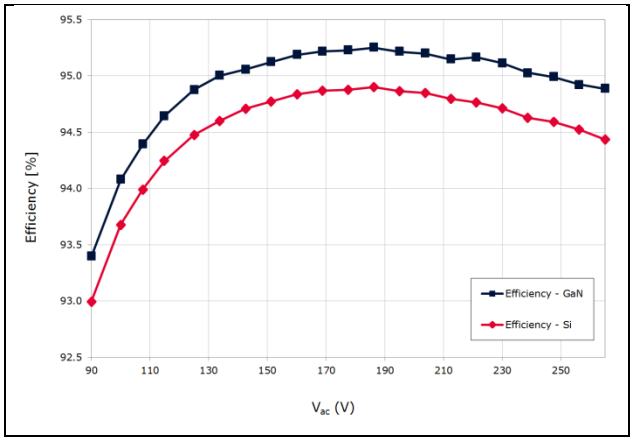

Figure 15 Red curve: Measured full load efficiency (P_{out} = 65 W) of the prototype in dependency of the input voltage for an output voltage of V_{out} = 20 V. Blue curve: Efficiency improvement possibility with 600 V/190 mΩ GaN HEMTs instead of 500 V/140 mΩ Si MOSFETs.

4 Summary

The application studies performed show a clear value for e-mode GaN HEMTs in a wide range of applications spanning low power adapters to high power server designs. GaN HEMTs allow us to push both efficiency and density frontiers.

This paper demonstrated a path towards 98.5 percent efficiency in 48V servers and towards a density of 100 W/in³ for 12 V servers thus offering large benefits in terms of OPEX and CAPEX savings.

For mobile applications GaN offers hitherto unachievable small form factors beyond 20 W/in³ for 65 W USB-PD adapters.

5 Literature

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