

Advantages of the 1200 V SiC Schottky Diode with MPS Design

Single- and three-phase inverters in solar, UPS or energy storage applications today demand for high efficiency, compact designs and extended reliability.

Inverter implementation in these applications is limited by silicon devices' high dynamic losses when operated at 1200 V. Alternative designs using 600 V/650 V devices can partially improve efficiency. However, they come at the expense of more complex topologies with special control schemes and high component count.

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A Silicon Carbide (SiC) Schottky diode has no real reverse recovery charge. Thus a hybrid set of 1200 V SiC diode and 1200 V Silicon (Si) IGBT enables simpler 2-level topologies by reducing the diode turn-off loss as well as dramatically lowering the turn-on loss of the Si IGBT. In this setup the static losses of the SiC diode often limit the optimization potential of Si IGBT/SiC diode solutions. To overcome this limitation, the new generation 5 diode from Infineon comes with a reduction of forward voltage and its temperature dependency to reduce static losses. This article describes how consistent innovations in device design and assembly techniques improve diode performance, reliability and cost position resulting in easier system implementation for efficient, reliable and robust inverter designs.

Zero reverse recovery charge – the signature of SiC Schottky diodes

Silicon pin diodes are bipolar devices depending on the injection of minority charge carrier which are characterized by a large reverse recovery charge. During conduction state of the diode, charge carriers are injected into the device and need to be removed from the device before a voltage can be blocked or, in other words, a space-charge region can be built-up. A higher charge carrier concentration will result in a high reverse recovery charge. Moreover, reverse recovery charge

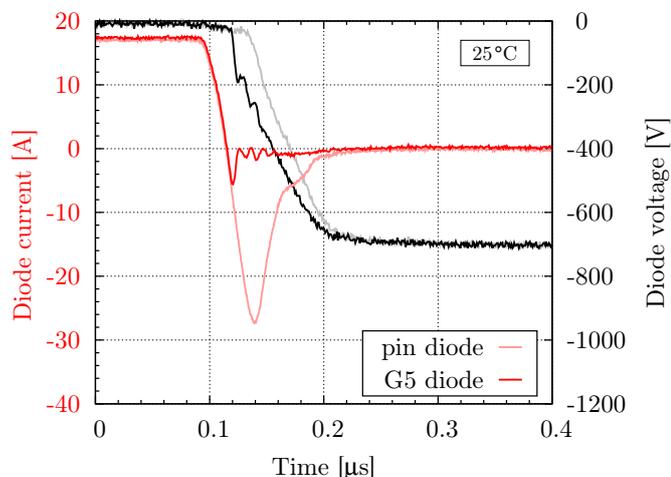


Figure 1: Reverse recovery behavior of a fast state of the art 1200 V Si-pin diode and SiC Schottky diode generation 5 (G5). $V_{DC}=700$ V, switch: 1200 V IGBT, $di/dt=1300$ A/ μ s, losses: 50 μ Ws for G5, 190 μ Ws for Si-pin diode. Reverse voltage applied to the diode is represented in black curves.

is dependent on forward current and device junction temperature. The advantage of using SiC Schottky diodes being a majority carrier device is that they virtually show zero reverse recovery charge. Looking at the switching waveforms in Figure 1, the reverse recovery current peak is very small compared to a fast Si pin diode. Only the displacement current from the junction capacitance is visible. This leads to significantly lower turn-off losses. Moreover, since the dynamic characteristic of a Schottky diode is capacitive in nature, the reverse recovery characteristic of a SiC Schottky diode is independent from forward current, di/dt and device junction temperature.

Static loss reduction and improved thermal performance

The new 1200 V SiC Schottky diodes implement a merged pn-Schottky (MPS) structure, representing the same technology base as the latest 650 V diode generation. To better understand this MPS design, the anode side of a SiC Schottky diode is shown in Figure 2. The blocking capability of a SiC diode during reverse voltage application is provided by a drift layer. This layer is also a major contributor to the overall resistance of the device. In this regard, it is best to lower the drift resistance to lower the forward voltage when the diode is conducting. A higher drift layer doping (n) lowers the resistance but at the expense of higher device leakage current.

Introducing p^+ islands in this structure additionally shields the electric field from the Schottky contact thus reducing the leakage currents. Hence, using MPS structure enables lower overall resistance by increasing drift layer doping without significantly increasing the leakage current.

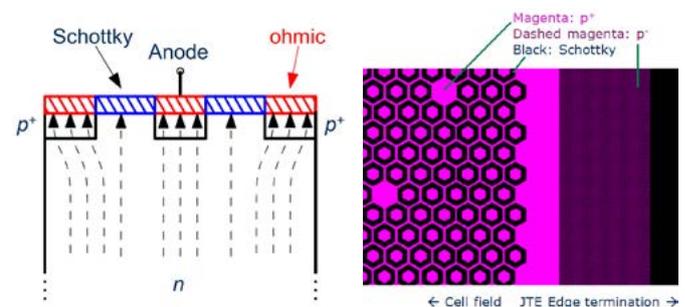


Figure 2: 1200 V thinQ!™ SiC Schottky diode generation 5 design. MPS (merged-pin-Schottky) structure combines the shielding of the electric field from the Schottky barrier and an increased surge current capability by hole injection. Dashed lines (left) show current density at higher currents. Cell design (right) of an optimized cell structure with hexagonal p^+ islands.

The new diode with MPS design enables a 50 percent reduction of drift resistance compared to the previous Schottky design. In Figure 3 the corresponding forward voltage contributions at 600 A/cm² are compared. Current densities of a final product are usually lower and mainly depend on the achievable thermal resistance R_{th} of the packaging vehicle. The reduction in drift resistance results in a mild increase in forward voltage with temperature. The forward voltage of generation 5 diodes only increases by 35 percent when the temperature is raised from 25 °C to 150 °C, significantly lower than the 60 percent increase in previous generation using Schottky design.

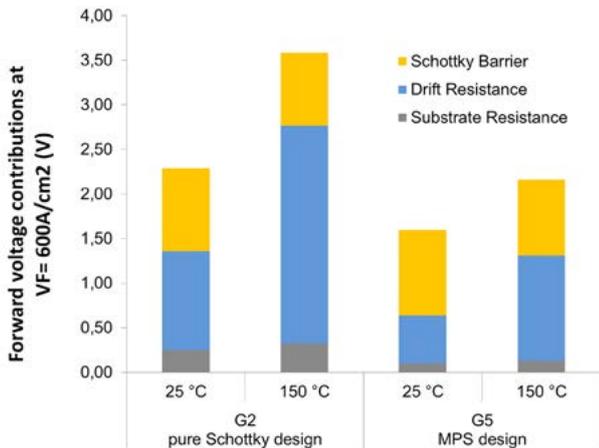


Figure 3: Comparisons of resistive contributions to forward voltage of a Schottky diode design and MPS design at junction temperatures 25 °C and 150 °C.

Massively increased surge current handling

Another positive side effect of the MPS design is the increased surge current capability. At higher currents the built-in voltage of the p+ islands in n-junction is overcome and holes are injected into the drift layer. The diode becomes bipolar in terms of forward characteristics, as shown in Figure 4. Due to this design, Infineon’s generation 5 1200 V SiC Schottky diode is able to withstand surge current levels more than 15 times the nominal current for a typical 10 ms sine half-wave.

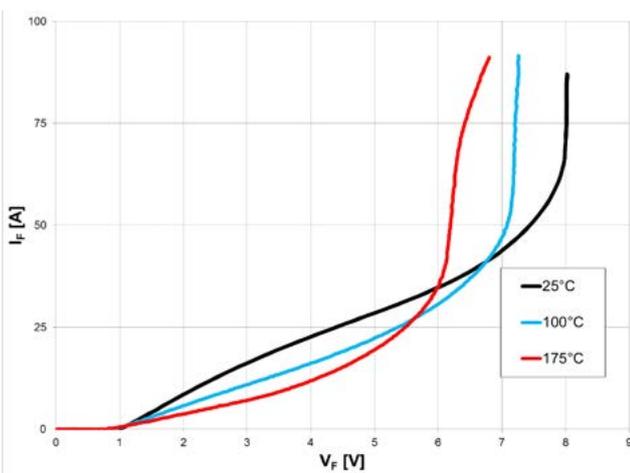


Figure 4: I-V curve of a 5 A rated generation 5 1200 V SiC Schottky diode (TO-220) at high currents.

Thin wafer technology for lower forward voltage and improved thermal performance

To provide mechanical stability to the semiconductor device, a substrate is used which is depicted in Figure 5 as a schematic cross section of a SiC Schottky diode. The substrate resistivity labeled as

R_{bulk} is also a contributor to the diode’s total differential resistance. The thickness of this substrate has a direct impact on the forward voltage when the diode is conducting. It is therefore best to reduce this thickness to lower the forward voltage while considering mechanical stability.

The well-established thin wafer technology allows for the reduction of the substrate thickness to around one third compared to the original layout. With this thickness, the reduced total differential resistance leads to a 150 mV to 200 mV reduction of typical forward voltage for the identical chip sizes.

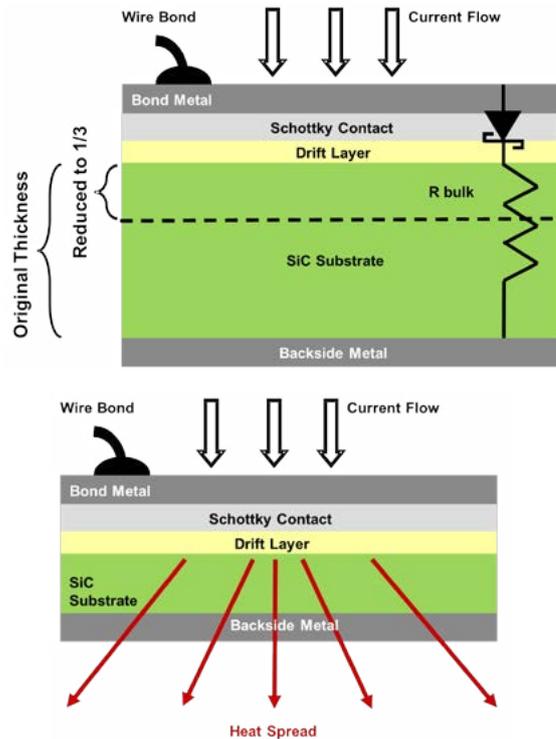


Figure 5: Schematic representation of a SiC Schottky diode indicating thick and thin wafers and showing the thermal path for the heat generated in the junction of the diode. Merged pn junction is not represented for simplicity.

Besides the reduction of the forward voltage, the reduced chip thickness also leads to an improved thermal resistance which, in return, is beneficial for the power dissipation of the device. Obviously, a thinner substrate layer offers a shorter thermal path for the heat generated inside the Schottky junction and drift layer of the diode. The heat spread from the junction is enhanced, thus reducing the thermal resistance between junction and the package lead-frame or case. This holds true especially if sophisticated low R_{th} die attach techniques like diffusion soldering are used. In addition, the thin substrate enhances the propagation of the thermal flux not just only vertically but also laterally as shown in Figure 5b. The reduction in thermal resistance thus corresponds to an equivalent increase of power dissipation for the same case temperature. However, it has to be kept in mind that by wafer thinning the “junction-near” thermal capacitance (C_{th}) is reduced. Regarding short-time events like surge current there is a trade-off between the reduction of forward voltage drop and the reduction of C_{th} .

Experimental results in a boost topology

The performance of SiC and Si diodes was evaluated in a boost circuit. The test setup has an input voltage of 400 V_{DC} and an output of 800 V_{DC} capable of delivering 3000 W output power. 1KW25N120H3,

a 25 A 1200 V IGBT from Infineon is used as a boost switch switching at 20 kHz. A commercially available 18 A ultrafast Si diode commonly integrated for this output power range was used. The boost inductor has an inductance value of 2.5 mH. Figure 6 plots the efficiency curves and boost diode case temperature as a function of the output power for a 10 A SiC and 18 A Si diodes used as boost diode. The tests were performed at an ambient temperature of 25 °C.

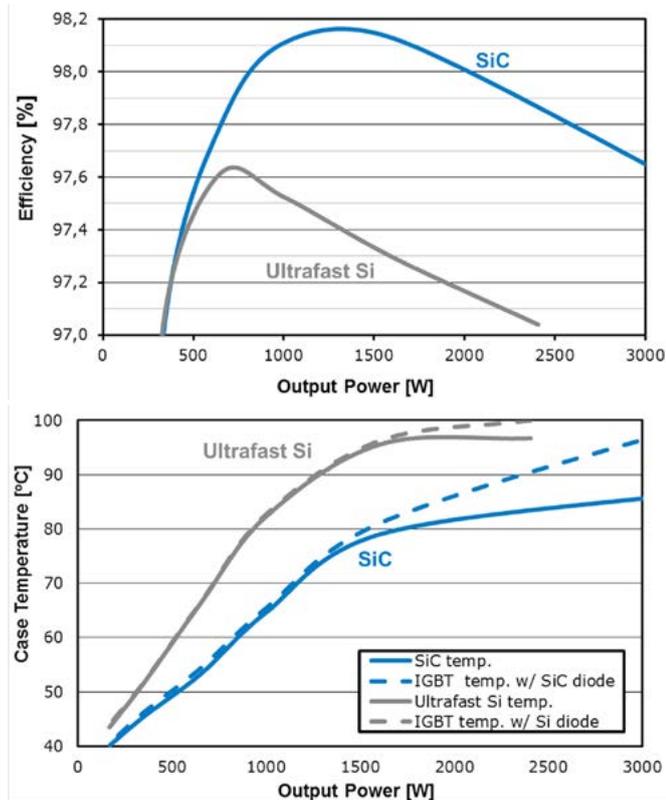
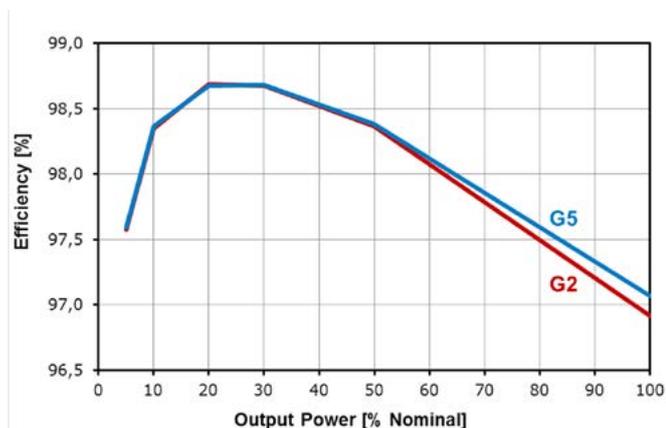


Figure 6: Efficiency results (top) of boost circuit and boost diode case temperature (bottom) of the 10 A SiC and 18 A Si diode over a maximum output power of 3000 W.

At 2400 W output power, the boost efficiency using SiC is 97.9 percent compared to Si diodes' 97.0 percent. The measured case temperature at this output power for the Si diode is 96.7 °C while the SiC diode reaches 84 °C. Due to reduced reverse recovery charge of SiC, the boost output power can reach 3000 W at a case temperature of 85 °C.



To compare the efficiency improvement of the SiC diode technology generations, the same test setup mentioned above is used, except for the boost switch. In this test a SiC JFET is used as the boost switch, which enables a maximum output power of 6 kW. Figure 7 plots the efficiency curves and boost diode case temperature as a function of the output power percentage.

At 100 percent output power, boost efficiency using generation 5 is 97.1 percent while generation 2 achieves 96.2 percent. Moreover, at this output power the measured case temperature for generation 5 is 93.6 °C while generation 2 is 115.1 °C. This reduction of device temperature at 100 percent output power is the result of the diodes' loss reduction which amounts to 30 percent.

Conclusion

Compared to a pure Si based solution design engineers gain a higher flexibility in system optimization for UPS, solar inverters, energy storage and other industrial applications when using hybrid Si IGBT/ SiC diode sets. The replacement of a Si by a SiC diode increases the system reliability because of lower device temperatures. Additionally, a higher output power in the same form factor can be achieved. By minor additional system changes, power density can be increased when using smaller heatsinks and EMI filters. The new generation 5 1200 V SiC Schottky diode from Infineon supports this higher flexibility with a low-loss turn-off, a dramatic improvement in static losses especially at elevated temperature and a massively increased surge current capability.

References

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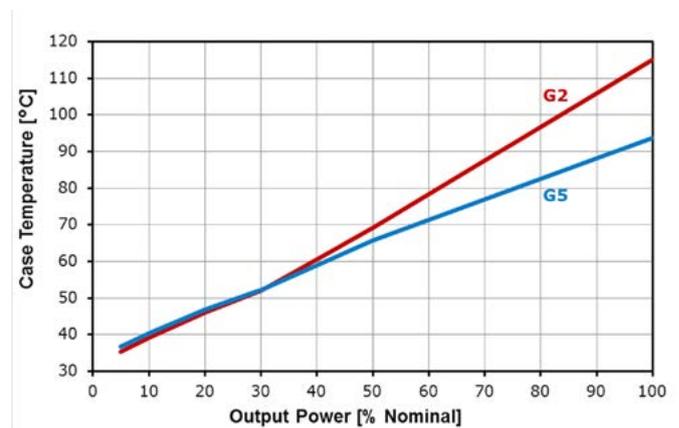


Figure 7: Efficiency (left) and SiC diode case temperature (right) results of a boost circuit with 800V output voltage, with Infineon's generation 5 and generation 2 10A SiC Schottky diodes in TO-247.