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Addressing space and efficiency in high-power applications

Power density is crucial for high-power applications, but is also a key factor for low- to mid-power designs

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One of the most important features in switched mode power supplies is power density. It is crucial for high-power applications like server and telecom but it is also a key factor for low- to mid-power designs like battery chargers and adapters.

Let's explore the performance of advanced solutions like Infineon Technologies` latest leadless SMT package concept, ThinPAK 5x6, in comparison to conventional SMT packages like DPAK. Such devices are suitable replacement for high-voltage conversion MOSFETs, where space saving is a key element. The ThinPAK 5x6 family is available from 360mΩ to 2100mΩ including 600V C6 and P6 technology and 650V C6 technology.

Comparing Package Outlines: DPAK vs.ThinPAK 5x6

The main benefit by replacing DPAK with ThinPAK 5x6 is the reduced volume of around 80% (DPAK maximum 170mm³ and ThinPAK 5x6 maximum 32mm³) with a maximum profile thickness of 1mm (see **Figure 1**). This

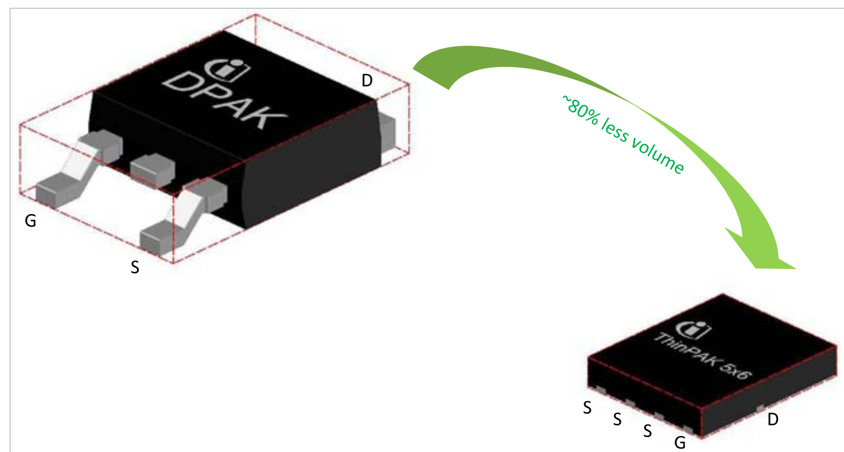

Figure 1: Volume reduction and pin connection

package height brings the benefit by implementing the HV MOSFET on the backside of the printed circuit board while gathering additional space between MOSFET case and application main case. This results in a reduction of possible thermal hot spots on the case of the application.

An additional benefit results from the reduction of the MOSFET`s internal and external parasitics coming from, for example, lead length and the possibility to reduce the commutation loop to a minimum in an application. Especially the source, which is ~3nH lower than DPAK and drain inductance difference can conclude in much lower gate oscillation and reduce the maximum drain source voltage peak when switching with high drain and source current slopes (di/dts) due to the well-known equation for calculating the voltage drop over an inductance (VL=L*di/dt) (see **Figure 2**).

This measurement is done in a classic PFC circuitry without load, which means that in every applied pulse the current through the PFC choke and the drain current increases, depending on the input voltage of the PFC and the inductance value of the PFC choke. With this setup it is possible to analyze the gate oscillation up to saturation of the MOSFET itself. In these diagrams the green lines correspond to the gate source

Figure 2: Gate oscillation ThinPAK 5x6 vs. DPAK

voltage, the pink line to the drain source voltage and the blue line to the current through the PFC choke. It is clearly visible that the gate source voltage oscillation at 4A drain current (ID) is much lower in amplitude than with DPAK.

By considering these lower parasitics it is possible to decrease the external gate resistor and therefore improve the efficiency or keep the same external gate resistor and enhance the voltage ringing behavior of the whole system while still achieving the same efficiency. Now that the benefits of this new package design are known the following sections addresses the application measurements.

Application Test 1 – 150W DCM PFC (CrCM PFC) for LCD TVs

As already anticipated in the headline a critical conduction mode PFC (CrCM PFC) is typically used in LCD TVs up to 300W output power. This kind of PFC is used in order to minimize the turn ON losses (EON) as much as possible due to a valley switching behavior (drain source voltage of the MOSFET during turn ON is already much lower than the bulk voltage).

There is only one problem to outline a correct efficiency comparison. The drain source voltage oscillation is depending on the output capacitance of the MOSFET, which could lead to higher switching frequency because the valley is reached earlier with a MOSFET with a smaller output capacitance. This could also lead to wrong system efficiency measurements.

In order to remove this change of frequency only matched devices with the same parameters and the same technology were used. In all these mentioned application measurements the efficiency and thermal performance will be analyzed in comparison to standard SMT packages like DPAK. According to this analysis the setup will run in worst case condition with the following initial and boundary conditions:

input voltage Vin = 90VAC
output voltage Vout = 400VDC
external gate resistor RG,ext = 10Ω for turn ON and OFF of the MOSFET
switching frequency fsw = variable due to the given topology used (CrCM)
heat sink is preheated to 60°C
DUT = IPL65R650C6S vs. IPD65R600C6

With this setup the system efficiency and thermal performance was reached as seen in **Figure 3**. The efficiency comparison makes it visible that all the measured values are equal. As represented the graph only shows the values from 100W onwards. In lower power

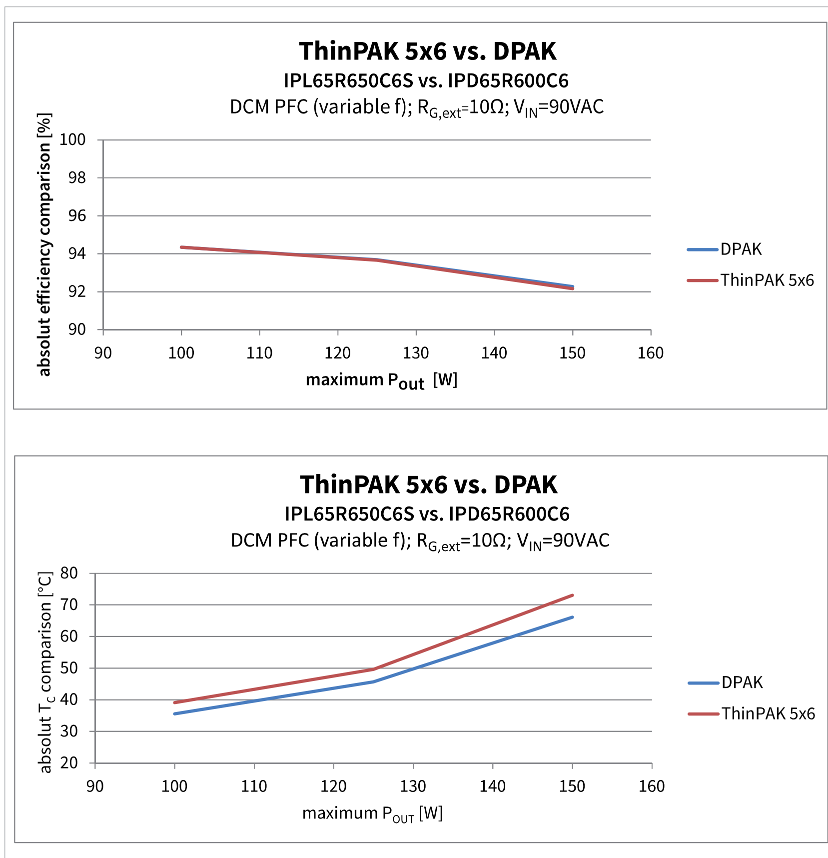

Figure 3: efficiency (upper) and thermal (lower) performance of ThinPAK 5x6 vs. DPAK

ranges the analysis is not needed due to the usage of the same silicon in a different package.

The most interesting comparison is the one covering thermal performance were a slight higher case temperature of around 3-4°C of ThinPAK 5x6 is visible. The reader may ask now, why is the efficiency the same but the case temperature is higher for ThinPAK 5x6? This higher temperature and reaching the same efficiency is due to the thicker mold compound material of DPAK which has a very high thermal resistance that leads to a higher case temperature on ThinPAK 5x6 but the junction temperature is equal on both DUTs. The mold compound thickness falsifies the results. The picture in **Figure 4** explains this phenomenon.

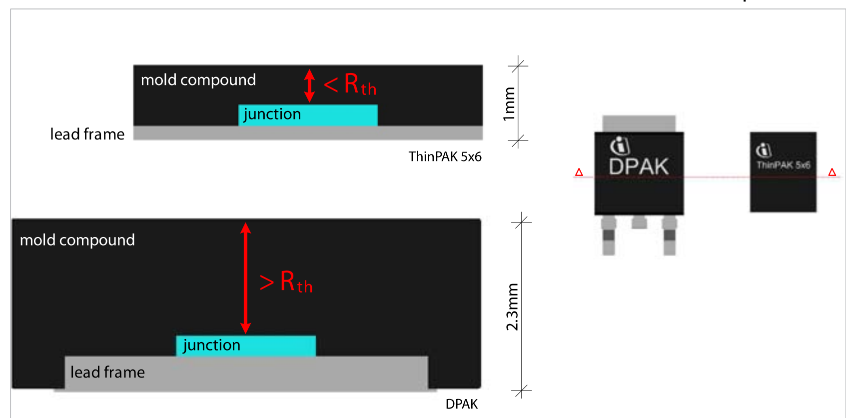

Figure 4: simplified cross section of DPAK and ThinPAK 5x6 (mold compound influence on thermal measurement)

As clearly visible in **Figure 4**, the mold compound portion of the whole package is much higher on DPAK than on ThinPAK 5x6. This influences any thermal measurement an engineer is able to execute. Therefore, a thermal comparison with different packages always needs to be questioned otherwise it would lead to "unfair" comparisons of such different packages.

Finally it was illustrated that ThinPAK 5x6 brings the same performance like DPAK in this measurement setup with the same copper area connected to the lead frame.

Application Test 2 – 35W quasi-resonant (QR) flyback converter typically used as net-book adapter

Two technologies are compared in this measurement - the C6 and P6 technology from Infineon. In this case there is no heat sink attachment of the MOSFET - the only restriction is the used copper area of the PCB which is around 40mm² for both packages.

Test Setup for the efficiency comparison:

Vin = 90VAC
Vout = 19VDC
output current Iout = up to 1.85A

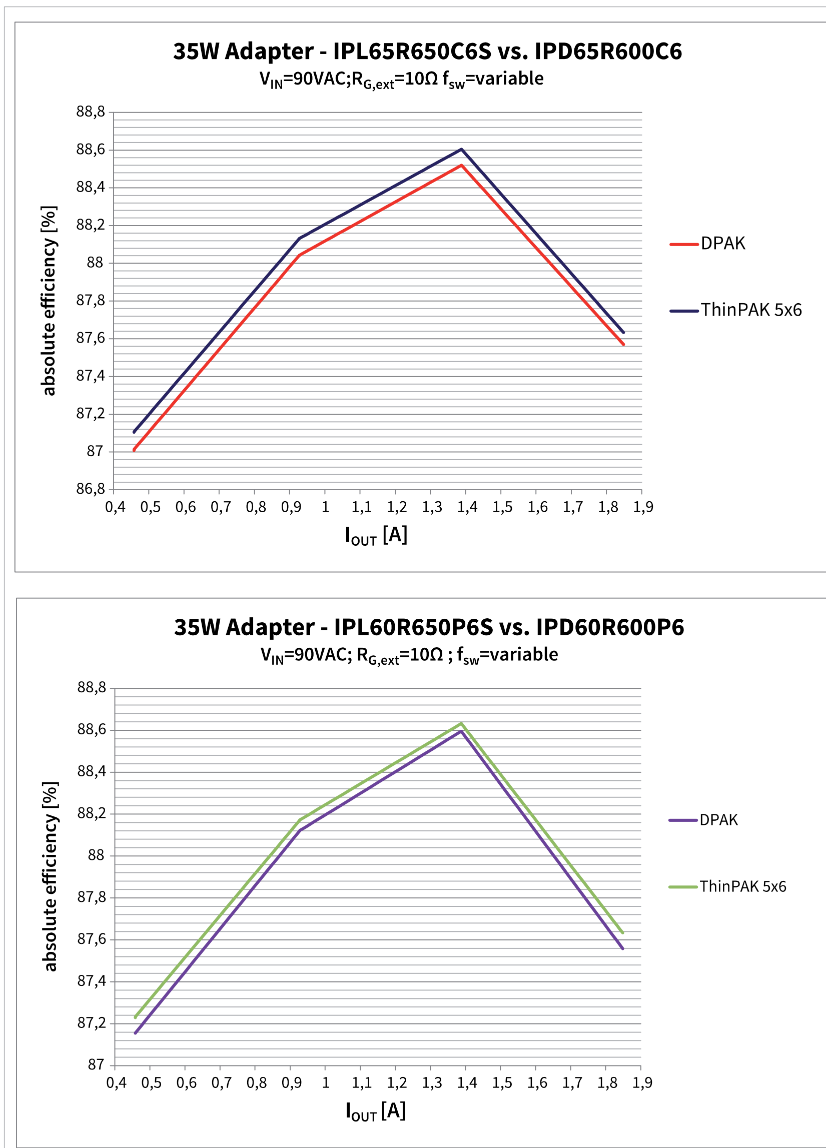

Figure 5: Efficiency comparison of ThinPAK 5x6 vs. DPAK in 35W QR flyback
RG,ext = 10Ω
fsw = variable

Test Setup for the thermal comparison:
Vin = 115VAC
Vout = 19VDC
Iout = 1.85A
RG,ext = 10Ω
dwell time = 30min (after 30min runtime the case temperature was stable and the values are represented)

In these measurements ThinPAK 5x6 behaves the same as DPAK with respect to efficiency on both technologies, which is represented in **Figure 5**. Every efficiency measurement point at 25%, 50%, 75% and 100% of output power is slightly better.

As already explained in the thermal analysis in the CrCM PFC the case temperature shows a difference of 3-5°C at full load. This temperature difference follows the same explanation as before. Only one very important point needs to be clarified when using SMT packages without a top-side or bottom-side cooling concept. By removing any heat sink connection of the lead frame the thermal resistance from junction to case (RthJC) of only some Kelvin per Watt (K/W) is not the driving factor anymore. There the designer really needs to consider how to reduce the thermal resistance from junction to ambient (RthJA).

The easiest way to reduce the RthJA is by implementing as much copper in the PCB as possible, which is then at the end connected to the lead frame of the MOSFET. In this case it would even be possible to have a better thermal performance with ThinPAK 5x6 than DPAK. Nevertheless with minimum footprint ThinPAK 5x6 will have a worse thermal behavior than DPAK. With the minimum footprint and without heat sink connection the RthJA of ThinPAK 5x6 is around 125K/W and for DPAK around 90K/W.

Small and thin for size driven applications

ThinPAK 5x6 represents a 2nd generation of surface mounted devices which can be a suitable replacement for standard SMT packages in size driven applications.

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