Application note: safety limits for ISO2H8xx-ICs

ISO2H827V2.5 / ISO2H823V2.5

About this document

Scope and purpose

This is an application note describing the safety limits for the ISO2H8xx-ICs series of coreless transformers with isolated eight-channel 0.6 A digital output and high-side switch.

Intended audience

For engineers interested in industrial automatization.

Table of contents

1 Introduction

Safety limits of allowed current or allowed power dissipation are intended to prevent an over-temperature condition. They are also intended to prevent potential damage to the isolation barrier and a voltage breakdown between the two voltage domains.

Precautions were taken during the conception phase of the architecture (described in chapter 2). In chapter 3 the electrical and thermal parameters are listed, which are used for calculation of the allowed current in the power chip and the uC interface chip. The most important chapters are 4 and 5. In these chapters the junction temperature T_j is calculated based on the variable ambient temperature and the temperature rise due to the I_{LOAD} current in the power chip or the I_{VCC} current in the uC interface chip. These chapters give the worst-case overview where the maximum drain-source resistance of the switching transistor is $R_{on}(150°C)$ used at the junction temperature of $T_j = 150°C$. Chapter 6 (Incorporation of a derating curve and $R_{ON}(T_j = T_A + \Delta T)$) improves the calculation with the realistic $R_{ON}(T_j = T_A + \Delta T)$ and introduces a derating curve. The related power dissipation is multiplied with the thermal resistance junction-to-air. The criterion for the allowed currents is T_j less than 150°C and for the maximum power dissipation of the whole chip it is P_{tot_max} less than or equal to 1.5 W. From these requirements a limitation for I_{LOAD} and I_{VCC} is derived.

All figures and curves are calculated with reference to the electrical and thermal characteristics of the datasheet.

2 Safety-relevant architecture

Figure 1 emphasizes the location of the coreless transformer. It is placed on the uC interface chip (DIE 1). The temperature-critical chip is the power chip (DIE 2). The chips DIE1 and DIE2 are located on a split lead-frame to establish the isolation. Any temperature increase on the power chip has only indirect influence on the uC interface chip and therefore on the coreless transformer only via the split lead-frame and the package.

Additionally the power chip is protected by a temperature shut-down at T_j = 150°C (each channel). Only short periods of higher temperature of T_j = 200°C are permitted during the start-up of a cold lamp. A global temperature sensor assures that the package temperature does not exceed 125°C.

An over-load current protection for each channel limits the current to a maximum of 1.3 A. For switching on a cold lamp the current of each channel is typically limited to 1.5 A.

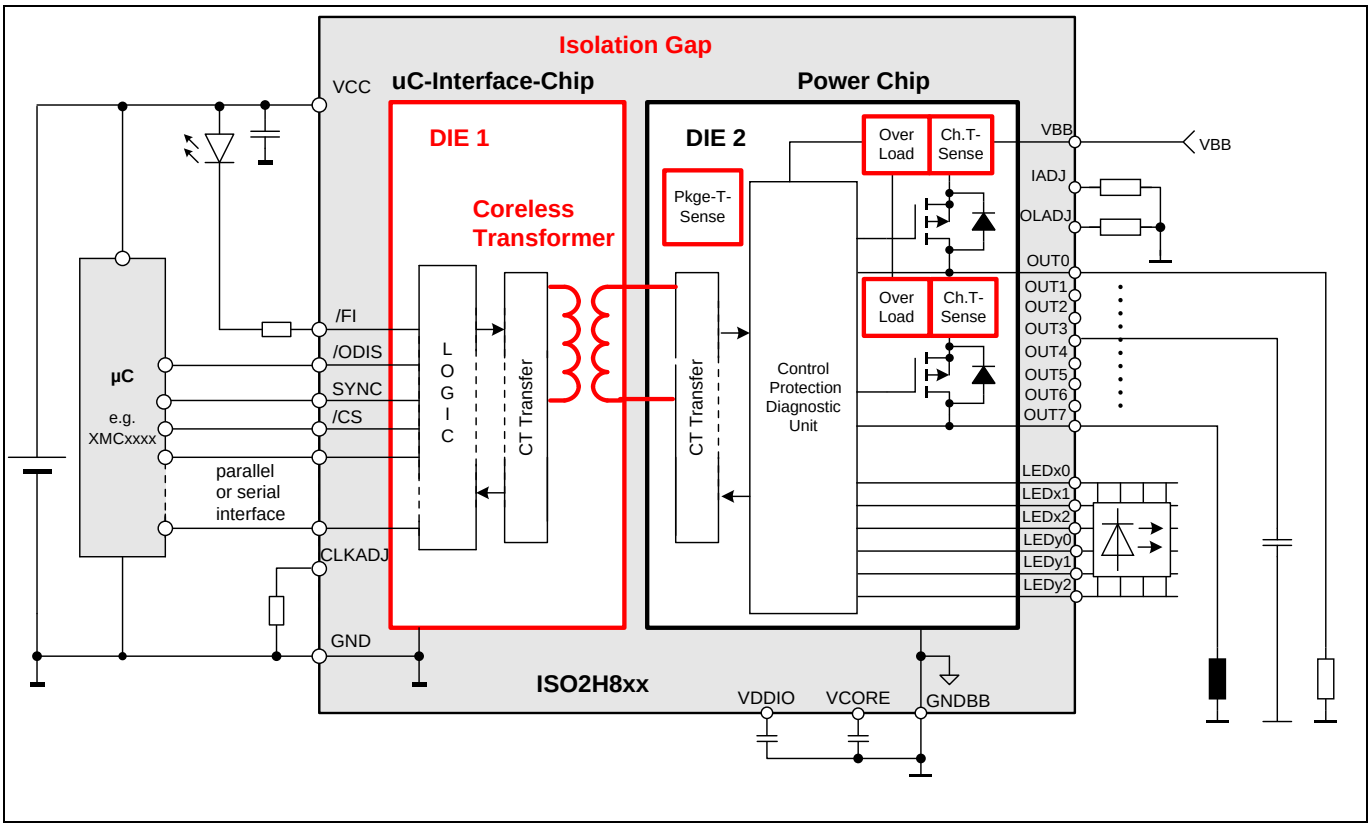


Figure 1 Typical application diagram with internal structure of galvanic isolation

3 Prerequisites for calculating safety limits

For calculating the safety limits the maximum values of the relevant parameters are chosen. Figure 2 visualizes the parameters used. All underlying calculations refer to these parameters.

Table 1 Prerequisites for calculating safety limits

Parameter	Maximum value used	Comment
$R_{th(JA)}$	(23 *1.5) K/W	Thermic resistance junction-ambient, typical (factor 1.5 for creating safety margin), see Note: Specified $R_{TH(JA)}$-value
I_{VCC}	0.013 A	Maximum V_{CC} current of uC interface chip, SPI traffic included, V_{CC} = 3.6 V
$I_{VBB=11V}$ $I_{VBB=24V}$ $I_{VBB=35V}$	0.011 A 0.013 A 0.015 A	Maximum quiescent current of power chip, all channels inactive, V_{BB} = 11 V, V_{BB} = 24 V, V_{BB} = 35 V
P_{tot_max}	1.5 W	Maximum rating of total dissipated power
T_{jmax}	150.0°C	Maximum junction temperature
R_{on}(-40°C) R_{on}(125°C) R_{on}(150°C)	0.105 Ω 0.25 Ω 0.272 Ω	Maximum drain-source resistance of switching transistor
$P_{VCC=3.6\ V}$	0.047 W	Maximum power dissipation of uC interface chip, all channels inactive, V_{CC} = 3.6 V
$P_{VBB=11V}$ $P_{VBB=24V}$ $P_{VBB=35V}$	0.121 W 0.312 W 0.525 W	Maximum quiescent power dissipation of power chip, all channels inactive, V_{BB} = 11 V, V_{BB} = 24 V, V_{BB} = 35 V

Note: Specified $R_{TH(JA)}$ value is according to Jedec JESD51-2, -5, -7 at natural convection on FR4 2s2p board; the product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm board with two inner copper layers (2 × 70 mm Cu, 2 × 35 mm Cu). Where applicable a thermal via array under the exposed pads contacted the first inner copper layer. The customer must ensure that the two exposed pads of the package are soldered to the application board over the entire area.

Table 2 Formulas for calculating safety limits without derating curve

Purpose	Formula
Total power dissipation	**$P_{tot}(T) = P_{VCC=3.6V} + P_{VBB=xV} + R_{ON}(T) * I_{LOAD} * I_{LOAD} * 8$** 8 channels
Condition for $I_{LOAD\_Allowed}$ (T_A)	**Condition: T less than or equal to 150°C and P_{tot} less than 1.5 W --> allowed I_{LOAD}: for worst-case estimation use R_{ON}(T = 150°C)** **$150°C = T_A + (P_{VCC=3.6V} + P_{VBB=xV}) * R_{TH(JA)} + (I_{LOAD} * I_{LOAD} * R_{ON}(150°C) * 8) * R_{TH(JA)}$**
$I_{LOAD\_Allowed}$ (T_A)	**allowed I_{LOAD} :** **$I_{LOAD\_Allowed} = SQRT((150 - T_A - (P_{VCC=3.6V} + P_{VBB=xV}) * R_{TH(JA)})/(R_{ON}(150°C) * 8 * R_{TH(JA)}))$**
P_{tot} (150°C, $I_{LOAD\_Allowed}$)	**$P_{tot}(150°C) = P_{VCC=3.6V} + P_{VBB=xV} + R_{ON}(150°C) * I_{LOAD\_Allowed} * I_{LOAD\_Allowed} * 8$**
$I_{VCC\_Allowed}$ (T_A)	Limit **$I_{LOAD\_Allowed} = I_{LOAD\_max} = 0.65$ A** **$I_{VCC\_Allowed} = (P_{tot\_max} - P_{VBB=xV} - R_{ON}(150°C) * I_{LOAD\_Allowed} * I_{LOAD\_Allowed} * 8)/(V_{CC} = 3.6\ V)$**

Table 3 Derating conditions

Derating condition 1	**Total load current**	**Number of channels**
T_{A1} = - 40°C - + 40°C	**$I_{Total} = 5.2$ A**	**$8/I_{max} = 0.65$ A**
T_{A2} = 41°C - + 60°C	$I_{Total} = 2$ A	$4/I_{max} = 0.5$ A
T_{A3} = 61°C - + 80°C	$I_{Total} = 2$ A	$4/I_{max} = 0.5$ A
T_{A4} = 81°C - + …	$I_{Total} = 2$ A	$4/I_{max} = 0.5$ A
Derating condition 2		
T_{A1} = - 40°C - + 40°C	**$I_{Total} = 5.2$ A**	**$8/I_{max} = 0.65$ A**
T_{A2} = 41°C - + 60°C	$I_{Total} = 4$ A	$8/I_{max} = 0.5$ A
T_{A3} = 61°C - + 80°C	$I_{Total} = 3$ A	$8/I_{max} = 0.375$ A
T_{A4} = 81°C - + …	$I_{Total} = 2$ A	$8/I_{max} = 0.25$ A
Derating condition 3		
T_{A1} = - 40°C - + 40°C	**$I_{Total} = 5.2$ A**	**$8/I_{max} = 0.65$ A**
T_{A2} = 41°C - + 60°C	$I_{Total} = 3.9$ A	$6/I_{max} = 0.65$ A
T_{A3} = 61°C - + 80°C	$I_{Total} = 3$ A	$6/I_{max} = 0.5$ A
T_{A4} = 81°C - + …	$I_{Total} = 2$ A	$4/I_{max} = 0.5$ A

Table 4 Formulas for calculating safety limits with derating curve and $R_{ON}(T_j = T_A + \Delta T)$

Purpose	Formula

Prerequisites for calculating safety limits

Purpose	Formula
P_{tot} (T_A)	$P_{tot}(T_A) = P_{VCC=3.6V} + P_{VBB=xV} + R_{ON}(T_A) * I_{LOAD_max}(T_A) * I_{LOAD_max}(T_A) *$number of channels($T_A$)
ΔT	$\Delta T = P_{tot}(T_A) * R_{TH(JA)}$
$I_{LOAD\_Allowed}$ (T_A)	$I_{LOAD\_Allowed}$ = SQRT ((150 - T_A - ($P_{VCC=3.6V}$ +$P_{VBB=xV}$) *$R_{TH(JA)}$)/(R_{ON}(T_j=T_A + ΔT) *number of channels *$R_{TH(JA)}$)) (condition: limit $I_{LOAD\_Allowed}$ = I_{LOAD_max} = 0.65 A or 0.5 A or 0.375 A or 0.25 A, each channel)
$I_{VCC\_Allowed}$ (T_A)	$I_{VCC\_Allowed}$ = (P_{tot_max} - $P_{VBB=xV}$ - R_{ON}(T_j = T_A + ΔT) *$I_{LOAD\_Allowed}$ *$I_{LOAD\_Allowed}$ *number of channels)/(V_{CC} = 3.6 V)

4 Safety limits for the power chip

The maximum allowed power dissipation of the power chip is limited by two constraints: the junction temperature has to be less than T_j = 150°C and the total power dissipation of the total chip (including two dies) has to be less than 1.5 W.

Based on the ambient temperature the temperature increase is calculated due to three power dissipation parts:

1. power dissipation of the uC interface chip (in this calculation fixed to 47 mW)

2. constant power dissipation of the power chip (dependent on V_{BB}) and

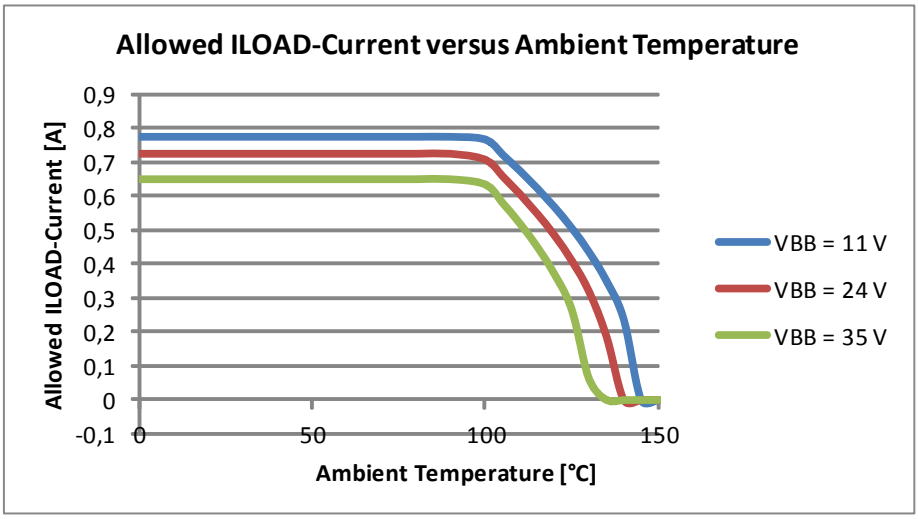
3. power dissipation due to the load current and the thermic resistance (junction-ambient).

Condition:
T less than or equal to 150°C and P_{tot} less than 1.5 W **-->** **allowed I_{LOAD}:** **for worst-case estimation use R_{ON}(T = 150°C)**

$150°C = T_A + (P_{VCC=3.6V} + P_{VBB=xV}) * R_{TH(JA)} + (I_{LOAD} * I_{LOAD} * R_{ON}(150°C) * 8) * R_{TH(JA)}$

I_{LOAD} is limited by 0.775 A (V_{BB} = 11 V), 0.725 A (V_{BB} = 24V), 0.65 A (V_{BB} =35 V) due to the allowed total power dissipation of 1.5 W and increasing the ambient temperature the allowed I_{LOAD} is reduced to fit with the maximum allowed junction temperature of the power chip of T_j= 150°C.

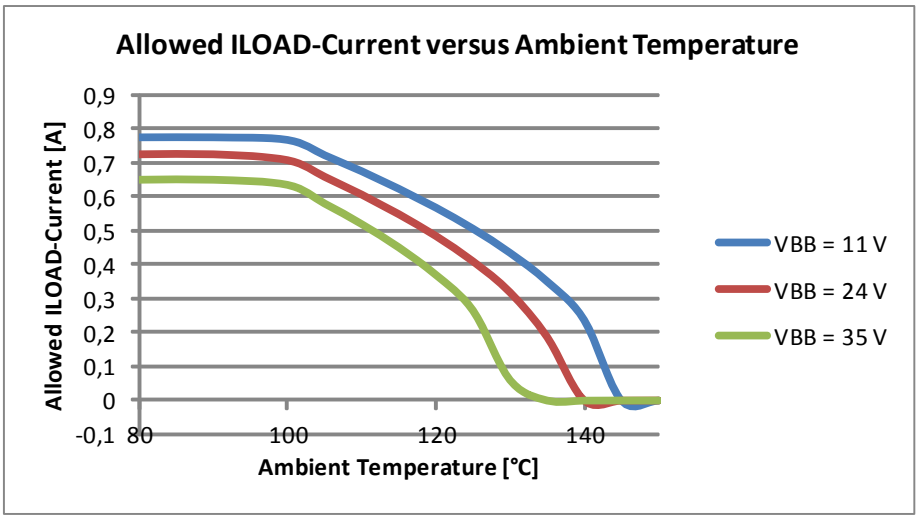
In this calculation V_{CC} = 3.6 V and V_{BB} = 11 V, 24 V, 35 V.



$I_{LOAD\_Allowed}$ =

$SQRT((150 - T_A - (P_{VCC=3.6V} + P_{VBB=xV}) * R_{TH(JA)}) / (R_{ON}(150°C) * 8 * R_{TH(JA)}))$

Figure 2 Safety I_{LOAD} current limits

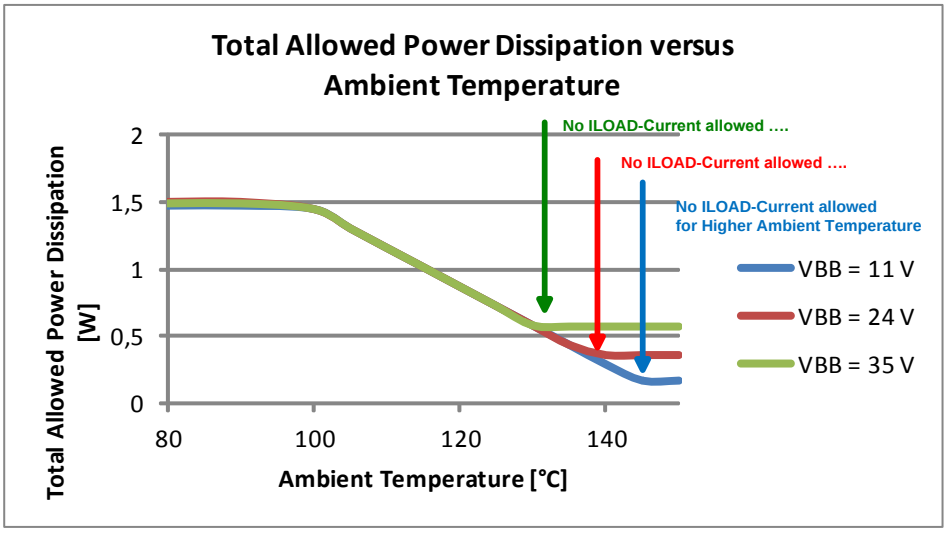


$I_{LOAD\_Allowed}$ =

$$SQRT((150 - T_A - (P_{VCC=3.6V} + P_{VBB=xV}) * R_{TH(JA)}) / (R_{ON}(150°C) * 8 * R_{TH(JA)}))$$

Figure 3 Safety I_{Load} current limits (detail)

Figure 4 classifies the lower values of ambient temperature from which no I_{LOAD} current is allowed because the internal power dissipation without I_{LOAD} current already leads to a junction temperature of 150°C.



$$P_{tot}(150°C) = P_{VCC=3.6V} + P_{VBB=xV} + R_{ON}(150°C) * I_{LOAD\_Allowed} * I_{LOAD\_Allowed} * 8$$

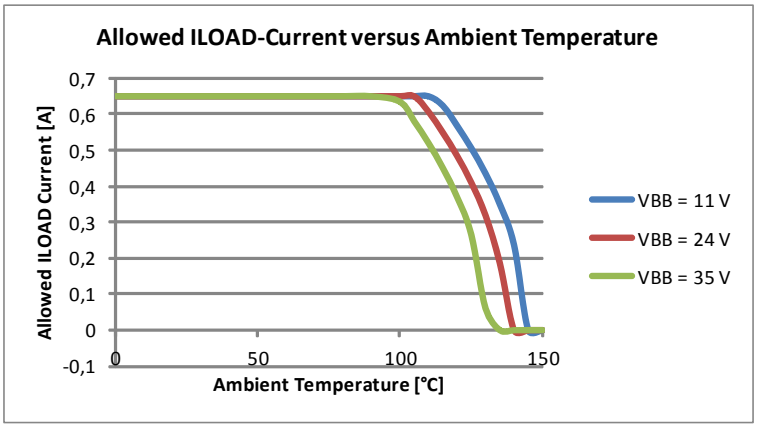
Figure 4 Safety power limits of the power chip

5 Safety limits for the uC interface chip

For calculating the power limits for the uC interface chip the maximum I_{LOAD} current of the power chip is fixed at 0.65 A. The difference of the actual power dissipation and the maximum allowed power dissipation of 1.5 W is the basis for constraining the current of the uC interface chip.

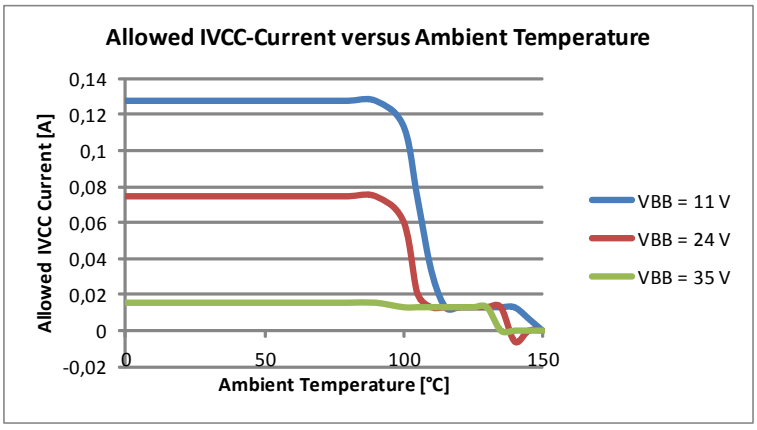
In Figure 5 the reduction of the allowed I_{LOAD} current with increasing the ambient temperature and (what is new in this context) the required reduction of the allowed I_{VCC} current is seen. An I_{VCC} current of maximum 13 mA has to be provided to operate the system.

The allowed I_{VCC} is only calculated for V_{CC} = 3.6 V.



$I_{LOAD\_Allowed}$ =
SQRT((150 - T_A - ($P_{VCC=3.6V}$ +$P_{VBB=xV}$) *$R_{TH(JA)}$) / (R_{ON}(150°C) * 8 * $R_{TH(JA)}$))

(condition : limit $I_{LOAD\_Allowed}$ = I_{LOAD_max} = 0.65 A, each channel)



Condition 1 : **$I_{VCC\_Allowed}$ = (P_{tot_max} - $P_{VBB=xV}$ - R_{ON}(150 °C) * $I_{LOAD\_Allowed}$* $I_{LOAD\_Allowed}$*8) / (VCC=3.6 V)**

Condition 2 : **$I_{VCC\_Allowed}$ = (150 - T_A - ($P_{VBB=xV}$ + RON(150°C) * $I_{LOAD\_Allowed}$* $I_{LOAD\_Allowed}$*8) *$R_{TH(JA)}$)) / (VCC = 3.6 V * $R_{TH(JA)}$)**

Figure 5 Safety limits for I_{Load} and I_{VCC} current

6 Incorporation of a derating curve and $R_{ON}(T_j = T_A + \Delta T)$

The customer introduces precautions to avoid an overheating in the application: a derating curve dependent on the ambient temperature.

Possible precautions can be as follows:

a. Allow all eight channels to be activated with ambient temperatures of less than 40°C. At the same time a maximum I_{LOAD_max} current of 0.65 A/channel is allowed.

b. If the ambient temperature of 40°C is exceeded every second channel has to be switched off. Allow only four channels to be activated. At the same time the I_{LOAD_max} current/channel is limited to 0.5 A.

In the calculations in chapters 4 and 5 the parameter R_{ON} was applied at the maximum temperature of T_j = 150°C, $R_{ON}(T_j = 150°C)$. Especially for low ambient temperatures this is not true and imposes more stringent application of relevant protection mechanisms (derating curve).

In the calculations below we introduce $R_{ON}(T_j)$ where T_j is calculated in three steps:

a. Calculation of the total dissipated power at T_A with $R_{ON}(T_A)$:

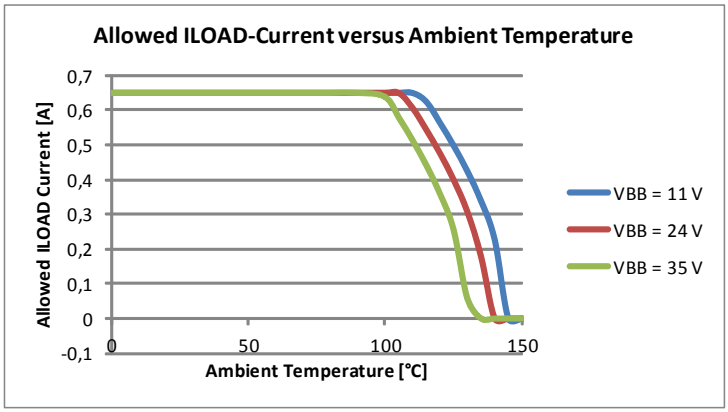
$$P_{tot}(T_A) = P_{VCC=3.6V} + P_{VBB=xV} + R_{ON}(T_A) * I_{LOAD\_max}(T_A) * I_{LOAD\_max}(T_A) * \text{number of channels}(T_A)$$

During these calculations the derating curve has been incorporated.

b. Calculation of the related temperature step by applying $R_{th(JA)}$: ΔT.

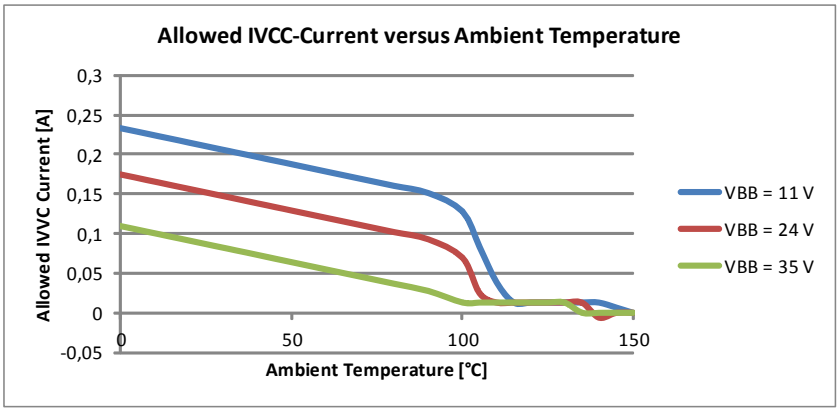
c. Calculation (means interpolation) of $R_{ON}(T_j = T_A + \Delta T)$.

$R_{ON}(T_j = T_A + \Delta T)$ is applied in all subsequent formulas instead of $R_{ON}(150°C)$.



$I_{LOAD\_Allowed}$ =
SQRT((150 - T_A - ($P_{VCC=3.6V}$ +$P_{VBB=xV}$) *$R_{TH(JA)}$) / ($R_{ON}(T_j=T_A + \Delta T)$ * #Channels * $R_{TH(JA)}$))

(condition : limit $I_{LOAD\_Allowed}$ = I_{LOAD_max} = 0.65 A , each channel)



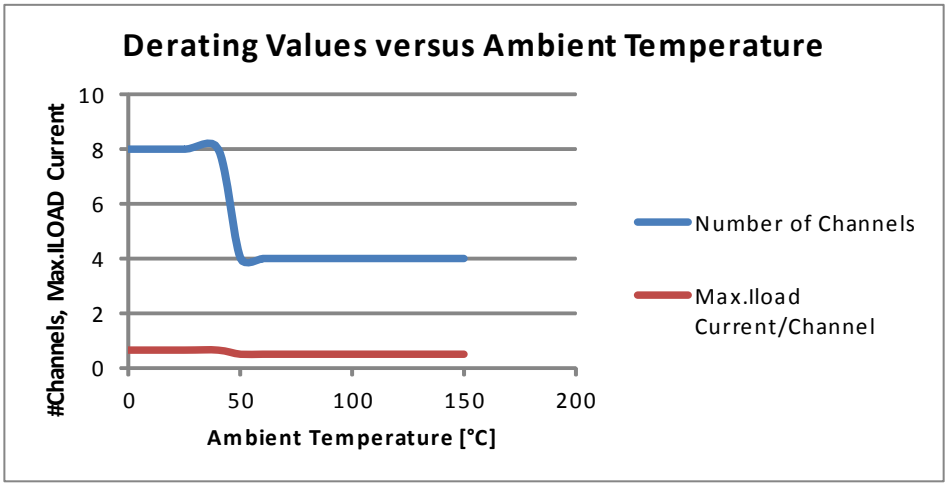
Condition 1 : $I_{VCC\_Allowed}$ = (P_{tot_max} - $P_{VBB=xV}$ - $R_{ON}(T_j = T_A + \Delta T)$ * $I_{LOAD\_Allowed}$* $I_{LOAD\_Allowed}$*#Channels) / (VCC=3.6 V)

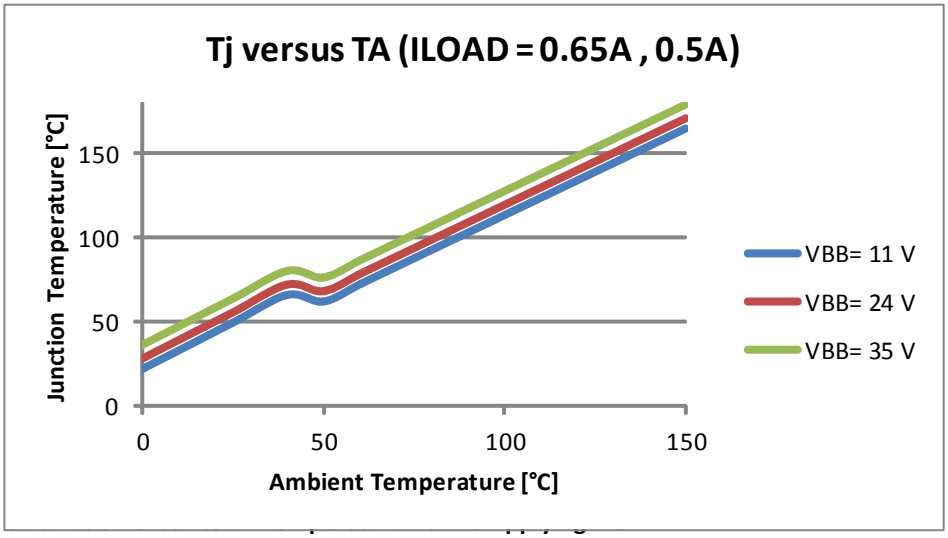
Condition 2 : $I_{VCC\_Allowed}$ = (150 - T_A - ($P_{VBB=xV}$ + RON(T_j) * $I_{LOAD\_Allowed}$* $I_{LOAD\_Allowed}$*#Channels) *$R_{TH(JA)}$)) / (VCC = 3.6 V * $R_{TH(JA)}$)

Figure 6 Safety limits for I_{Load} and I_{VCC} current, no derating curve, only introduction of $R_{ON}(T_j=T_A + \Delta T)$, corresponds to Figure 5.

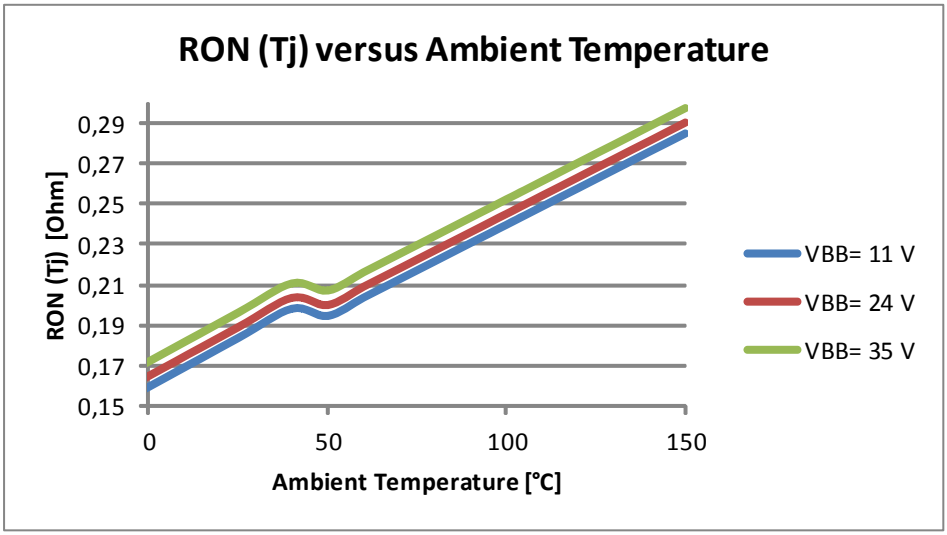
Figure 7 also incorporates a possible derating requirement for T_A greater than 40°C: only four channels are invoked and the I_{Load} current is limited to 0.5 A.

Figure 8 shows the effect of the derating requirement on the $I_{Load\_Allowed}$ and $I_{VCC\_Allowed}$ current. Figure 9 and Figure 10 deal with other derating requirements.



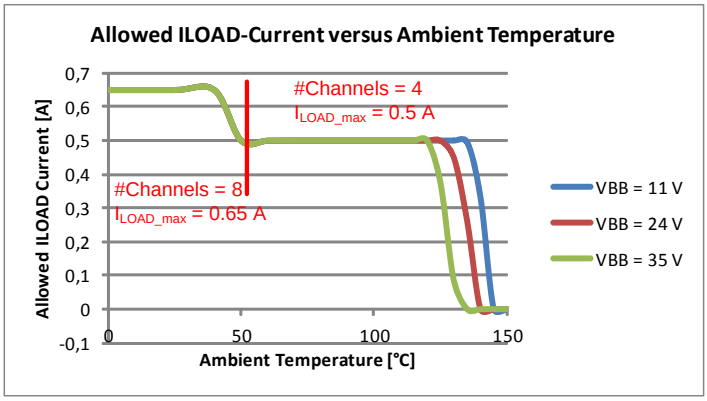


(condition :
limit activated channels to 4 (T_A > 40°)
limit $I_{LOAD\_Allowed}$ = I_{LOAD_max} = 0.65 A (0.5 A for T_A > 40°C), each channel)



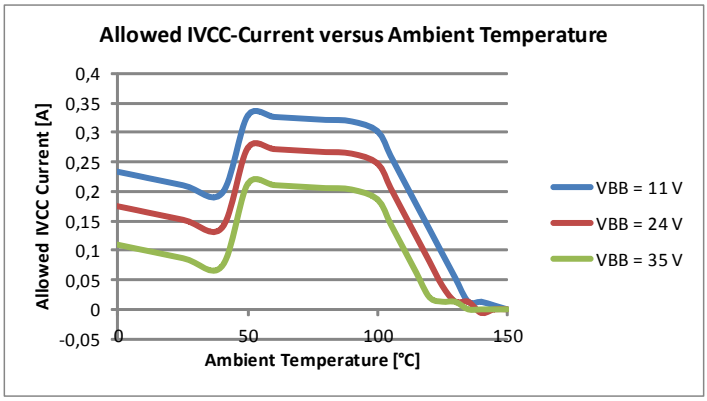
Calculation of R_{ON} (Junction Temperature)

Figure 7 **Derating information and calculation of $T_j = T_A + \Delta T$ and $R_{ON}(T_j = T_A + \Delta T)$**



$I_{LOAD\_Allowed}$ =
SQRT((150 - T_A - ($P_{VCC=3.6V}$ +$P_{VBB=xV}$) *$R_{TH(JA)}$) / ($R_{ON}(T_j=T_A + \Delta T)$ * #Channels * $R_{TH(JA)}$))

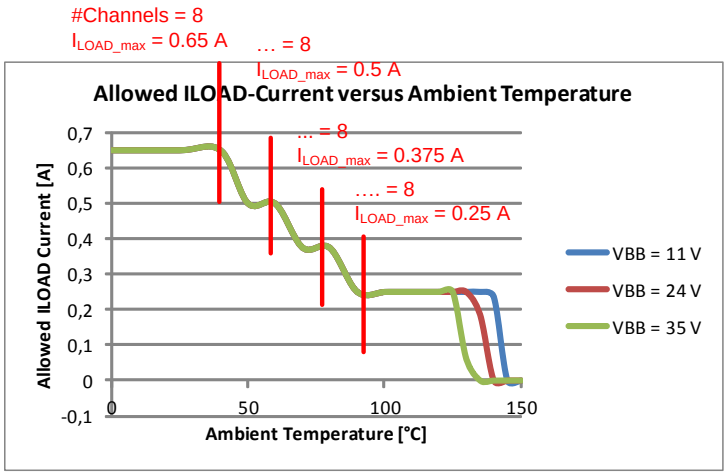
(condition : limit $I_{LOAD\_Allowed}$ = I_{LOAD_max} = 0.65 A or 0.5 A, each channel)



Condition 1 : $I_{VCC\_Allowed}$ = (P_{tot_max} - $P_{VBB=xV}$ - $R_{ON}(T_j = T_A + \Delta T)$ * $I_{LOAD\_Allowed}$* $I_{LOAD\_Allowed}$*#Channels) / (VCC=3.6 V)

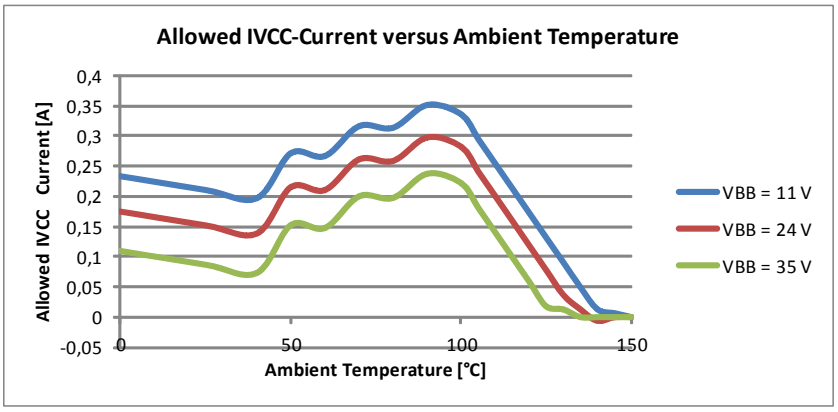
Condition 2 : $I_{VCC\_Allowed}$ = (150 - T_A - ($P_{VBB=xV}$ + RON(T_j) * $I_{LOAD\_Allowed}$* $I_{LOAD\_Allowed}$*#Channels) *$R_{TH(JA)}$)) / (VCC = 3.6 V * $R_{TH(JA)}$)

Figure 8 Safety limits for I_{Load} and I_{VCC} current incorporating the derating curve 1



$I_{LOAD\_Allowed}$ =
SQRT((150 - T_A - ($P_{VCC=3.6V}$ +$P_{VBB=xV}$) *$R_{TH(JA)}$) / ($R_{ON}(T_j=T_A + \Delta T)$ * #Channels * $R_{TH(JA)}$))

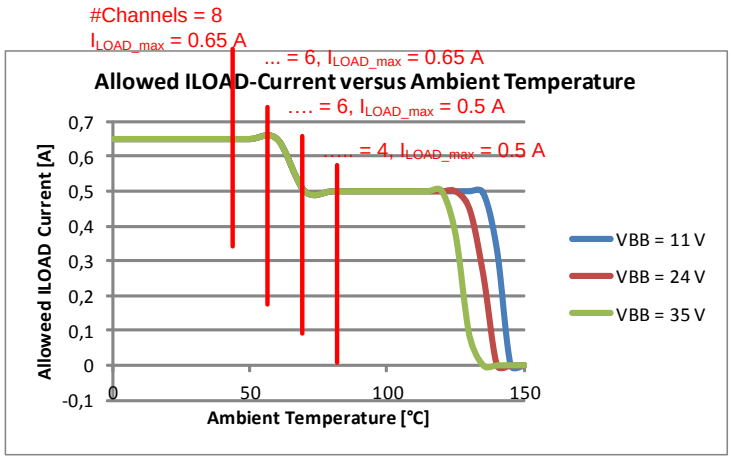
(condition : limit $I_{LOAD\_Allowed}$ = I_{LOAD_max} = 0.65 A or 0.5 A or 0.375 A or 0.25 A, each channel)



Condition 1 : $I_{VCC\_Allowed}$ = (P_{tot_max} - $P_{VBB=xV}$ - $R_{ON}(T_j = T_A + \Delta T)$ * $I_{LOAD\_Allowed}$* $I_{LOAD\_Allowed}$*#Channels) / (VCC=3.6 V)

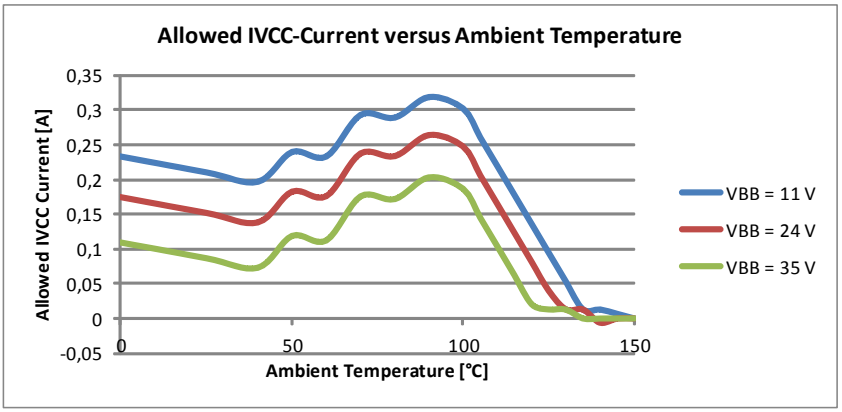
Condition 2 : $I_{VCC\_Allowed}$ = (150 - T_A - ($P_{VBB=xV}$ + RON(T_j) * $I_{LOAD\_Allowed}$* $I_{LOAD\_Allowed}$*#Channels) *$R_{TH(JA)}$)) / (VCC = 3.6 V * $R_{TH(JA)}$)

Figure 9 Safety limits for I_{Load} and I_{VCC} current incorporating the derating curve 2



$I_{LOAD\_Allowed}$ =
SQRT((150 - T_A - ($P_{VCC=3.6V}$ +$P_{VBB=xV}$) *$R_{TH(JA)}$) / ($R_{ON}(T_j=T_A + \Delta T)$ * #Channels * $R_{TH(JA)}$))

(condition : limit $I_{LOAD\_Allowed}$ = I_{LOAD_max} = 0.65 A or 0.5 A, each channel)



Condition 1 : $I_{VCC\_Allowed}$ = (P_{tot_max} - $P_{VBB=xV}$ - $R_{ON}(T_j = T_A + \Delta T)$ * $I_{LOAD\_Allowed}$* $I_{LOAD\_Allowed}$*#Channels) / (VCC=3.6 V)

Condition 2 : $I_{VCC\_Allowed}$ = (150 - T_A - ($P_{VBB=xV}$ + RON(T_j) * $I_{LOAD\_Allowed}$* $I_{LOAD\_Allowed}$*#Channels) *$R_{TH(JA)}$)) / (VCC = 3.6 V * $R_{TH(JA)}$)

Figure 10 Safety limits for I_{Load} and I_{VCC} current incorporating the derating curve 3

7 Demagnetization energy of external coils

For switching and demagnetizing external coils we refer to the datasheet – especially the absolute maximum rating figure: E_{AS} = 150 mJ max.

“Inductive load switch-off energy dissipation for each channel, single pulse, all channels are switching

simultaneously, T_j = 125°C, I_L = 0.6 A”

is emphasized.

Curves for the typical thermal impedance as a function of the switching frequency and the pulse/pause ratio are sketched in the chapter “Typical Performance Characteristics”. Different PCB layouts have been simulated.

The target is to avoid a maximum junction temperature of T_{jmax} = 150°C for each channel and a maximum package temperature of 125°C.

In the same chapter figures treating the “Maximum Allowable Load Inductance” as a function of the load current are included.

Revision history

Document version	Date of release	Description of changes
V1.0	2018-02-16	1st release

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