Dynamic thermal behavior of MOSFETs

Simulation and calculation of high power pulses

About this document

Scope and purpose

Thermal management can be a tricky task. As long as the losses are constant it is easy to derive the maximum chip temperature from simple measurements and/or calculations. Short high-power pulses lead to a peak junction temperature that is hard or impossible to measure using standard lab equipment.

This AN focuses on two methods to check violations of the device's limits – using simulation software together with Infineon's SPICE models, and a simple "pocket calculator method".

Intended audience

Power-supply designers

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1 Introduction

Temperature is one of the most important parameters that influences the behavior of a MOSFET. This is reflected in several figures and diagrams in a datasheet showing them for different temperature values.

MOSFET reliability is the main topic here. Parameter drift, reduced lifetime or early destruction could be the result of increased chip temperature. Knowing the chip temperature is therefore a key factor.

There are four common methods to determine the chip's temperature:

1. Use of thermal probes or a thermal camera
2. Finite Element Analysis (FEA)
3. Calculation based on datasheet diagrams
4. Simulation with Infineon's SPICE libraries

Another method is to apply a current to the body diode of the MOSFET to derive the chip temperature from the forward voltage drop. This method has many limitations and disadvantages, and so it is not included in this AN.

Determining the temperature for static loads is easy. In most cases a thermal probe or a thermal camera will do the job.

With pulsed loads the situation changes dramatically. The thermal time constants inside a MOSFET and also the reaction times of probes and cameras don't allow the correct measurement of the chip temperature for load pulses in the µs or ms range.

Nevertheless the chip temperature has to be determined to enable a judgment about the MOSFET's temperature stress.

Using FEA requires special software and experience, so this AN focuses only on the following methods: calculation based on datasheet diagrams, and simulation with Infineon's SPICE libraries. Both ways to estimate the chip's temperature are explained in detail and the results and limitations of each method are shown and compared using different use cases:

1. A single high-power pulse
2. Repetitive high-power pulses with different thermal management

This AN is structured in seperate parts. In ***Chapter 2*** the simulation with Infineon's SPICE librairies is explained in detail. ***Chapter 3*** shows the way the "pocket calculator method" works in principle. ***Chapter 4*** and ***Chapter 5*** show typical use cases.

2 Thermal simulation with SPICE

Infineon MOSFET SPICE models include an internal thermal network. To access this it is necessary to use the level 3 (L3) models. They have either no suffix or _L3, as can be seen in ***Figure 1***. Here the MOSFET junction and case temperature can be accessed via extra terminals, enabling the addition of a cooling network and measurement of those temperatures.

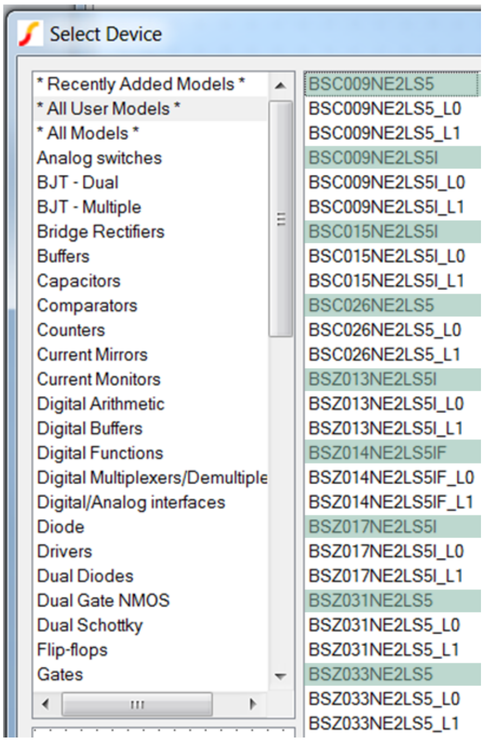

Figure 1 SPICE models for OptiMOS™5 – 25 V; L3 models are marked

The SPICE models can be found at ***www.infineon.com***. After searching for the MOSFET needed and following the “simulation” link the models can be downloaded. For a general introduction to the Infineon models and Simetrix simulation, please refer to AN 2014-02 “Introduction to Infineon’s Simulation Models for Power MOSFETs”.

2.1 Thermal model of the MOSFET

Inside the L3 MOSFET model a network of thermal resistances and capacitances is provided, like the one shown in ***Figure 2***. T_j is connected very close to the channel, with only R_{thb} in between and C_{thb} in parallel. This represents the thermal resistance and capacitance of the bond wires or clip. T_{case} has additional resistance-capacity pairs in the path to account for the inferior thermal connection, compared to T_j.

Thermal simulation with SPICE

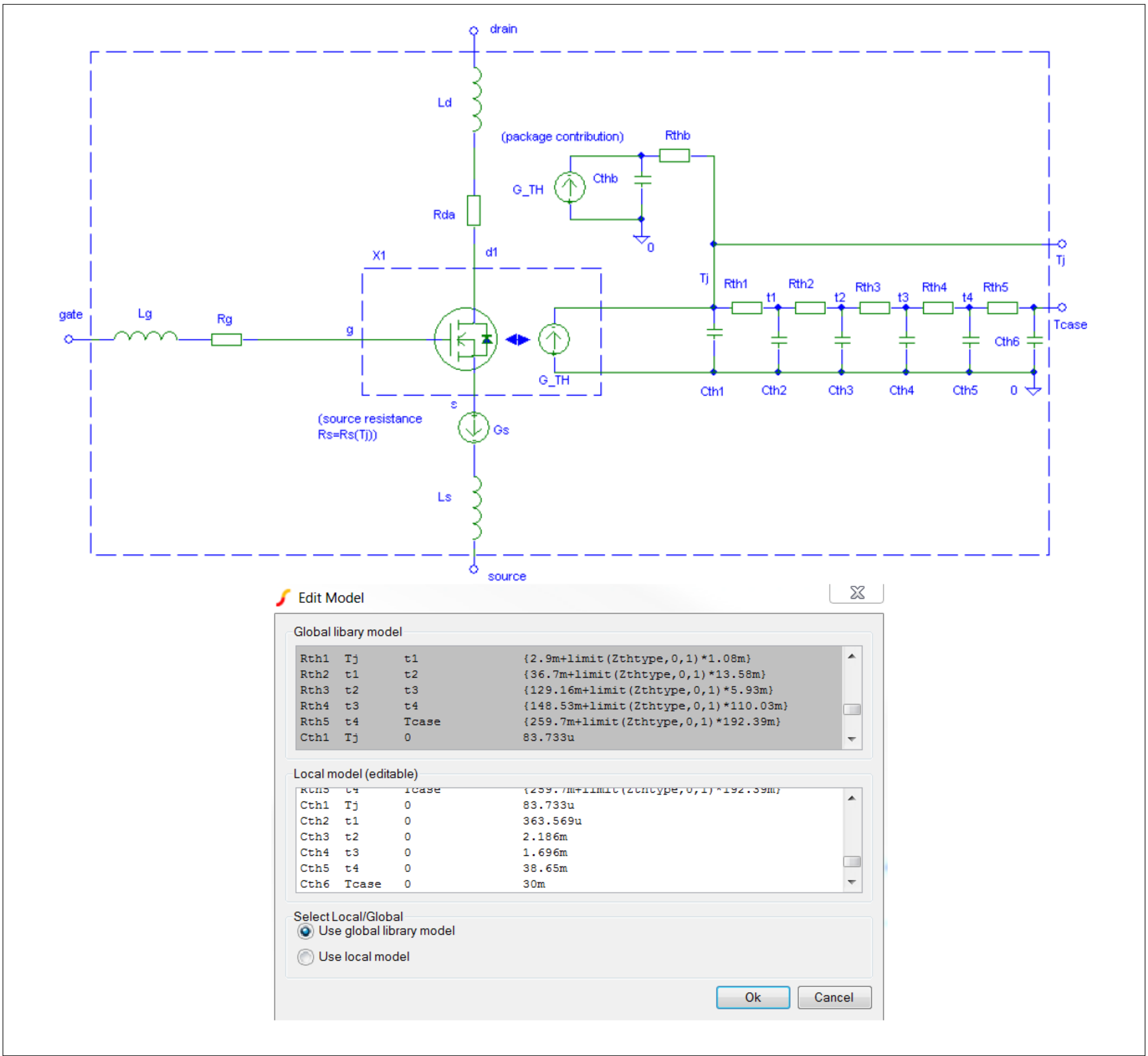

Figure 2 **Underlying structure of an L3 MOSFET model and the thermal parameters inside it**

2.2 Case temperature and cooling

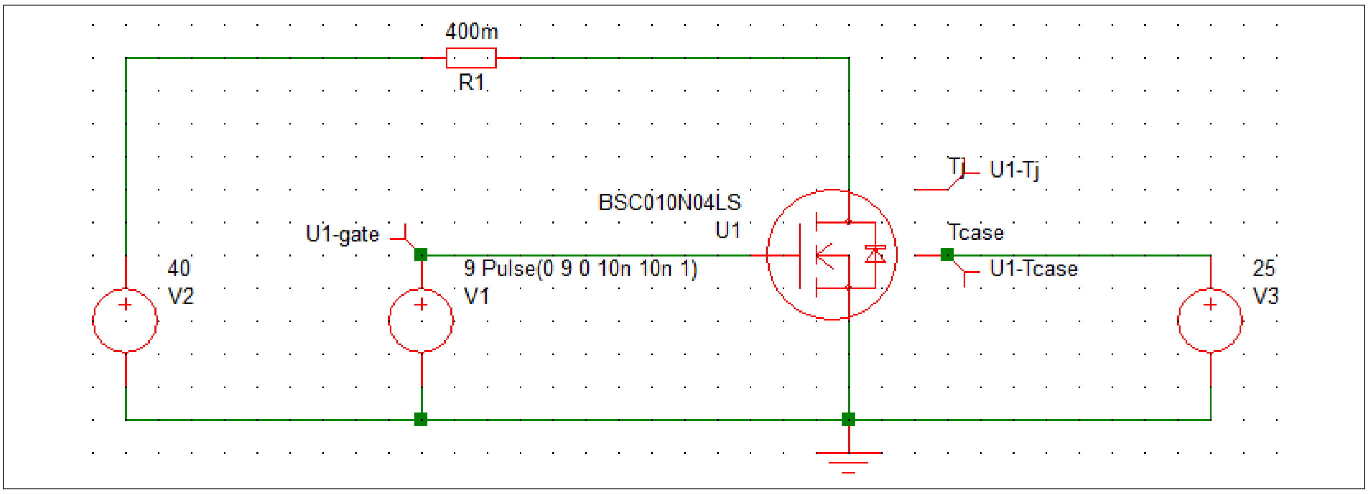

Figure 3 Switched MOSFET with the case perfectly cooled to 25°C

Figure 3 shows a circuit of a switched MOSFET. V2 provides 40 V between drain and source, R1 limits the maximum current to 100 A and V1 switches the MOSFET on for 1 s. T_j (junction temperature) and T_{case} (case temperature) are the terminals for the temperatures. V3 sets the ambient temperature to 25°C. At T_{case} and T_j a potential difference of 1 V equals 1 K and an external voltage of 0 V equals 0°C. The models are not limited to positive values. For example, connecting a potential of -40 V between ground and T_j will set the junction temperature to -40°C. Voltage probes are added to the MOSFET gate bus and T_{case}.

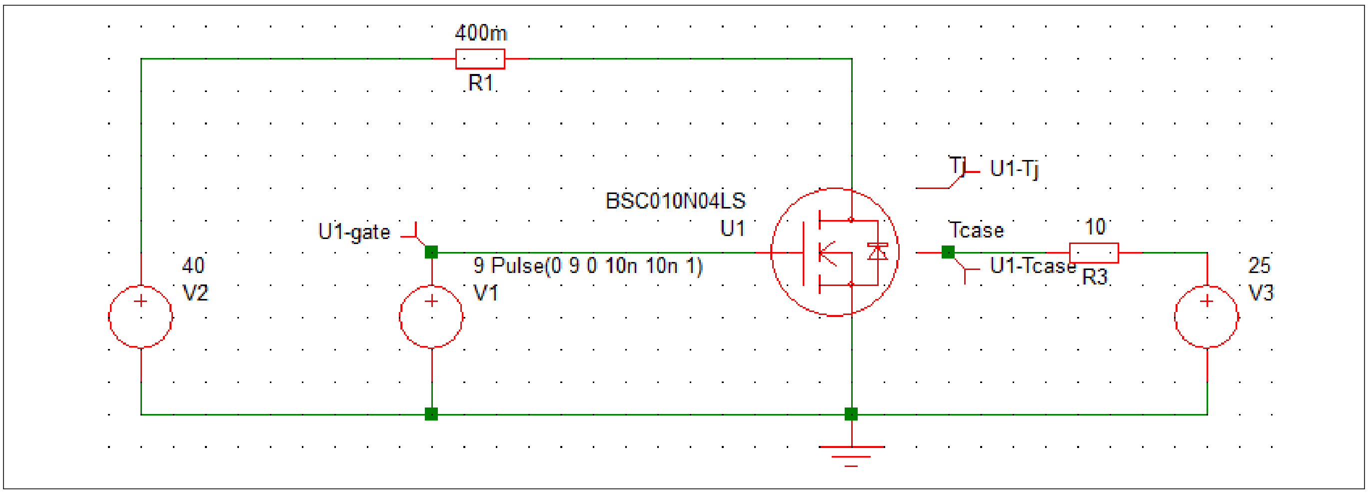

Figure 4 Switched MOSFET with added thermal resistance

In ***Figure 4*** we add the thermal resistance R3, which is connected to the case. An electrical resistance of 1 Ω equals a thermal resistance (R_{th}) of 1 K/W.

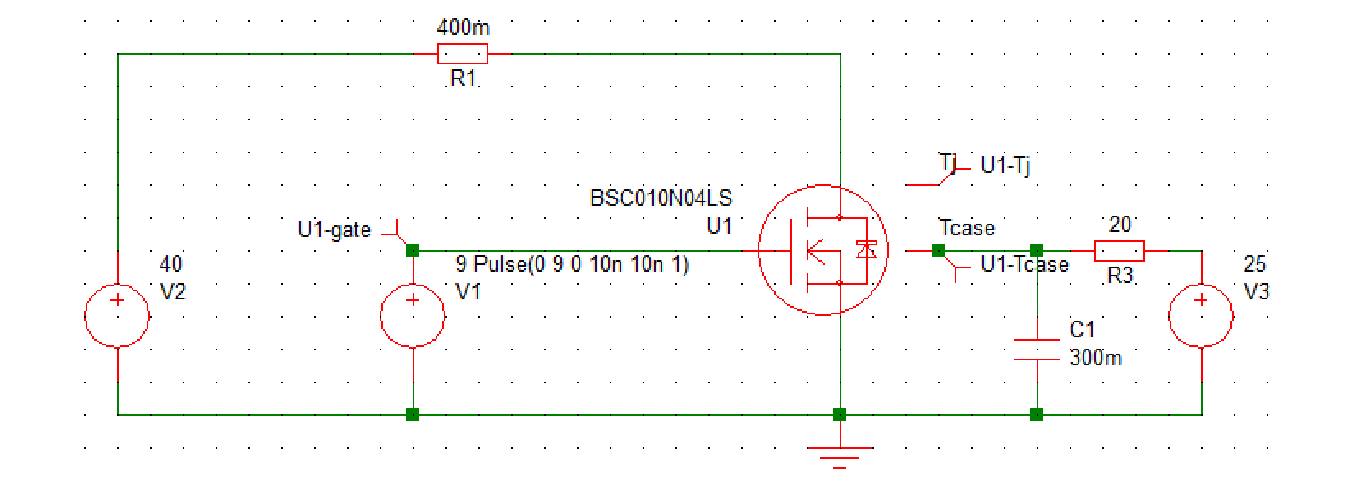

Figure 5 Switched MOSFET with thermal capacitance and thermal resistance

Finally a thermal capacity C1 is added in *Figure 5*. An electrical capacitance of 1 F equals a thermal capacitance (C_{th}) of 1 Ws/K. The resistance R3 is increased to 20 Ω, which, equals 20 K/W.

After running the simulation, curves like those shown in *Figure 6* are obtained. The gate signal is shown in green. The T_{case} voltage is simulated for the different scenarios shown from *Figure 3* to *Figure 5*. In the first one C1 and R3 are removed (red curve), so T_{case} is perfectly connected to 25 V (25°C). The case temperature doesn't increase at all. Second, a resistance R3 of 10 Ω is introduced, resulting in the blue curve. Finally, the circuit as depicted in *Figure 3*, with R3 = 20 Ω (20 K/W) and a capacity C1 = 300 mF (300 mWs/K) is simulated, resulting in the yellow curve. For the last two curves there is an increase in temperature as long as the device is switched on, and a cooling afterwards. Due to the high thermal capacity in the last case the temperature increase at the start is lower. The high thermal resistance slows down the cooling afterwards, so that the yellow and blue lines cross.

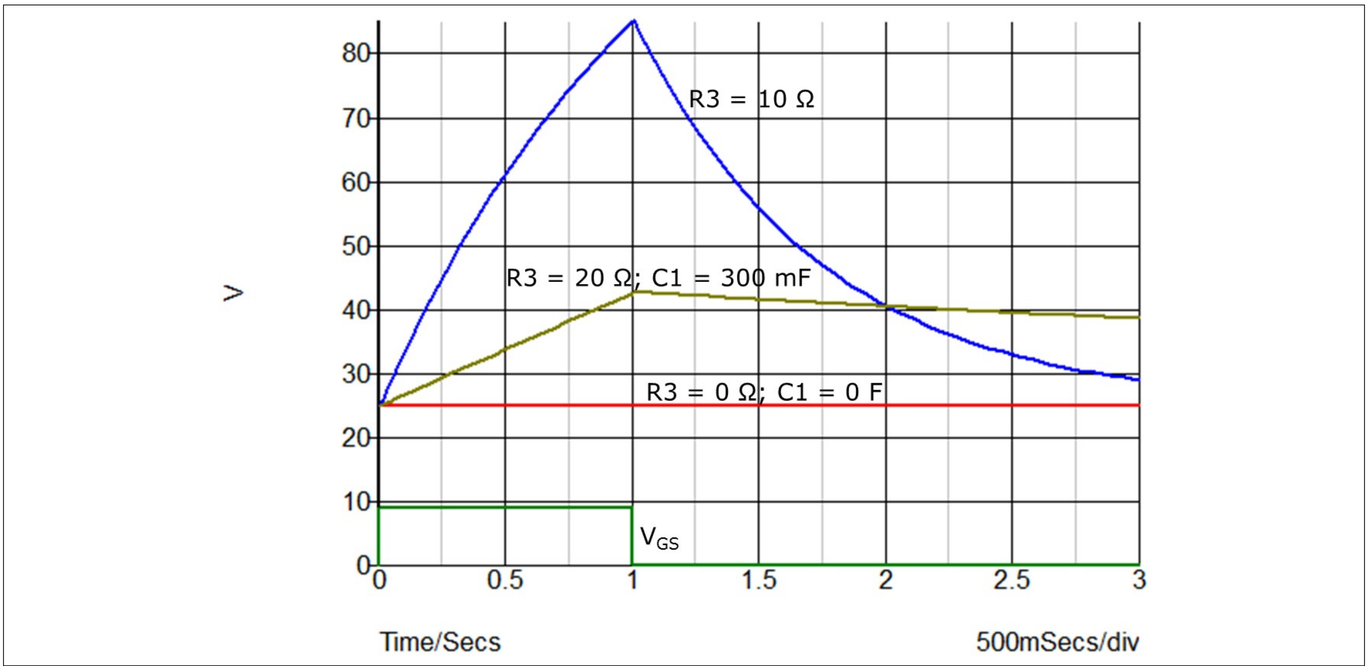

Figure 6 Measurement curves of the circuit in Figure 3 to Figure 5 showing the gate signal (green) and the voltage of the T_{case} node with thermal resistance and capacitance (yellow). The latter is also shown without any resistance and capacitance in the thermal network (red) and with only a resistor R3 = 10 Ω (10 K/W, blue)

2.3 Junction temperature

The junction temperature of the MOSFET can also be monitored. Here the circuit of ***Figure 4*** with R3=10 Ω (10 K/W) and no thermal capacity is used, as for the blue curve in in ***Figure 6***. The MOSFET is now switched on for 1 ms.

The temperatures can be read from the graphs in ***Figure 7***, keeping in mind that 1 V voltage difference equals 1 K temperature difference, and 0 V versus ground (0 V in the graphs) equals 0°C. During the time the MOSFET is switched on the temperature of the junction rises by roughly 1.5 K. The case temperature doesn't change significantly. After the device is switched off, the junction temperature immediately decreases, because no more heat is generated inside the device. Now the case temperature rises, as the heat from from the silicon gets transmitted to the package of the MOSFET. The total change in temperature is much less for the case than it is for the junction, because its combined thermal capacitance is much higher. After a few more ms the junction and case temperature will be equal. Then the whole device has a homogenous temperature and will slowly cool down.

Looking closely at the junction temperature in the left half of ***Figure 7***, a very short temperature increase at the maximum is visible. This is when the MOSFET gets switched off. A high current flows through the device while the resistance is increasing. A detailed view of this situation is shown on the right-hand side in ***Figure 7***. The temperature increases at the junction by 0.15 K. At the same time no kink in the temperature change for the case is visible, even at high magnification.

Short temperature changes at the junction will not impact the case temperature. The entire packaging as well as the MOSFET die itself have thermal capacities and thermal resistances, which cause a delay and averaging over time of the thermal behavior of the junction.

In ***Figure 7*** a temperature change of 1.7 K can be seen for the junction, which leads to a change of only around 0.1 K at the case.

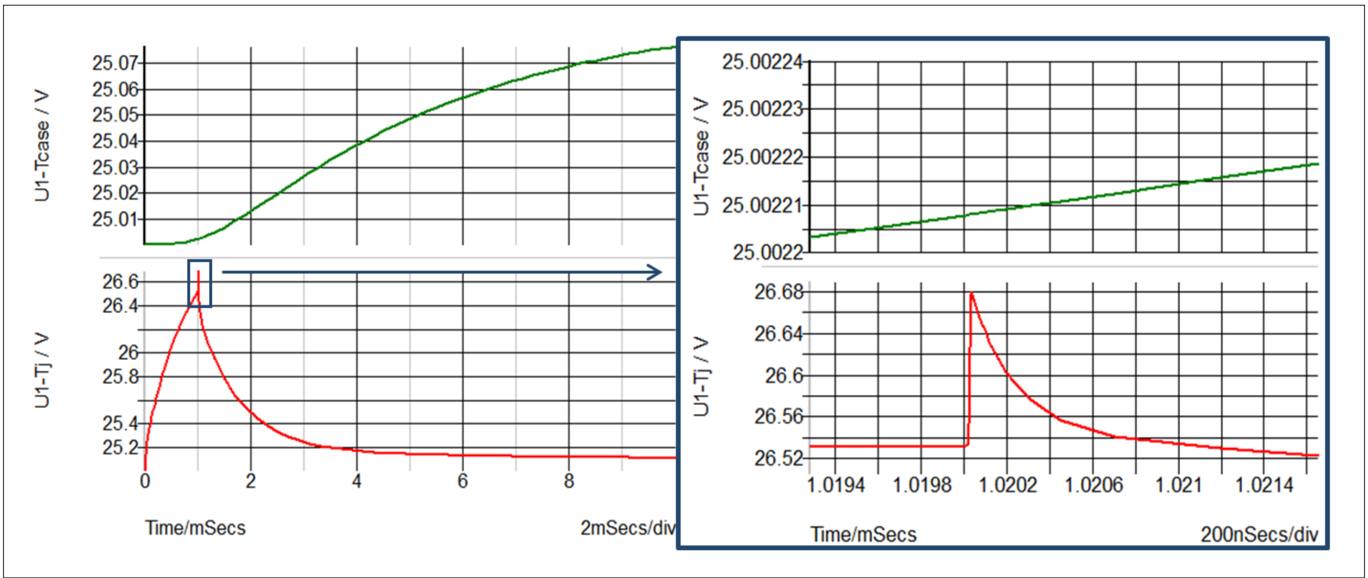

Figure 7 **Voltage on the case (green) and junction (red) node of the MOSFET. On the right-hand side a close-up of the time the MOSFET is switched off can be seen**

3 Pocket calculator method

In some cases it is easy to use the datasheet to derive the junction temperature.

If there is a single (nearly) rectangular power pulse, the Z_{thJC} (or, for small-signal MOSFETs, the Z_{thJA}) diagram can be used easily.

If the pulse doesn't have a rectangular shape some assumptions have to be made. This method is shown in the next chapter.

3.1 Calculation of the junction's peak temperature

Let's assume a current pulse of 300 A in a fully switched on IPB048N15N5.

The start condition is 70°C and the (single) pulse length is 100 µs (***Figure 8***).

What will be the peak junction temperature, $T_{j,max}$?

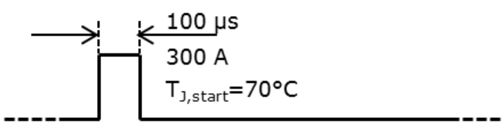

Figure 8 Pulse conditions

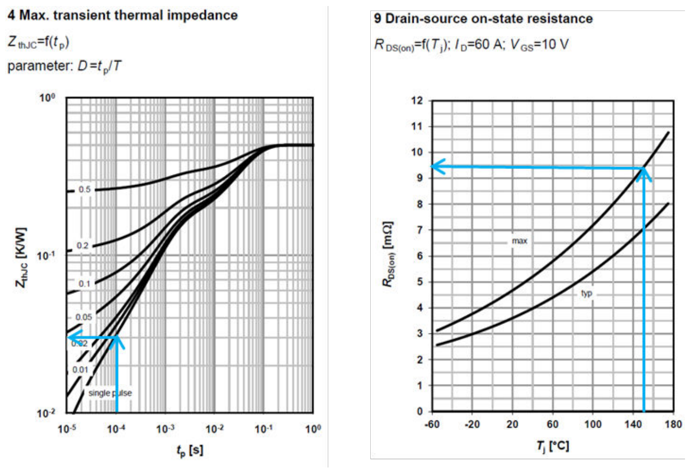

Figure 9 IPB048N15N5: Max. transient thermal impedance and drain-source on-state resistance

In only five steps the result is achieved, using datasheet diagrams (***Figure 9***) and a few simple formulas.

These five steps are shown for ohmic losses, e.g. $P = I^2 * R_{DS(on)}$.

An example for a more complex mode is shown in ***Chapter 4.3***.

Step 1: Find the working point in the Z_{thJC} diagram. With 100 µs (10^{-4} µs) the pulse Z_{thJC} is ~0.03 K/W.

Step 2: Use the $R_{DS(on),max}$ of the MOSFET under worst-case conditions (150°C): ~9.5 mΩ.

Step 3: Take the well-known fomula $P = I^2 * R_{DS(on)}$.

Step 4: Use the formula $\Delta T = P * Z_{thJC}$, exchange "P" with "$I^2 * R_{DS(on)}$" (from step 3): $\Delta T = I^2 * R_{DS(on)} * Z_{thJC}$.

Step 5: Insert values: $\Delta T = (300\ A)^2 * 0.0095\ \Omega * 0.03\ K/W \sim 25.65\ K$.

The start temperature of 70°C results in a junction temperature T_j ~95.65°C.

Please be aware that this is not the temperature of the complete and packaged part – it is only the junction temperature, the hottest spot.

For the $R_{DS(on)}$ a chip temperaure of 150°C is assumed. Now taking the calculated maximum temperature we can easily increase the precision by starting again from step 2, but now using the $R_{DS(on)}$ at ~96°C: ~7.1 mΩ instead of 9.5 mΩ followed by steps 3–5.

The Z_{thJC} diagram is only applicable if the case temperature (e.g. the bottom side of the lead frame) is kept constant. This is only possible with good thermal management (a heatsink mounted to the copper) or with a pulse short enough (several hundreds of µs) to not heat up the lead frame. For a SuperSO8 this time is potentially much shorter than with a D2PAK due to the much smaller and thinner lead frame.

For repetitive pulses the calculation is similar. Please take into account here that the Z_{thJC} diagram is only valid if the case temperature is kept at a constant temperature. In reality, without very good thermal management, the case heats up and the start temperature for the next "shot" is increased. Then the new start temperature can be calculated, as shown in ***Chapter 3.2***.

3.2 Calculation of the MOSFET's end temperature

If repetitive pulses are applied it is necessary to know the start temperature for the next pulse. In the last chapter the temperature increase of the hottest point, the junction of the MOSFET, was calculated. Without perfect thermal management the complete MOSFET is heated up to a certain temperature, which is the starting temperature of the next "shot". The SPICE library can be used to calculate this temperature (***Figure 10***).

```
.SUBCKT IPB048N15N5 drain gate source Tj Tcase PARAMS: dVth=0 dRdson=0 dgfs=0 dC=0 Zthtype=0 Ls=1.8n Ld=1n Lg=4n

.PARAM Rs=641u        Rg=1.1        Rd=50u       Rm=148u
.PARAM Inn=87         Unn=10        Rmax=4.8m    gmin=72
.PARAM RRf=350m       Rrbond=12m    Rtb=5.3      g2=729m
.PARAM act=26.4       Rsp=0.15

.FUNC   Pb(I,dT,Rb)  {Rb/(2*Rtb)*(I-limit(dT/(max(I,1n)*Rb)+RRf*I*g2,0,I))**2}

X1  d1 g s sp Tj S5_150_f_var PARAMS: a={act} Rsp={Rsp} dVth={dVth} dR={dRdson} dgfs={dgfs} Inn={Inn} Unn={Unn}
                                +Rmax={Rmax} gmin={gmin} RS={Rs} Rp={Rd} dC={dC} Rm={Rm}
Rg     g1     g     {Rg}
Lg     gate   g1    {Lg*if(dgfs==99,0,1)}
GS     s1     s     VALUE={V(s1,s)/(Rs*(1+(limit(V(Tj),-200,999)-25)*4m)-Rm)}
Rsa    s1     s     1Meg
Ls     source s1    {Ls*if(dgfs==99,0,1)}
Rda    d1     d2    {Rd}
Ld     drain  d2    {Ld*if(dgfs==99,0,1)}
Rsb    source s1     10
Rga    gate   g1     10
Rdb    drain  d2     10

G_TH   0    Tb  VALUE =  {Pb(abs(I(Ls)),V(Tj,Tcase),Rrbond*(1+(limit((V(Tb)+V(Tj))/2,-200,999)-25)*4m))}
Cthb   Tb       0              8.05m
Rthb   Tb       Tj             {Rtb}
Rth1   Tj       t1             {1.24m+limit(Zthtype,0,1)*463.24u}
Rth2   t1       t2             {13.66m+limit(Zthtype,0,1)*5.05m}
Rth3   t2       t3             {30.08m+limit(Zthtype,0,1)*6.99m}
Rth4   t3       t4             {67.06m+limit(Zthtype,0,1)*55.32m}
Rth5   t4       Tcase          {175.43m+limit(Zthtype,0,1)*144.71m}
Cth1   Tj       0              367.547u
Cth2   t1       0              834.731u
Cth3   t2       0              3.434m
Cth4   t3       0              4.488m
Cth5   t4       0              133.595m
Cth6   Tcase    0              190m
```

Figure 10 Screenshot of SPICE parameters for IPB048N15N5, with thermal capacitances marked in red

Values inside the red boxes show the thermal capacitances, where "u" means "micro" and "m" stands for "milli". The unit for the thermal capacitance is Ws/K. In summary, the overall thermal capacitance results in ~0.34 Ws/K.

The temperature rise can be calculated to:

$\Delta T = P * t / C_{th} = I^2 * R_{DS(on)} / C_{th}$

With the values of our example in the last chapter, and using the SPICE figures for the thermal capacitance, this results in a temperature rise of:

$\Delta T \sim (300\ A)^2 * 0.0095\ \Omega * 100\ \mu s / (0.34\ Ws/K) \sim 0.25\ K$

This means the complete part heats up by only ~0.25 K if no external heatsink is used.

In our example this results in an end temperature of 80.25°C, and this is the start temperature for the next "shot".

4 Repetitive high-power pulses without sufficient cooling

4.1 Short description of the cases and their technical background

Small pulses, which on their own aren't critical for the MOSFET, can become critical with a high-enough repetition rate and insufficient cooling time.

Figure 11 shows the circuit used for this investigation. It represents a short-circuit case in the application. A battery supplies the voltage of V1 = 36 V, and parasitic inductances and resistances are represented by L1 and R3. The active device is the 60 V MOSFET IPT007N06N.

V2 switches this MOSFET on for 50 µs with V_{GS} = 10 V and then off for 10 ms. This mimics a short-circuit case, which is registered and canceled by switching the MOSFET off within 50 µs.

R2 = 100 Ω is used as a gate resistor and to allow active clamping through D2. For this a diode with breakdown voltage of 47 V is used. This is to ensure that it breaks down under the whole temperature range before the MOSFET does. Then it raises V_{GS} by roughly V_{DS} – 47 V, slowly switching the device on and avoiding V_{DS} rising to a level which could cause avalanche in the device.

D1 is used to avoid current flow from gate to drain in the case that the MOSFET switches on with a very low drain-source voltage ($V_{GS} > V_{DS}$). The thermal network is connected to T_j.

C1 is setting the start temperature to 25°C. It is important that this capacitance is very small in order not to change the thermal behavior of the MOSFET. R1 represents the thermal resistance, here 10 K/W.

V3 is setting the ambient temperature to 25°C. A voltage probe at the T_j terminal provides the information about the temperature of the junction of the MOSFET.

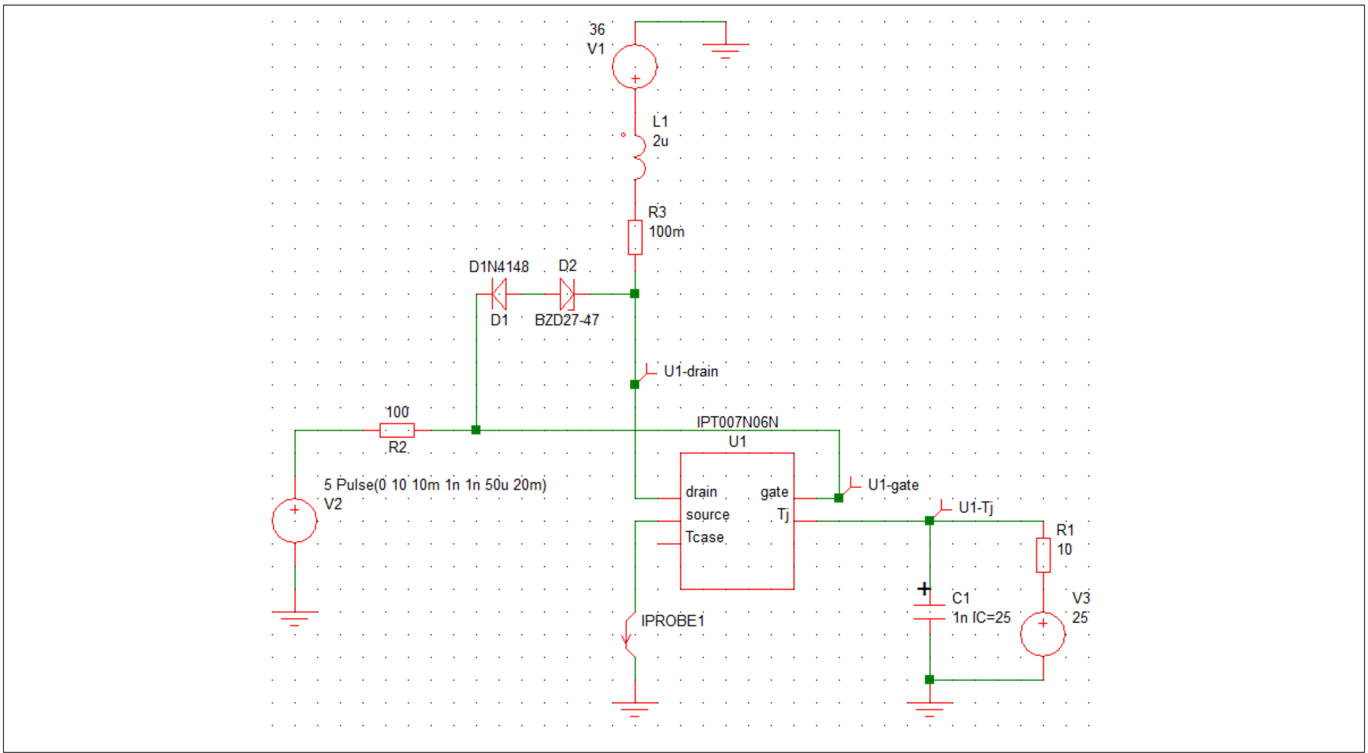

Figure 11 Circuit example for thermal simulation

4.2 Thermal simulation with SPICE

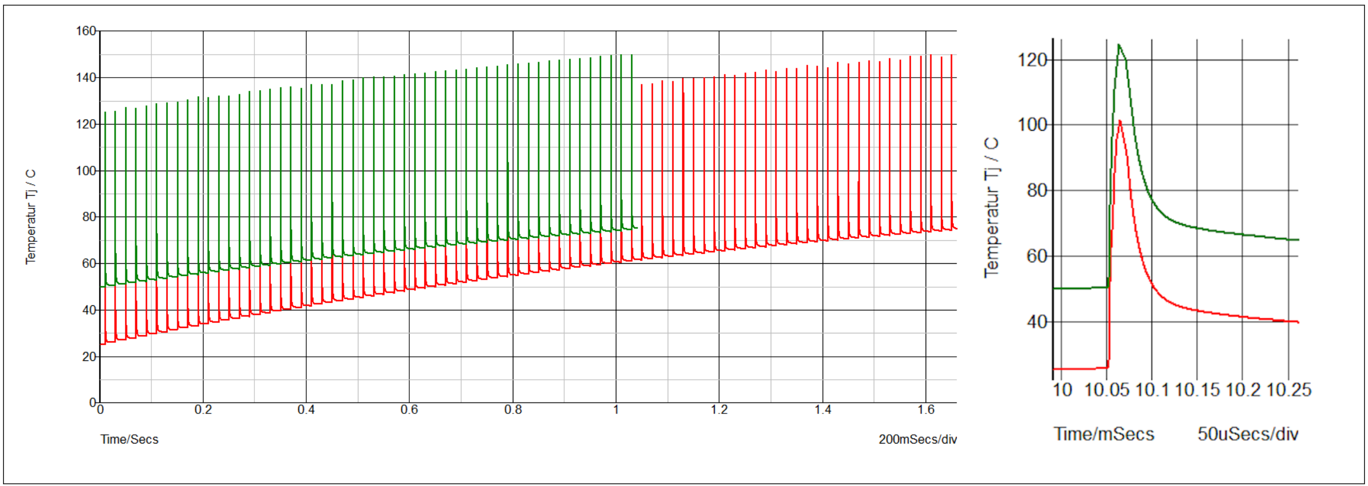

Figure 12 Temperature response of the circuit of Figure 11 with a starting temperature of 25°C (red) and 50°C (green). The voltage equals the temperature in degrees Celsius. On the right-hand side a detail of the first pulse is shown

If, due to board limitations for example, we allow a maximum temperature of 150°C, we see in ***Figure 12*** that we can allow 83 pulses or slightly more than 1.6 s without violating this limit. If we chose a starting temperature of 50°C, we can only allow 52 pulses, or a bit more than 1 s.

4.2.1 The effect of cooling

In the schematic of ***Figure 11*** cooling is already integrated. The high frequency of the pulses still heat the device up to its limits. Further immediate pulses will heat the device above its datasheet specification. A typical solution is to avoid the occurrence of those conditions for a certain time, e.g. by shutting down the application. ***Figure 13*** shows the temperature response of the circuit in ***Figure 11***, as shown in ***Figure 12***, followed by a pause of around 1 s to allow the device to cool down. The first set of pulses starts at the ambient temperature of 25°C, heats up the device close to 150°C at the peak, and lets it cool down to 50°C. This is the starting temperature of the new set of pulses. It can be clearly seen now that fewer pulses can be allowed until the previously set temperature limit is reached. This also fits the results in ***Figure 12***.

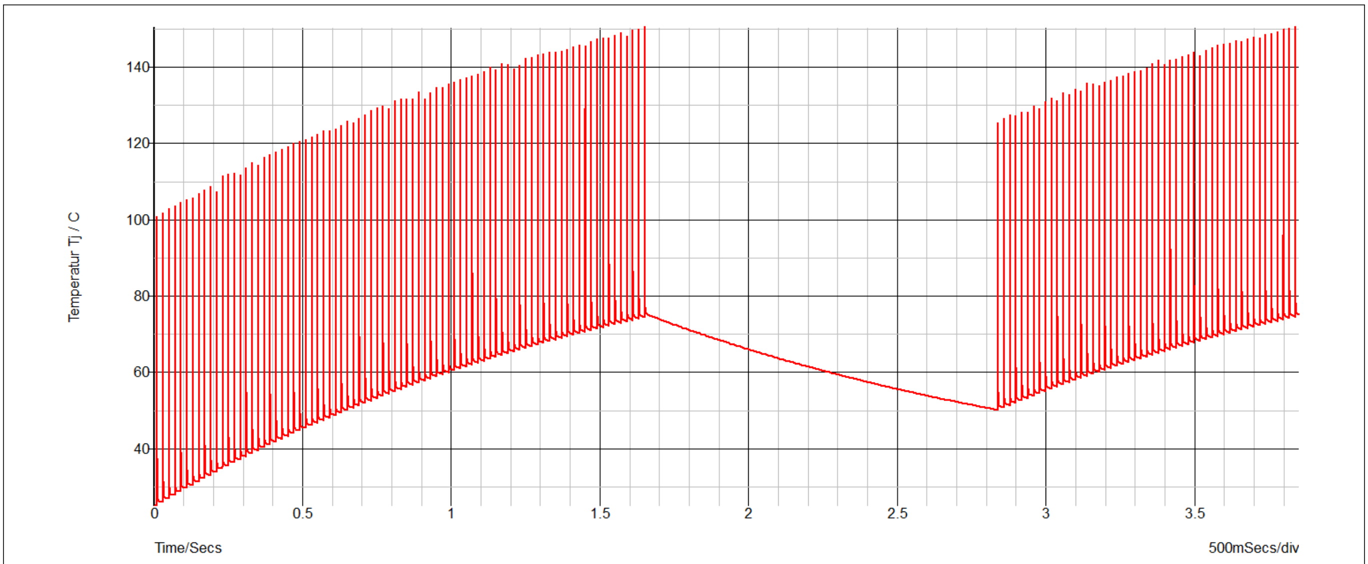

Figure 13 The simulation of Figure 12 followed by 1 s pause and additional pulses

4.3 Pocket calculator method

In ***Chapter 3*** a method was explained for rectangular pulses. As seen in ***Figure 14***, in reality voltage and/or current do not have this perfect shape.

So at first glance the method described earlier doesn't work in this scenario.

For short pulses, e.g. up to a few hundred µs, it is nevertheless possible without losing too much precision.

In the following a scenario in which the current increases due to a malfuntion (short-circuit or similar) from a very low to a very high level is assumed.

In the example of ***Chapter 4*** the drain current rises up to 320 A before the current protection starts to switch off the MOSFET. Immediately the drain-sourve voltage V_{DS} jumps to the clamping level ~55 V.

The MOSFET's drain-source voltage is limited by the clamping circuit described in ***Chapter 4***. Drain-source voltage and drain current are shown in ***Figure 14*** and already simplified in ***Figure 15***. The drain current decreases and reaches 0 V after ~21 µs. Now the V_{DS} again reaches the original value of 36 V.

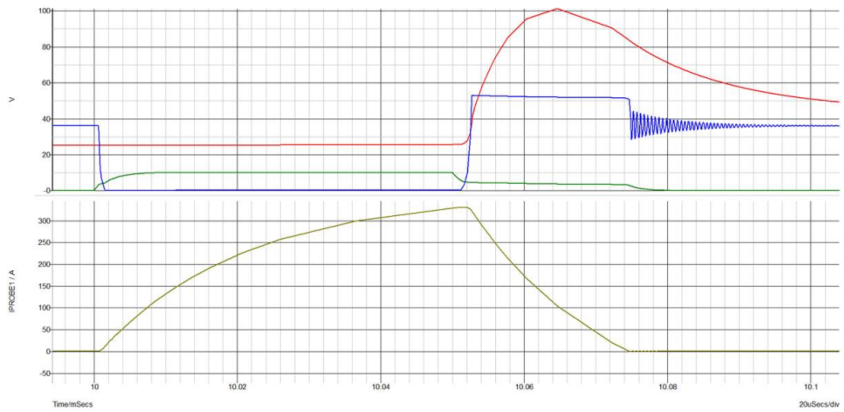

Figure 14 Drain-source voltage and drain current

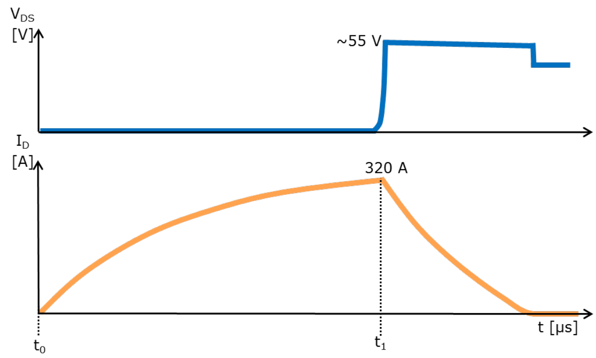

Figure 15 Drain-source voltage and drain current simplified

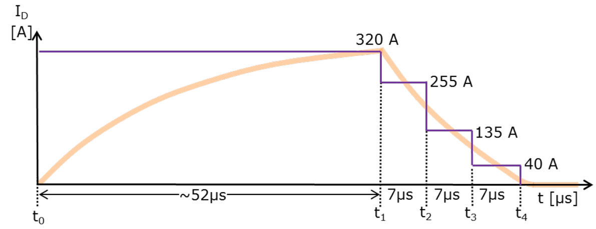

Figure 16 Drain current step-by-step approximation

In the first ~50 µs seconds ($t_0 \rightarrow t_1$) the current rises to the maximum value of ~320 A. For a first approximation the current can be assumed to be a rectangular 200 A pulse. The MOSFET is completely switched on, i.e. the maximum power losses occur at the end of this short pulse with $I^2 * R_{DS(on)}$~28 W.

Using steps 1–5 from chapter ***Chapter 3.1*** we get with (28 W 50 µs) and Z_{thJC}~0.02 K/W:

→ ΔT~28 W * 0.02 K/W = 0.56 K

This is a negligible junction temperature rise. Even if a rectangular current pulse with 320 A is assumed the temperature only rises by ΔT~1.26 K during this time.

As mentioned in chapter ***Chapter 3*** the Z_{thJC} diagram is valid only for rectangular pulses. But with a few assumptions the waveform can be replaced by a series of separate rectangular current pulses (***Figure 17*** to ***Figure 19***).

In the first step the decreasing current is chopped into a few slices, ideally with the same length (***Figure 17***).

The next step is to connect these points with straight lines. This also includes a small safety margin, as these lines are above the original waveform

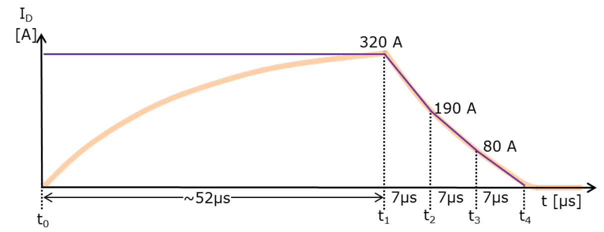

Figure 17 Drain current step-by-step approximation

Simplifying further by taking the average current in each time frame leads to this picture (***Figure 18***):

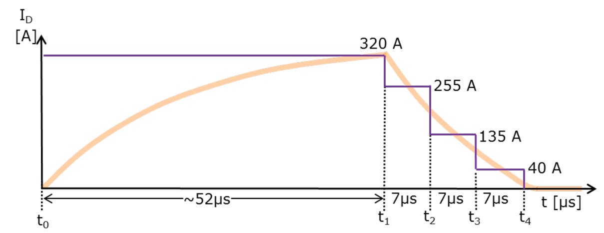

Figure 18 Drain current step-by-step approximation

Between t_2 and t_4 we have losses following P = V * I and this allows us to again build an average value:

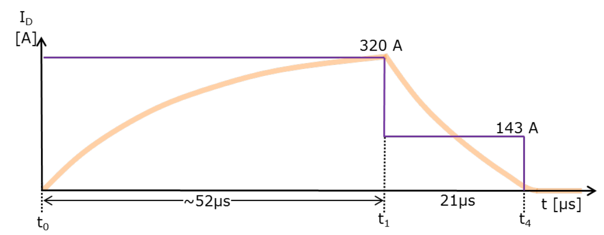

Figure 19 Drain current step-by-step approximation

In the following, the five-step approach shown in ***Chapter 3*** is modified.

Step 1: Find the working point in the Z_{thJC} diagram. With a 21 µs pulse Z_{thJC} is ~0.011 K/W.

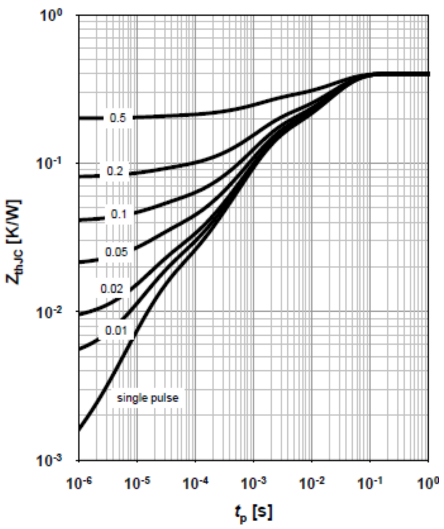

Figure 20 Z_{thJC}~0.011 for a single 21 µs pulse

Steps 2 and 3 can be skipped, and the losses can be calculated directly using voltage and current:

P = 55 V * 143 A~7865 W

Step 4: Use the formula $\Delta T = P*Z_{thJC}$.

Step 5: Insert values: ΔT = 55 V * 143 A * 0.011 K/W ~ 86 K.

With our start temperature of 25°C we get a junction temperature of T_j~111°C.

Please be aware that this is not the temperature of the complete and packaged part; it is only the junction temperature.

Adding the temperature rise between t_0 and t_1 results in a junction temperature increase by a few degrees Celsius, resulting in a junction temperature of ~112°C, which is still acceptable.

As a last step it is necessary to know the start temperature for the next "shot", shown in detail in chapter ***Chapter 3.2***, now modified for the IPT007N60N.

Each shot increses the overall temperature of the device by ~0.5 K, e.g. with a starting temperature of 25°C appromimately 70 shots are possible without violating the 150°C limit.

4.4 Limitations of the pocket calculator method

The method described is useful if a quick assumption is required. It uses a few worst-case assumptions, resulting in too-high values.

This simple way to extract temperatures is limited if the thermal management is more complex, as in the case of external thermal resistances, e.g. a heatsink.

Then the temperature does not rise by the same amount each time, and the temperature will reach a maximum value without further increase, as shown in ***Chapter 5.3***.

4.5 Comparison

The simulation and the calculation results are slightly different for 75 K rather than 86 K.

This difference is due to the safety margins we used in our simple calculation.

The pocket calculator method can be used to prove the results of the simulation, and is also useful if no simulation software is available.

5 Repetitive high-power pulse with sufficient cooling

5.1 Short description of the cases and their technical background

5.2 Thermal simulation with SPICE

An alternative to shutting down the device to allow it to cool down is to limit the repetition rate of the conditions causing the device to heat up. In ***Figure 21*** the 50 µs pulses of the previous graphs are shown, with a frequency of 30 Hz. This allows the device to cool down sufficiently and avoid over-heating.

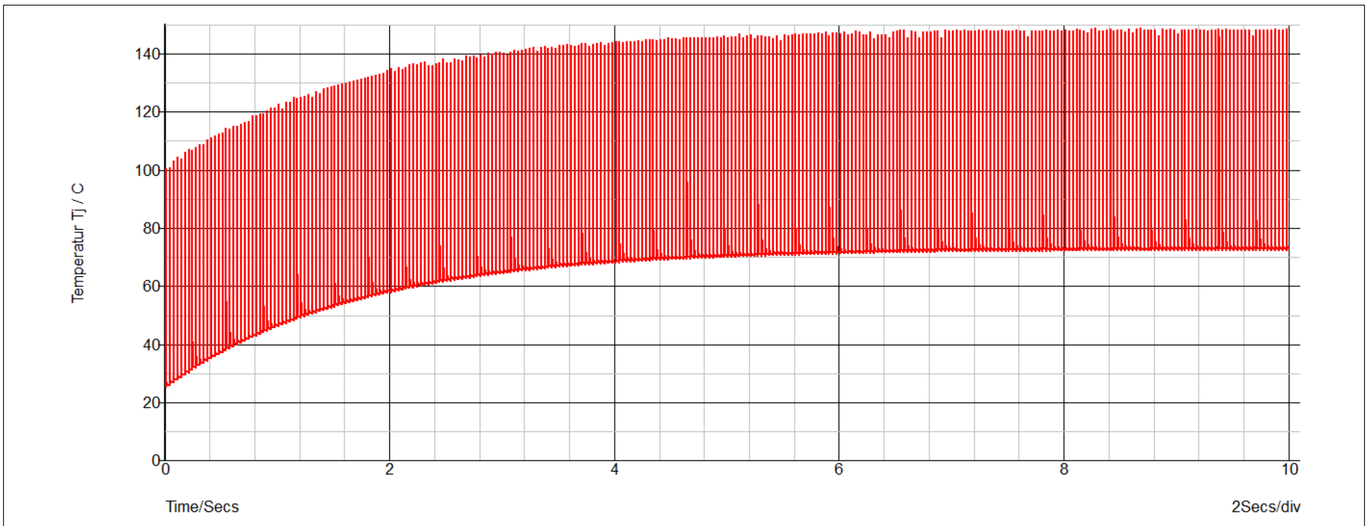

Figure 21 The simulation of the circuit of Figure 11 with a low duty cycle. The device is switched on for 50 µs and then switched off for 40 ms

5.3 Pocket calculator method

In ***Chapter 4.3*** the peak temperature rise was calculated to ~90 K.

A continuous pulsed mode is possible if the averaged power losses are low enough that the junction temperature doesn’t exceed the 150°C limit. So each pulse has to start at 150°C - 90°C = 60°C (or less) .

The thermal resistance is taken from the case to the ambient assumed with 10 K/W in our (simulation) example.

The averaged power can be calculated using the results from chapter ***Chapter 4.3*** together with the repetition rate of

40 ms: P_{avr} ~4 W.

The peak temperature is not visible outside, and the case shows the averaged temperature increase of ΔT = 4 W * 10 K/W = 40 K, e.g. a starting temperature for each pulse of 25°C + 40°C = 65°C.

5.4 Comparison

The results differ ~10% (65°C versus 72°C), which should be acceptable. Simulation and the simple calculation both lead to reasonable results.

6 Hot-swap applications/limitations

In hot-swap applications the MOSFET has to work for a much longer time (up to tenths of ms) in the linear mode.

Due to some more complex effects like hot-spot creation the methods shown can't be used under these conditions to check the datasheet limits for standard MOSFETs.

Special devices like the Linear FET are optimized for working in hot-swap applications like telecoms, or similar.

Please refer to AN_201705_PL11_005 "Linear FET combines advantages of Planar and Trench MOSFETs".

7 Summary

There are several ways to check whether the devices operate within the specifications.

Both simulation and the simpler method lead to similar results and either could be used depending on the complexity.

The simulation software allows for more complex conditions beyond the scope of the “pocket calculator method”.

If simulation software and good SPICE models are available, this should be the first choice.

Otherwise the “pocket calculator method” is a good way to get acceptable results.

Revision history

Document version	Date of release	Description of changes
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		•

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