120 W 24 V 3.5 A 12 V 3 A SMPS demonstrator with IDP2303

About this document

Scope and purpose

This document describes the 120 W 24 V 3.5 A 12 V 3 A 85 V_{AC} ~ 265 V_{AC} input off-line PFC-LLC converter demoboard featuring Infineon's digital PFC-LLC combi controller IDP2303 and MOSFETs IPD60R400CE and IPD60R1K5CE.

Intended audience

This document is intended for users of the IDP2303 who wish to design a PFC plus LLC converter with a non-auxiliary power supply for LED TV SMPS applications.

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1 Abstract

The demo board described in this document is a 120 W SMPS using a digital PFC-LLC combi controller (the IDP2303), which is the second generation of digital combi controller with a 16pin package developed by Infineon Technologies. The IDP2303 is specially designed for switch mode power supplies used in TV power system applications.

The IDP2303 is a highly integrated multi-mode power factor correction (PFC) and half-bridge LLC (HB LLC) controller. Multi-mode operation of the PFC controller and zero voltage switching of the LLC MOSFETs can significantly increase the power conversion efficiency, especially light load efficiency, while the system costs are minimized by the integrated high-voltage start-up cell, regulator for the PFC converter, MOSFET drivers and internal communication between the PFC and LLC controllers. The auxiliary power supply can be eliminated by the integrated high-voltage start-up cell and advanced burst mode control. With an active X-CAP discharge function, low stand-by power consumption during burst mode is supported. A comprehensive set of built-in protection features can greatly enhance the system operation and safety. Up to 40 different parameters ensure flexibility during system design and achieve optimal performance. All of these features make the IDP2303 a very competitive AC-DC controller for PFC-HB LLC resonant converter.

DPAK power MOSFETs are used in this reference design. For LED TVs, a slim SMPS board is a desire and also a challenge due to the limitations of active and passive components. Compared to FullPAK MOSFETs which are used in conventional TV SMPS design, DPAK MOSFETs have the advantage of being thinner and also easier to assemble. In this reference design, two IPD60R400CE are used in parallel for the PFC stage, and two IPD60R1K5CE are used in the LLC stage.

2 Demonstrator board

This document contains a list of features, the power supply specification, schematic, bill of material and the transformer construction documentation. Typical operating characteristics such as performance curves and oscilloscope waveforms are shown at the end of the document.

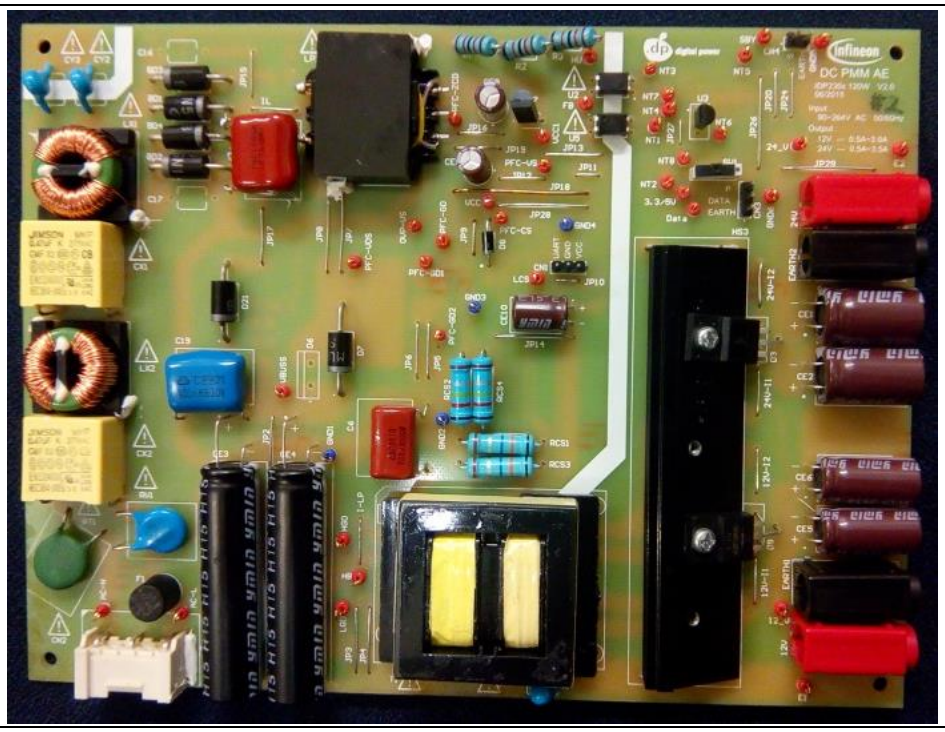


Figure 1 DEMO-IDP2303-120W PFC+LLC converter (top view)

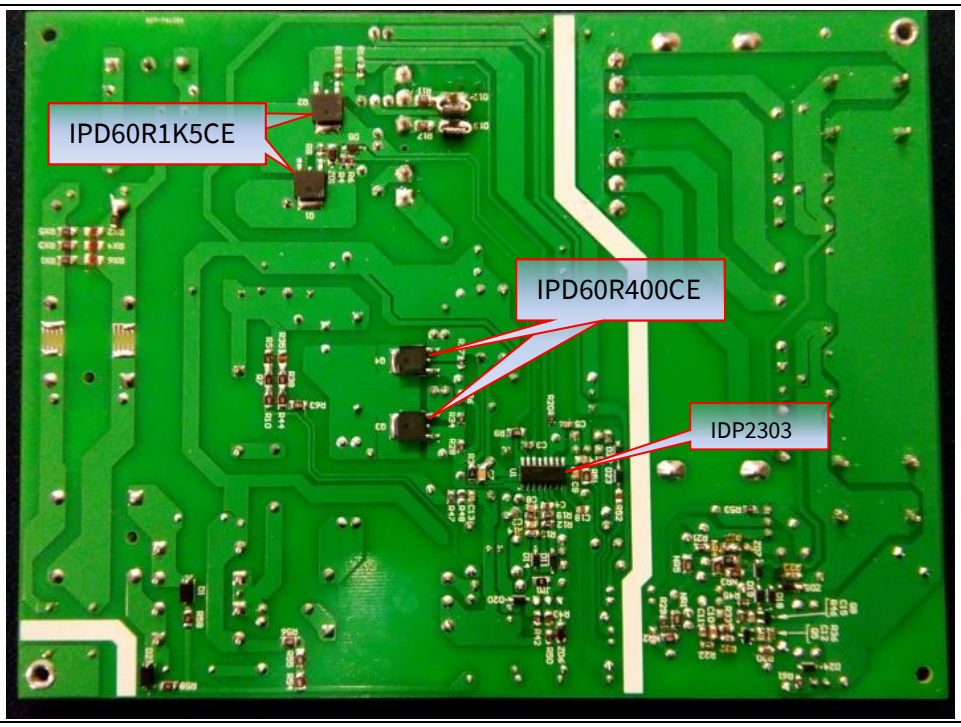


Figure 2 DEMO-IDP2303-120W PFC+LLC converter (bottom view)

3 Specifications of demonstrator board

Table 1 Specifications of DEMO-IDP2303-120W

Input voltage	85 V_{AC} ~ 265 V_{AC}
Input frequency	50/60 Hz
Output load	Full load : 12 V 3 A 24 V 3.5 A; Min load : 12 V 0.1 A 24 V 0.1 A; Stand by load : 10 V 17 mA 24 V 0 A
Power efficiency	>90% @230 V_{AC}
Power factor	>0.95 (230 V_{AC})
Controller IC	IDP2303
PFC/LLC MOSFET	IPD60R400CE/IPD60R1K5CE
Form factor (L x W x H)	200 mm x 150 mm x 14 mm

4 Features of IDP2303

Table 2 Features of IDP2303

Integrated 600 V start-up cell
Integrated floating driver for HB high-side MOSFET
Multi-mode operation of PFC
Integrated PIT regulator for PFC controller
Active X-CAP discharge function supports low stand-by power consumption
Comprehensive set of PFC/LLC protection features
Internal communication between PFC and LLC controller
Plenty of configurable parameters and failure protection modes
UART interface for communication and in-circuit configuration
Adaptive burst mode
Low ripple during standby
Parameter patching during DV/PV/production

5 Circuit description

5.1 Introduction

The circuit consists of two power stages; a front-end PFC pre-regulator and a half-bridge LLC resonant converter based on the IDP2303 controller.

5.2 Mains input and rectification

The AC line input side comprises the input fuse F1 as an over current protection device. The X capacitors (CX1, CX2), chokes (LX1, LX2), and Y capacitors (CY1-CY3) form a mains filter to minimize the feedback of RFI into the main supply. An NTC thermistor (RT1) is placed in series with the input to limit the initial peak inrush current.

5.3 Multi-mode PFC converter

After the bridge rectifier, there is a boost type PFC converter consisting of Q3, Q4, D7, CE3 and CE4. Two CoolMOS™ IPD60R400CE are used as the power switch Q3 and Q4. Due to its low R_{dson} and low output capacitance, the MOSFET conduction and switching loss can be effectively reduced. Output capacitor CE3 and CE4 provides energy buffering to reduce the PFC output voltage ripple.
The PFC choke current is sensed by the external shunt resistors RCS2 and RCS4. The sense voltage is fed into the CS0 pin and compared to the internal voltage level for current limiting.
Multi-mode operation is implemented by the IDP2303. Based on constant on time control, it does not require a direct sine wave reference signal. At heavy loads, it is beneficial for the PFC to work in CrCM mode. However, with CrCM operation, the PFC switching frequency may increase to a quite a high value at light load, which leads to high switching losses. In this controller, the PFC can lower the switching frequency by adding an additional delay into each switching cycle through selecting further PFC MOSFET drain-source voltage valleys to achieve QR2, QR3 and up to QR10 operation. In this way, the switching frequency is limited between a minimum and maximum value.
The IDP2303 provides enhanced PFC output overvoltage protections with two different levels. Thus, it can effectively monitor and protect the PFC bus voltage against any overshoot in the case of the abrupt load or input voltage variations.
The IDP2303 provides a redundant PFC output overvoltage protection through the MFIO pin. During certain fault conditions, such as the resistance of the VS voltage divider low-side resistor being reduced by 30% after long term operation, the PFC bus voltage could exceed the limit of its output capacitor, leading to a serious failure. With the PFC redundant OVP feature, an independent bus voltage sensing path is used to protect against this type of failure in the PFC output.
The IDP2303 features VS pin open loop protection, which can effectively protect the whole system in the case of the VS pin external high side resistor becoming open circuit.
Brown-in and brown-out protections are provided with the integrated startup cell via the HV pin to avoid the system working at extremely low AC input.
In order to meet the increasingly stringent system safety requirements, the IDP2303 also features VS pin open circuit protection and VS pin short to adjacent pin protection.
In addition, the IDP2303 features long term continuous conduction mode protection, which can help to protect the whole system in the case of a shorted PFC bypass diode or heavy load condition.

5.4 Half-bridge LLC resonant converter

The second stage is a half bridge LLC resonant converter, operating with zero-voltage switching. The PFC-LLC combi controller (IDP2303) incorporates the necessary functions to drive the half bridge's high side and low side MOSFETs (Q1 and Q2) with a 50% duty cycle including a configurable dead time. The switching frequency can be changed by the IDP2303 to regulate the output voltage against the load and input voltage variations.

Circuit description

During operation, the primary MOSFETs Q1 and Q2 are turned-on under a ZVS condition and the secondary rectifier diodes D3 and D9 are turned-on and turned-off under a ZCS condition. Hence, high power conversion efficiency is achieved.
As the IDP2303 has the half bridge high side MOSFET driver built-in based on Infineon coreless transformer technology, there is no requirement to add an external driver module, such as a pulse transformer or driver IC, to drive the high side MOSFET. Hence, the system BOM cost and design effort is greatly reduced.
The mains transformer (T1) uses a magnetic integration approach, incorporating the resonant series and shunt inductances. Thus, no additional external coils are required for resonance. The transformer configuration for the secondary winding is center-tapped, and the output rectifiers, D3 and D9, are schottky type diodes, in order to reduce the power dissipation.
The voltage across the half bridge shunt resistors (RCS1 and RCS3) is fed into the CS1 pin of the IDP2303. Thus, the current flowing through the primary winding is strictly controlled to ensure the system max power limitation and over current protection.
Since the IDP2303 has an internal voltage reference and pull-up resistor for the HBFB pin, the feedback signal from the opto-coupler (U2) can be directly fed into this pin, which also minimizes the BOM cost and design effort. Thus, with the feedback information, the IDP2303 is able to regulate the LLC frequency to achieve the LLC load regulation and line regulation.
In the case of an overload condition, the HBFB pin voltage will rise and may reach $V_{_OlpHB}$, which will trigger the overload protection. As a result, the LLC will stop switching after a blanking time and enter the auto-restart mode, with a configurable break time to protect the whole power supply system.
In the case of an extremely light load condition, the voltage on the HBFB may drop and reach another threshold ($V_{_burst_enter}$), which will cause the LLC to stop switching and enter the burst mode after a blanking time. When the voltage on the HBFB pin increases to reach the threshold $V_{_burst_on}$, the LLC will resume switching. Thus, at extremely light load conditions, with this burst mode feature, the LLC output will still be under regulation.
When a heavy load is applied, the HBFB pin voltage exceeds $V_{_burst_exit}$ or the burst on time reaches its maximum setting $t_{_burst_on_max}$, the LLC will leave burst mode and resume normal operation.
To achieve good cross regulation, a weighted voltage control is adopted. R23, NR3, R27, NR4, R32 and R33 form a voltage divider network that senses both of the output voltages. When the Power_On signal (switch SW1 pin 1 connects to pin 3) is high, transistor Q5 is turned on, and R32 and R33 are connected in parallel, thus the output voltage is regulated at the target level during normal operation. On the other hand, during standby operation (switch SW1 pin 1 disconnects from pin 3), Q5 is off, and R32 is disconnected, which will reduce the output voltage to lower standby power consumption. Output voltage regulation is controlled through the shunt regulator TL431 (U3) and the optocoupler (U2) provides electrical isolation between the primary and secondary sides. Resistor R29 provides the bias current required by U3 and is placed in parallel with U2 to ensure that the bias current to the TL431 does not become a part of the feedback current. Resistor R21 sets the overall DC loop gain and limits the current through U2 during transient conditions. R22, C10 and C11 set the frequency response for the feedback circuit.

6 Circuit diagram

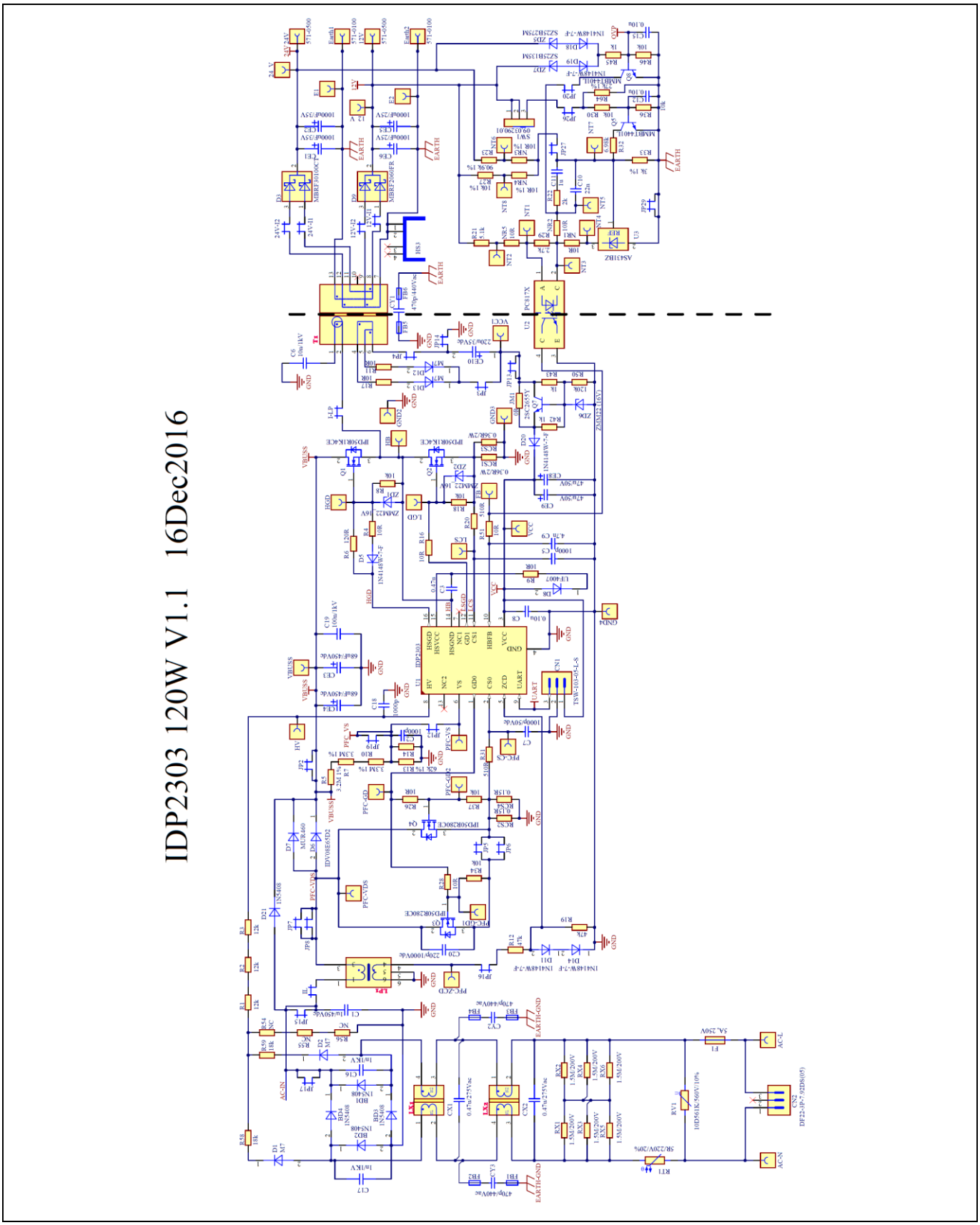


Figure 3 Schematics of 120 W PFC + LLC converter

7 PCB layout

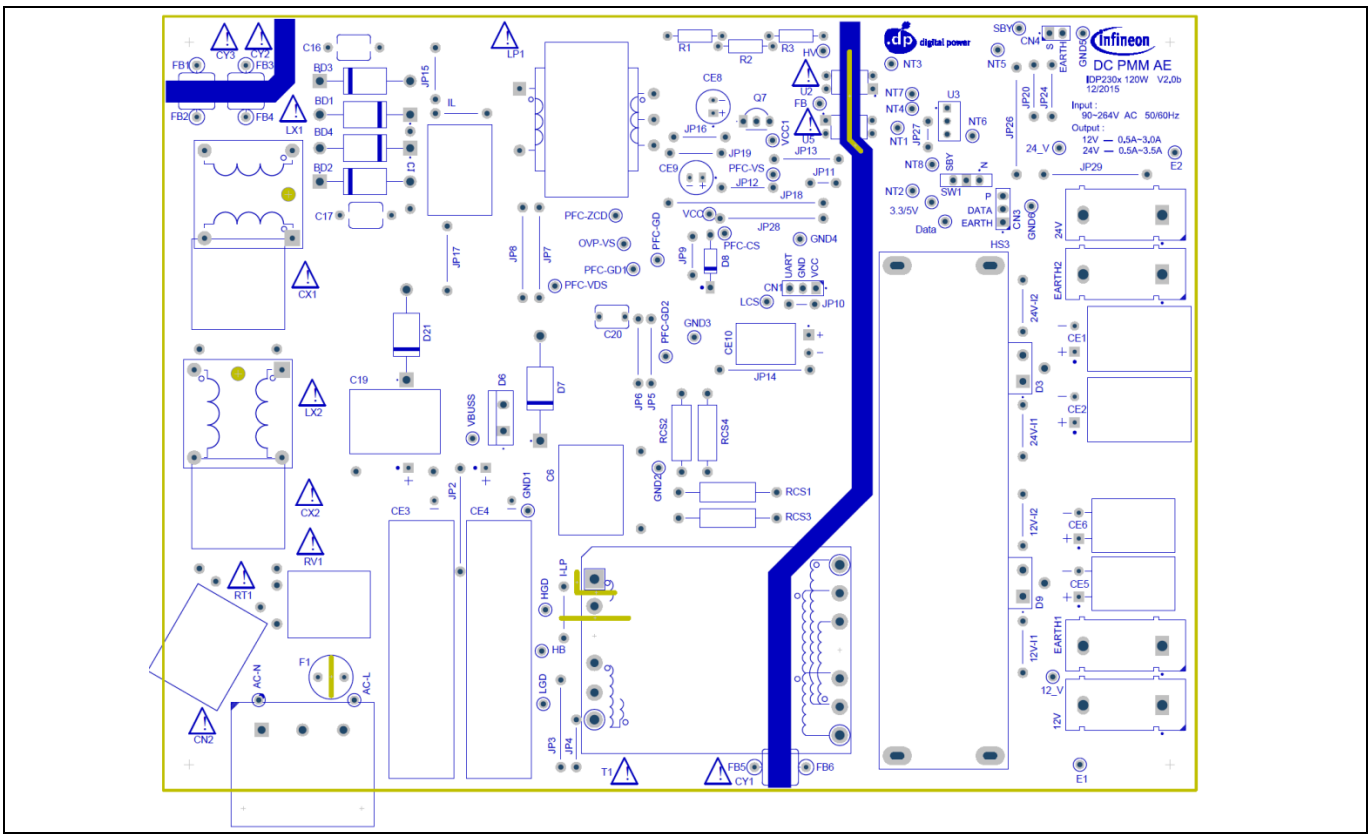


Figure 4 Top side component legend– View from component side

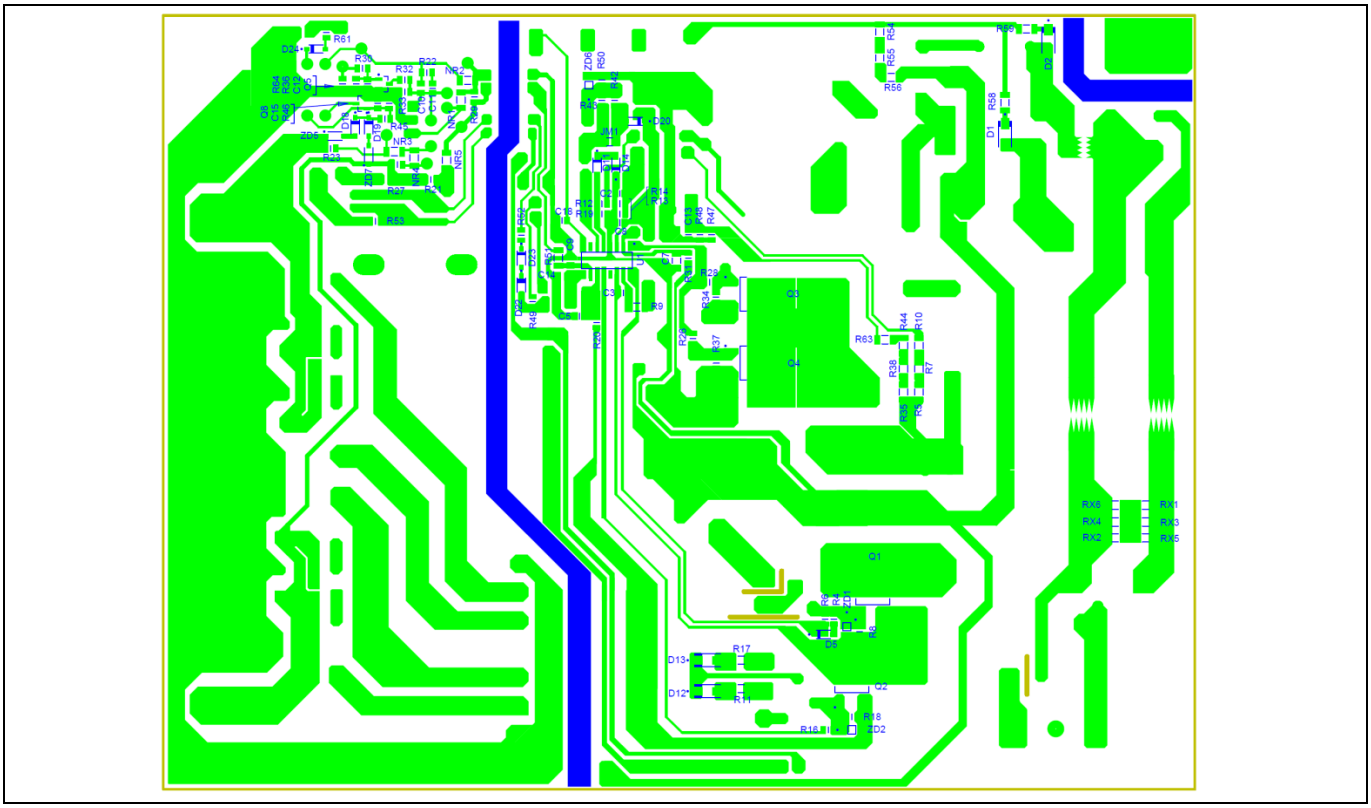


Figure 5 Bottom side component legend– view from solder side

8 Bill-of-material

Table 3 Bill of material

Item	Circuit code	Qty	Description / value	Package	Manufacturer
1	12 V, 24 V (output socket)	2	Banana socket, Red,'571-0500	2pin	
2	Earth1,Earth2 (output socket)	2	Banana socket, black,'571-0100	2pin	
3	12V-I1, 12V-I2, 24V-I1, 24V-I2, JP2, JP4, JP5, JP6, JP9, JP12, JP18, JP19, JP20, JP21, JP23	15	JP-THT-1.00_2.20_10_0.80-2P	axial	
4	IL, JP3, JP10, JP11	4	JP-THT-1.00_2.20_15_0.80-2P	axial	
5	JP1, JP8, JP13, JP15	4	JP-THT-1.00_2.20_20_0.80-2P	axial	
6	JP14	1	JP-THT-1.00_2.20_5_0.80-2P	axial	
7	JP22	1	JP-THT-1.00_2.20_12.5_0.80-2P	axial	
8	JP7	1	JP-THT-1.00_2.20_17.5_0.80-2P	axial	
9	3.3/5V, 12_V, 24_V, AC-L, AC-N, Data, FB, HB, HGD, HV, LCS, LGD, NT1, NT2, NT3, NT4, NT5, NT6, NT7, NT8, OVP-VS, PFC-CS, PFC-GD, PFC-GD1, PFC-GD2, PFC-VDS, PFC-VS, PFC-ZCD, SBY, VBUSS, VCC, VCC1	32	Test point, THT, '5003	pin	
10	E1, E2, GND5, GND6	4	Test point, THT, '5004	pin	
11	GND1, GND2, GND3, GND4	4	Test point, THT, '5002	pin	
12	HS3	1	heatsink for D3, D9	4 holes	
13	CN1	1	3pin heasder, TSW-103-05-L-S	3pin	
14	CN2	1	Input socket, DF22-3P-7.92DS(05)	3pin socket	
15	CN3	1	3pin header. TSW-103-05-L-S,	3-pin	
16	CN4	1	2pin header, TSW-102-05-L-S,	2-pin	
17	BD1	1	3 A 1 KV diode, 1N5408	axial	
18	BD2	1	3 A 1 KV diode, 1N5408	axial	
19	BD3	1	3 A 1 KV diode, 1N5408	axial	
20	BD4	1	3 A 1 KV diode, 1N5408	axial	
21	C1	1	1 u/450 V, mpp flim	radial	
22	C10	1	47 n	SMD 0805	
23	C11	1	2.2 u	SMD 0805	

Bill-of-material

Item	Circuit code	Qty	Description / value	Package	Manufacturer
24	C12	1	0.10 u	SMD 0805	
25	C13	1	1000 p	SMD 0805	
26	C14	1	1000 p	SMD 0805	
27	C15	1	0.10 u	SMD 0805	
28	C18	1	n.a	SMD 0805	
29	C19	1	100 n/1 kV, mpp flim	radial	
30	C2	1	1800 p	SMD 0805	
31	C20	1	220 p 1 kV ceramic	radial	
32	C3	1	0.47 u	SMD 0805	
33	C4	1	nil	SMD 0805	
34	C5	1	1000 p	SMD 0805	
35	C6	1	10 nF 5% 1 kV, mpp film cap	radial	
36	C7	1	1000 p/50 V, 1206	SMD 1206	
37	C8	1	0.10 u	SMD 0805	
38	C9	1	4.7 n	SMD 0805	
39	CE1	1	1000 uF/35 V, HV 12.5x20, E-cap	12.5x20	
40	CE10	1	220 u/35 V, KMG 8x11.5, E-cap	8x11.5	
41	CE2	1	1000 uF/35 V, HV 12.5x20 E-cap	12.5x20	
42	CE3	1	68 uF/450 V, KXJ 12.5x50, E-cap	12.5x50	
43	CE4	1	68 uF/450 V, KXJ 12.5x50, E-cap	12.5x50	
44	CE5	1	1000 uF/25 V, VZ 10x20, E-cap	10x20	
45	CE6	1	1000 uF/25 V, VZ 10x20, E-cap	10x20	
46	CE8	1	33 u/50 V, YXG, 6.3x11, E-cap	6.3x11	
47	CE9	1	47 u/50 V, YXG, 6.3x11, E-cap	6.3x11	
48	CX1	1	0.47 u/275 V_{AC}, X2-cap	radial	
49	CX2	1	0.47 u/275 V_{AC}, X2-cap	radial	
50	CY1	1	470 p/330 V_{AC}, Y1-cap	radial	
51	CY2	1	470 p/300 V_{AC}, Y1-cap	radial	
52	CY3	1	470 p/300 V_{AC}, Y1-cap	radial	
53	D1	1	M7, 1 A 1 kV diode	SMD	
54	D11	1	1N4148W-7-F, diode	SMD	
55	D12	1	MBRS360BT3G 3 A 60 V schottky diode	SMD	
56	D13	1	MBRS360BT3G 3 A 60 V schottky diode	SMD	
57	D14	1	1N4148W-7-F, diode	SMD	

Bill-of-material

Item	Circuit code	Qty	Description / value	Package	Manufacturer
58	D18	1	1N4148W-7-F, diode	SMD	
59	D19	1	1N4148W-7-F, diode	SMD	
60	D2	1	M7, 1 A 1 KV diode	SMD	
61	D20	1	1N4148W-7-F, diode	SMD	
62	D21	1	1N5408, 3 A 1 KV diode	axial	
63	D22	1	1N4148W-7-F, diode	SMD	
64	D23	1	1N4148W-7-F, diode	SMD	
65	D24	1	1N4148W-7-F, diode	SMD	
66	D3	1	MBRF30100CT, 30 A 100 V schottky diode (dual diodes) in TO220 FullPAK	TO-220 FullPAK	
67	D5	1	1N4148W-7-F, diode	SMD	
68	D7	1	MUR460, 4 A 600 V ultra fast diode	axial	
69	D8	1	UF4007, 1 A 1 KV diode	axial	
70	D9	1	MBRF2060CT, 20 A 60 V schottky diode (dual diode) in TO220 FullPAK	TO-220 FullPAK	
71	F1	1	5 A, 250 V time lag TR5 fuse	TR5	
72	JM1	1	0 R, 1206	SMD 1206	
73	LP1	1	200 uH, EQ30/ER30, 39T:5T	EQ30/ER30	
74	LX1	1	18 mH x2, CMC toroid Φ20, wire Φ0.43	toroid with holder	
75	LX2	1	18 mH x2, CMC toroid Φ20, wire Φ0.43	toroid with holder	
76	Q1	1	IPD60R1K5CE, 600 V 1.5 Ω	DPAK	Infineon Technologies
77	Q2	1	IPD60R1K5CE, 600 V 1.5 Ω	DPAK	Infineon Technologies
78	Q3	1	IPD60R400CE, 600 V, 0.4 Ω	DPAK	Infineon Technologies
79	Q4	1	IPD60R400CE, 600 V, 0.4 Ω	DPAK	Infineon Technologies
80	Q5	1	MMBT4401L, NPN transistor	SMD	
81	Q7	1	2SC2655Y, NPN Transistor	TO92	
82	Q8	1	MMBT4401L, NPN transistor	SMD	
83	R1	1	11 k 1%, 1 W/0.5 W	axial	
84	R10	1	3.3 M 1%, 1206	SMD 1206	

Bill-of-material

Item	Circuit code	Qty	Description / value	Package	Manufacturer
85	R11	1	2.7 R	SMD 0805	
86	R12	1	47 k	SMD 0805	
87	R13	1	63.4 k 1%	SMD 0805	
88	R14	1	Nil	SMD 0805	
89	R16	1	10 R	SMD 0805	
90	R17	1	2.7 R	SMD 0805	
91	R18	1	10 k	SMD 0805	
92	R19	1	47 k	SMD 0805	
93	R2	1	11 k 1%, 1 W/0.5 W	axial	
94	R20	1	510 R	SMD 0805	
95	R21	1	5.1 k	SMD 0805	
96	R22	1	1 k	SMD 0805	
97	R23	1	90.9 k 1%	SMD 0805	
98	R26	1	10 R	SMD 0805	
99	R27	1	10.2 k 1%	SMD 0805	
100	R28	1	10 R	SMD 0805	
101	R29	1	2.7 k	SMD 0805	
102	R3	1	11 k 1%, 1 W/0.5 W	axial	
103	R30	1	10 k	SMD 0805	
104	R31	1	510 R/200 V/1%, 1206	SMD 1206	
105	R32	1	9.76 k 1%	SMD 0805	
106	R33	1	2.67 k 1%	SMD 0805	
107	R34	1	10 k	SMD 0805	
108	R35	1	1 M 1%, 1206	SMD 1206	
109	R36	1	10 k	SMD 0805	
110	R37	1	10 k	SMD 0805	
111	R38	1	1 M 1%, 1206	SMD 1206	
112	R39	1	10 k	SMD 0805	
113	R4	1	10 R	SMD 0805	
114	R40	1	10 k	SMD 0805	
115	R41	1	10 k	SMD 0805	
116	R42	1	1 k	SMD 0805	
117	R43	1	1 k	SMD 0805	
118	R44	1	909 k 1%, 1206	SMD 1206	
119	R45	1	1 k	SMD 0805	
120	R46	1	10 k	SMD 0805	
121	R47	1	7.32 k 1%	SMD 0805	
122	R48	1	Nil	SMD 0805	
123	R49	1	10 k	SMD 0805	

Bill-of-material

Item	Circuit code	Qty	Description / value	Package	Manufacturer
124	R5	1	3.3 M 1%, 1206	SMD 1206	
125	R50	1	120 k	SMD 0805	
126	R51	1	10 R	SMD 0805	
127	R52	1	100	SMD 0805	
128	R53	1	3 k	SMD 0805	
129	R54	1	680 k, 1206	SMD 0805	
130	R55	1	680 k, 1206	SMD 1206	
131	R56	1	680 k, 1206	SMD 1206	
132	R58	1	18 k 1%, 1206	SMD 1206	
133	R59	1	18 k 1%, 1206	SMD 1206	
134	R6	1	120 R	SMD 0805	
135	R60	1	1 M, ¼ W axial	axial	
136	R61	1	1k	SMD 0805	
137	R62	1	1M, 1/4W axial	axial	
138	R63	1	2M 1%, 1206	SMD 1206	
139	R7	1	3.3 M 1%, 1206	SMD 1206	
140	R8	1	10 k	SMD 0805	
141	R9	1	10 R, 1206	SMD 1206	
142	RCS1	1	0.36 R 1% /2 W	axial	
143	RCS2	1	0.24 R 1% /2 W	axial	
144	RCS3	1	0.36 R 1% /2 W	axial	
145	RCS4	1	0.24 R 1% /2 W	axial	
146	NR1	1	10 R	SMD 0805	
147	NR2	1	10 R	SMD 0805	
148	NR3	1	10 R 1%	SMD 0805	
149	NR4	1	10 R 1%	SMD 0805	
150	NR5	1	10 R	SMD 0805	
151	RT1	1	NTC, 5 R/220 V/20%	radial	
152	RV1	1	MOV, 10D561K/560 V/10%	radial	
153	SW1	1	3pin SW, '09.03290.01	3pin	
154	T1	1	EFD38, Lp=1100 uH, Lr=240 uH, 51T:6T:3T:4T	EFD38	
155	U1	1	IDP2303	SO16	Infineon Technologies
156	U2	1	PC817C	DIP-4	
157	U3	1	AS431BZ	TO-92	
158	U5	1	PC817C	DIP-4	
159	ZD1	1	ZMM22 (22 V)	SMD	
160	ZD2	1	ZMM22 (22 V)	SMD	

Bill-of-material

Item	Circuit code	Qty	Description / value	Package	Manufacturer
161	ZD5	1	SZ25B275M (27 V)	SMD	
162	ZD6	1	ZMM22 (22 V)	SMD	
163	ZD7	1	SZ25B135M (13 V)	SMD	
163	FB2	1	Ferrite bead	add to lead of Y cap	
164	FB4	1	Ferrite bead	add to lead of Y cap	
165	FB5	1	Ferrite bead	add to lead of Y cap	
166	For JP2, JP15, JP17, +ve lead of CE3 and CE4, +ve lead of C19	1	Heat shrinkable tube		
167	For D3 and D9	1	Heat sink (refer to the real system with slope in one side)		
168	For D3 and D9	2	screw		
169	For D3 and D9	2	thermal grease to smooth the contact surface		

9 Transformer construction

9.1 PFC choke, LP1

Core: ER30, PC40 or equivalent
Primary inductance Lp: 200 uH, between pin 1 and pin 3 (Gapped)

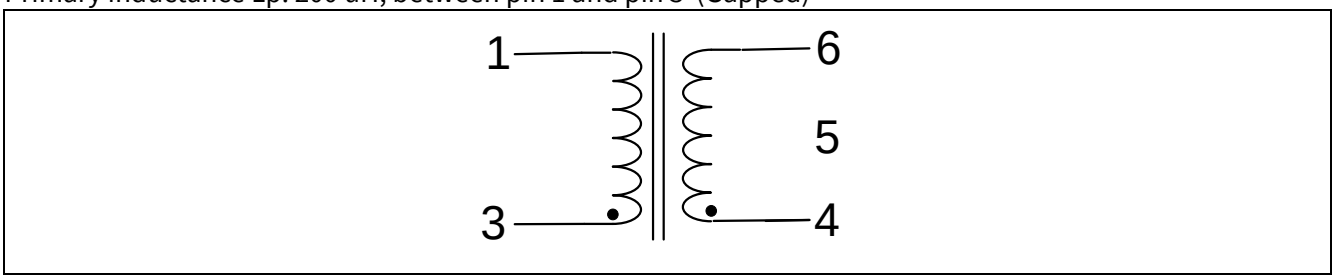


Figure 6 PFC choke electrical diagram

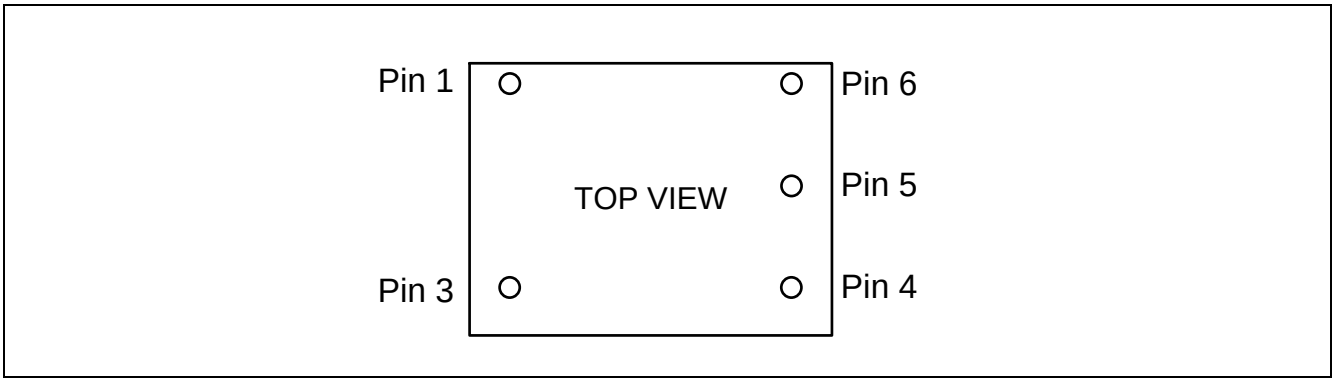


Figure 7 LLC resonant transformer complete – top view

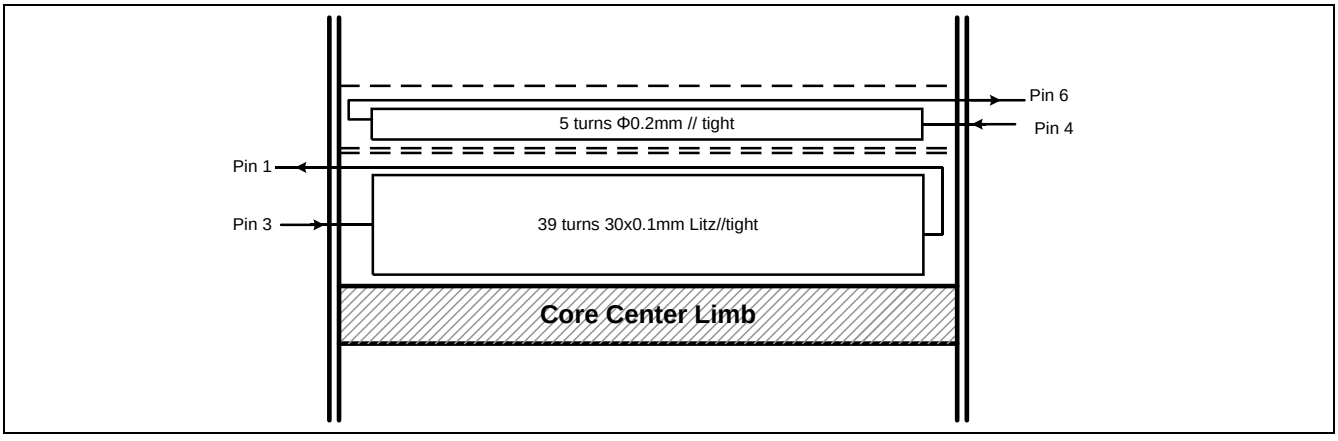


Figure 8 PFC choke winding position

Table 4 LLC resonant transformer winding characteristics

Windings	Start	End	Wire	Turns	Method
1	3	1	30 x 0.1 mm Litz	39	Tight
2	4	6	Φ0.2 mm	5	Tight

9.2 LLC transformer, T1

Core: EFD38, PC40 or equivalent
Primary inductance Lp: 1.1 mH±3%, between pin 1 and pin 2 (Gapped)
Leakage inductance: 260 uH with shorted all other pins

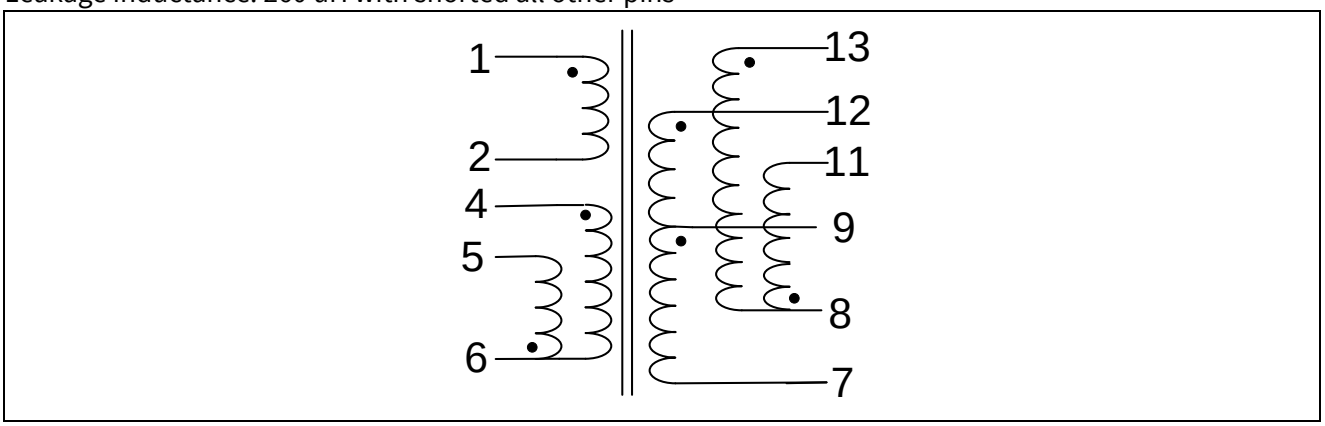


Figure 9 LLC resonant transformer electrical diagram

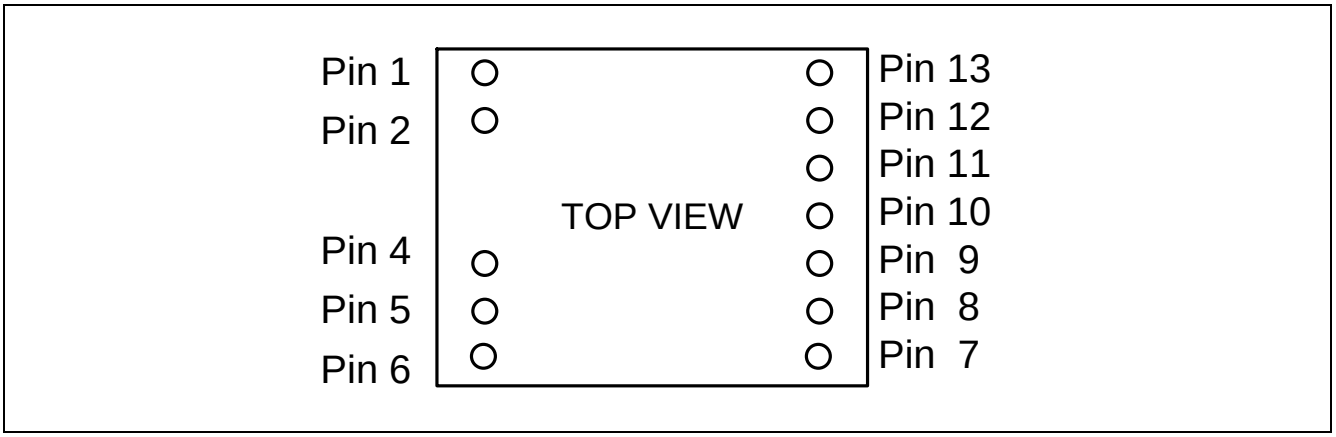


Figure 10 LLC resonant transformer complete – top view

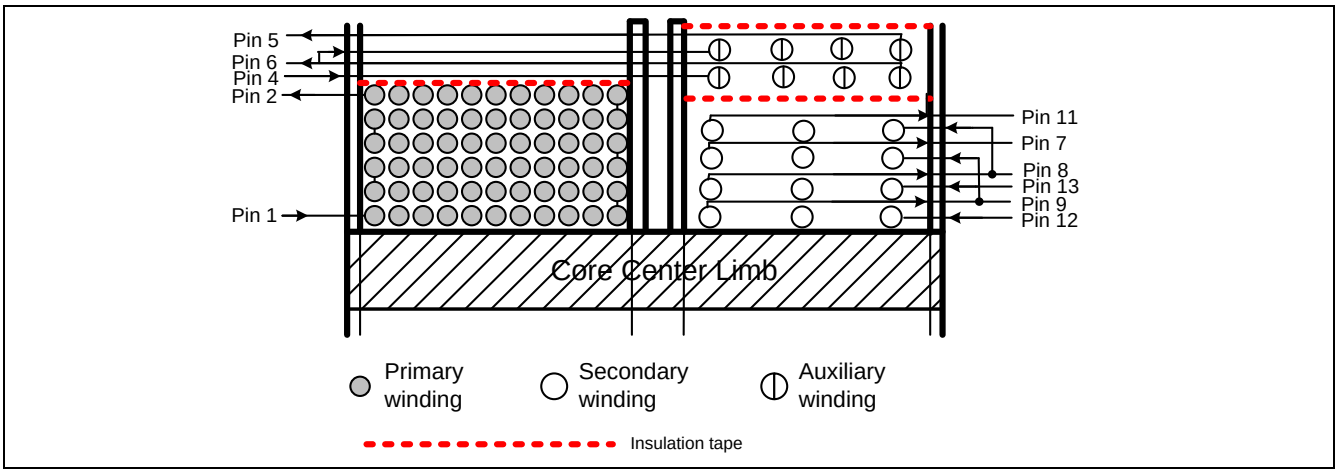


Figure 11 LLC resonant transformer winding position

Table 5 LLC resonant transformer winding characteristics

Transformer construction

Windings	Start	End	Wire	Turns	Method
1	1	2	20 x 0.1 mm Litz	51	Tight
2	12	9	60 x 0.1 mm Litz	3	Tight
3	13	8	60 x 0.1 mm Litz	3	Tight
4	9	7	60 x 0.1 mm Litz	3	Tight
5	8	11	60 x 0.1 mm Litz	3	Tight
6	4	6	Φ0.2 mm TIW	4	Tight
7	6	5	Φ0.2 mm TIW	4	Tight

9.3 Common mode choke, LX1 and LX2

Core: T18 x x10 x 6 , holder : 21 x 21, wire dia : 0.43 mm
Inductance: 18 mH min.

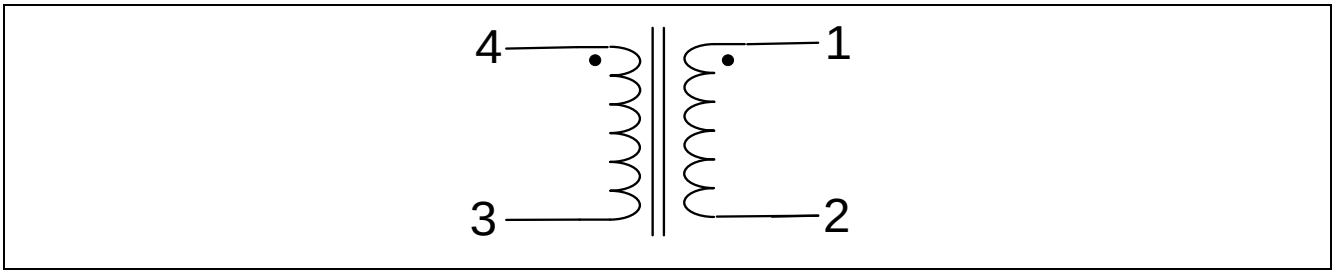


Figure 12 Common mode choke electrical diagram

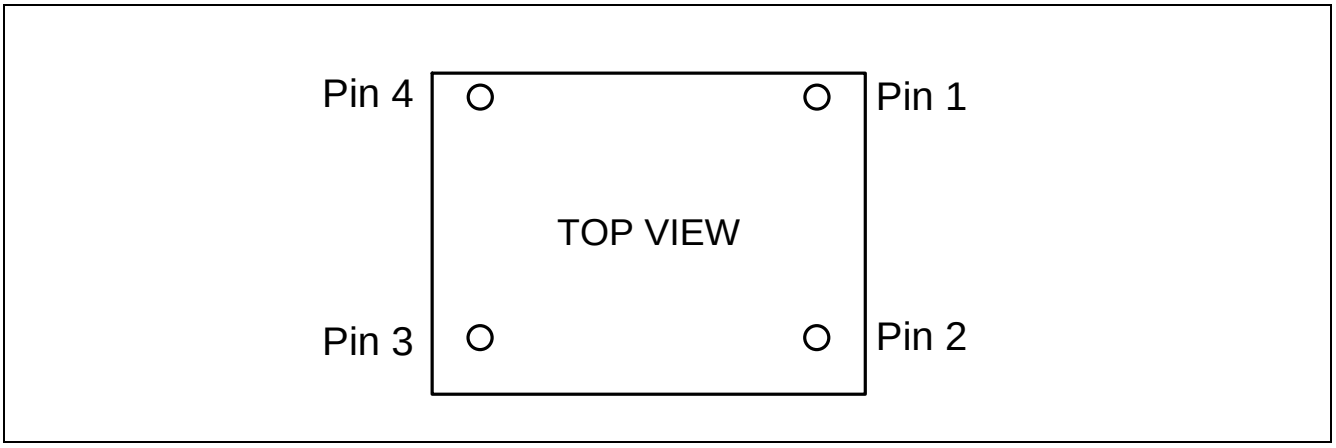


Figure 13 Common mode choke complete – top view

10 Test results

10.1 Efficiency

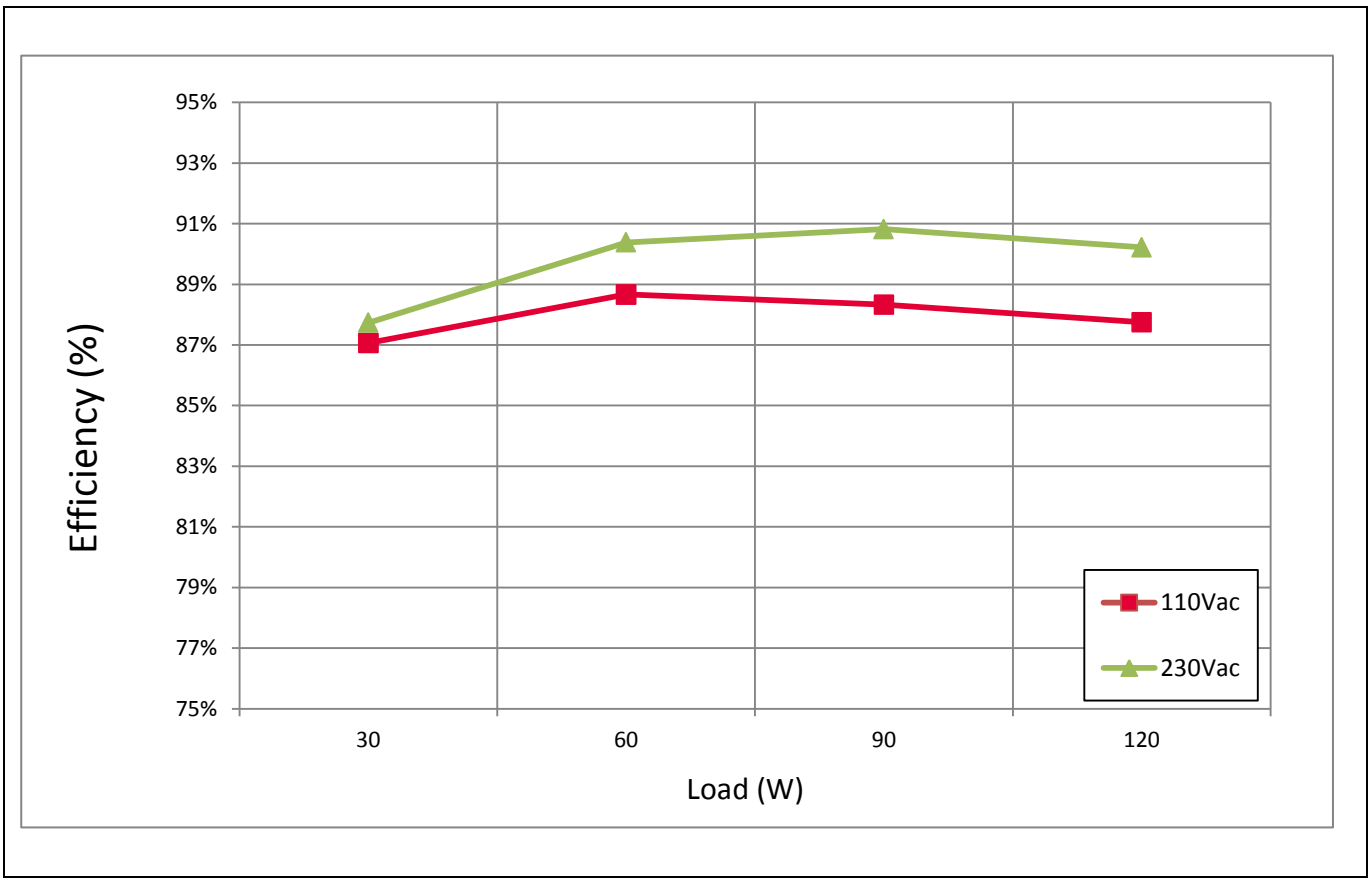


Figure 14 Efficiency measurments

The overall effiency curve is higher than 87% for both high and low line over the load range from 25% to 100%. The full load efficiency at 230 V_{AC} reaches 90.2%.

10.2 Standby power

The standby power consumption is less than 270 mW at 230 V_{AC} with 125 mW load.

Standby power consumption

Loading	Input voltage	Input power (mW)
+24 V / 0 A, +9 V/14 mA	110 V_{AC}	241.9
+24 V / 0 A, +9 V/14 mA	230 V_{AC}	261.3

10.3 Surge immunity (EN61000-4-5)

The surge immunity test was measured with a Noiseken LSS-15AX lightning surge simulator. The output common was connected to the primary side PE.
Pass 4.5 kV common mode test (line to earth) and
Pass 2 kV differential mode test (line to line).

10.4 Conducted emissions (EN55022 class B)

The conducted EMI was measured by a Schaffner SMR25503 in accordance with EN55022 (CISPR 22) class B. The demoboard was set up at maximum load (120 W) with an input voltage of 115 V_{AC} and 230 V_{AC}. To further improve conducted EMI performance at high frequency, two ferrite beads are added to the output rectifier diodes, which are not shown in the BOM. The system passes CISPR22 class B with over 6 dB margin.

Note: The system has a metal chasis during the measurement.

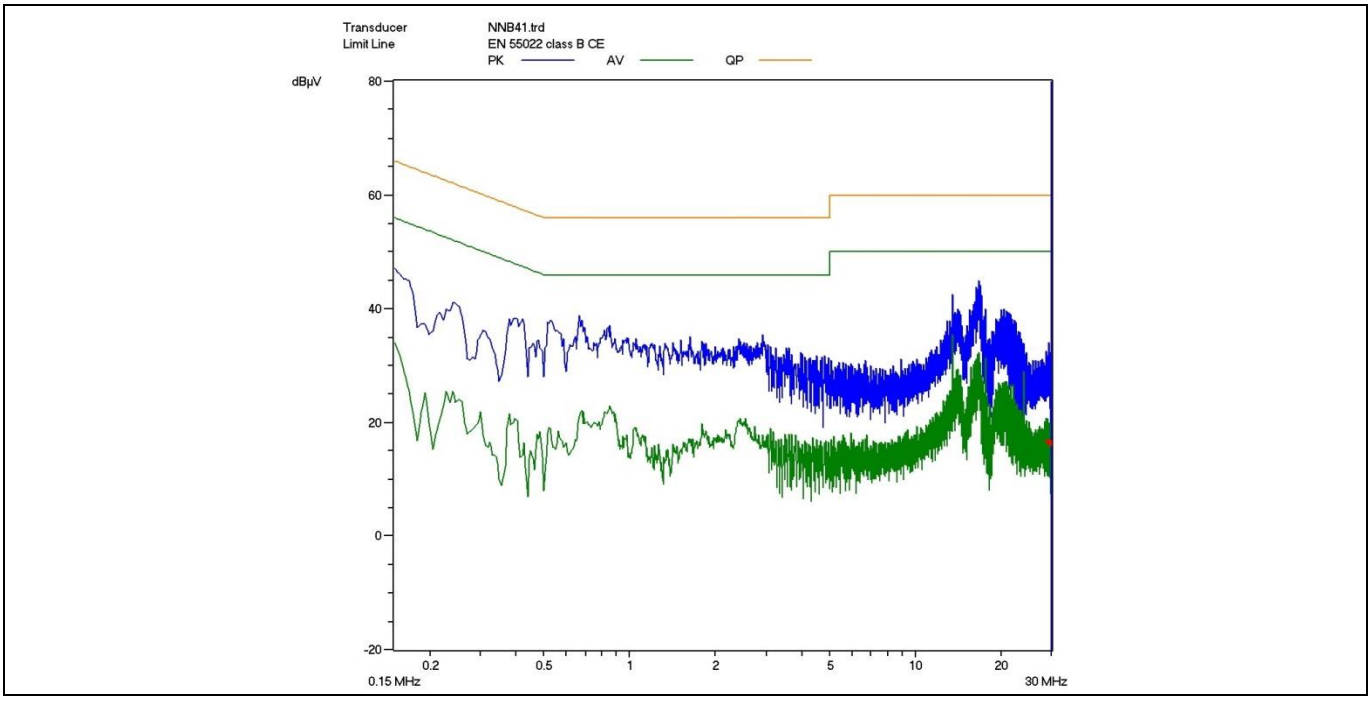


Figure 15 Conducted emissions(line) at 115 V_{AC} and maximum load

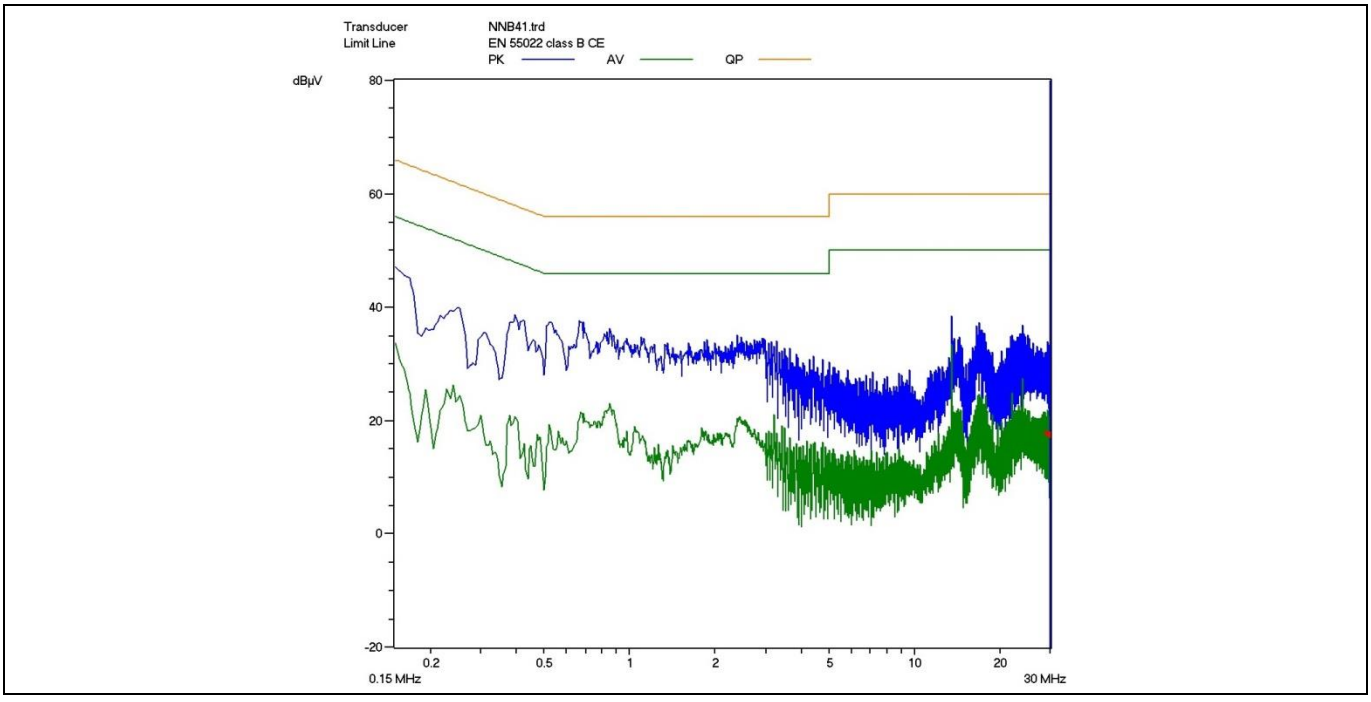


Figure 16 Conducted emissions(neutral) at 115 V_{AC} and maximum load

Test results

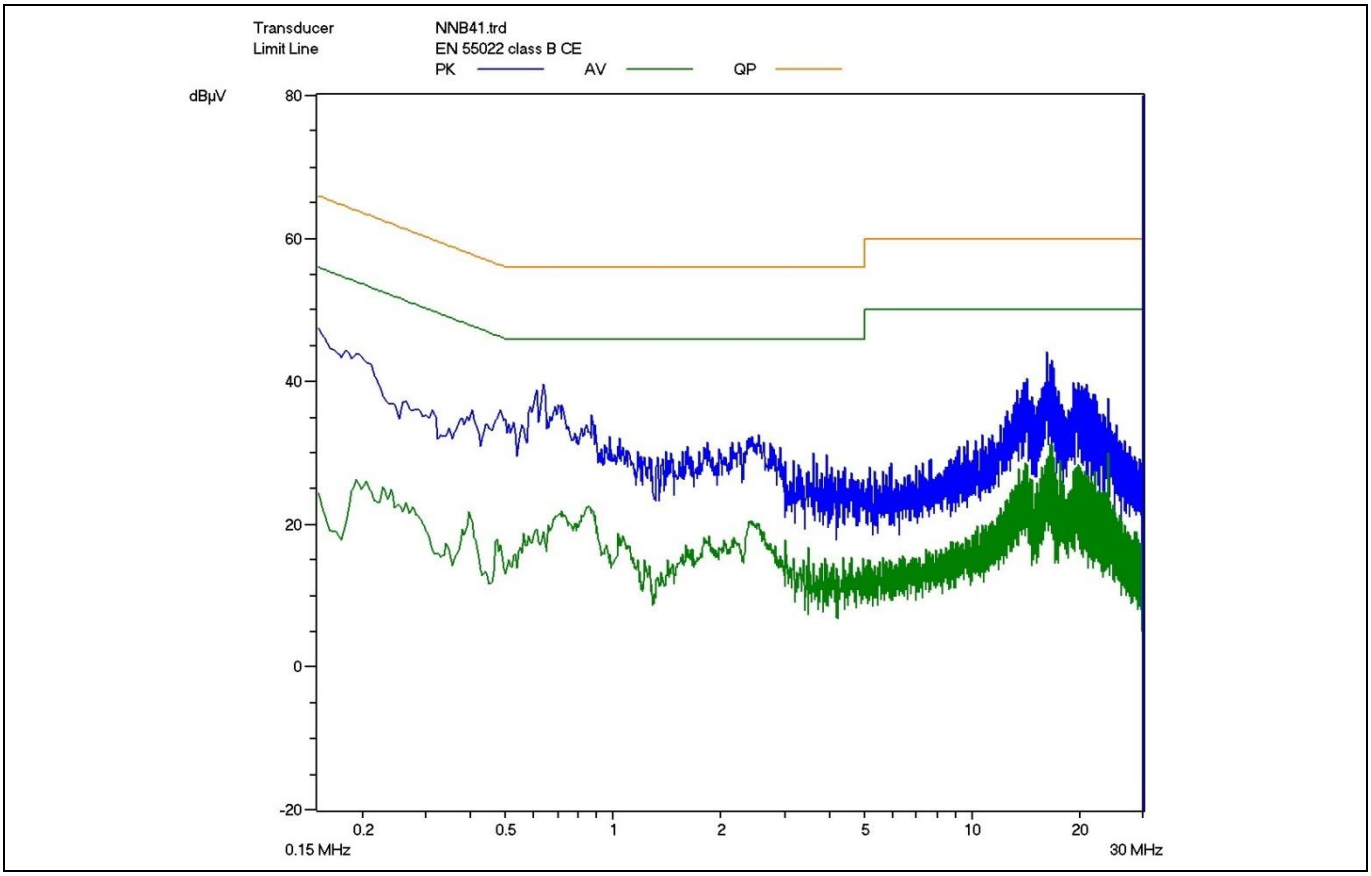


Figure 17 Conducted emissions(line) at 230 V_{AC} and maximum load

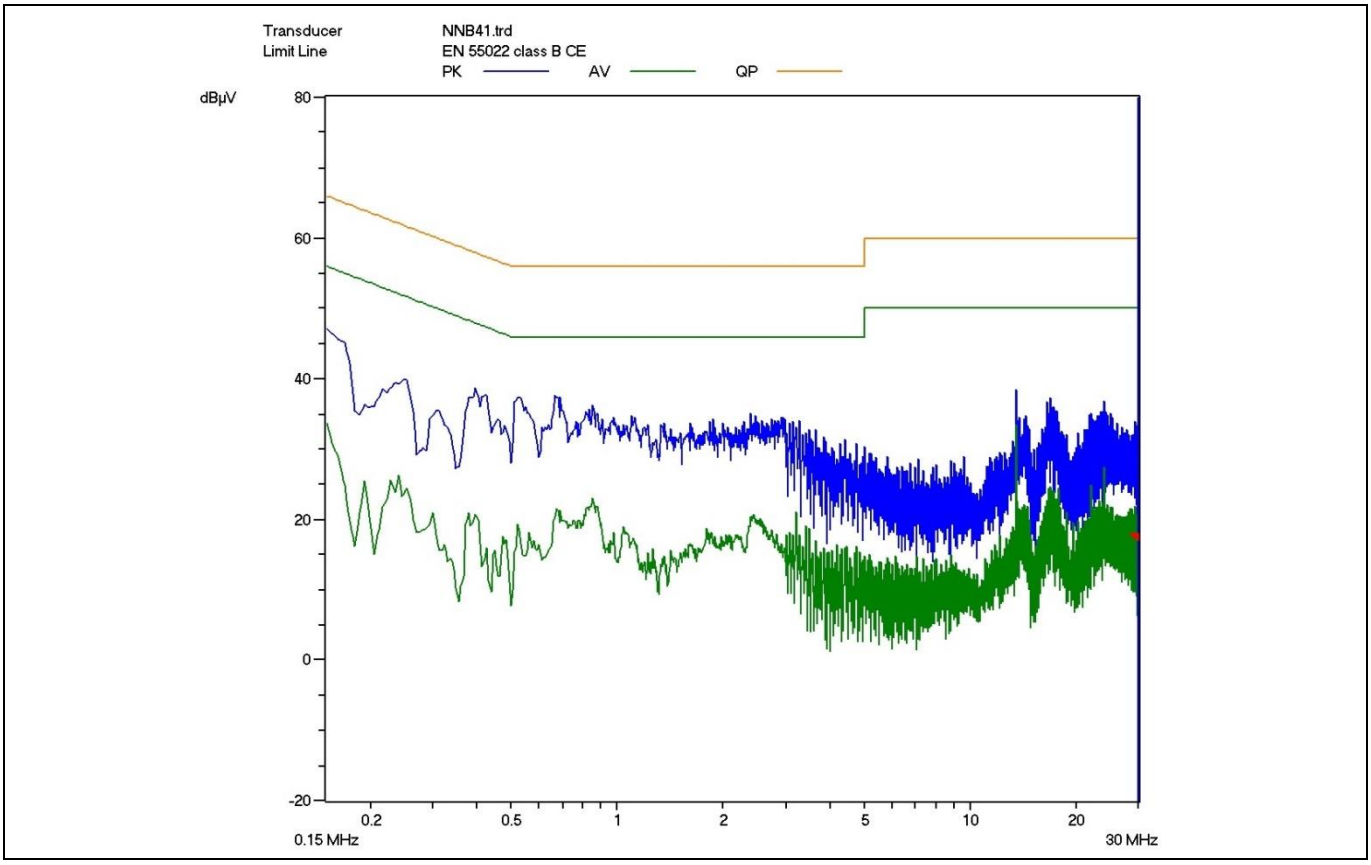


Figure 18 Conducted emissions(neutral) at 230 V_{AC} and maximum load

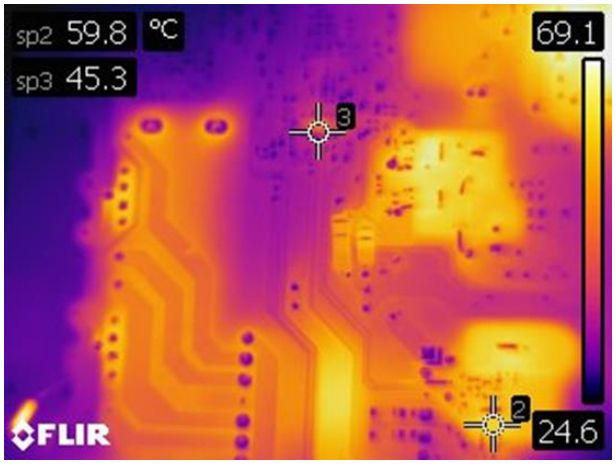
10.5 Thermal measurement

The thermal test of the open frame demoboard was performed using an infrared thermography camera (TVS-500EX) at an ambient temperature of 25°C. The measurements were taken after two hours running at full load.

Table 6 Hottest temperature of demo board

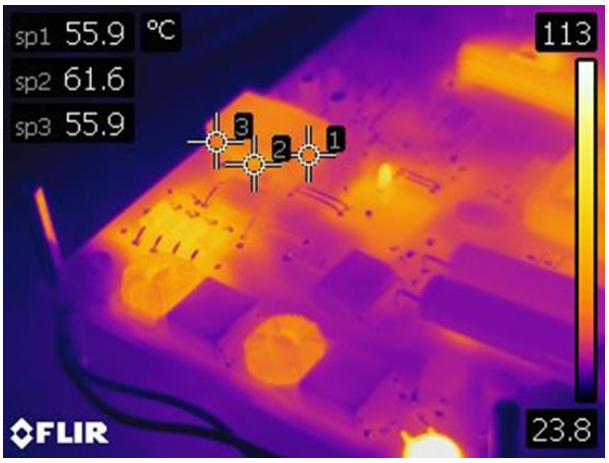
No.	Major component	Temperature (°C) @90 V_{AC}
1	LLC transformer	61.1
2	PFC inductor	58.1
3	12 V output diode	65.2
4	24 V output diode	68.2
6	IDP2303	45.3
7	PFC MOSFET	60.5
8	PFC MOSFET	63.6
9	LLC high-side MOSFET	59.8
10	LLC low-side MOSFET	58.2
11	Ambient	25

MOSFETs



IDP2303

LLC transformer

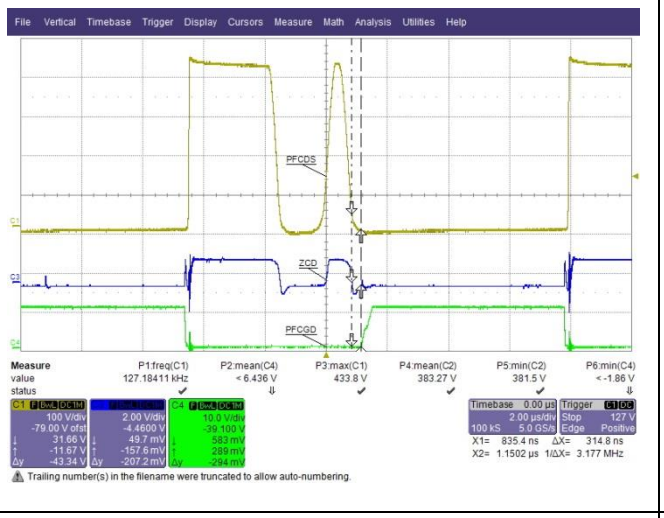


PFC choke

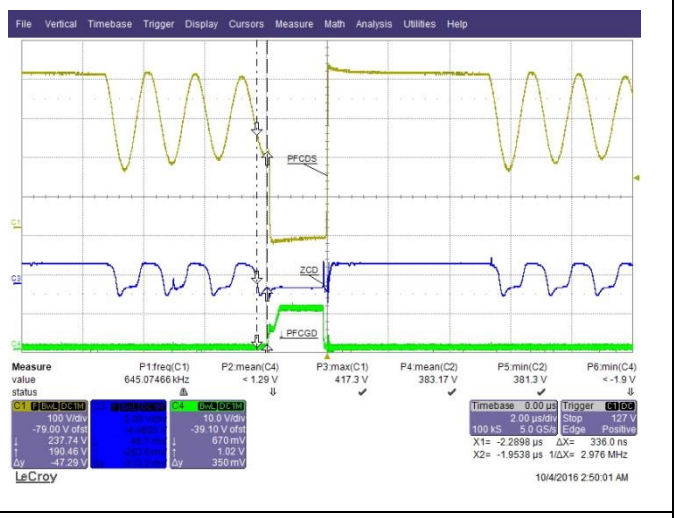
Figure 19 Infrared thermal image of DEMO-IDP2303-120W

10.6 PFC with valley switching

The IDP2303 features a multi-mode PFC, which has a default frequency range from 60 kHz to 120 kHz. The PFC MOSFET is determined to turn on by the PFC ZCD signal, when the PFC ZCD signal falls below 40mV and after a certain blanking time, the PFC MOSFET turns on to charge up the PFC choke again. Due to this simple mechanism, PFC MOSFET valley switching is achieved, as shown in Figure 20, hence the PFC turns on loss can be significantly reduced. Moreover, with multi-mode operation, the PFC switching frequency is limited to the design range, which breaks down the switching loss under high line and light load.



PFC Valley switching @ 110 V_{AC} and full load

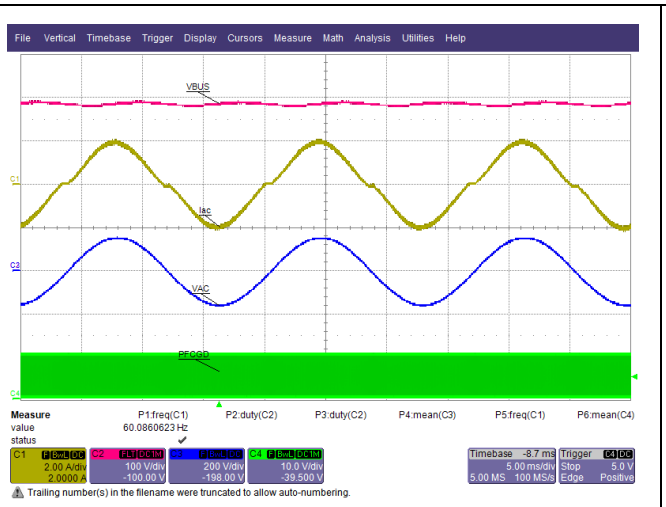


PFC Valley switching @ 230 V_{AC} and full load

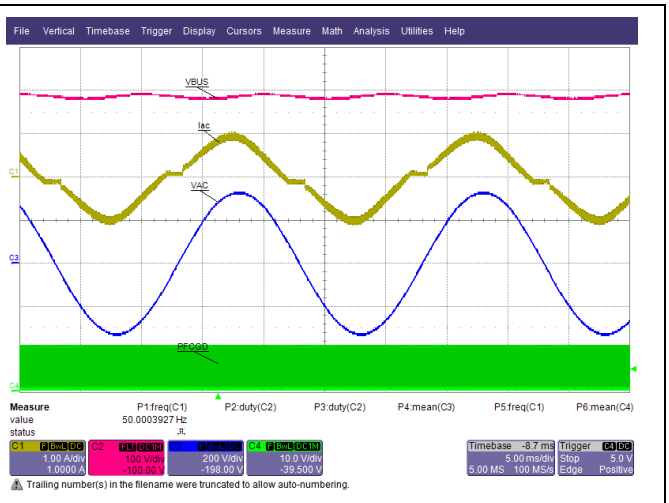
Figure 20 Multi-mode PFC with valley switching

10.7 Multi-mode PFC with unity power factor

As described in the IDP2303 datasheet, constant on time control is applied to achieve unity power factor. In Figure 21, the AC input current is sinusoidal and synchronous with the AC input voltage. Hence, unity power factor has been achieved.



AC input current @ 110 V_{AC} and full load

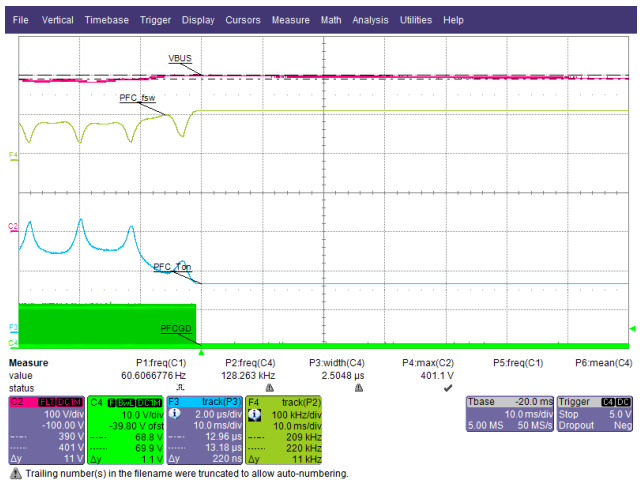


AC input current @ 230 V_{AC} and full load

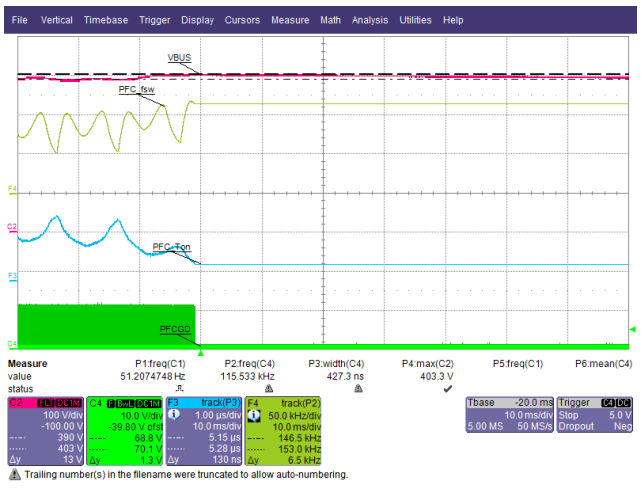
Figure 21 PFC AC input current

10.8 PFC dynamic response

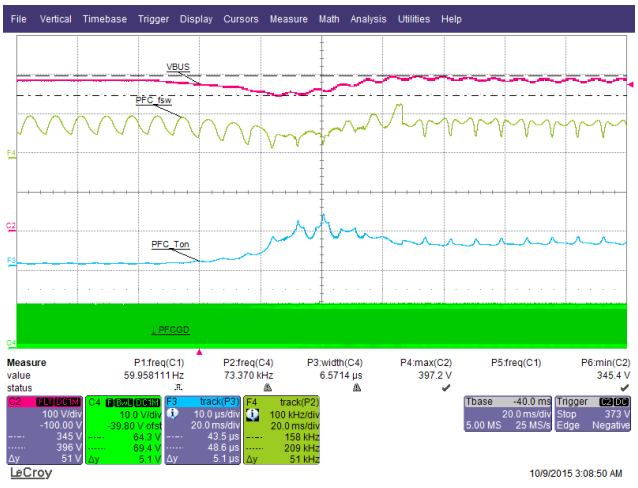
As described in the IDP2303 datasheet, the PFC regulator is built-in to modulate the PFC MOSFET on time to regulate the PFC bus voltage under control. In Figure 22, even in the case of an extremely dynamic load change between minimum and full load, the PFC bus voltage only varies within the acceptable range. Accordingly the following LLC stage will vary its switching frequency to maintain the LLC output under regulation.



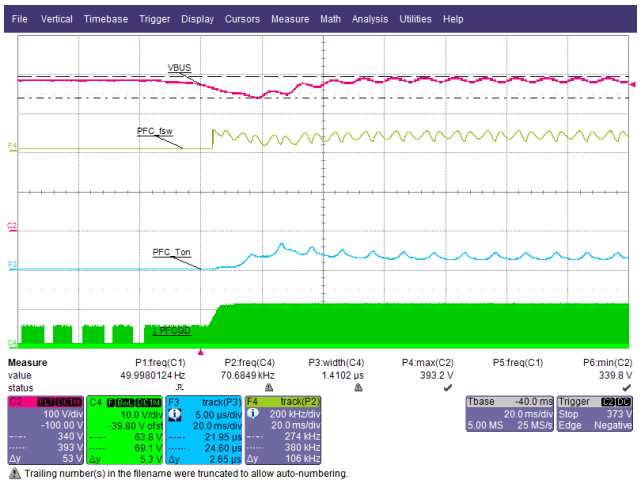
PFC Bus ripple @ full load to min load and 110 V_{AC}



PFC Bus ripple @ full load to min load and 230 V_{AC}



PFC Bus ripple @ min load to full load and 110 V_{AC}

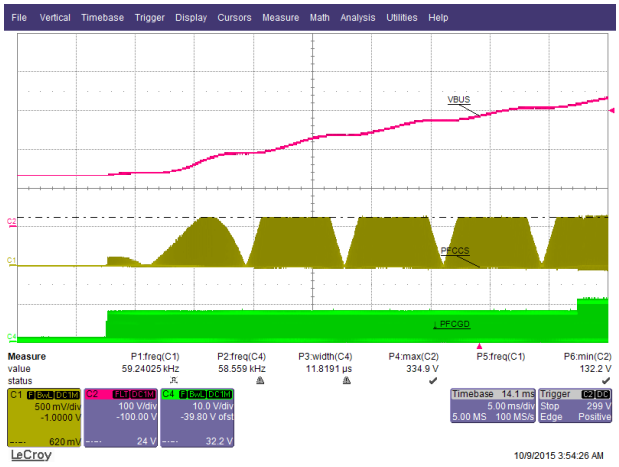


PFC Bus ripple @ min load to full load and 230 V_{AC}

Figure 22 PFC Bus voltage ripple when load changes

10.9 PFC over current protection

In order to limit the current flowing through the PFC choke, PFC over current protection is built-in to the IDP2303. In Figure 23, the voltage across RCS2 and RCS4 is used to sense the PFC current. When the CS0 voltage exceeds 0.6 V (typ.), and after a propagation delay, the PFC MOSFET will be turned off to stop the current increasing.

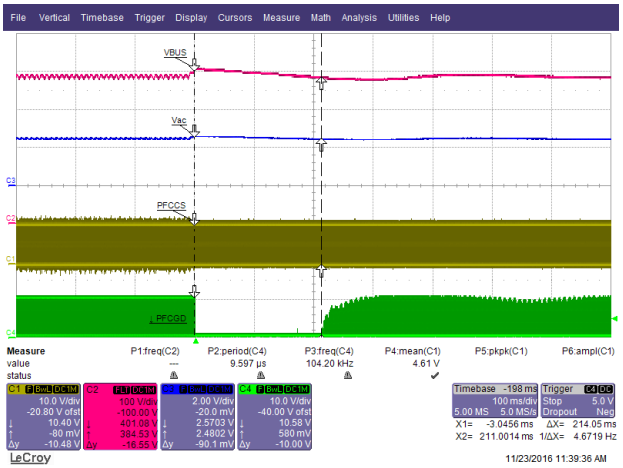


PFC over current protection

Figure 23 PFC over current protection @ 90 V_{AC} and full load

10.10 PFC over voltage protection

As described in the IDP2303 datasheet, the PFC features over voltage protection (OVP1 and OVP2) to strictly limit the bus voltage overshoot. In the case of an extreme load or line jump, the PFC output may suffer significant overshoot. In Figure 24, under a load jump from full to min load, the PFC OVP1 is triggered and PFC switching is stopped immediately. The measured OVP1 threshold is 2.57 V in the waveform, which is the same as the value set by the firmware in the controller IC. The LLC continues switching, and once the PFC bus voltage drops to below its regulation target, the PFC resumes switching with a soft-start. For PFC OVP2, the threshold is fixed by hardware comparator at 2.8 V, which will respond immediately once the threshold is triggered. The response and delay time of OVP2 will be much shorter than OVP1 as it is designed to prevent serious failures.

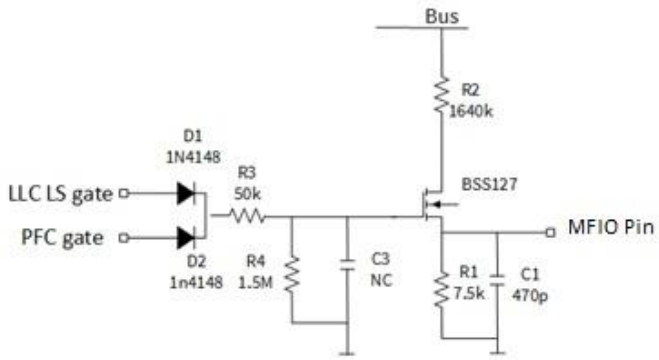


Load jump from full load to min load @110 V_{AC}

Figure 24 PFC over voltage protection

10.11 PFC redundant OVP protection

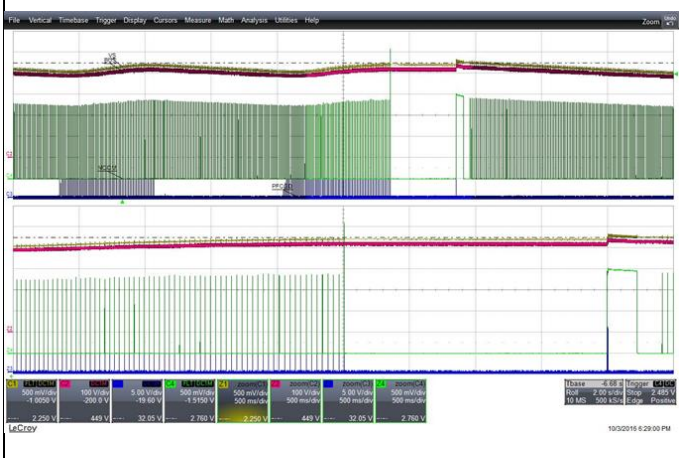
To further improve the reliability of the system, the IDP2303 provides an independent bus overvoltage protection via the MFIO pin to prevent a serious PFC output failure resulting from damage to the voltage divider on the VS pin. The MFIO pin is a multi-function pin, which can be used to sense the redundant PFC OVP and to provide a UART communication IO interface for parameter configuration.
However, the requirements on standby power consumption are becoming tighter. Thus, in order to reduce the power consumed by the voltage divider on the MFIO pin, a lossless sensing circuit with a BSS127 is recommended as shown in Figure 25.



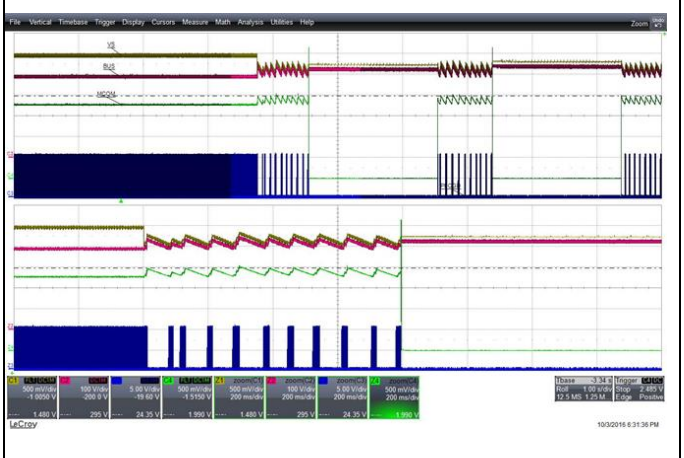
Lossless sensing circuit for PFC ROVP

Figure 25 PFC over voltage protection

As shown in Figure 26, in order to clearly demonstrate the PFC redundant OVP (ROVP) feature, a resistor is deliberately placed in parallel with the VS divider low-side resistor R13 to create the fault condition. Thus, the bus voltage increases immediately since the PFC is working in a closed loop and trying to regulate the VS voltage to 2.45 V. When voltage on the MFIO pin hits the threshold $V_{_ROVP_set}$, the PFC stops switching but LLC continues. After the bus voltage drops and the MFIO pin voltage reaches its reset threshold $V_{_ROVP_reset}$, the PFC resumes switching with a soft-start. If the fault condition is not removed, after ten continuous triggers of an ROVP event, the system will enter auto-restart mode. For more details, please refer to the IDP2303 datasheet.



PFC ROVP @ 230 V_{AC} and standby load

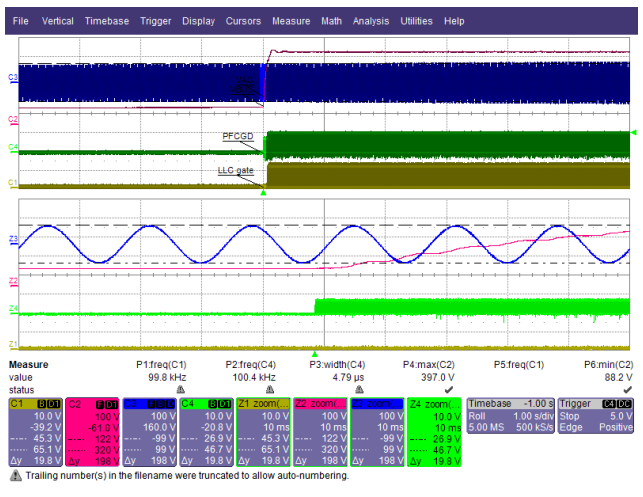


PFC ROVP @ 230 V_{AC} and full load

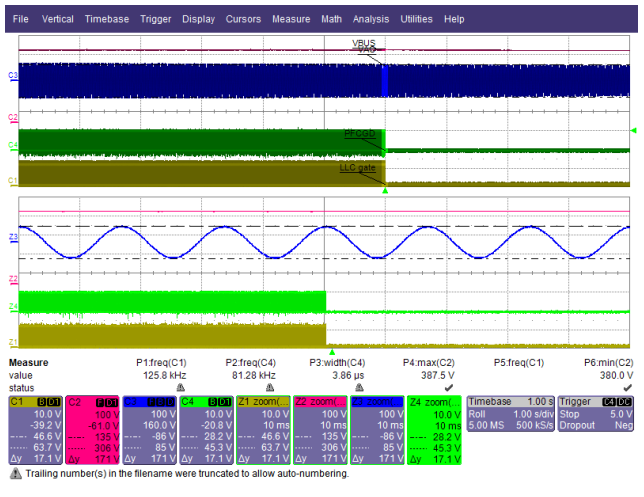
Figure 26 PFC redundant OVP protection

10.12 PFC brown-in/brown-out protection

To prevent the system working under extremely low AC input voltages, brown-in/brown-out protection is designed with configurable thresholds via the HV pin. It is implemented with a 51 kΩ HV resistor connected to the AC input, where the default thresholds are: brown-in 70 V_{AC} (RMS) and brown-out 60 V_{AC} (RMS). In Figure 27, with AC slew rate of 1 V/s, the brown-in/brown-out protection is demonstrated. The measured brown-in threshold is 99 V peak (around 70 V_{AC} RMS), and the brown-out threshold is 85 V peak (around 60 V_{AC} RMS).



Brown-in @ 20% full load



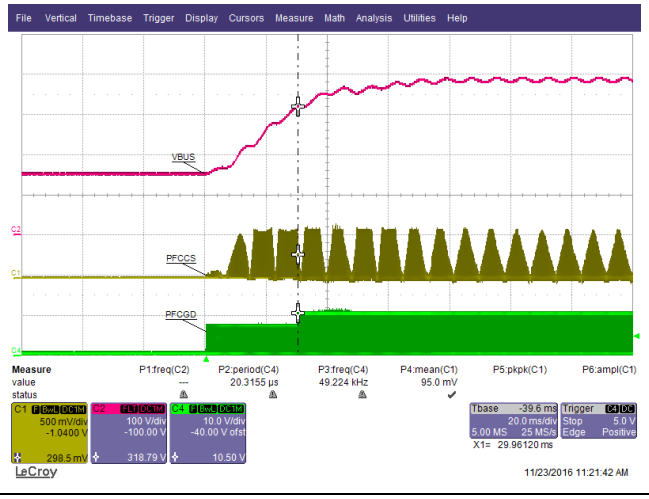
Brown-in @ 20% full load

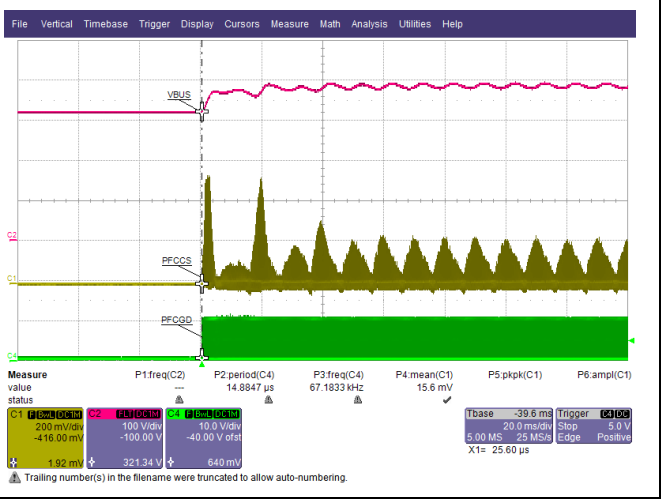
Figure 27 Brown-in/brown-out protection

10.13 PFC/LLC start-up behavior

As described in the IDP2303 datasheet, both PFC and LLC soft-start features are implemented. In Figure 28 and Figure 29, the PFC bus voltage smoothly increases until reaching the target regulation value. To shorten the start-up time, the default svp (PFC PIT1 P coefficient) is set to 4 during the start-up phase. While under normal operation, svp is set to 6 to achieve more stable operation. Moreover, during the PFC start-up phase, its gate driver voltage is set to 7.5 V, when bus voltage reaches the LLC start-up threshold, the PFC gate driver voltage is reset to 10.5 V.

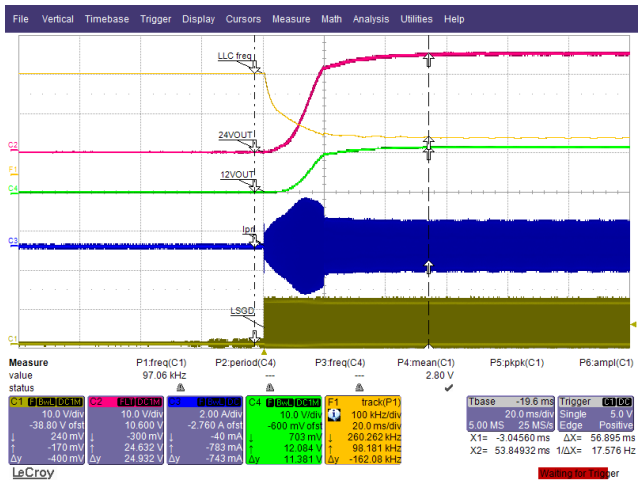
Accordingly, when the VS voltage reaches 2.05 V, the LLC starts switching with configurable soft-start behaviour. Its default maximum soft-start frequency is 270 kHz, and the LLC switching frequency smoothly sweeps from a high level to a low level and finally enters normal operation. For more details, please refer to the IDP2303 datasheet.

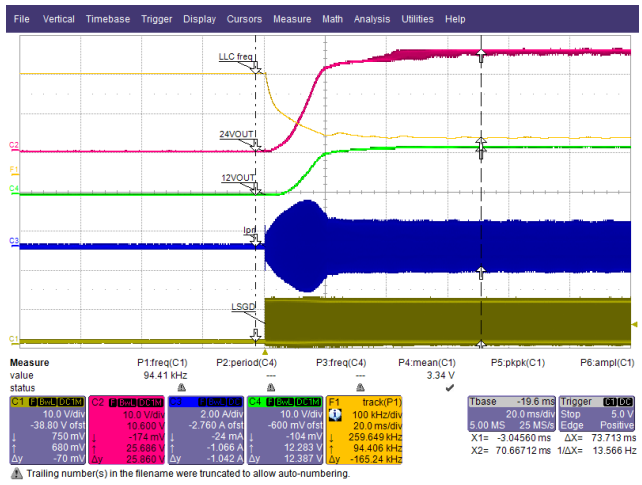




PFC start-up @ 110 V_{AC} and full load	PFC start-up @ 230 V_{AC} and full load

Figure 28 PFC startup behavior



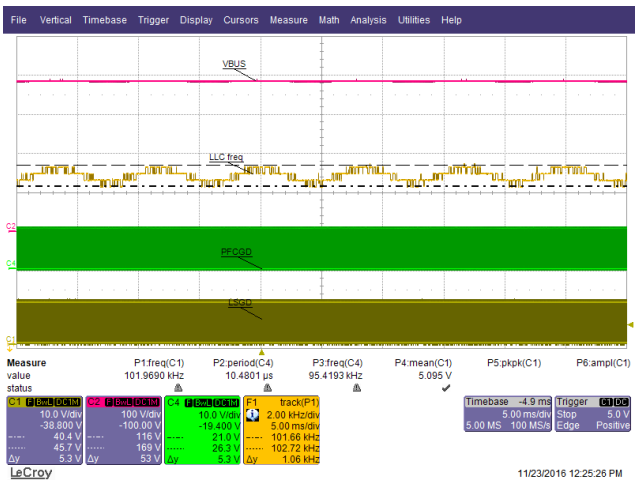


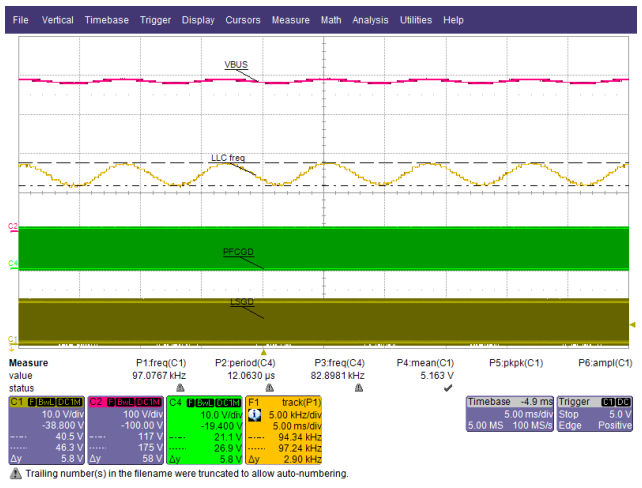
LLC start-up @ 110 V_{AC} and full load	LLC start-up @ 230 V_{AC} and full load

Figure 29 LLC startup behaviour

10.14 LLC line regulation

The LLC switching frequency will vary with reference to the PFC bus voltage ripple to regulate the LLC output. For example, at 110 V_{AC} and 20% of full load, the LLC switching frequency (f_{sw}) varies by 1.4 kHz from 106.7 kHz to 108.1 kHz to regulate its output. At 110 V_{AC} and 100% full load, the LLC f_{sw} varies by 2.6 kHz to regulate the output.





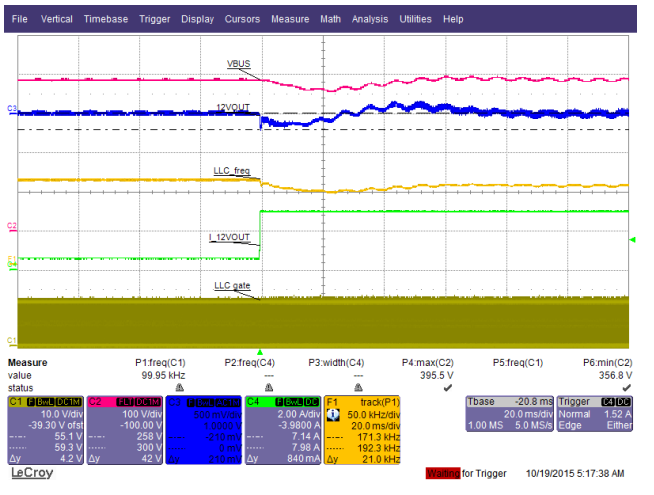
LLC f_{sw} @ 110 V_{AC} and 20% full load	LLC f_{sw} @ 110 V_{AC} and 100% full load

Figure 30 LLC switching frequency varies against the PFC bus voltage

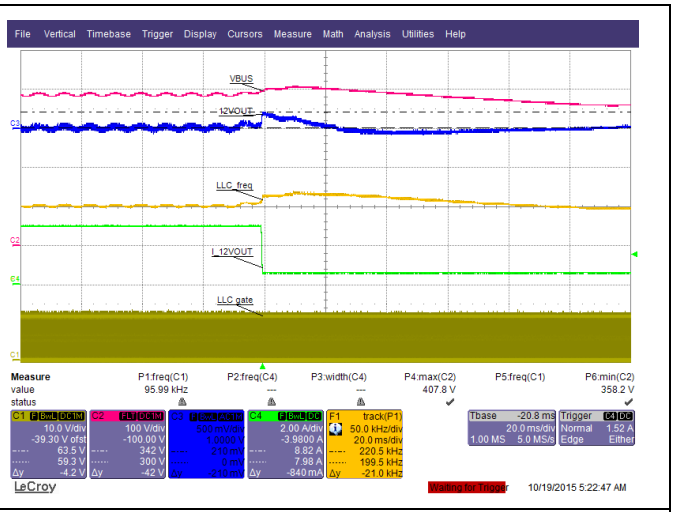
10.15 LLC load regulation

Figure 31 shows the dynamic behavior of the LLC stage during a load variation between 20% and 100% of full load. It can be seen that the LLC switching frequency varies against the load changes, and the measured output voltage ripple at 12 V is around 210 mV.

Test results



LLC fsw @ 110 V_{AC} and 20% ~ 100% full load

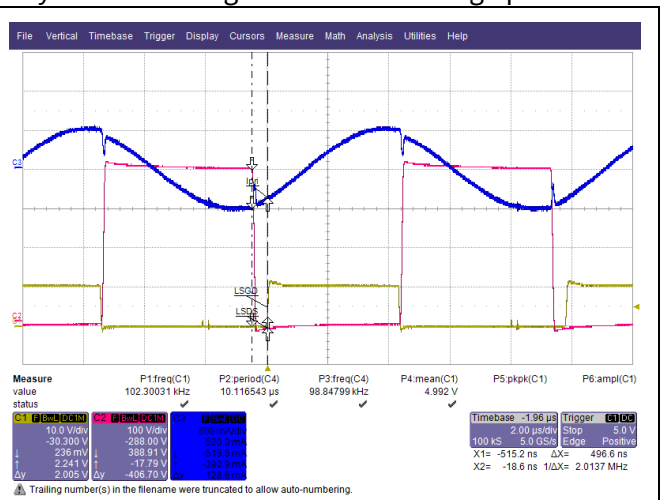


LLC fsw @ 110 V_{AC} and 20% ~ 100% full load

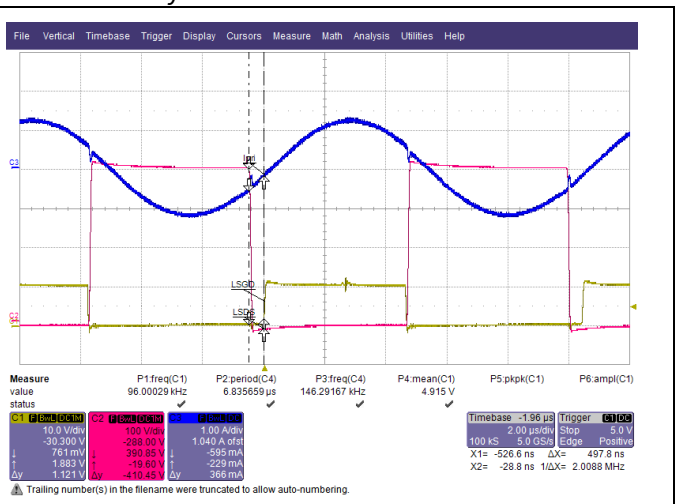
Figure 31 LLC switching frequency varies against the load changes

10.16 LLC zero voltage switching

From the test results of Figure 32, it can be seen that the LLC zero voltage switching (ZVS) can be achieved over a very wide load range which ensures high power conversion efficiency.



LLC ZVS @ 110 V_{AC} and 20% full load



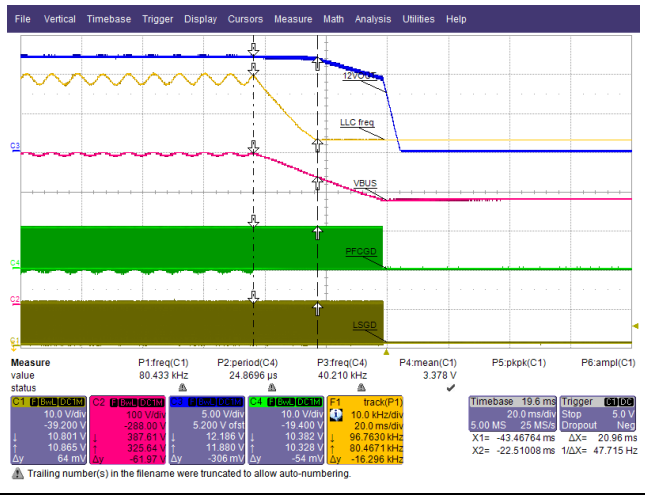
LLC ZVS @ 110 V_{AC} and 100% full load

Figure 32 LLC zero voltage switching

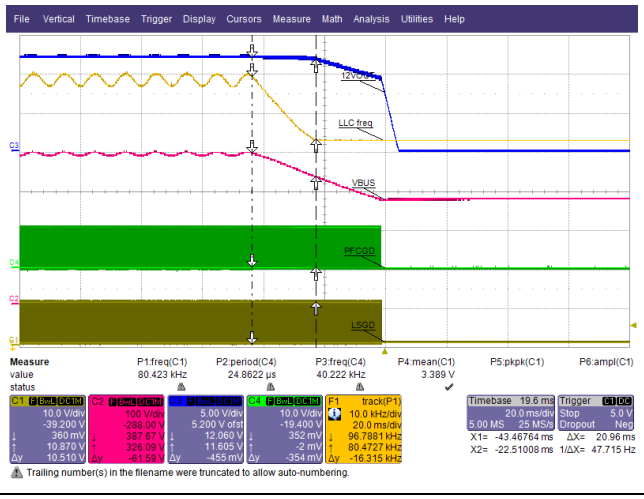
10.17 PFC and LLC operation during holdup time

In order to meet the holdup time requirement, the LLC stage is required to cover a wide PFC bus voltage range. During the holdup time, the LLC switching frequency drops to regulate the output voltage against the bus voltage drop. As shown in Figure 33, after shutting down the AC input, the LLC keeps switching until the PFC bus voltage drops the undervoltage protection threshold. The measured holdup time is around 24 ms, which meets most of the power supply specification.

When the undervoltage threshold is triggered, the PFC and LLC both stop switching and the IC keeps active until Vcc reaches its UVLO threshold.



PFC/LLC operation @ 110 V_{AC} off, full load



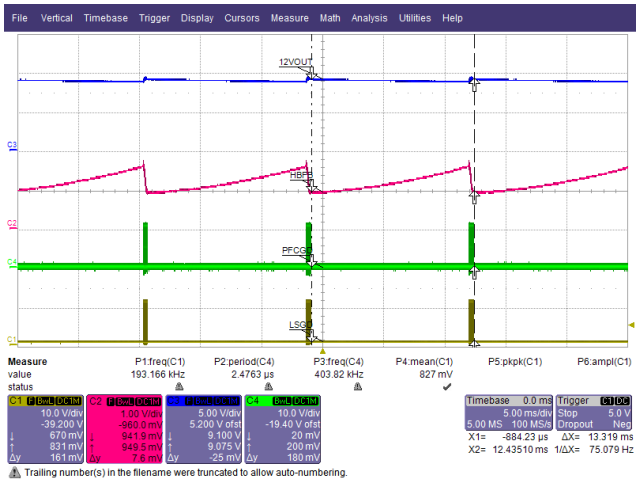
PFC/LLC operation @ 230 V_{AC} off, full load

Figure 33 PFC and LLC operation after shutdown AC input with full load

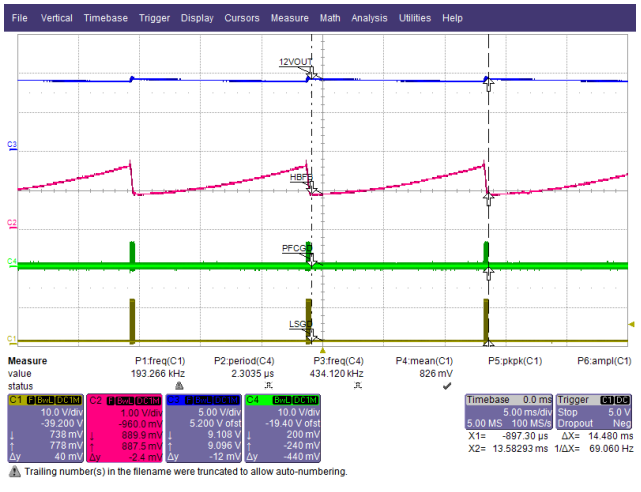
10.18 Burst mode operation

Burst mode operation is implemented in the IDP2303 to achieve low power consumption during standby operation. For this advanced burst mode control, the PFC and LLC are synchronized. However, during the burst on period if the bus voltage is higher than its target, then the PFC will not switch. To achieve ultra-low standby power consumption, the default target bus voltage during burst mode is around 350 V (the VS reference is set at 2.2 V).

In Figure 34, during burst mode operation, when V_{HBFB} drops to the burst off threshold $V_{_burst_off}$, which is 0.3 V, the switching signals will be disabled and the IC will enter sleep mode after a certain blanking time. V_{HBFB} will then increase as Vout starts to decrease due to the absence of an LLC switching signal. Once V_{HBFB} reaches the burst on threshold $V_{_burst_on}$, which is 1.65 V, the IC wakes up and resumes switching. The default LLC switching frequency under burst mode is set to 110 kHz, which is configurable and should be based on the LLC resonant tank design. For a detailed description of burst mode operation, please refer to the IDP2303 datasheet.



LLC burst mode operation @ 110 V_{AC}, standby load

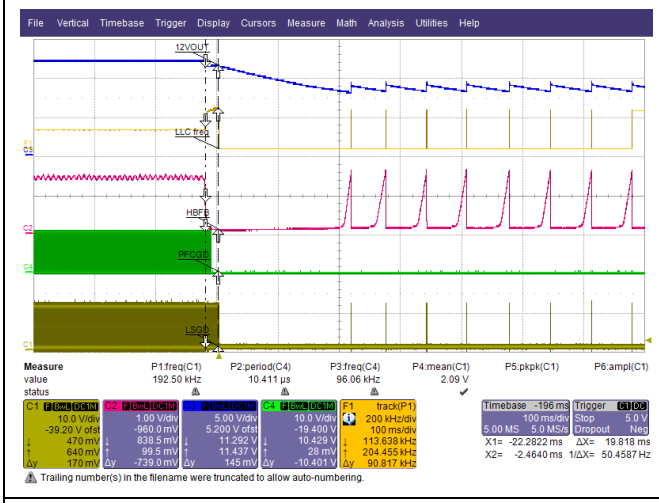


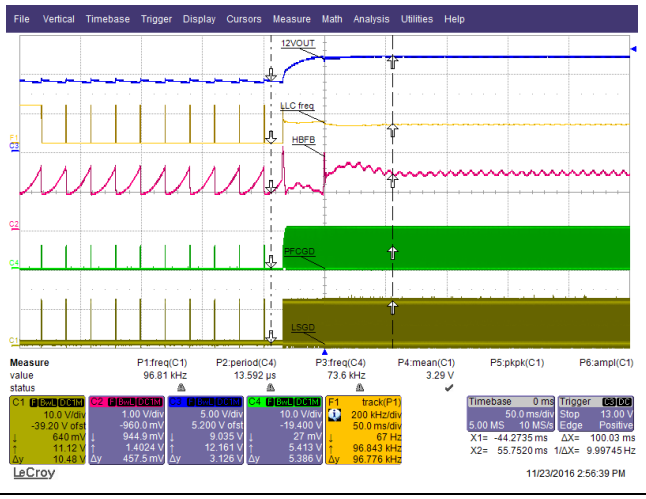
LLC burst mode operation @ 230 V_{AC}, standby load

Figure 34 Burst mode operation at standby load

As shown in Figure 35, the LLC enters burst mode when the load jumps from full load to standby load. At the same time the Power_On signal is switched off (switch SW1 pin 1 disconnects from pin 3), The system leaves

burst mode when full load returns. At the same time the Power_On signal is switched on (switch SW1 pin 1 connects to pin 3). There is a 10ms blanking time before the system enters burst mode as shown in the left side waveform. In the right side waveform, the system is leaving burst mode. It can be seen that another quick soft-start is implemented for the LLC when the system is leaving burst mode. Thus, the LLC output may drop slightly during the load jump from standby load to full load.





LLC Jumps from full load to standby load @ 110 V_{AC}	LLC Jumps from standby load to full load @ 110 V_{AC}

Figure 35 LLC entering/leaving burst mode operation

10.19 LLC over current protection

The IDP2303 features two different over current protections: a first level overcurrent protection with the threshold $V_{_OCP1}$ (there are 3 different $V_{_OCP1}$ thresholds during soft-start, normal operation and burst mode, please refer to the datasheet) by software and a second level over current protection with the threshold V_{OCP2} by hardware, where the threshold $V_{_OCP1}$ is lower than the threshold V_{OCP2}. Overcurrent protection triggered by these two thresholds has different reactions in the HB LLC converter.

During LLC operation, the voltage across the shunt resistors RCS1 and RCS3 is compared with the threshold $V_{_OCP1}$. Once the voltage is higher than the threshold, the LLC frequency will be increased to 200 kHz immediately, which is configurable and should be based on the LLC resonant tank design, followed by a soft-start. If during the soft-start, the over current situation is removed, the LLC will change from TCO to VCO and enters normal operation. But, if the overcurrent condition remains, after eight continuous OCP1 event triggers, the PFC and LLC will be stopped and enter auto-restart.

The second level over current protection is designed to prevent an extremely large current flowing through the shunt resistor. Once the LLC OCP2 is triggered, the PFC and LLC will immediately stop switching and enter auto-restart by default, which can be configured as a latch based on system requirements.

In Figure 36, during normal operation, the first level OCP is triggered when the 24 V output is shorted to ground. Accordingly, the LLC switching frequency jumps to 200 kHz to limit the primary current. After eight continuous OCP1 triggers, the system enters auto-restart mode with two seconds break time. Once the overcurrent condition is removed, the system will recover with a soft-start.

Test results

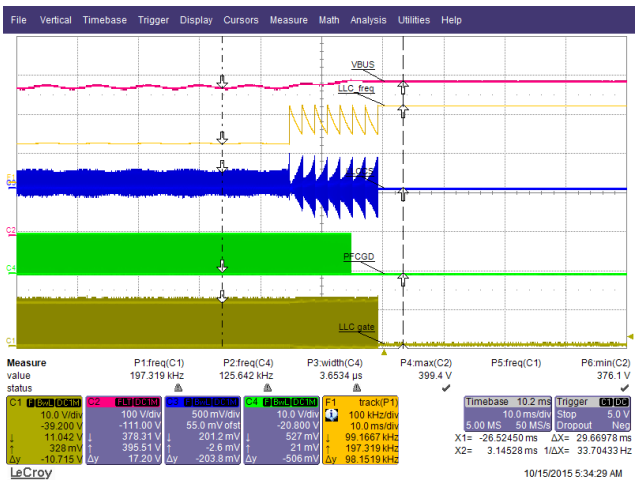
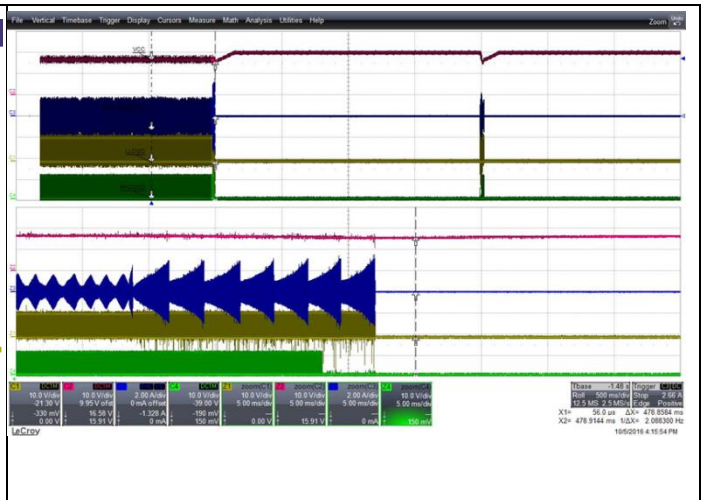
	
OCP1 @ 110 V_{AC} and 24 V output shorted	OCP1 @ 110V_{AC} and 24 V output shorted

Figure 36 LLC 1st level over current protection

10.20 X-Capacitor discharge during burst mode

In order to achieve low standby power consumption, the IDP2303 provides an active X-Capacitor discharge feature to remove the passive discharge resistor. The AC input voltage is measured via the HV pin during burst mode, and once the AC is unplugged, the IC detects the event, and after a blanking time, it turns on the start-up cell to discharge the X-Capacitor. For details, please refer to the IDP2303 datasheet.

In Figure 37, the X-Capacitor discharge feature during burst mode with typical standby loading is demonstrated, where it takes less than 1 s to detect and discharge the X-Capacitor after the AC is unplugged.

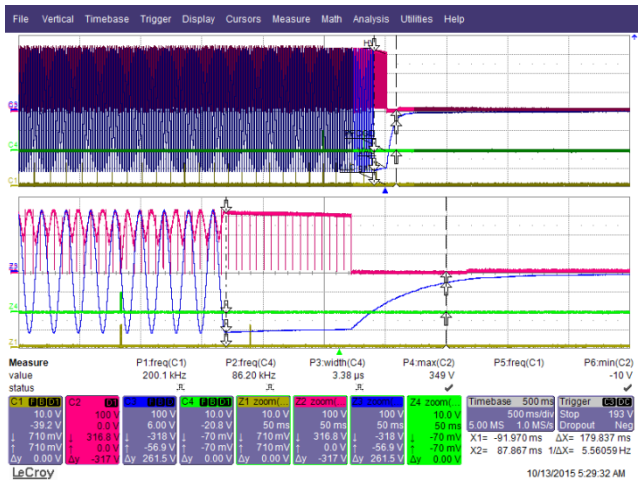
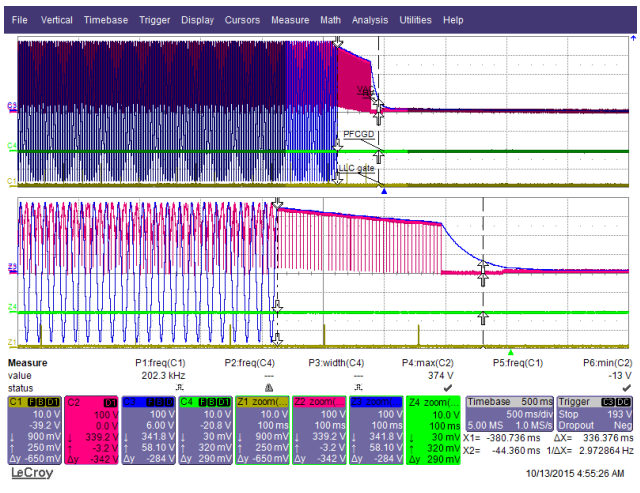
	
X-Capacitor discharge @ 230 V_{AC} and burst mode	X-Capacitor discharge @ 264 V_{AC} and burst mode

Figure 37 X-Capacitor discharge during burst mode

11 Configuration tools

The configurable parameters can be set via dpVision as shown in Figure 38. With selected applications, the table of its configurable parameters can be loaded as shown in the right side of the figure. In order to provide a clear understanding, the parameters are explained with images, waveforms and descriptions. Detailed information about the configurable parameters is shown in the datasheet, and a detailed description of the configuration tool is shown in the dpVision user manual.

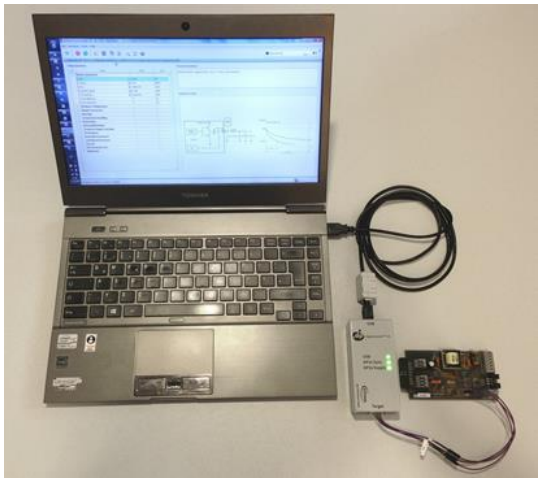
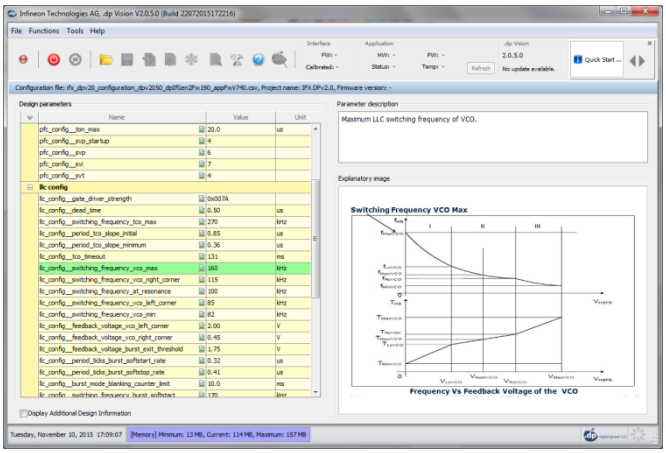
	
Configuration tool dpVision setup	dpVision parameter configuration page

Figure 38 Parameter configuration tool – dpVision

12 References

[1] IDP2303 datasheet, Infineon Technologies AG, 2016
[2] IDP60R400CE datasheet, Infineon Technologies AG, 2014
[3] IDP60R1K5CE datasheet, Infineon Technologies AG, 2015

Revision history

Document version	Date of release	Description of changes
1.1	2022-03-07	Editiorial changes
1.0	2017-04-25	Initial release

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