XDPL8105 single-stage PFC Flyback dimmable constant current controller

40 W reference design with CDM10V isolated 0-10 V dimming interface

XDP™ digital power

About this document

Scope and purpose

This document contains the specifications, schematics, Bill of Materials (BOM) and measurement results of the 40 W LED driver with 0 to 10 V dimming interface, using Infineon's XDPL8105 and CDM10V. It also includes a fine-tuning guide, debugging guide and frequently asked questions to ease the process of designing a customized LED driver with the XDPL8105 based on the user's own project requirements.

Intended audience

This document is intended for anyone wishing to design high-performance single-stage digital Flyback dimmable LED drivers using the XDPL8105 and the isolated 0 to 10 V dimming interface using CDM10V.

Table of contents

1 Introduction

The XDPL8105 40 W reference design is a digitally configurable LED driver with a universal input of 90 to 305 V AC, a wide output load range of 16 to 45 V DC and isolated 0 to 10 V dimming (with CDM10V). Please refer to the next page for the main design features of this board based on Infineon's XDPL8105 and CDM10V.

*Note: The 40 W reference design sample is ready to be tested on being received and without the need for any pre-programming by the user, as the XDPL8105 chip on the PCB has already been burned with the first full configuration set of working parameters. Please connect the AC input, LED output and dimming input as shown in **Figure 1** for the test set-up.*

ATTENTION: LETHAL VOLTAGES ARE PRESENT ON THIS REFERENCE DESIGN. DO NOT OPERATE THE BOARD UNLESS YOU ARE TRAINED TO HANDLE HIGH VOLTAGE CIRCUITS. DO NOT LEAVE THIS BOARD UNATTENDED WHEN IT IS POWERED UP.

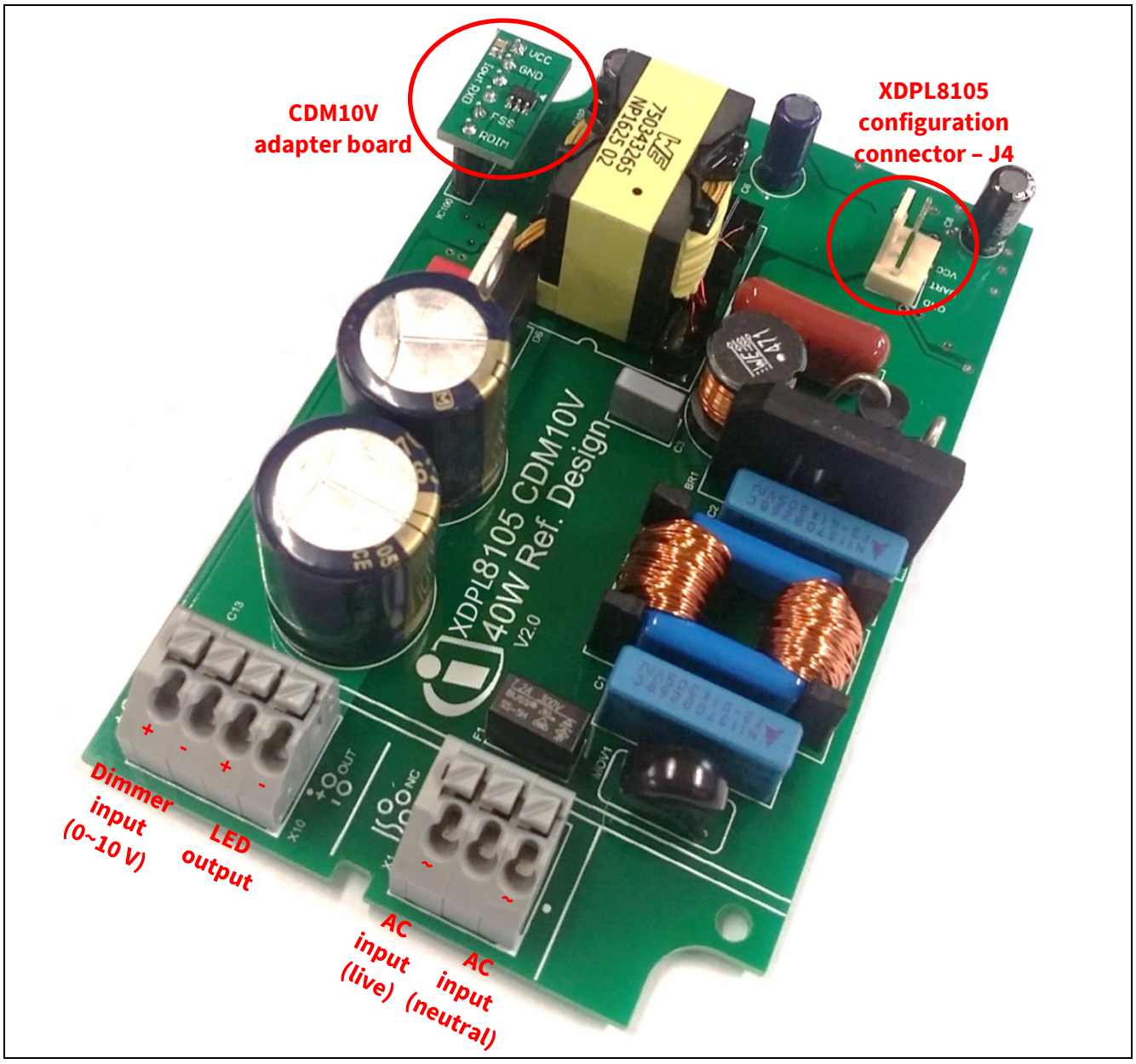


Figure 1 XDPL8105 40 W reference design with CDM10V adapter board and configuration connector

2 Design features

- Single-stage Flyback with Power Factor Correction (PFC) and high-precision primary-side-controlled constant current output
- Excellent current accuracy (±3 percent) across universal-input voltage range (90 to 305 V AC) and wide-output voltage range (18 V to 45 V)
- Integrated 600 V HV cell for fast start-up
- High efficiency with QR operation
- Low dimming output with Discontinuous Conduction Mode (DCM) and Active Burst Mode (ABM) operation
- High Power Factor (PF) and low input current Total Harmonic Distortion (iTHD) with advanced switching-cycle modulation scheme
- Low BOM
- Configurable dimming curve to either linear or quadratic (eye-adaptive)
- Configurable output current at minimum dimming input (from 10 percent to 1 percent)
- Quick design and variant handling supported by digital parameter configurability with .dp Vision GUI – e.g. output current setting, dimming curve shape selection, protection handling and operation fine-tuning
- Supports transformer-less IEC60929-compliant isolated 0 to 10 V dimming using CDM10V

Note: *CDM10V is a device which transmits analog voltage-based signals from a 0 to 10 V dimmer or potentiometer to the dimming or PWM input of a lighting controller IC in the form of a 5 mA current-based PWM signal to drive an external isolated optocoupler. It replaces many components in a traditional solution and reduces BOM and PCB space significantly. For more details about CDM10V, please visit the Infineon website: http://www.infineon.com/cdm10v*

3 Design specifications

Table 1 and **Table 2** respectively list the electrical specifications and system protections of this reference design.

Table 1 Electrical specifications

Specification	Symbol	Value	Unit
AC input voltage range	V_{AC}	90~305	Vrms
Output LED load range (includes dimming)	V_{LED}	16~45	V
Non-dimmed output current setting[1]	$I_{\_out\_set}$	880	mA
Total line, load regulation	-	±3	%
Dimming input voltage range	V_{DIMMER}	0~10	V
Dimming input resistance range[2]	R_{DIMMER}	5~50	kΩ
Minimum output current setting[1]	$I_{\_out\_dim\_min}$	88	mA
Output current dimming curve[1]	$C_{\_dim}$	Quadratic	–
Efficiency (V_{in}: 120~277 V AC, V_{out}: 30~45 V, non-dimming)	η	More than 89	%
Power factor (V_{in}: 120~277 V AC, V_{out}: 30~45 V, non-dimming)	PF	More than 0.95	–
Input current total harmonic distortion (V_{in}: 120~277 V AC, V_{out}: 30~45 V, non-dimming)	iTHD	Less than 10	%

[1] Configurable in XDPL8105 .

[2] Based on CDM10V pin R_{dim+} default bias current of 200 µA. See **Table 3** for configurable options.

Table 2 System protections

Protection	Symbol	Value	Unit
Nominal input Over-Voltage Protection (OVP) level[1]	$V_{\_inOV}$	329	Vrms
Nominal input Under-Voltage Protection (UVP) level[1]	$V_{\_inUV}$	62	Vrms
Nominal output OVP level[2]	$V_{\_outOV}$	48.4	V
Nominal output over-current (average) protection level[3]	$I_{\_out\_max\_avg}$	1320	mA
Nominal output over-current (peak) protection level[1]	$I_{\_out\_max\_peak}$	1980	mA
IC over-temperature detection threshold[2]	$T_{\_critical}$	119	°C
Input OVP reaction	$Reaction_{\_OVP\_Vin}$	Latch mode	–
Input UVP reaction	$Reaction_{\_UVP\_Vin}$	Auto-restart	–
Output OV (output open) protection reaction[4]	$Reaction_{\_OVP\_Vout}$	Auto-restart	–
Output UV (output short) protection reaction	$Reaction_{\_UVP\_Vout}$	Auto-restart	–
Output over-current (average) protection reaction	$Reaction_{\_Iout\_max\_avg}$	Auto-restart	–
Output over-current (peak) protection reaction	$Reaction_{\_Iout\_max\_pk}$	Auto-restart	–
IC over-temperature protection reaction	$Reaction_{\_TP}$	Latch mode	–
Auto-restart time[5]	$t_{\_auto\_restart}$	1.0	s

[1] Protection can be disabled and its level can be configured.
[2] Protection cannot be disabled but its level can be configured.
[3] Protection can be disabled but its level cannot be configured and fixed as 150 percent of $I_{\_out\_set}$.
[4] Protection reaction can be configured to either auto-restart or latch mode.
[5] Auto-restart time of the protections can be configured.

4 Schematic and PCB layout

Figure 2 shows the schematic of this reference design.

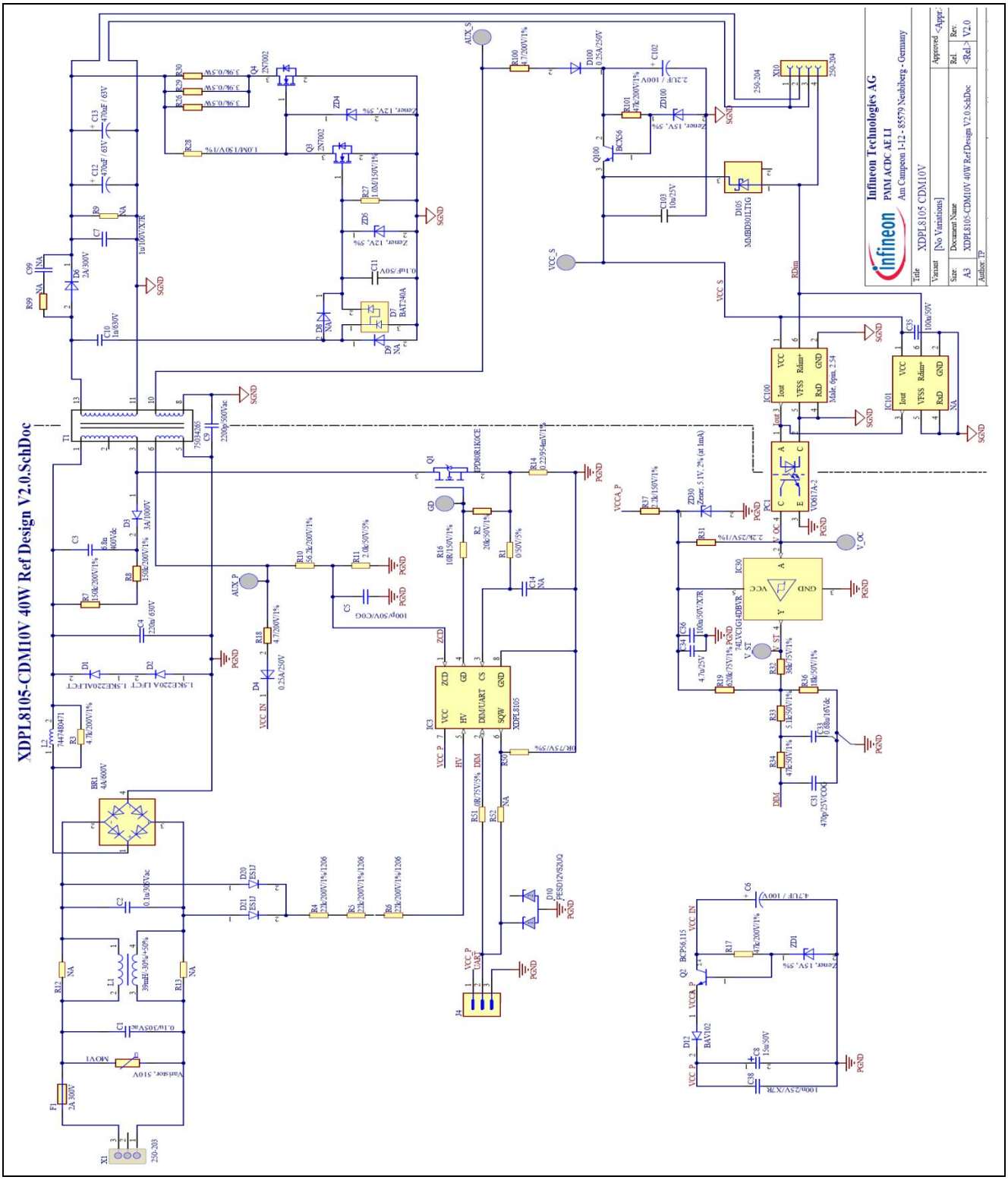


Figure 2 Schematic

Note: By default, the reference design main board is connected with the CDM10V adapter board via IC100. If necessary, the user can unplug the adapter board and mount CDM10V on the main board via IC101.

Figure 3 and **Figure 4** respectively show the PCB top and bottom layouts of this reference design.

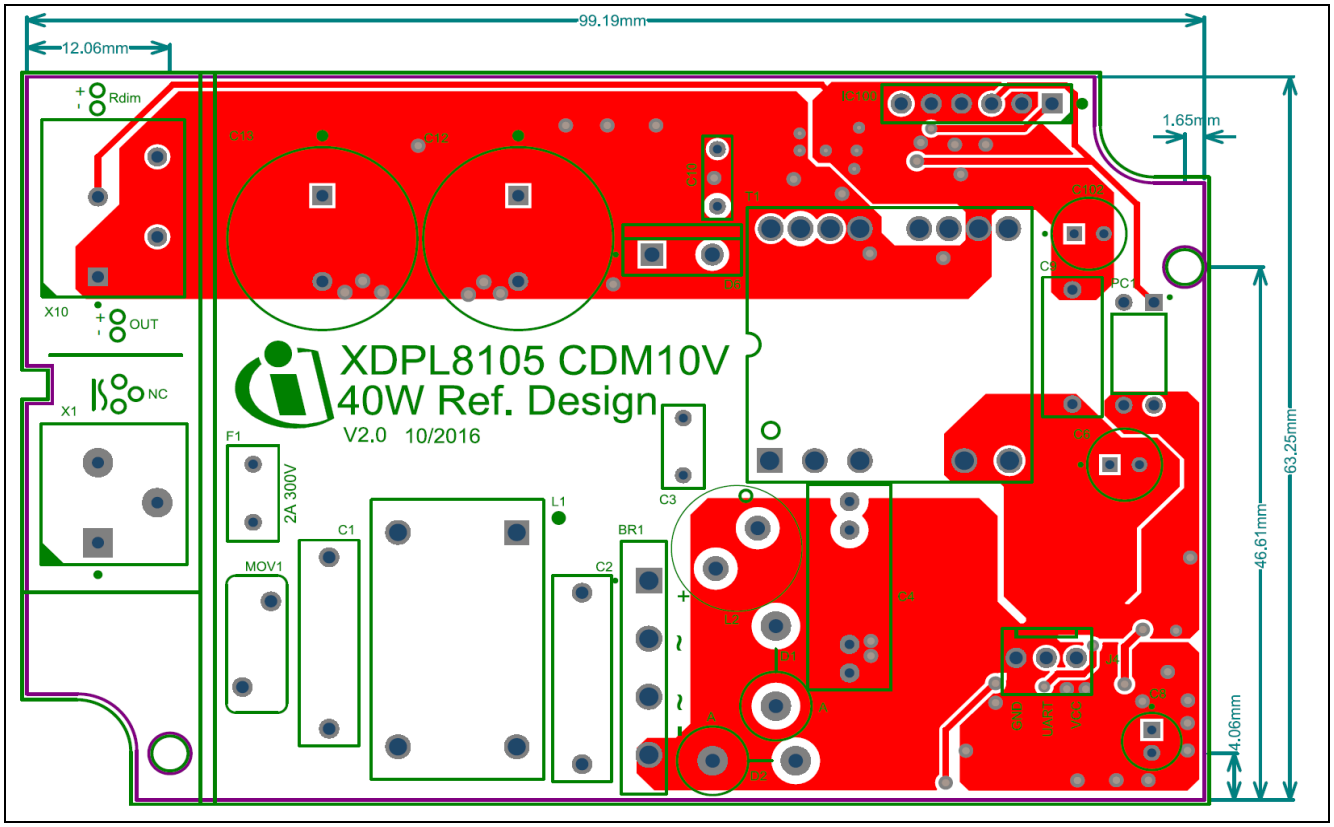


Figure 3 PCB top layout and dimensions

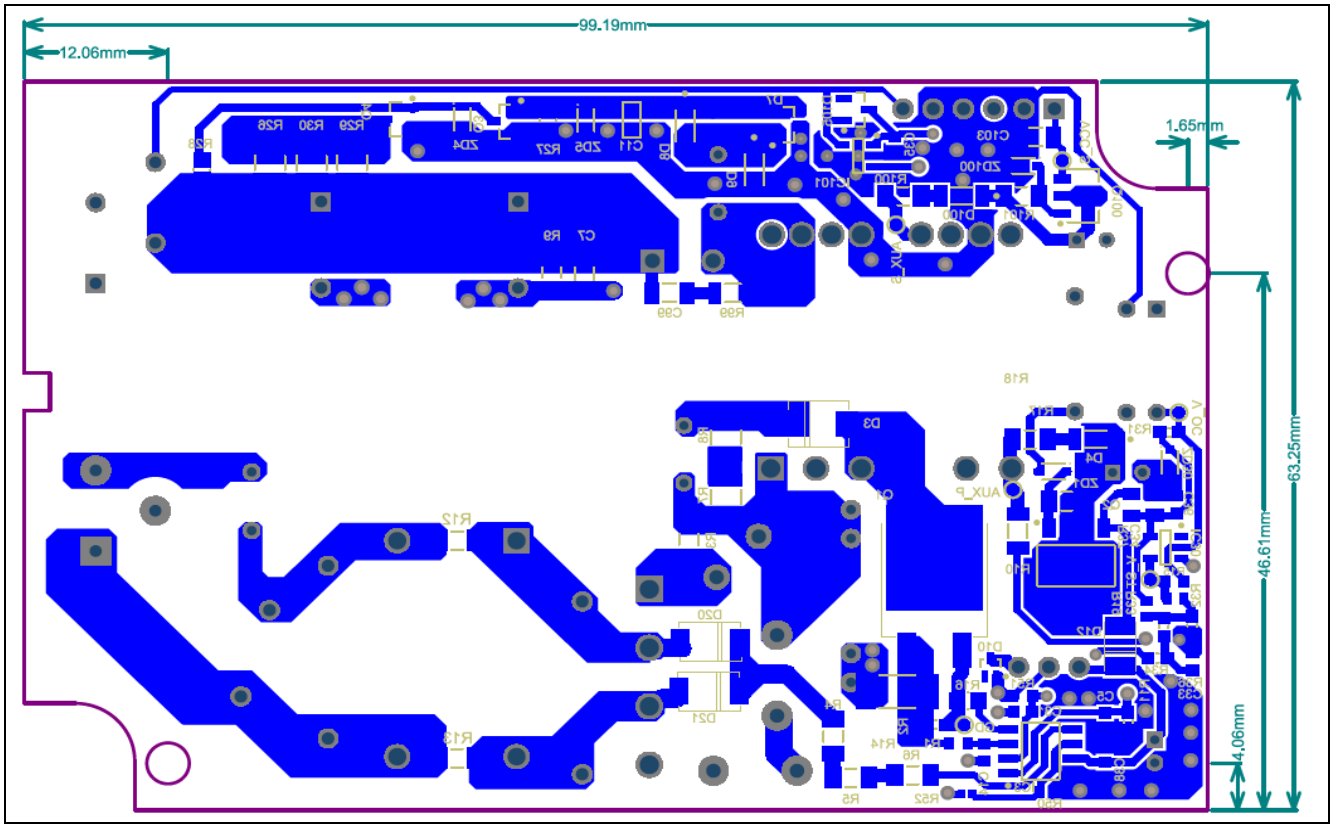


Figure 4 PCB bottom layout and dimensions

5 CDM10V circuit design and operation

R100, D100 and C102 form a rectifier circuit which supplies a voltage from the transformer winding based on a ratio of the output load voltage. In this design, it is necessary to add the voltage regulator circuitry (consisting of R101, ZD100, Q100 and C103) after the rectifier circuitry to ensure that the CDM10V pin V_{CC} voltage supply is kept stable and within the limits while supporting the wide output load voltage range of 16~45 V. By selecting a Zener diode, ZD100, which has a low voltage rating and yet is sufficient to supply the CDM10V operating voltage, the CDM10V chip losses can be kept low. A 15 V Zener is used in this design.

D105 is connected between pin R_{dim+} and pin V_{CC} to ensure the voltage level at pin R_{dim+} does not exceed its maximum voltage rating of V_{CC} + 0.7 V, in case of an active voltage source (e.g. DC power supply) being applied to the 0 to 10V dimmer input of this reference design for testing purposes. For productive use only a passive voltage source (e.g. potentiometer, current sink dimmer) can be connected to pin R_{dim+}, and D105 can be omitted. For productive use either the active or passive voltage source can be connected to pin R_{dim+}, and it is highly recommended to use a low-leakage Schottky diode for D105 such as MMBD301LT1G, to maintain high accuracy of the dimmer voltage measurement on pin R_{dim+}.

CDM10V pins GND, RxD and V_{FSS} are directly connected to a secondary-side ground plane, which is also used as the cooling area.

The optocoupler, PC1, is directly driven by a 5 mA current-based PWM signal from pin I_{out} of CDM10V. The PWM duty cycle changes based on the voltage level at CDM10V pin R_{dim+}, which should be connected to either the 0 to 10 V dimmer or the potentiometer.

There are many ways of designing the primary-side circuitry connecting to the optocoupler, depending on the dimming input type of the primary controller. This reference design presents an exemplary circuit based on the primary controller XDPL8105, which has an analog non-inverting dimming input.

IC30, a single-channel Schmitt trigger inverter IC, is used here for many reasons. One is to invert the receiving signal of PC1 so that it matches the XDPL8105 non-inverting dimming input. A second reason is to reconstruct the receiving signal of PC1, which is heavily distorted by the slow-rising slope, into a more accurate digital PWM signal (the slow-rising slope is caused by the low pull-up current to the coupler and the selection of a slow-switching optocoupler). The final reason is that the required analog voltage levels can be adjusted with the two resistor dividers after and over it (R19 and R36 for the minimum voltage/maximum dimming and R32 and R36 for the maximum voltage/no dimming).

The supply voltage of 5.1 V for IC30 and the coupler of PC1 (via pull-up resistor R31) is stepped down from the regulated auxiliary self-supply voltage of the D12 anode by using a resistor (R37), a Zener diode (ZD30) and two capacitors (C34 and C36). For fast and smooth XDPL8105 start-up, D12 is necessary to ensure the XDPL8105 pin HV charging current only flows to its V_{CC} capacitors (C8 and C38), but not to other parts of the primary circuit.

Since the XDPL8105 has an analog dimming input, the digital PWM signal generated by IC30 must be filtered. As the XDPL8105 already has an internal six-stage digital filter for its dimming input sensing, an external single-stage low-pass filter (R33 and C33) with a cut-off frequency at 100 Hz is deployed in this reference design. Otherwise, it is strongly recommended to have two stages of a 100 Hz low-pass filter.

In order to retain both the signal integrity of the communication and the dimming functionality of XDPL8105, the pin DIM/UART impedance cannot be too low, and thus an additional RC filter (C31 and R34) is deployed after the 100 Hz low-pass filter (R33 and C33). It is important to note that C31 should not exceed 1 nF.

Since ZD30, the Zener voltage (Vz), serves as the reference voltage of the digital PWM-to-analog signal conversion, it is very important to select a 5.1 V Zener part number of ZD30 which has good Vz-Iz characteristics (stable Vz with low Zener current, Iz) and a low tolerance (e.g. 2.5 percent or below) for highly accurate

dimming input signals. **Figure 5** shows how to determine the good and poor Zener Vz-Iz characteristics from two different part numbers (X and Y) with 5.1 V Zener voltage.

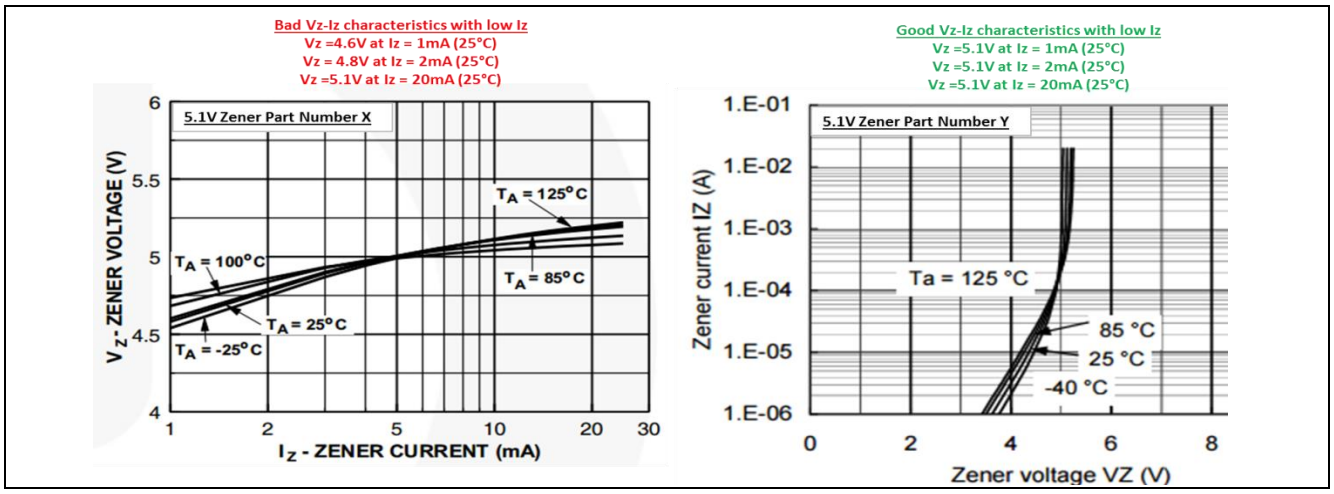


Figure 5 Example of how to determine good and poor Zener Vz-Iz characteristics

Table 3 shows the default and configurable settings of the four parameters in the CDM10V device. The CDM10V adapter board in this reference design uses the default settings. If necessary, please refer to **Section 8.2** for more information on CDM10V configuration.

Table 3 Default and configurable settings of the four parameters in the CDM10V device

Parameter	Fuse bits setting and description		Remark
Pin R_{dim+} bias current	00	200 µA	Default CDM10V setting
	01	100 µA	–
	10	50 µA	–
	11	500 µA	–
Dim-to-off option	0	Disabled	Default CDM10V setting
	1	Enabled	–
Pin I_{out} PWM output frequency	00	1000 Hz	Default CDM10V setting
	01	500 Hz	–
	10	200 Hz	–
	11	2000 Hz	–
Pin I_{out} PWM output Minimum duty cycle	00	5 percent	Default CDM10V setting
	01	2 percent	–
	10	1 percent	–
	11	10 percent	–

6 Performance

6.1 Non-dimming

The measurement results under non-dimming conditions are presented in this section.

6.1.1 Output regulation and tolerance

The total line (V AC = 90~300 V_{rms}) and load regulation (V_{LED} = 18~45 V) of the output current under non-dimming conditions are ±2 percent or less, based on the output current set-point of 880 mA.

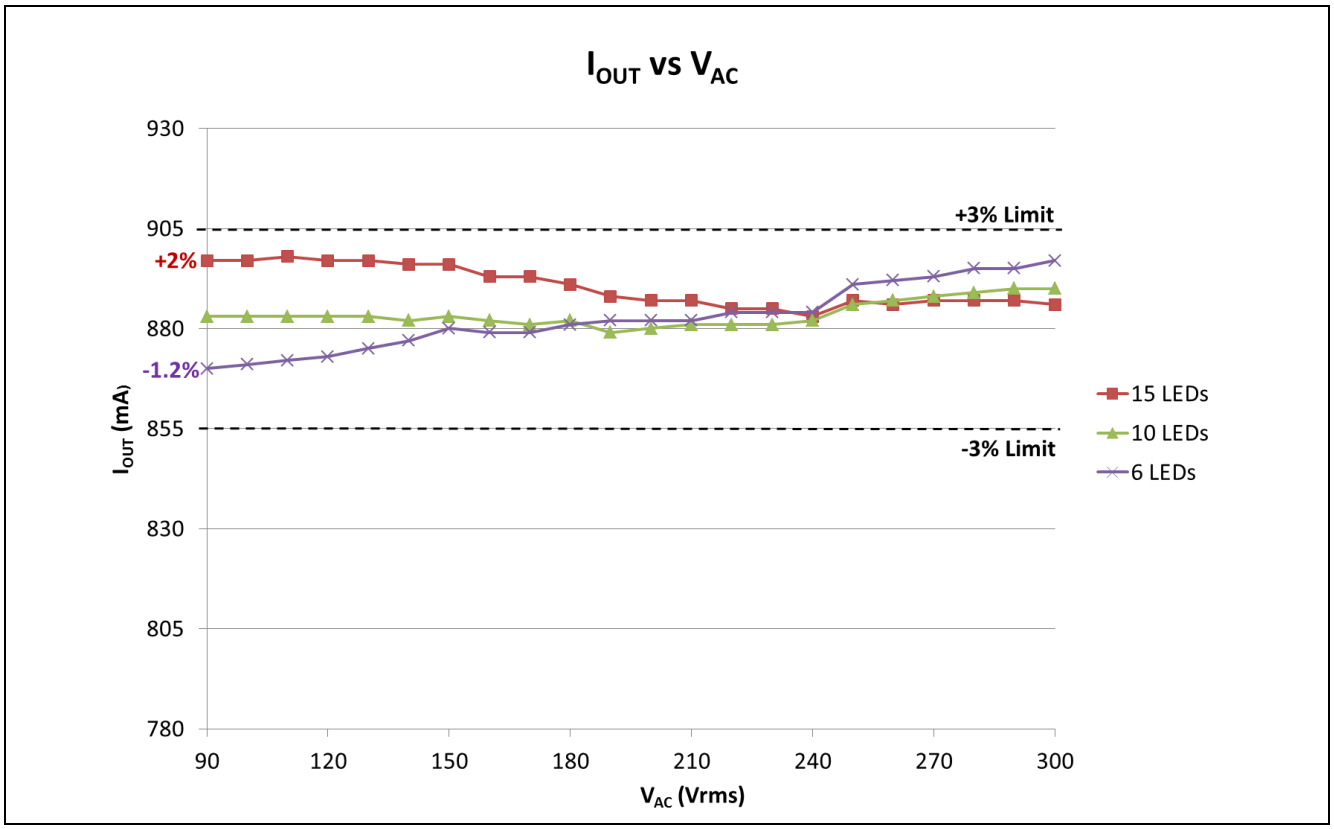


Figure 6 Line and load regulation of output current under non-dimming conditions

In total 50 reference design samples have been tested, and the non-dimmed output current of each board was recorded using the same test condition (V AC input: 90 Vrms, output: 15 LEDs and ambient temperature of 25°C) to check the output tolerance, which is contributed to by both the IC and external components' tolerance. The tolerance study was done based on this test condition because it has the highest output current regulation of +2 percent (see **Figure 6**), so that the total output regulation and sample output tolerance can be estimated.

Figure 7 shows the distribution data of the non-dimmed output current.

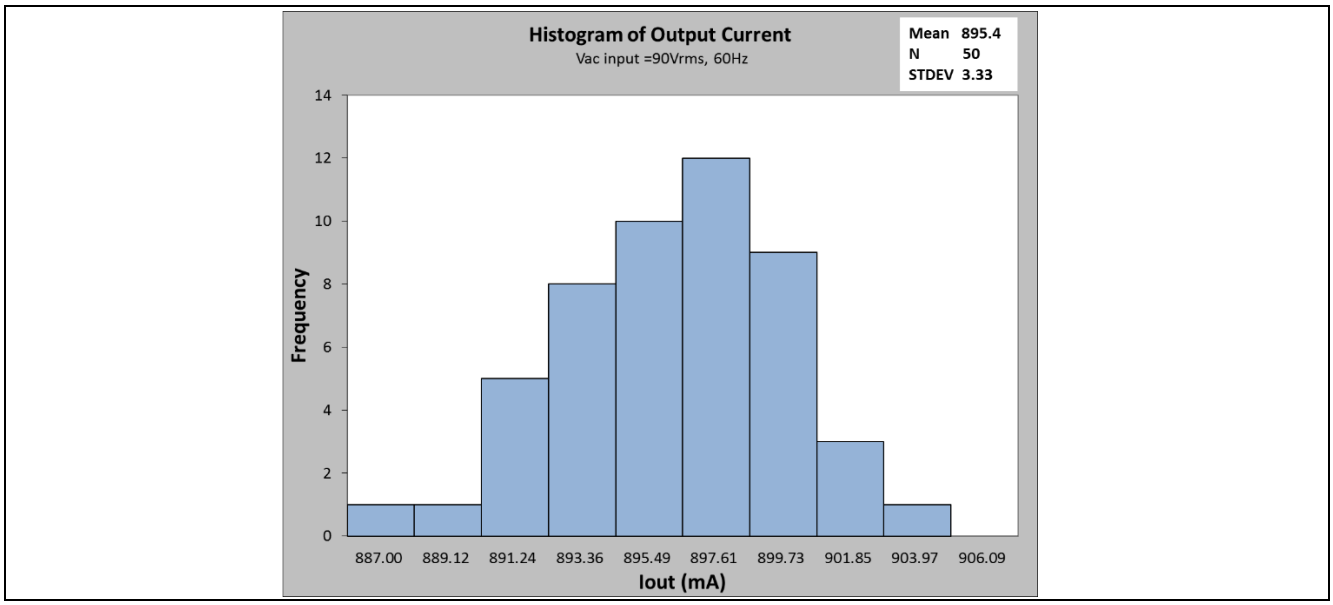


Figure 7 Output current histogram based on 50 reference design samples

The result shows that the output current tolerance is approximately ±1 percent and standard deviation is 3.33 mA. Therefore, the total output regulation and sample output tolerance is approximately ±3 percent.

6.1.2 System efficiency

The system efficiency measurements under non-dimming conditions are shown in **Figure 8**.

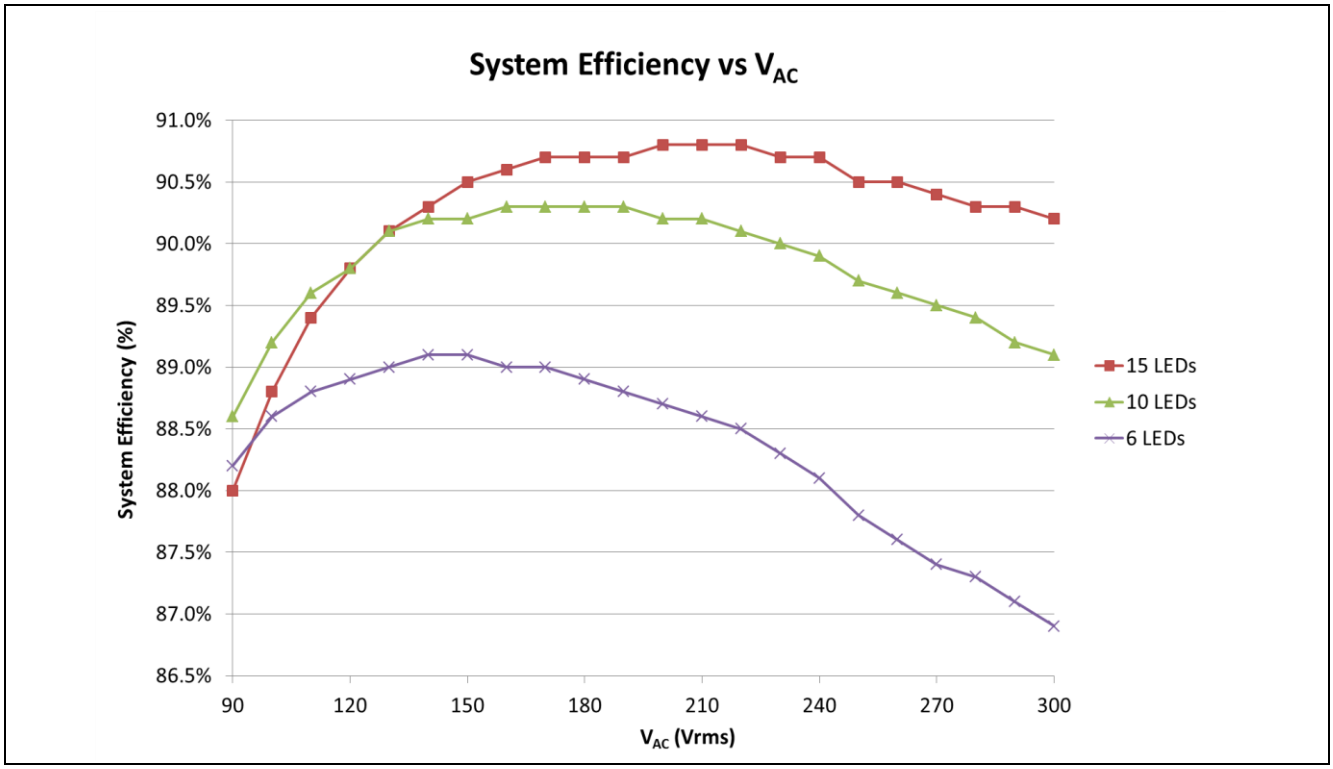


Figure 8 System efficiency under non-dimming conditions

6.1.3 PF and iTHD

The PF and iTHD measurements under non-dimming conditions are shown in **Figure 9** and **Figure 10**.

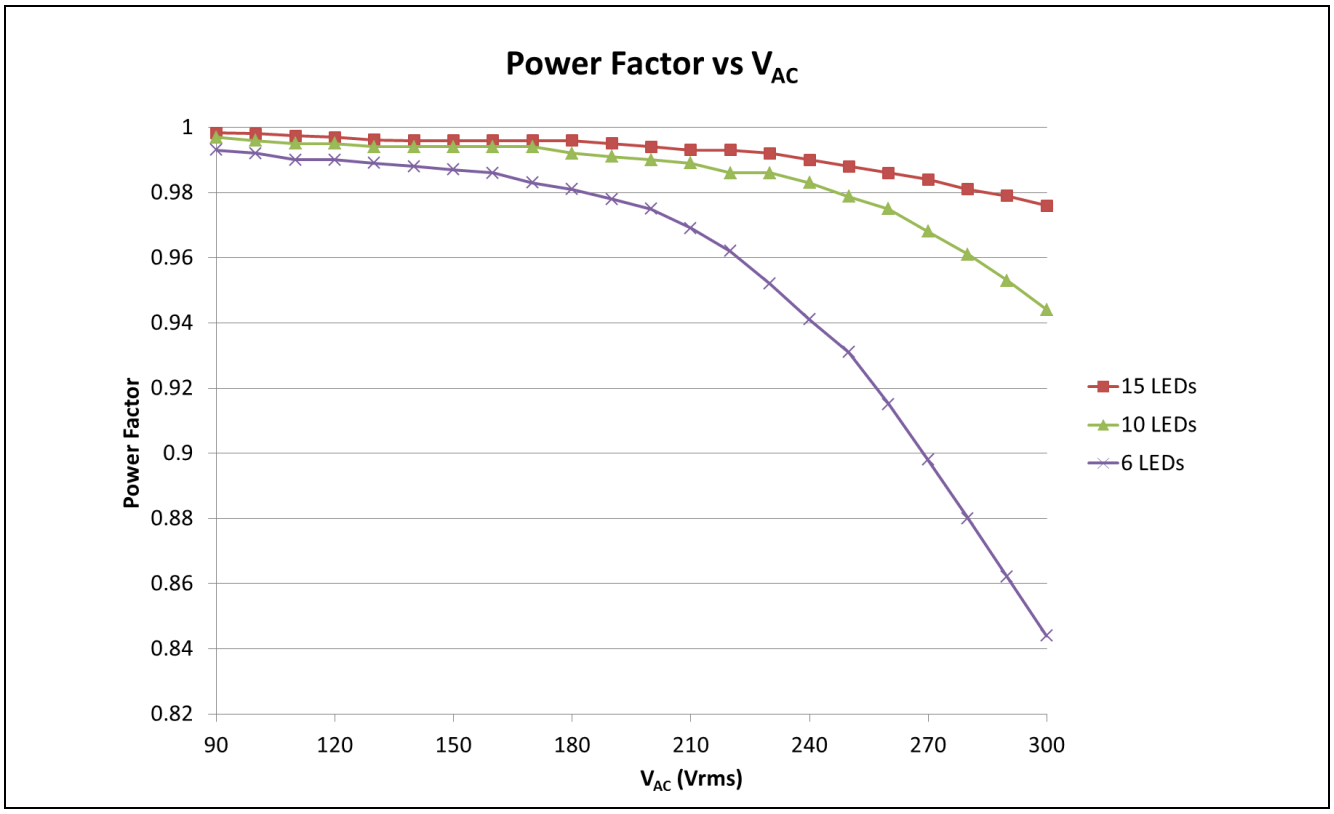


Figure 9 PF under non-dimming conditions

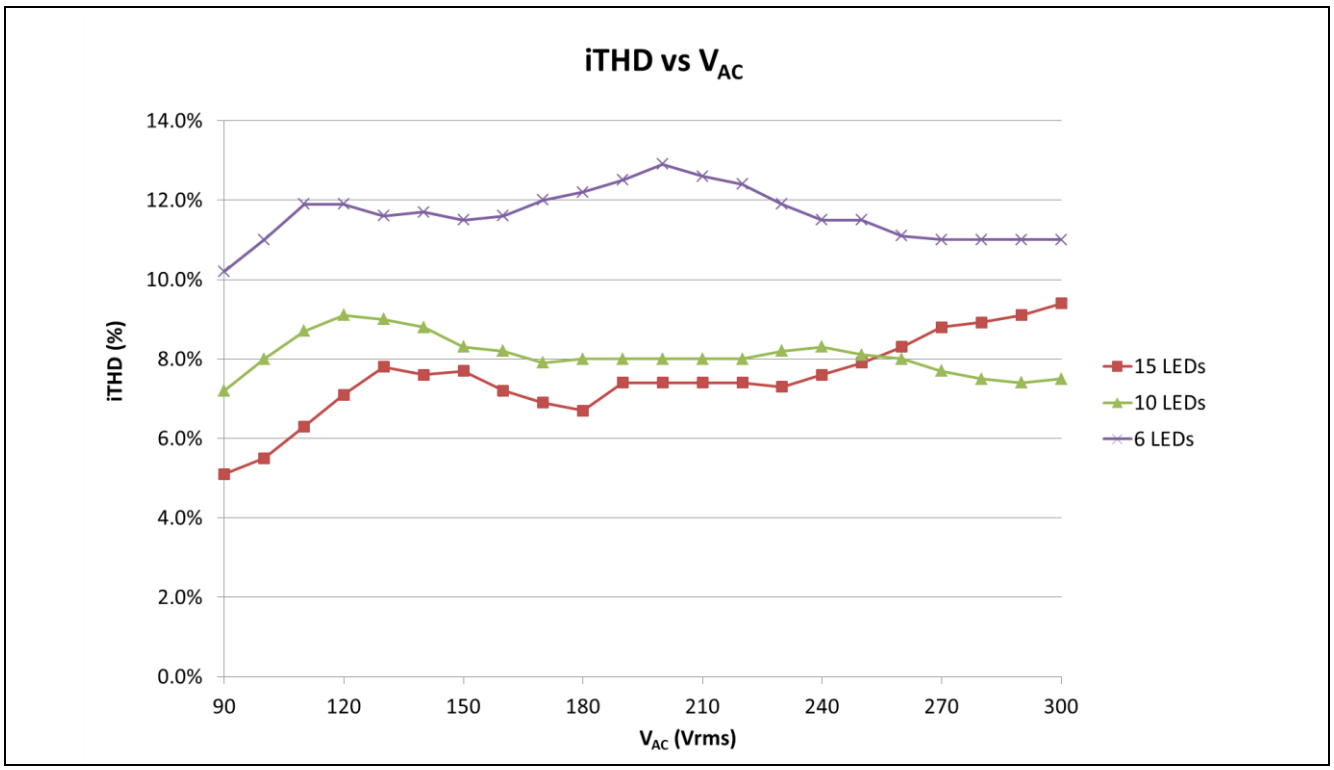


Figure 10 iTHD under non-dimming conditions

6.1.4 Thermal test

The open-frame thermal test was done on the reference design using an infrared thermography camera (TVS-500EX) at an ambient temperature of 20°C.

The temperature measurements of the following main components (see **Table 4**) were taken after two hours running at maximum LED voltage and maximum output current.

Table 4 Main components for temperature measurements

PCB bottom		PCB top	
Component	**Description**	**Component**	**Description**
Q2	Primary V_{CC} regulator NPN transistor	D6	Output diode
IC3	Flyback-controlled XDPL8105	IC101	CDM10V
Q1	Flyback MOSFET IPD80R1K0CE	PCB	Hottest PCB area
ZD5	Output bleeder Zener diode	T1 – core	Flyback transformer core
Q100	Secondary V_{CC} regulator NPN transistor	T1 – winding	Flyback transformer winding

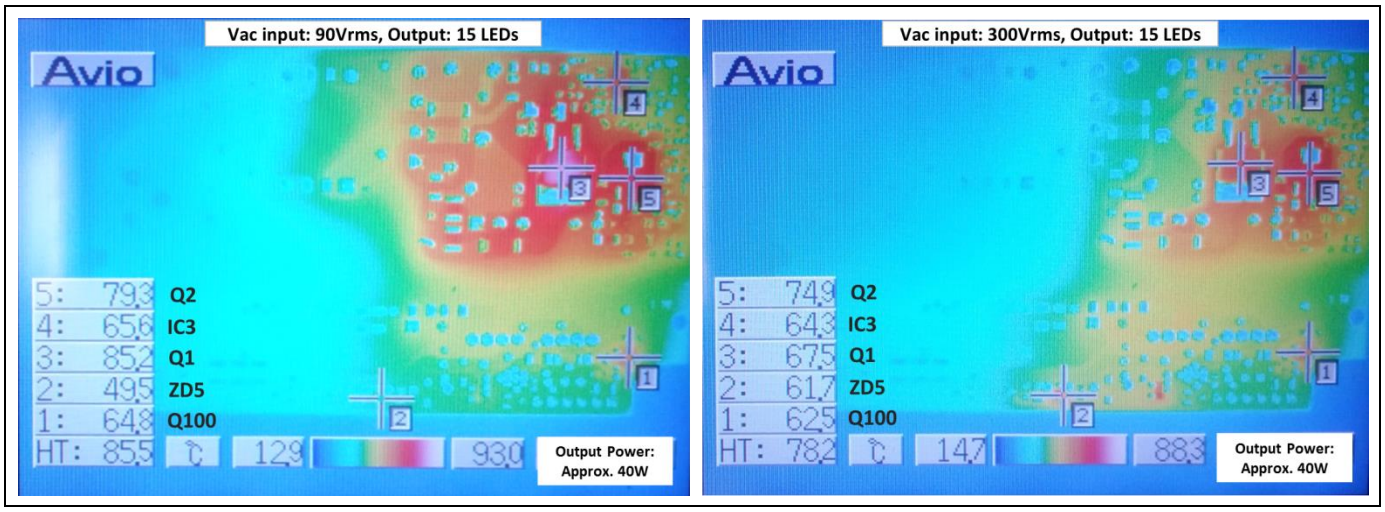


Figure 11 Infrared thermal image of PCB bottom components

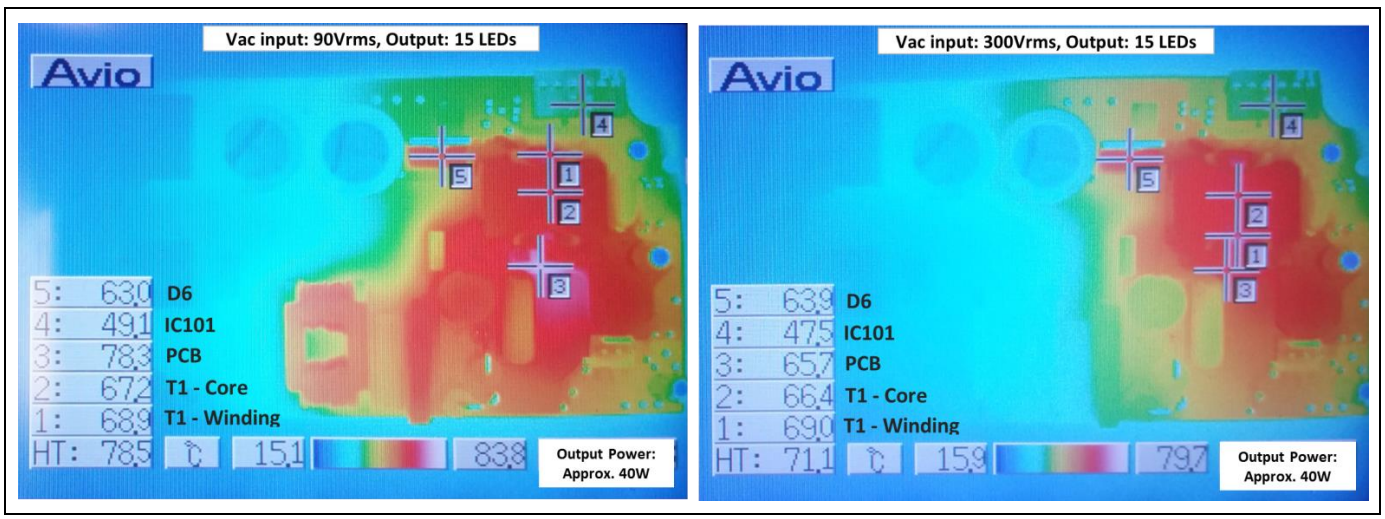


Figure 12 Infrared thermal image of PCB top components

6.1.5 Conducted emissions (EN 55015B)

The conducted emissions test was performed at maximum output power (40 W) of this reference design (maximum output LED load voltage under non-dimming conditions) and there is more than 3 dB margin observed for both live and neutral measurements based on EN 55015 standard Class B limits.

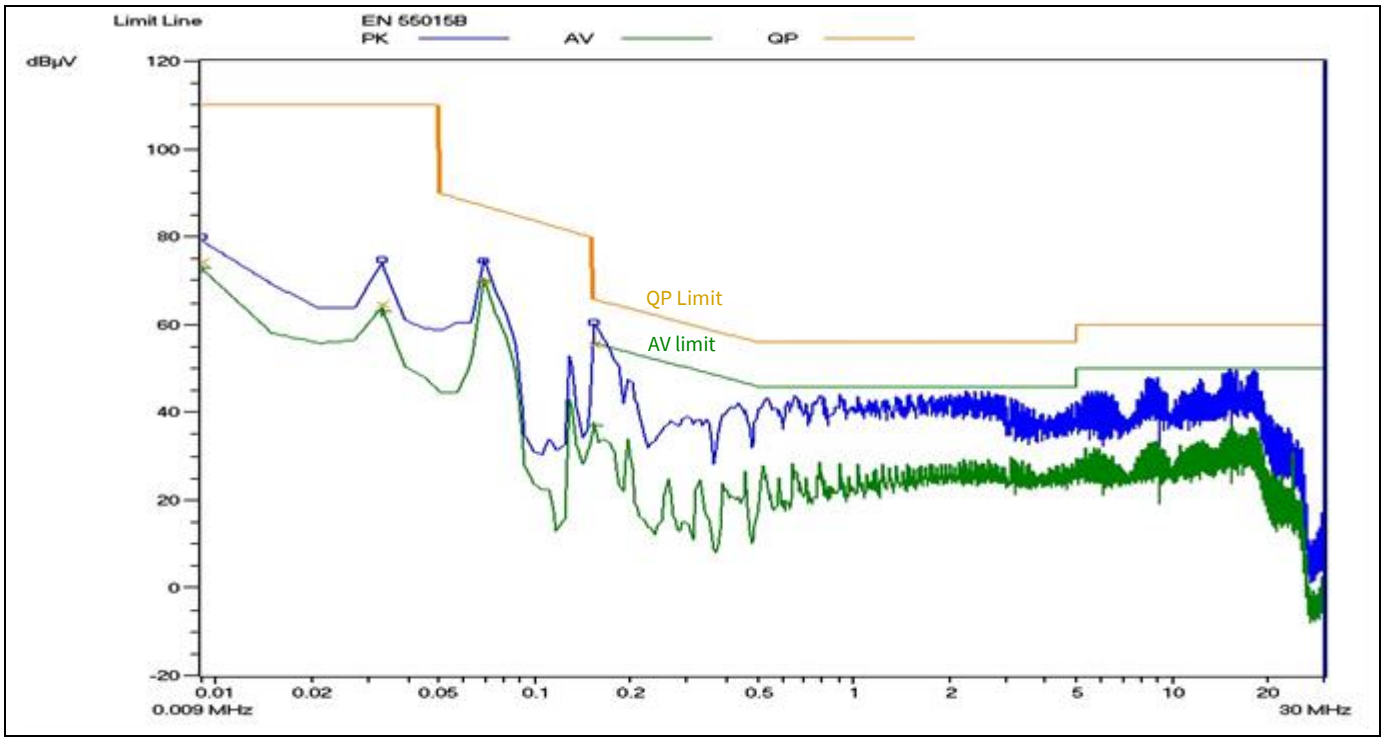


Figure 13 Conducted emissions (live) at 110 V AC, 50 Hz at maximum output power 40 W

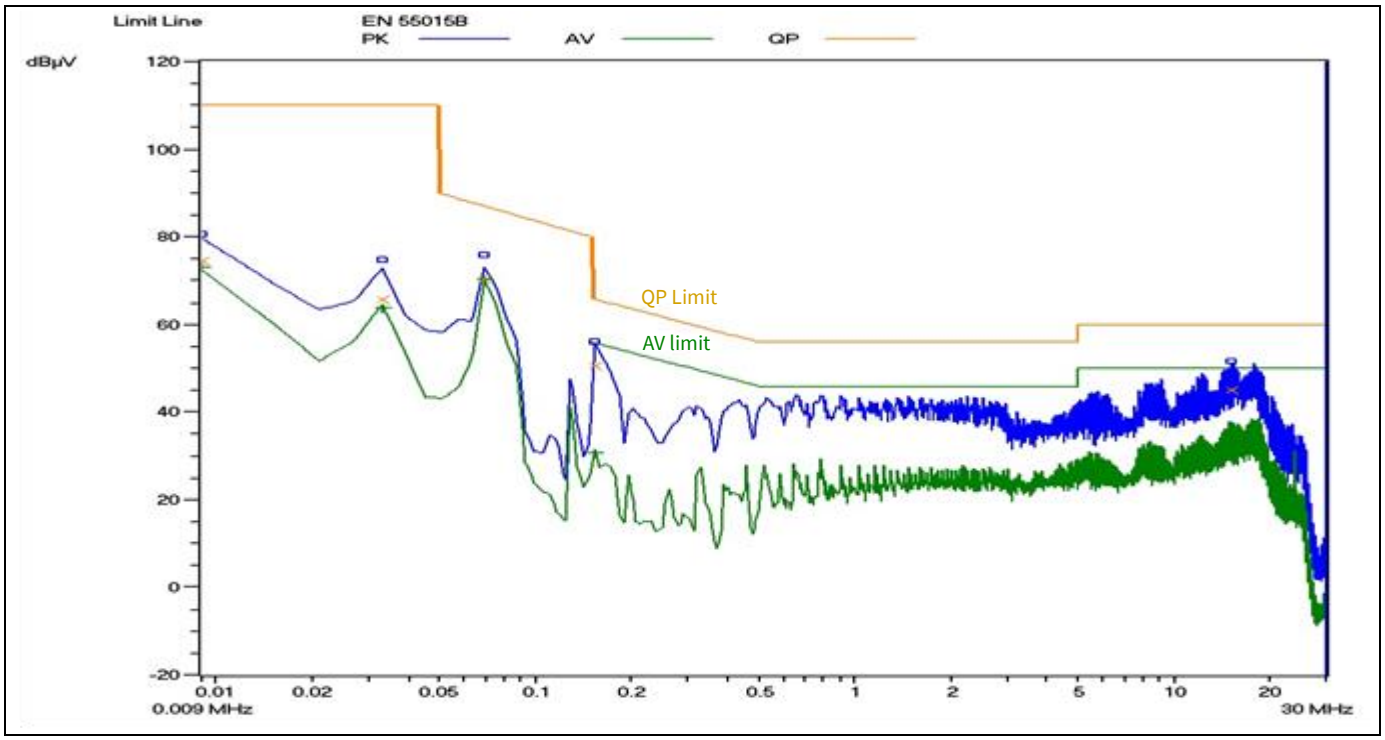


Figure 14 Conducted emissions (neutral) at 110 V AC, 50 Hz at maximum output power 40 W

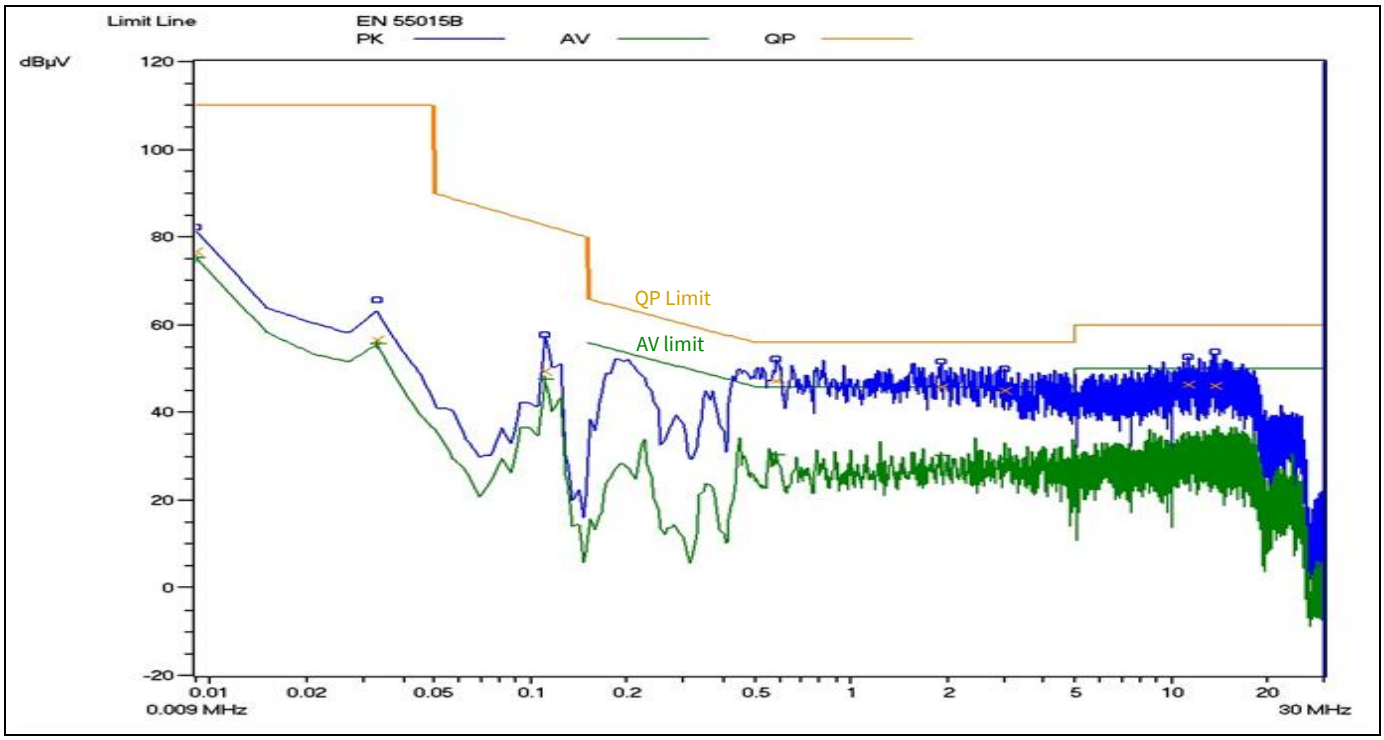


Figure 15 Conducted emissions (live) at 230 V AC, 50 Hz at maximum output power 40 W

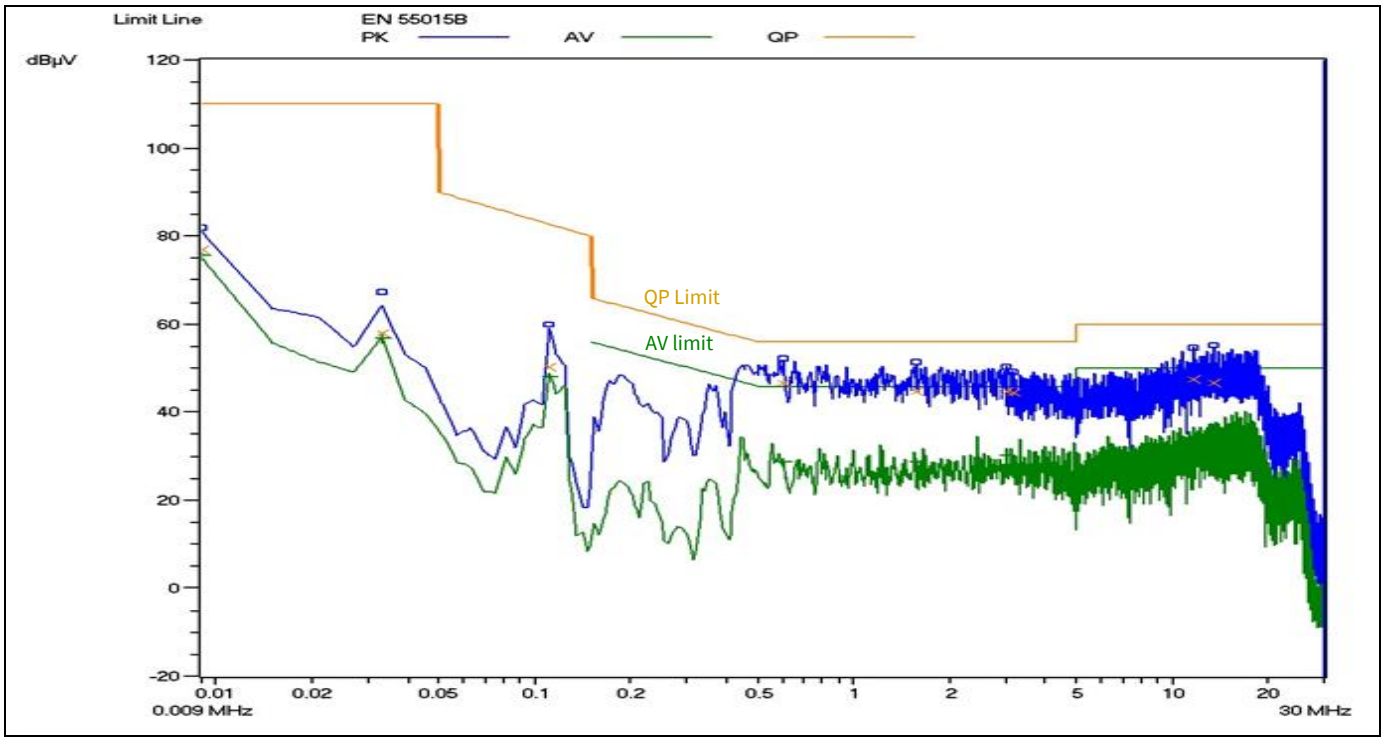


Figure 16 Conducted emissions (neutral) at 230 V AC, 50 Hz at maximum output power 40 W

Note: The items of measuring equipment used for this conducted emissions test were Schaffner NNB41 and SMR4503.

6.2 Dimming

This section provides the output current, I_{OUT}, measurement results when V_{DIMMER} = 0~10 V is applied (see **Table 5**), with an AC input voltage of 277 Vrms, 60 Hz and an output load of 10 LEDs.

Based on the measurement results, the plotted dimming curve has a quadratic shape (see **Figure 17**) because the reference design XDPL8105 chip has already been burned with the parameter *C_DIM* setting “Quadratic”.

Note: The user can configure the dimming curve shape parameter, C_DIM, to either “Linear” or “Quadratic”.

Table 5 Output current dimming measurement

V_{DIMMER} (V)	0	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0
I_{OUT} (mA)	89	89	89	94	108	132	163	203	252	311

V_{DIMMER} (V)	5.5	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	10.0
I_{OUT} (mA)	377	446	522	606	695	790	882	888	888	888

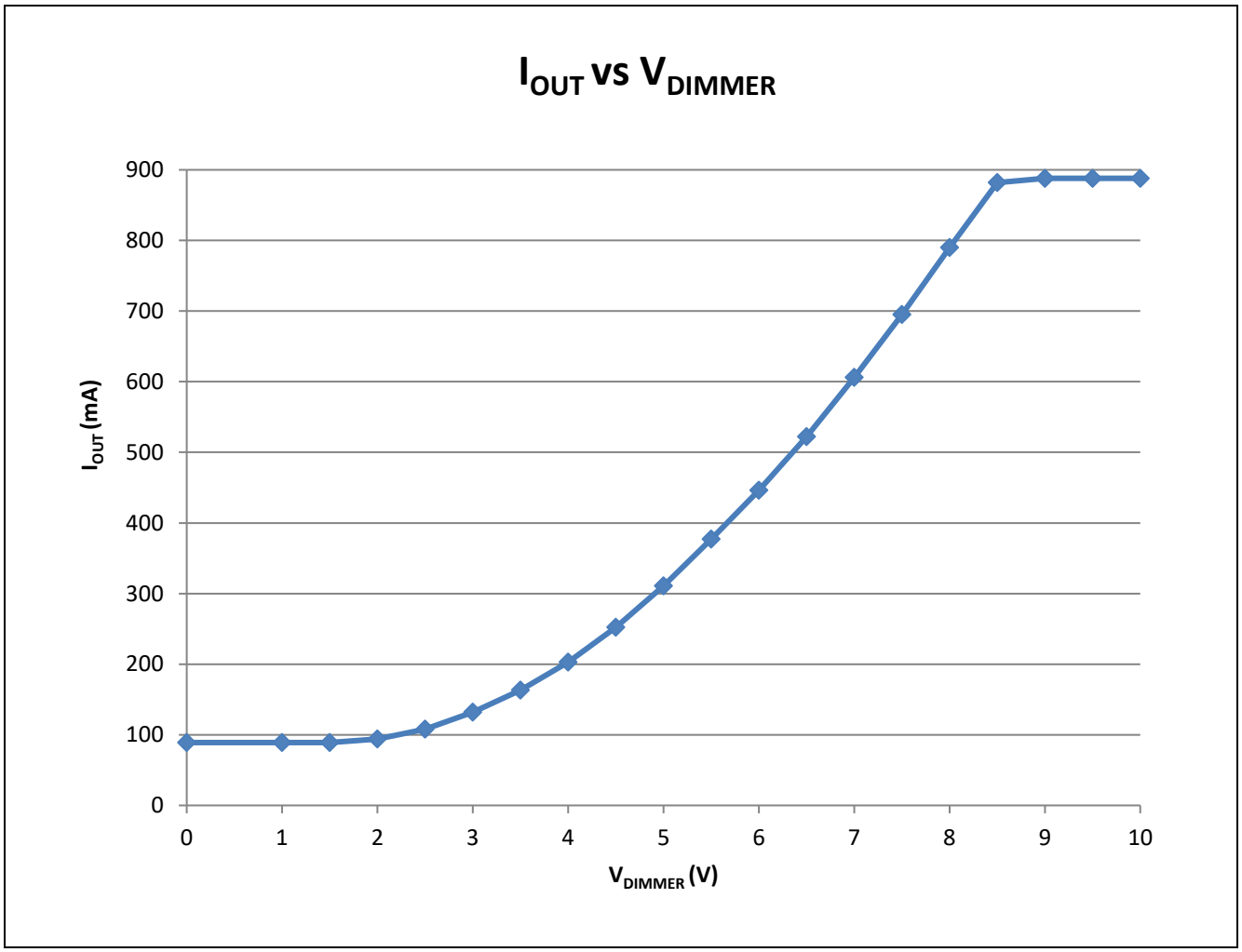


Figure 17 Quadratic dimming curve (adapted to eye sensitivity)

7 Bill of Materials

This section provides the BOM and also the transformer specifications.

7.1 BOM

Table 6 BOM of main board

Designator	Value	Part number	Manufacturer	Quantity
BR1	4 A/600 V	GBU4J-E3/45	Vishay	1
C1, C2	0.1 µ/305 V AC	B32922C3104K	Epcos	2
C3	6.8 n/400 V	BFC237065682	Vishay	1
C4	220 n/630 V	ECW-FA2J224J	Panasonic	1
C5	100 p/50 V/C0G	C0603C101F5GAC	Kemet	1
C6	4.7 µF/100 V 20 percent radial	ECA2AM4R7	Panasonic	1
C7	1 µ/100 V	12061C105K4Z2A	AVX	1
C8	15 µ/50 V	EEU-FC1H150H	Panasonic	1
C9	2200 p/500 V AC	VY1222M47Y5UQ63V0	Vishay	1
C10	1 n/630 V	FKP2J011001D00JSSD	Wima	1
C11	0.1 µF/50 V	GRM188R71H104KA93D	Murata	1
C12, C13	470 µF/63 V/20 percent radial	EEU-FC1J471	Panasonic	2
C31	470 p/25 V/COG	06033A471K4T2A	AVX	1
C33	0.68 µ/16 V	GRM188R61C684KA75#	Murata	1
C34	4.7 µ/25 V	C2012X7R1E475K125AB	TDK	1
C35, C36, C38	100 n/50 V	MC0603B104K500CT	Multicomp	3
C102	2.2 µF/100 V/20 percent radial	UPW2A2R2MDD	Nichicon	1
C103	10 µ/25 V	GRM31CR71E106KA12L	Murata	1
D1, D2	220 V/1.5 kW	1.5KE220A	STMicroelectronics	2
D3	Diode, fast, 3 A, 1000 V	RS3MB-13-F	Diodes	1
D4, D100	Diode, fast, 0.25 A, 250 V	BAV103,115	NXP Semiconductors	2
D6	Schottky, 40 A, 250 V	MBR40250G	On Semiconductor	1
D7	Schottky, 0.4 A, 240 V	BAT 240A E6327	Infineon	1
D10	ESD diode, 12 V	PESD12VS2UQ	NXP	1
D12	Diode, fast, 0.25 A, 200 V	BAV102	NXP	1
D20, D21	Diode, fast, 1 A, 600 V	ES1J	FAIRCHILD	2
D105	Schottky, 0.2 A, 30 V	MMBD301LT1G	ONSEMI	1
F1	Fuse 300 V/2 A	SS-5H-2A-APH	Bussmann by Eaton	1
IC3	Digital Flyback controller IC	XDPL8105	Infineon	1
IC30	Single Schmitt trigger inverter	SN74LVC1G14DBVR	Texas Instruments	1
IC100	Male, six-pin, 2.54 connector to CDM10V adapter board	SL1.025.36Z cut six-pin	Fischer Elektronik	1
J4	2.54 mm header, three-pin, vert.	MC34631	Multicomp	1
L1	39 mH/0.8 A	B82732F2801B001	Epcos	1
L2	470 µH/1.15 A	7447480471	Würth Elektronik	1
MOV1	Varistor, 510 V	ERZE08A511	Panasonic	1
PC1	VO617A-2	VO617A-2	Vishay	1
Q1	MOSFET, 0.95 Ω, 800 V, DPAK	IPD80R1K0CEBTMA1	Infineon	1
Q2	NPN, 1 A, 80 V, SOT-223	BCP56,115	NXP	1
Q3, Q4	MOSFET, 0.3 A, 60 V, SOT-23	2N7002	Infineon	2

Bill of Materials

Designator	Value	Part number	Manufacturer	Quantity
Q100	NPN, 1 A, 80 V, SOT-89	BCX56-16,115	NXP	1
R1, R50, R51	0 R	RC0603JR-070RL	Yageo/Phycomp	3
R2	20 k	AC0603FR-0720KL	Yageo/Phycomp	1
R3	4.7 k	RC1206FR-074K7	Yageo/Phycomp	1
R4, R5, R6	22 k	RC1206FR-0722K	Yageo/Phycomp	3
R7, R8	150 k/0.5 W	CRCW1210150KFKEA	Vishay	2
R10	56.2 k	CRCW120656K2FKEA	Vishay	1
R11	2.0 k	AC0603JR-072KL	Yageo/Phycomp	1
R14	0.22	RCWE1206R220FKEA	Vishay	1
R16	10 R	RC0805FR-0710R	Yageo/Phycomp	1
R17, R101	47 k	RC1206FR-0747K	Yageo/Phycomp	2
R18	4.7	AC1206FR-074R7L	Yageo/Phycomp	1
R19	620 k	CRCW0603620KFKEA	Vishay	1
R26, R29, R30	3.9 k/0.5 W	ERJU14F3901U	Panasonic	3
R27, R28	1.0 meg	AC0805FR-071ML	Yageo/Phycomp	2
R31	2.2 k	MCHP03W8F2201T5E	Multicomp	1
R32	36 k	CRCW060336K0FKED	Vishay	1
R33	5.1 k	AC0603FR-075K1L	Yageo/Phycomp	1
R34	47 k	AC0603FR-0747KL	Yageo/Phycomp	1
R36	18 k	AC0603FR-0718KL	Yageo/Phycomp	1
R37	2.2 k	RC0805FR-072K2L	Yageo/Phycomp	1
R100	4.7	AC1206FR-074R7L	Yageo/Phycomp	1
T1	PQ2020; Lp = 544 µH; Np = 58; Ns = 15; Na = 15; N_{sec_aux} = 15	750343265 Rev03	Würth Elektronik	1
X1	250-203	250-203	WAGO	1
X10	250-204	250-204	WAGO	1
ZD1, ZD100	Zener, 15V, 5 percent	BZX384-C15	NXP	2
ZD4, ZD5	Zener, 12V, 5 percent	BZX384-C12	NXP	2
ZD30	Zener, 5.1V, 2.5 percent	DZ2J051M0L	Panasonic	1

Table 7 BOM of adapter board

Designator	Value	Part number	Manufacturer	Quantity
C1	100 n/50 V	C0805C104K5RACTU	Kemet	1
IC101	CDM10V	CDM10V	Infineon	1
JP1	Female, six-pin, 2.54 mm connector	BL5.36Z cut six-pin	Fischer Elektronik	1

7.2 Transformer specifications

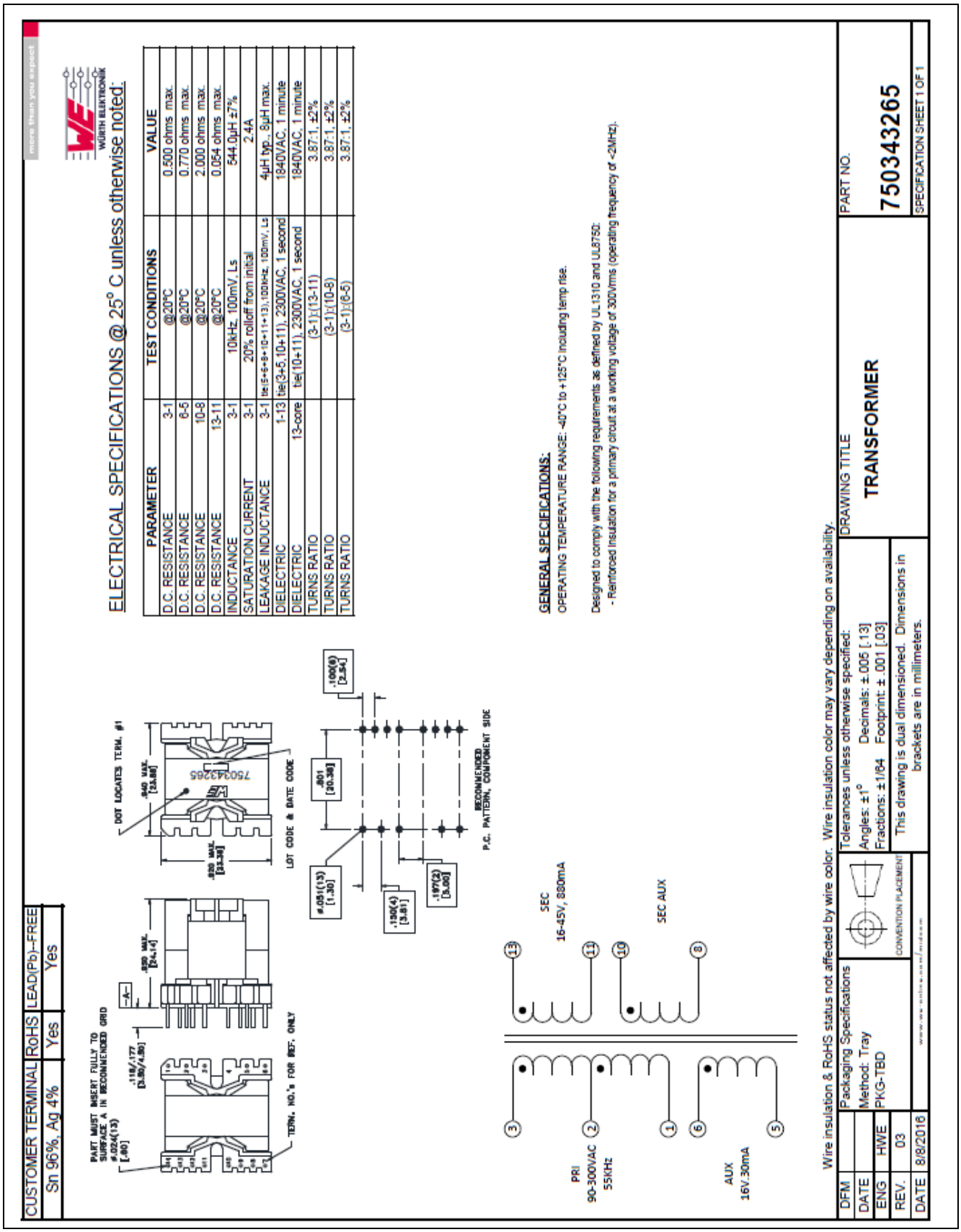


Figure 18 Flyback transformer (T1) specifications

8 Configuration set-up and procedures

8.1 XDPL8105 configuration

The tools needed for XDPL8105 parameter configurations are listed in **Table 8**.

Table 8 Tools needed for XDPL8105 parameter configurations

Tool type	Tool name	Description	Ordering/ download link	Ordering/download content
Hardware	.dp Interface Gen2	.dp Interface board	IF-BOARD.DP-GEN2	.dp Interface Gen2 x 1 USB cable x 1
Software	.dp Vision	GUI for parameter configuration of all .dp products	.dp Vision	Latest version of the .dp Vision installer (*.exe)
	XDPL8105 parameters csv file	XDPL8105 parameters configuration file	XDPL8105 40 W reference board homepage *Note: Please download the zipped package which contains the .dp Vision folder set-up file (*.msi)*	Latest version of .dp Vision folder set-up file (*.msi), which installs the following: XDPL8105 application note and the 40 W reference design parameter configuration file (*.csv), including images for the configuration file. XDPL8105 design tool (*.xlsm) and design tool user guide (*.pdf)

Figure 19 shows the hardware set-up needed between the PC and the configuration connector (J4 of the 40 W reference design) for XDPL8105 parameter configuration.

Note: Please ensure the reference design board is not supplied with any voltage before connecting the programmable cable to the board configuration connector J4.

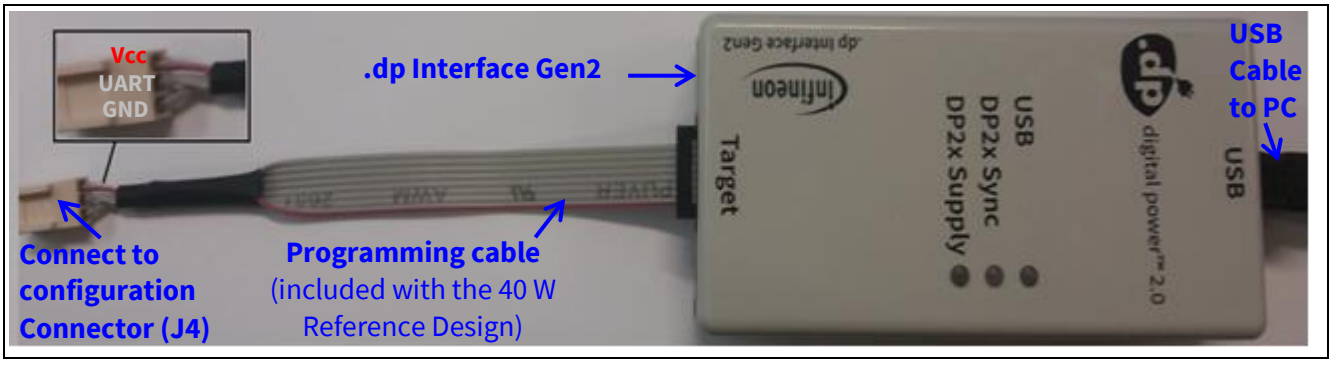


Figure 19 Hardware set-up for XDPL8105 configuration

Please download the latest .dp Vision user manual from this homepage link for detailed instructions on the installation and how to use this GUI for parameter configuration. Alternatively, the following simple guide is also available for quick and easy reference.

For the software tools installation, .dp Vision needs to be installed first before running the XDPL8105 .dp Vision folder set-up file (see **Table 8** for the download links). After setting up the hardware connection for XDPL8105 configuration (see **Figure 19**), please start the program by clicking the shortcut ".dp Vision" on the desktop.

Note: During the program start-up, if the system shows there is a newer version of .dp Vision, please follow the procedure and update accordingly. Since the following screenshots were taken based on .dp Vision version 2.0.8.0, newer versions of .dp Vision might appear different.

Then open the XDPL8105 parameter configuration file (*.csv) from the installation folder of the XDPL8105 project add-on, as shown in **Figure 20**. The default installation folder is located at *C:\Users\<Username>\Infineon Technologies AG\.dp vision\Parameters*

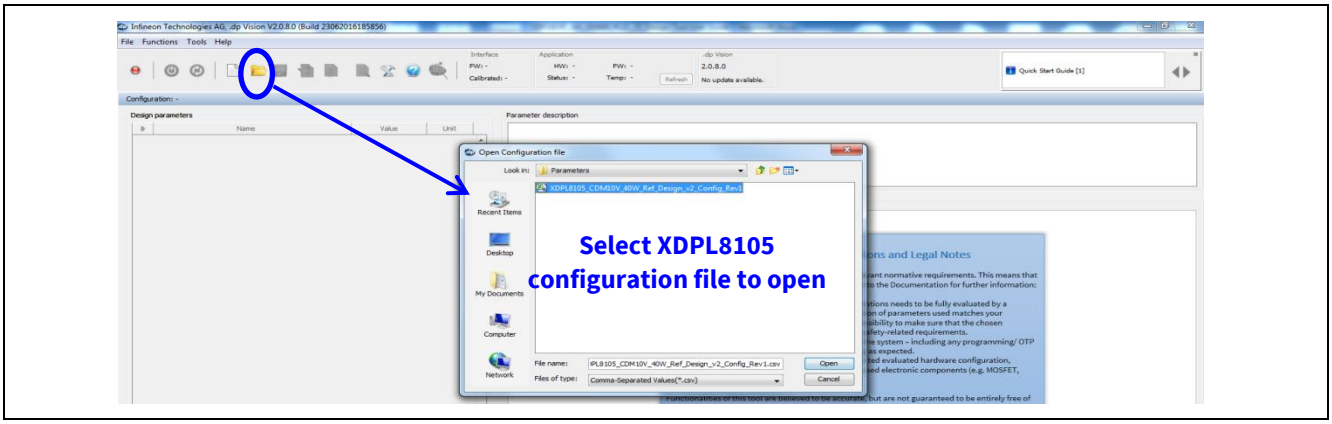


Figure 20 Opening the XDPL8105 parameter configuration file (*.csv) in .dp Vision

After opening the parameter csv file, a list of XDPL8105 configurable parameters will be shown (see the box on the left in **Figure 21**). If a parameter value is changed and no limit violation is found, the changed value itself will turn blue, like the example of changing *I_out_set* parameter from 880 mA to 700 mA in **Figure 21**. Otherwise, if an error is detected (e.g. exceeded min./max. value), the parameter value that caused the error will turn red and the message bar of .dp Vision (see the top right of **Figure 21**) will show an error message.

Note: The user is not allowed to test or burn the configuration if an error is detected.

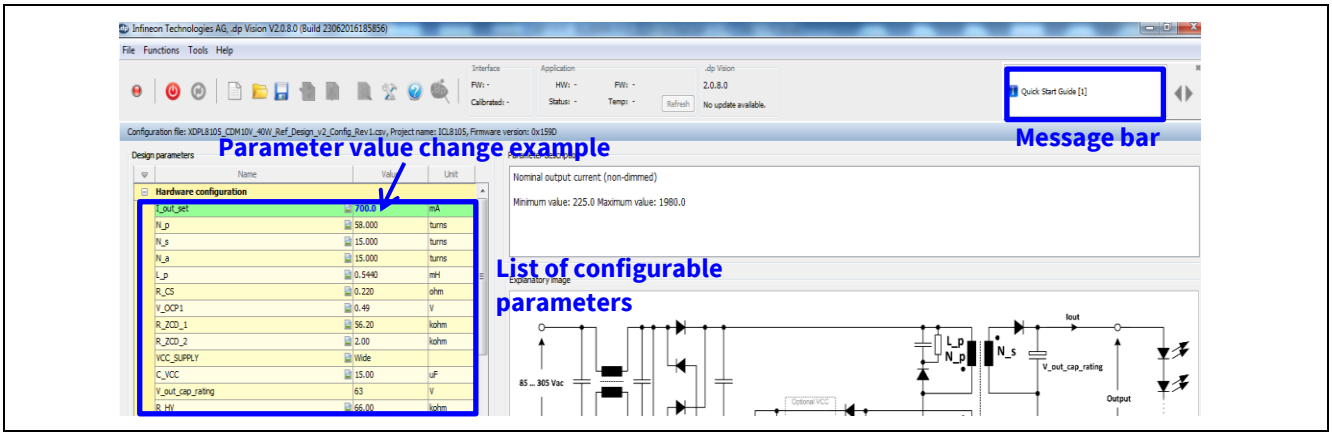


Figure 21 Changing parameter values of XDPL8105 configuration file in .dp Vision

There are two options available to configure the IC based on the list of parameter values shown in .dp Vision.

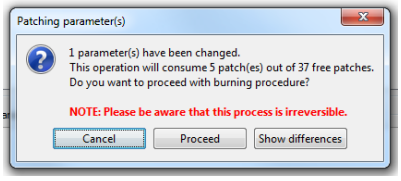
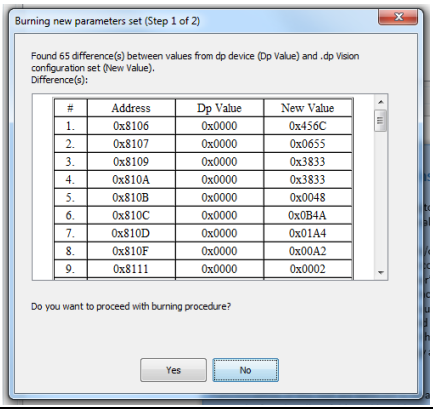
- Burn configuration

  As the XDPL8105 chip on the 40 W reference design PCB has already been permanently burned with a first full set of parameters in its OTP memory space, any parameter value change using this option is considered as parameter patching. The OTP memory space dedicated for patching or burning the parameter value change has a memory size of 77 words.

  Each time the burn configuration function is executed, .dp Vision will detect if there is parameter value difference between the saved configuration file and the target XDPL8105. If a difference is detected, each burn configuration will consume a minimum of three words. However, the process will be aborted if it requires more memory space than is available on the target IC. In that case, the user will have to replace the XDPL8105 chip with a new one in order to burn the configuration. It is important to note that the new XDPL8105 chip from Infineon does not contain any parameters, so the user should burn a first full set of parameters using this function before any application testing.

  Table 9 below shows the recommended procedures for using the burn configuration function in .dp Vision to burn a first full set of parameters or patch the parameters into the OTP memory.

Table 9 Burn configuration procedures

Step	Instruction
I	Open the configuration file using .dp Vision (see example in **Figure 20**).
II	If necessary, change any parameter value (see example in **Figure 21**), then press [File] >> [Save] or [File] >> [Save as] to save the configuration file. Otherwise, proceed to step III.
III	Ensure that the primary supply voltages (e.g. AC input) to the board are switched off or disconnected and the hardware connection for configuration is OK based on **Figure 19**.
IV	Press  to supply power and establish a connection to the target XDPL8105. After this step, the XDPL8105 will be in configuration mode (with V_{CC} voltage for OTP programming at 7.5 V ± 0.15 V) and the device status  should change to  .
V	Press  to burn the configuration to the target XDPL8105. After this step, you should see a pop-up window, which is similar to one of those below.  OR 
VI	Press “Proceed” or “Yes” to burn/patch the configuration. After this step, a pop-up window should show that the burning/patching is successfully completed.
VII	Press “OK” on the pop-up window, then disconnect the programming cable from the XDPL8105 configuration connector and test the application, if needed.

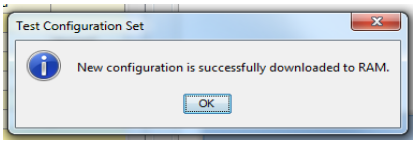
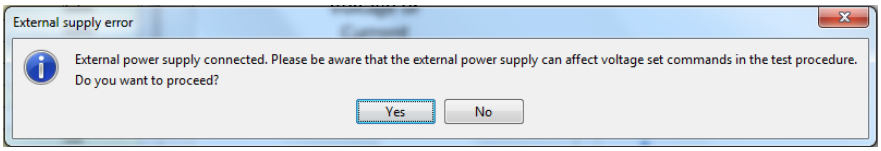
– Test configuration

This function will download the parameter values from the list in .dp Vision into the XDPL8105 RAM memory space. This will then be followed by an automatic IC start-up for application testing with the new configuration.

Unlike using the burn configuration, parameter configuration with this option is not permanent because the loaded RAM contents will be lost once the IC supply voltage is turned off, but the advantage of using this option is that it does not consume OTP memory space, thus there is no limit on the amount of parameter value changes. Please note that this option can only be used to test the application under non-dimming operation because the DIM/UART pin of the XDPL8105 cannot sense the dimming voltage while it is used for UART communication for the test configuration.

Table 10 shows the recommended procedures for using test configuration functions in .dp Vision to load the new parameter values to the RAM and test the application with the new configuration.

Table 10 Test configuration procedures

Step	Instruction
I	Open the configuration file using .dp Vision (see example in **Figure 20**).
II	Ensure that the primary supply voltage (e.g. AC input) to the board is switched off and the hardware connection for configuration is OK based on **Figure 19**.
III	Press to supply power and establish a connection to the target XDPL8105. After this step, the XDPL8105 will be in configuration mode and the device status should change to .
IV	Ensure the LED output is connected to the board and turn on the AC input (e.g. 230 V AC) to the board. After this step, the board does not start up because the XDPL8105 is still in configuration mode.
V	Change the necessary parameter value (see example in **Figure 21**) and press to test the new configuration with the target XDPL8105.
VI	If the IC automatically starts up with the new configuration, you should see a pop-up window like the one shown below. Press “OK” to proceed. 
VII	To test another configuration change, repeat steps II to VI. If the following message box appears in between the steps, press “Yes” to proceed.  Otherwise, turn off the AC input and disconnect the programming cable from the XDPL8105 configuration connector.

Note: If any error is encountered between steps I and VII of either the burn configuration or test configuration procedures, please kindly refer to the message bar of .dp Vision for the error message. For more details, please see the .dp Vision user manual.

8.2 CDM10V configuration

CDM10V configuration requires only a hardware tool, as shown in **Table 11**.

Table 11 Tool needed for CDM10V configuration

Tool type	Tool name	Description	Ordering link	Ordering content
Hardware	COOLDIM_PRG_BOARD	CDM10V programming board	COOLDIM_PRG_BOARD	CDM10V programming board x 1 USB cable x 1 User manual x 1

Figure 22 shows the CDM10V programming board and the hardware connection set-up needed to configure the CDM10V adapter board in this reference design.

*Note: The CDM10V adapter board is normally attached to the 40 W reference design mainboard for the application testing, as shown in **Figure 1**. For CDM10V configuration, the CDM10V adapter board has to be unplugged from the reference design mainboard and connected to the CDM10V programming board connector, as shown in **Figure 22**.*

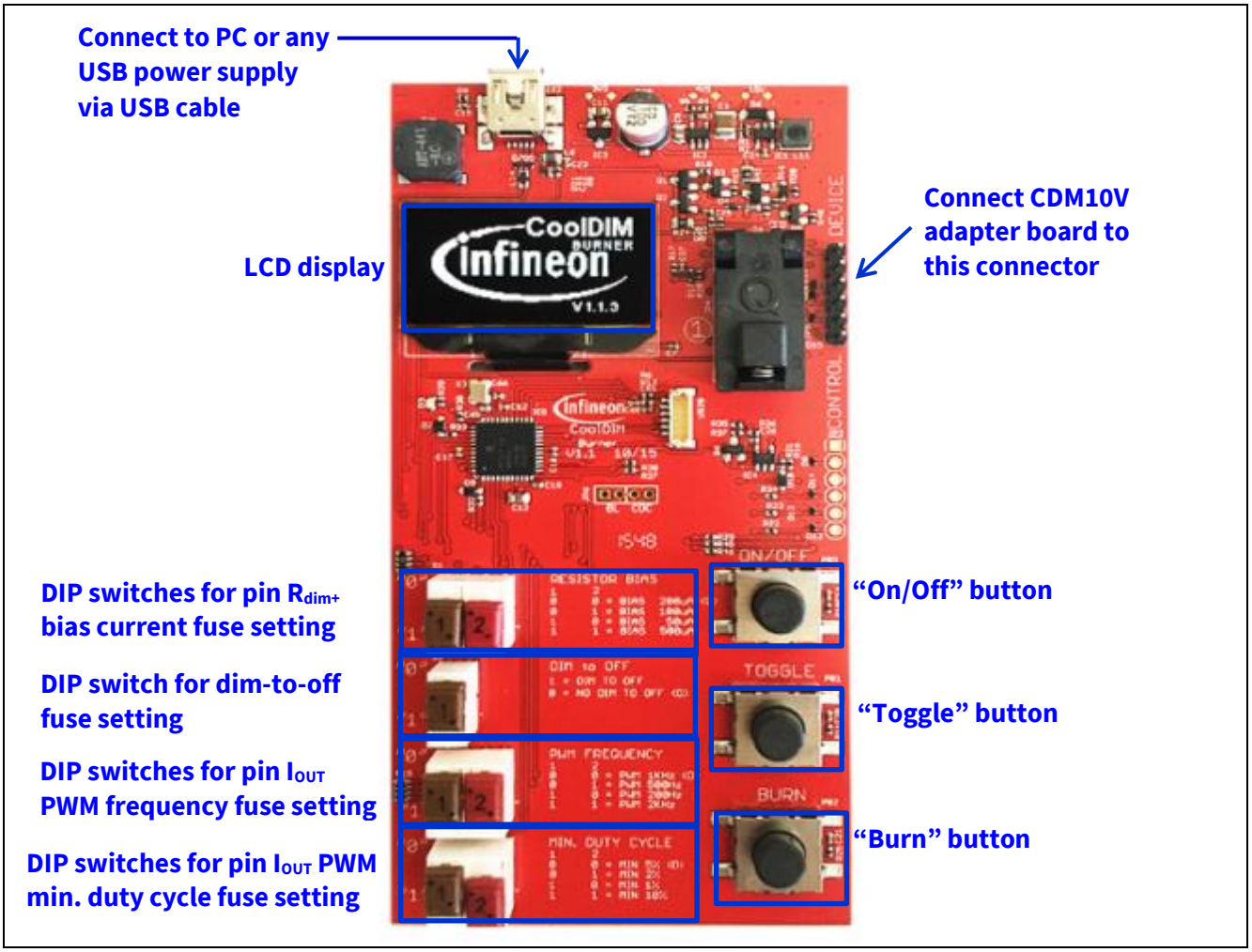


Figure 22 CDM10V programming board and hardware connection set-up for CDM10V configuration

Upon completing the hardware set-up and connection, please refer to **Table 12** below for the recommended procedures on CDM10V configuration or fuse burning.

Table 12 CDM10V configuration or fuse burning procedures

Step	Instruction
I	Press the “On/Off” button to supply voltage and establish connection to the chip. Once the chip is successfully powered up and connected, the setting of all four parameters inside the chip will be read and the chip settings will be displayed on the LCD display (see **Table 3** for the list of parameters).
II	Set the value (0 or 1) on each DIP switch to define each parameter bit setting to be fused, based on **Table 3** or on the description printed on the programming board PCB (beside each switch).
III	Press the “Toggle” button to toggle the LCD display to show either the chip settings or board settings (board settings refer to the parameter settings to be fused, which are decoded based on the values of programming board DIP switches). Ensure the LCD shows the board settings before proceeding to step IV.
IV	Press the “Burn” button to burn the fuse settings in the chip based on the board settings. Please note that the fuse burning will only be started if the board settings differ from the chip settings and if there is at least one bit fusing from “0” to “1” (bit fusing from “1” to “0” is not possible).

Note: If any error is encountered between steps I and IV, the user will be advised by firmware via the LCD on how to proceed. Alternatively, the user can also refer to the user manual for more details on the procedures on error handling. If no button is pressed for 5 minutes or more, the LCD is switched off automatically and the LED below the display will flash once per second. Pressing any button will switch on the display again.

Apart from performing the CDM10V configuration via the adapter board, the programming board also supports configuration of the CDM10V chip alone by using the IC socket, as shown in **Figure 23**.

Figure 23 IC socket on the programming board for CDM10V chip burning

*Note: Pin “1” of the chip should be located in the lower left-hand corner of the open socket, which is marked with a “1” on the PCB, as shown in **Figure 23**.*

9 Customizing your own system design

Figure 24 shows the recommended XDPL8105 system design and optimization process.

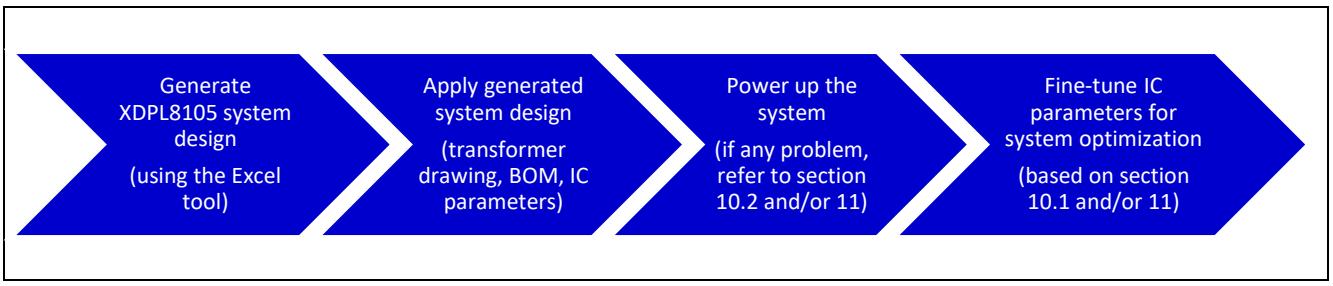


Figure 24 Recommended XDPL8105 system design and optimization process

A customized LED driver design based on the XDPL8105 can be easily achieved using an Excel tool named "XDPL8105 System Simulation & Design Creation Tool" as it is highly interactive, providing design tips and detection of any errors/warnings based on user inputs in each step.

Upon completion of the three main design steps in the Excel tool without any error, the transformer diagram, BOM and IC parameters are automatically generated.

This Excel tool also comes with a user guide document that describes the tool features and also helps the user to understand how to use them for XDPL8105 system design and optimization. Both the Excel tool and the user guide document are included in the XDPL8105 project add-on installer, and the download link is given in **Table 8**.

The default design shown in the Excel tool (when it is first opened) matches the 40 W reference design. Therefore, after creating a customized design based on their own project requirements, the user can simply modify the 40 W reference design according to its differences with the Excel tool's generated transformer, BOM and IC parameters.

Figure 25 shows an example of the auto-generated transformer diagram.

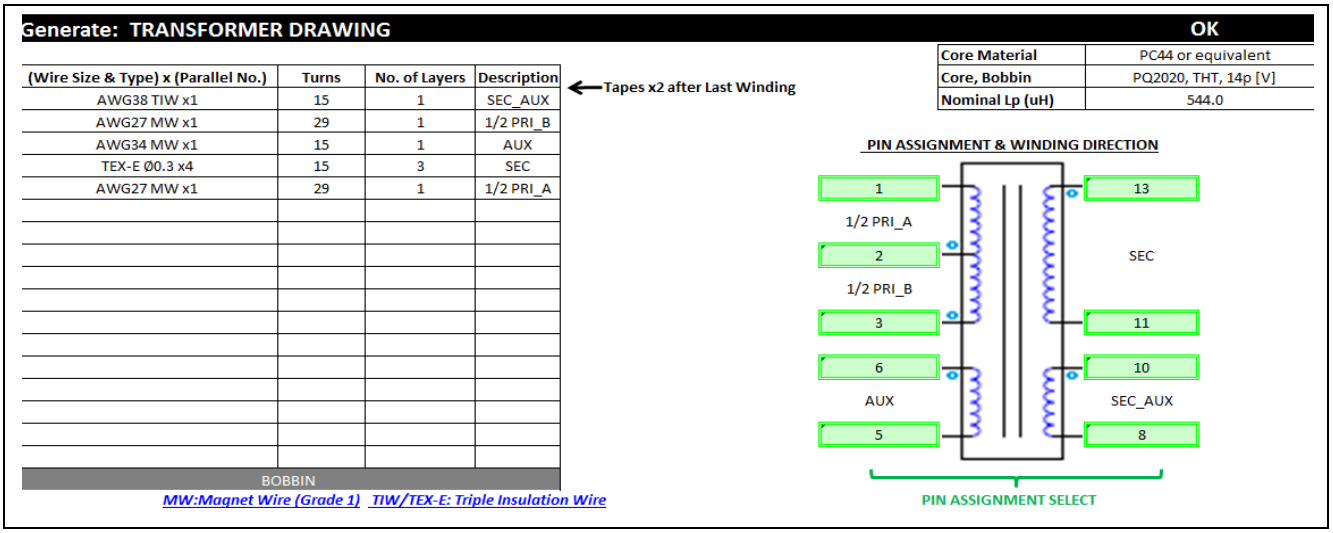


Figure 25 Example of transformer diagram auto-generated with the Excel tool

Figure 26 shows an example of the auto-generated BOM and IC parameters.

Auto-Generated BOM

Note: Based on sheet "SCH" schematic of 40W Ref Design. EMI Line Filter & Bridge not included in this BOM

Schematic Section	Symbol	Value	Rating	Supplier	Part Number/Package
FB_PRI	T1	Lp: 0.544mH; Np: 58; Ns: 15; Naux: 15; Nsec_aux: 15		WURTH	Core, Bobbin: PQ2020, THT, 14p [V]
	IC3	XDPL8105	-	INFINEON	XDPL8105 (DSO-8)
	Q1	IPD80R1K0CE	800V	INFINEON	DPAK
	D3	≥1A	≥800V	DIODES	RS3MB-13-F(SMB)
	D20, D21	1A	600V	FAIRCHILD	ES1J (SMA)
	C3	6800pF	> 378V	ANY	Film cap
	C4	0.22uF	> 498V	ANY	Film cap
	C5	100pF	50V, COG	ANY	SMD Package: 0603
	R2	20kohm	1%	ANY	SMD Package: 0603
	R4+R5+R6	66kohm	1%	ANY	SMD Package:1206 (3 pcs, in series)
	R7+R8	174.8kohm	≤5%	ANY	Power rating: >0.67W
	R10	56.2kohm	1%	ANY	SMD Package: 1206
	R11	2kohm	1%	ANY	SMD Package: 0603
	R14	0.22ohm	1%	ANY	Power rating: >0.12W
	R16	10ohm	1%	ANY	SMD Package: 0805
AUX VCC SUPPLY	Q2	NPN Transistor	Vceo >60V	ANY	Power rating: >0.72W
	D4	≥0.25A	>242V	ANY	BAV103 (SOD-80C)
	D12	0.25A	≥30V	ANY	BAV102 (SOD-80C)
	ZD1	Zener 15V	≤5%	ANY	SOD-323 or similar
	C6	4.7uF	>60V	ANY	Electrolytic Cap
	C8	15uF	≥25V	ANY	E-Cap or SMD1206
	C38	0.1uF	≥25V	ANY	SMD Package: 0603
	R17	47kohm	1%	ANY	SMD Package: 1206
	R18	4.7ohm	1%	ANY	SMD Package: 1206
DIMMING *Secondary 0-10V dimming with CDM10V*	IC30	Schmitt trig. IC	invert out	TI	SN74LVCG14DBVR
	IC100	CDM10V adapter	-	INFINEON	CDM10V adapter board
	PC1	Optocoupler	>4kV, UL	VISHAY	VO617A-2
	Q100	NPN Transistor	Vceo >57	ANY	SOT-89 or larger
	ZD30	Vz=5.1V at 1mA	≤2.5%	ANY	SOD323 or similar
	D100	0.25A	>242V	ANY	BAV103 (SOD-80C)
	D105	Schottky	low leakage	ANY	MMBD301LT1G(SOT23)
	ZD100	Zener 15V	≤5%	ANY	SOD-323 or similar
	C33	0.68uF	16V	ANY	SMD Package: 0603
	C34	4.7uF	25V	ANY	SMD Package: ≥0805
	C35, C36	0.1uF	≥25V	ANY	SMD Package: 0603
	C102	2.2uF	>60V	ANY	Electrolytic Cap
	C103	10uF	25V	ANY	SMD Package: 1206
	R19	620kohm	1%	ANY	SMD Package: 0603
	R31	2.2kohm	1%	ANY	SMD Package: 0603
	R32	36kohm	1%	ANY	SMD Package: 0603
	R33	5.1kohm	1%	ANY	SMD Package: 0603
	R34	47kohm	1%	ANY	SMD Package: 0603
	R36	18kohm	1%	ANY	SMD Package: 0603
	R37	2.2kohm	1%	ANY	SMD Package: 0805
	R100	4.7ohm	1%	ANY	SMD Package: 1206
	R101	47kohm	1%	ANY	SMD Package: 1206
FB_SEC	D6	> 8.1A	> 237V	ONSEMI	MBRB40250TG
	C7	0.1uF	≥70V	ANY	SMD Package: ≥0805
	C12//C13	940uF	63V	ANY	Electrolytic Cap
	C99	OPEN	-	-	-
	R99	OPEN	-	-	-
OUTPUT BLEEDER *Active (Auto-Discharge Circuit)*	Q3, Q4	2N7002	60V	INFINEON	2N7002 (SOT-23)
	D7	Dual Diode	> 237V	INFNEON	BAT240A (SOT-23)
	D8, D9	OPEN	-	-	-
	ZD4, ZD5	Zener 12V	≤5%	ANY	SOD-323 or similar
	C10	1000pF	> 296V	ANY	Discrete or SMD 1206
	C11	0.1uF	≥25V	ANY	SMD Package: 0603
	R26//R29 //R30	1.3kohm	1%	ANY	Power rating > 1W
	R27, R28	1Mohm	1%	ANY	SMD Package: 0805
	R9	OPEN	-	-	-
Y-CAP	C9	2200pF	≥277Vac	ANY	Safety Ceramic Cap
DEBUG/PROGRAMMING	C31	470p	≥25V, COG	ANY	SMD Package: 0603
	J4	3 pins	-	ANY	3 pins (Vcc, Uart, Gnd)
SAFETY & LINE SURGE *(Fuse is mandatory for your safety!)*	F1	UL safety fuse	>0.98A	ANY	-
	MOV1	surge absorber	UL Safety	ANY	Radial, Disc Type
	D1, D2	surge absorber	>216.3V	ANY	Case Style: 1.5KE
	D10	ESD Diode 12V	low leakage	ANY	-
JUMPERS	R1,R50,R51	0ohm	-	ANY	SMD Package: 0603

Auto-Generated IC Parameters

for XDPL8105 csv version: Rev1

Hardware configuration		
I_out_set	880.0	mA
N_p	58	turns
N_s	15	turns
N_a	15	turns
L_p	0.5440	mH
R_CS	0.220	ohm
V_OCP1	0.49 ~ 0.51	V
R_ZCD_1	56.2	kohm
R_ZCD_2	2.00	kohm
VCC_SUPPLY	Wide	
C_VCC	15	uF
V_out_cap rating	63	V
R_HV	66	kohm
I_GD_pk	49	mA
Protections		
t_auto_restart	1.0	s
t_auto_restart_fast	0.4	s
Reaction_OVP_Vout	Auto-Restart	
Speed_OVP_Vout	Slow	
V_outOV	48.4	V
EN_UVP_Vout	Enabled	
t_start_max	10.0	ms
EN_Iout_max_avg	Enabled	
EN_Iout_max_peak	Enabled	
I_out_max_peak	1980	mA
Speed_OCP_Iout	Slow	
EN_UVP_In	Enabled	
EN_OVP_In	Enabled	
V_inOV	329.0	V
V_in_start_max	329.0	V
V_in_start_min	72.0	V
V_inUV	62.0	V
Reaction_VCCP	Latch-Mode	
Debug_Mode	Disabled	
Temperature guard		
T_critical	119	°C
EN_ITP	Enabled	
T_hot	110	°C
I_out_red	220	mA
t_step	10	s
Startup & shutdown		
t_ss	0.50	ms
V_out_dim_min	11.9	V
V_out_start	9.5	V
V_start_OCP1	V_OCP1	V
Control_loop_init	DCM	
f_DCM_init	12	kHz
N_ABM_init	100	
Control loop		
PI_KP_QRM	550	
PI_KI_QRM	8	
PI_KI_DCM	17000	
PI_KI_DCM	200	
PI_KP_ABM	64	
PI_KI_ABM	32	
Dimming		
EN_DIM	Enabled	
V_DIM_min	0.2	V
I_out_dim_min	88.0	mA
C_DIM	Quadratic	
EN_DIM_TO_OFF	Disabled	
V_DIM_off	0.18	V
V_DIM_on	0.19	V
EN_SQW	Disabled	
Multimode		
f_sw_max	180.80	kHz
t_on_max	11.3	us
t_on_min	1.1	us
t_min_demag	3.0	us
f_sw_min_DCM	12.0	kHz
EN_ABM	Disabled	
Power Factor Correction		
C_EMI	0.1000	uF
Fine tuning		
t_ZCDPD	410	ns
t_PDC	200	ns
T_coupling	1.020	
R_in	11.90	ohm
N_DCM_mod_gain	8	
a_DIM	0.000	mV/K

PLEASE FINE TUNE BASED ON APP. NOTE

Figure 26 Example of BOM and IC parameters auto-generated with the Excel tool

Please note that there are a few IC parameters that could not be calculated but require fine-tuning at system level. These parameters are as shown in the green-highlighted cells in the IC parameters table in **Figure 26**. Please refer to **Section 10.1** for the fine-tuning guide.

Also, there are some application-related IC parameters below, which are each generated with an initial default value, instead of dynamically adapted based on the input or output from the preceding design steps. If necessary, the user can adjust each of these following parameter values later in .dp Vision according to the application needs.

For example, the dimming curve parameter *C_DIM* default setting (generated by the Excel tool) is “Quadratic”. If necessary, the user can choose to adjust this setting to “Linear”.

10 XDPL8105 fine-tuning and debugging guide

On successful powering up of the board, whose design is based on the generated BOM and IC parameters from the Excel tool, please refer to **Section 10.1** below for the XDPL8105 fine-tuning guide. If the board has problems powering up or shutting down during testing, please refer to **Section 10.2** for the system debugging guide.

10.1 XDPL8105 fine-tuning guide

This section presents guidelines on how to fine-tune the value of a few XDPL8105 parameters, based on the actual measurement waveform or data.

10.1.1 Input voltage-sensing parameter fine-tuning

When the primary MOSFET is switched on, the XDPL8105 measures the current flowing out of the ZCD ($-I_{IV}$) pin to estimate the input filter capacitor voltage (V_{IN}) based on the following equation.

$$V_{IN} = \frac{N_p}{N_a} \times \left[\left(-I_{IV} - \frac{V_{INPCLN}}{R_{ZCD_2}} \right) \times R_{ZCD_1} - V_{INPCLN} \right]$$

Note: V_{INPCLN} is a negative voltage clamped to pin ZCD, which is approximately -180 mV.

Ideally, V_{IN} should be a low-frequency (typically 100~120 Hz) rectified sinusoidal waveform, as shown in **Figure 27**, while the AC input rms value can be approximated as $V_{IN\_PEAK}/\sqrt{2}$. However, due to the input-line filter impedance and the filter capacitor Equivalent Series Resistor (ESR), the actual V_{IN} has a high-frequency switching ripple (in the kHz range) over the low-frequency sinusoidal waveform, whose ripple level varies based on the peak current being drawn by the transformer primary winding. Step III of **Table 13** shows an example of the actual V_{IN} waveform.

To achieve high accuracy in sensing the input voltage, parameter *R_in* fine-tuning is important for the XDPL8105 to estimate the correct V_{IN_PEAK} by compensating for such high-frequency ripples, which appears in $-I_{IV}$ measurements as well.

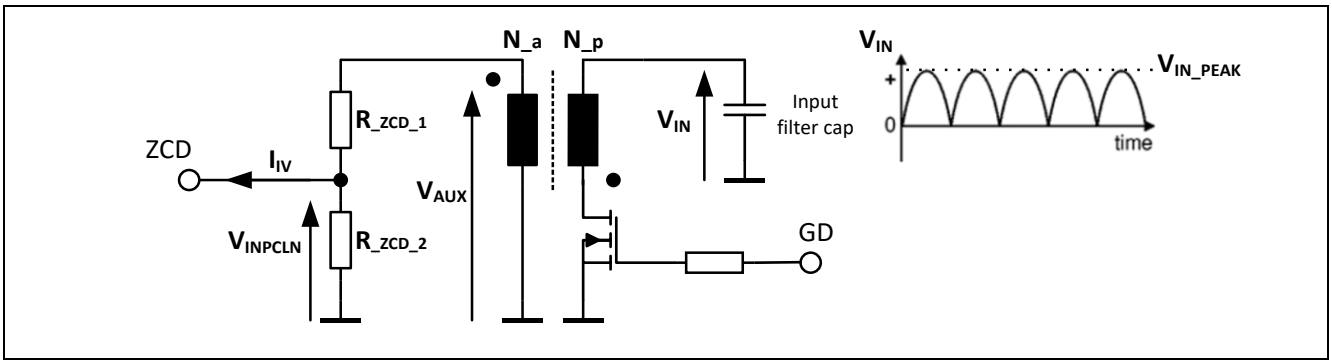
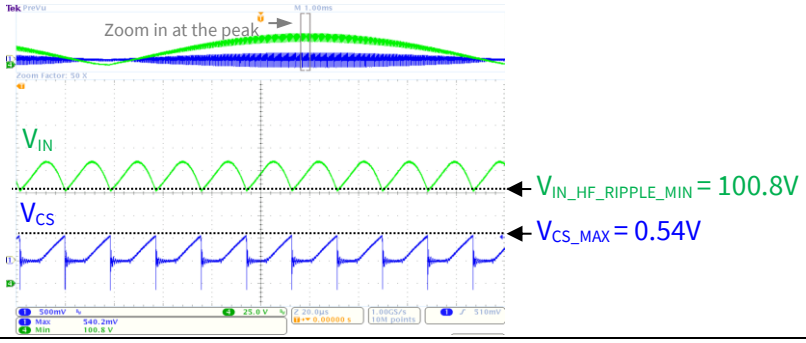


Figure 27 $-I_{IV}$ measurement for input voltage sensing

Table 13 shows the recommended procedures for parameter *R_in* fine-tuning.

Table 13 Recommended procedures for parameter *R_in* fine-tuning

Step	Instruction
I	Apply two voltage probes on the board, which measure the waveform of the input filter capacitor voltage (V_{IN}) and current sense resistor voltage (V_{CS}) respectively.
II	Ensure the target XDPL8105 has already been burned with at least a first full set of parameters. Power up the board in normal operation with minimum AC input rms voltage (V_{AC_min}) and maximum output LED voltage (V_{o_max}) under non-dimming conditions. If it cannot be powered up, please retry by burning the input UVP parameter *EN_UVP_IN* to "Disabled" (if it was not before) or refer to **Section 10.2** for a debugging guide.
III	Capture the voltage waveforms with a time base of 1 ms and zoom into the peak voltage for measuring the minimum level of the V_{IN} high-frequency voltage ripple ($V_{IN\_HF\_RIPPLE\_MIN}$) and the maximum level of V_{CS} (V_{CS_MAX}). Below is an example of a waveform captured on the 40 W reference design with V_{AC_min} = 90 V AC at 60 Hz and V_{o_max} = 45 V with non-dimming. 
IV	Turn off the AC input. Calculate R1 with the equation below and voltage measurements from step III: $R1 = R\_CS \times \left(\frac{V_{AC\_min} \times \sqrt{2} - V_{IN\_HF\_RIPPLE\_MIN}}{V_{CS\_MAX}}\right)$, based on V_{o_max} with non-dimming I_{OUT}. Calculation example based on 40 W reference design: $R1 = 0.22 \times \left(\frac{90 \times \sqrt{2} - 100.8}{0.54}\right) = 10.76\ \Omega$
V	Repeat steps II to III by changing the load to the minimum output LED voltage (V_{o_min}) to obtain the measurements of $V_{IN\_HF\_RIPPLE\_MIN}$ and V_{CS_MAX}, which are based on V_{o_min}.
VI	Turn off the AC input. Calculate R2 with the equation below and voltage measurements from step V: $R2 = R\_CS \times \left(\frac{V_{AC\_min} \times \sqrt{2} - V_{IN\_HF\_RIPPLE\_MIN}}{V_{CS\_MAX}}\right)$, based on V_{o_min} with non-dimming I_{OUT}. Calculation example based on 40 W reference design: $R2 = 0.22 \times \left(\frac{90 \times \sqrt{2} - 112.8}{0.33}\right) = 9.64\ \Omega$
VII	Calculate the parameter *R_in* with the following equation: $R\_in = 0.5 \times (R1 + R2) + R_{ds(on),FET} + R_{dc,pri\ winding} + R\_CS$ $R_{ds(on),FET}$ is the MOSFET $R_{ds(on)}$ and $R_{dc,pri\ winding}$ is the primary winding DC resistance. Calculation example based on 40 W reference design: $R\_in = 0.5 \times (10.76 + 9.64) + 1 + 0.5 + 0.22 \approx 11.9\ \Omega$
VIII	Use a burning configuration to patch the parameter *R_in* with the value from step VII and parameter *EN_UVP_IN* with "Enabled" (if it was set to "Disabled" before). Then, verify the AC input UV accuracy.

10.1.2 QR valley switching parameter fine-tuning

Unlike conventional analog solutions which achieve QR valley switching by introducing an external hardware delay on the zero-crossing signal with the ZCD pin capacitor, the XDPL8105 ZCD pin capacitor is only used for noise filtering. Therefore, a fixed capacitor value (e.g. 47 pF~100 pF) can be used across all designs with different power classes. To achieve QR valley switching, the XDPL8105 dynamically measures the LC resonant period and delays the MOSFET switch-on by a quarter of the resonant period after zero-crossing of the auxiliary winding voltage. This method gives the XDPL8105 the advantage of achieving not only excellent line and load regulation, but also tight output tolerance in mass production.

Parameter *t_ZCDPD* fine-tuning is, however, necessary to compensate for XDPL8105 internal propagation delay in ZCD and also external delay caused by the noise-filtering capacitor at the ZCD pin. **Table 14** shows the recommended procedures for parameter *t_ZCDPD* fine-tuning.

Table 14 Recommended procedures for parameter *t_ZCDPD* fine-tuning

Step	Instruction
I	Apply a differential probe on the board to measure the Flyback MOSFET drain voltage waveform.
II	Set parameter *t_ZCDPD* to 0 and use the test configuration function in .dp Vision to power up the board with typical AC input rms voltage (V_{AC_typ}) – e.g. 230 V AC and maximum output LED voltage (V_{o_max}) under non-dimming conditions. If the board cannot be powered up, please refer to **Section 10.2** for a debugging guide.
III	Capture the waveform with a 1 ms time base and zoom into the voltage peak with a 1 µs time base.
IV	Place a horizontal cursor at the highest possible level which crosses two points on the resonance part of the waveform (see a and b, below) and measure the time between them (t_{a-b}). In the example below, which is based on the 40 W reference design, t_{a-b} is measured to be approximately 820 ns. 
V	Set the parameter *t_ZCDPD* as half of t_{a-b} and burn the configuration.
VI	Power up the board and the Flyback MOSFET drain voltage waveform should be switching at the QR valley (see the example below based on the 40 W reference design with *t_ZCDPD* = 410 ns). 

10.1.3 Output current regulation parameter fine-tuning

Please note that QR valley switching parameter (*t_ZCDPD*) fine-tuning in **Section 10.1.2** should be done before output regulation parameter (*t_PDC, T_coupling*) fine-tuning.

The parameter *t_PDC* is used to compensate for the propagation delay from one end of the XDPL8105 pin GD gate pulse until the MOSFET drain current reaches zero, so that the accurate primary peak current can be estimated for better output regulation against input voltage variation.

Parameter *T_coupling* is to compensate for the non-ideal transformer primary-to-secondary peak current transfer ratio, so that the actual output current measurement matches the output current set-point parameter, *I_out_set*. Parameter *t_PDC* should be fine-tuned before *T_coupling*.

Table 15 shows the recommended procedures for *t_PDC* and *T_coupling* parameter fine-tuning.

Table 15 Recommended procedures for t_PDC and T_coupling parameter fine-tuning

Step	Instruction
I	Set the parameter *t_PDC* = 150 ns, *T_coupling* = 1 and test configuration using .dp Vision to power up the board and measure its output current in normal operation with the different conditions shown below: • Maximum AC input rms voltage (V_{AC_max}) and maximum output LED voltage (V_{o_max}) • Minimum AC input rms voltage (V_{AC_min}) and maximum output LED voltage (V_{o_max}) • Maximum AC input rms voltage (V_{AC_max}) and minimum output LED voltage (V_{o_min}) • Minimum AC input rms voltage (V_{AC_min}) and minimum output LED voltage (V_{o_min}) Please ensure there is no voltage probe connected to the board during the measurement. If it cannot be powered up in any condition above, please refer to **Section 10.2** for a debugging guide.
II	Calculate the total line, load regulation percentage based on the following equation: $\Delta I_{out} = \pm \left(\frac{I_{out\_max} - I_{out\_min}}{I_{out\_max} + I_{out\_min}} \times 100\ percent \right)$ Where: I_{out_min} is the minimum output current measured in the different conditions shown in step I I_{out_max} is the maximum output current measured in the different conditions shown in step I
III	Repeat steps I to II with the parameter *t_PDC* = 200, 250, 300 and 350 ns to select the best *t_PDC* value which gives the lowest ΔI_{out}.
IV	Calculate *T_coupling* based on the following equation: $T_{\_coupling} = 2 - \frac{2 \times I_{\_out\_set}}{I_{out\_max} + I_{out\_min}}$ Where: I_{out_min} is the minimum output current measured in step I with the best *t_PDC* value I_{out_max} is the maximum output current measured in step I with the best *t_PDC* value $I_{\_out\_set}$ is the non-dimmed output current parameter setting in the XDPL8105 configuration
V	Burn the configuration to the target XDPL8105 with the best *t_PDC* value selected in step III and the *T_coupling* value calculated in step IV.

10.1.4 Control loop and light quality-related parameter fine-tuning

The XDPL8105 uses a Proportional-Integral (PI) regulator as the control loop for its primary-side output current regulation, and thus the control loop response is determined by the proportional gain parameter (*Kp*) and integral gain parameter (*Ki*) of the regulator.

Based on the input voltage, output load voltage and dimming input conditions, the controller will autonomously decide to operate in either Quasi-Resonant Mode (QRM), DCM or ABM. For each operating mode, there is a dedicated set of control loop response parameters (*Kp*, *Ki*) and also the PI regulator output is different: on-time control for QRM, period control for DCM and pulse number control for ABM.

In most cases, the default values of parameters *Kp*, *Ki* generated by the Excel tool should be sufficient to deliver a satisfactory control loop response. If necessary, the user can also try to improve the control loop response by adjusting these parameter values, but it is important to be aware of the possible side-effects. **Table 16** shows the effects of increasing the values of parameters *Kp* and *Ki* respectively.

Table 16 Effects of increasing the values of parameters *Kp* and *Ki*

Parameter	Output rise time	Output overshoot	Output settling time	Output stability
Kp	Decrease	Increase	Small change	Degrade
Ki	Decrease	Increase	Increase	Degrade

Note: The effects of decreasing the values of the parameters Kp and Ki will be the opposite of what is shown in the table above.

To improve the light quality issue caused by the DCM hard-switching when the output is being dimmed, the DCM period control output by the PI regulator is being modulated. The modulation gain is controlled by the value of the parameter *N_DCM_MOD_GAIN*, based on **Table 17**.

Table 17 Modulation gain based on the value of parameter *N_DCM_MOD_GAIN*

	Parameter *N_DCM_MOD_GAIN* value				
	0	4	8	16	32
Modulation gain	None	Maximum	High	Medium	Minimum

The medium to maximum modulation gain typically gives the best light quality in DCM operation. Please choose the best setting based on the light quality of the actual dimming test result. Please also ensure that no voltage probe (except a differential probe) is connected to the primary-side circuit of the board while doing the light quality test.

10.1.5 Input power quality-related parameter fine-tuning

The PF can be enhanced by configuring the parameter *C_EMI* above zero and fine-tuning the value to compensate for the current shape and phase-shifting effect, which is mainly caused by the input filter capacitor. Higher *C_EMI* gives higher compensation, and vice-versa.

The default value of the parameter *C_EMI* generated by the Excel tool is 0.1 µF. If necessary, please fine-tune *C_EMI* using the test configuration in .dp Vision to achieve the optimized power factor and iTHD. Otherwise, it can also be set to zero if PF enhancement is not desired.

It is also possible to improve iTHD, especially at high input voltages, by reducing the values of the parameter *f_sw_max* or *N_DCM_MOD_GAIN* (except 0). However, please note that the efficiency could be impacted because of the increasing number of switching cycles (over the rectified input sine-wave period) which are unable to switch on the MOSFET at the QRM first valley.

*Note: If the parameter N_DCM_MOD_GAIN setting is above 0, the QRM maximum switching frequency is not constant (based on the parameter f_sw_max setting) but is modulated based on the rectified input sine wave phase angle. The gain of modulation is based on the parameter N_DCM_MOD_GAIN setting, as shown in **Table 17**.*

Please also ensure the dimming light quality remains good after any of these parameter values changes. If necessary, the designer can use the Excel tool to simulate the primary average input current current curve for iTHD optimization based on the parameter *f_sw_max* or *N_DCM_MOD_GAIN* value changes. For more details, please refer to the Excel tool user guide.

10.2 XDPL8105 debugging guide

This section presents guidelines on system debugging and troubleshooting if the board has any problem with powering up or shutting down during testing.

10.2.1 Pin GD and V_{CC} signal debugging

Scenario 1: If the V_{CC} stays above the turn-off threshold, e.g. 6 V, and the GD pin signal restarts with an interval based on the configured parameter *t_auto_restart*, it means the controller has encountered system protection with auto-restart reaction. See waveform examples in **Figure 28**.

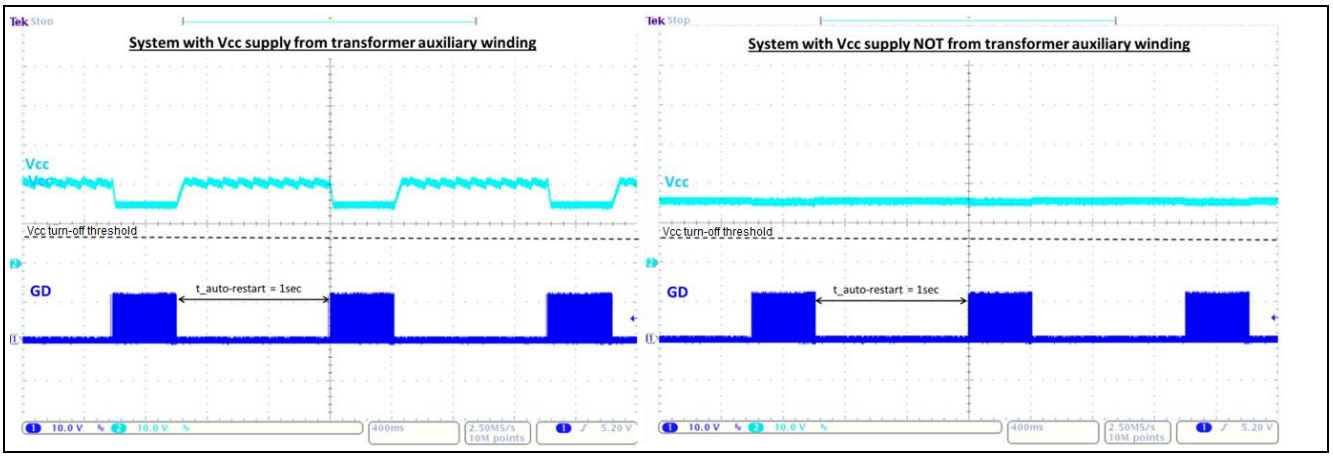


Figure 28 Waveform examples of system protection with auto-restart reaction

Scenario 2: If the V_{CC} stays above the turn-off threshold e.g. 6 V and the GD pin signal restarts with an interval based on the configured parameter *t_auto_restart_fast*, it means the controller has encountered either a system protection function with fast auto-restart reaction or dim-to-off operation (if the parameter *EN_DIM_TO_OFF* is set to “Enabled”). See waveform examples in **Figure 29**.

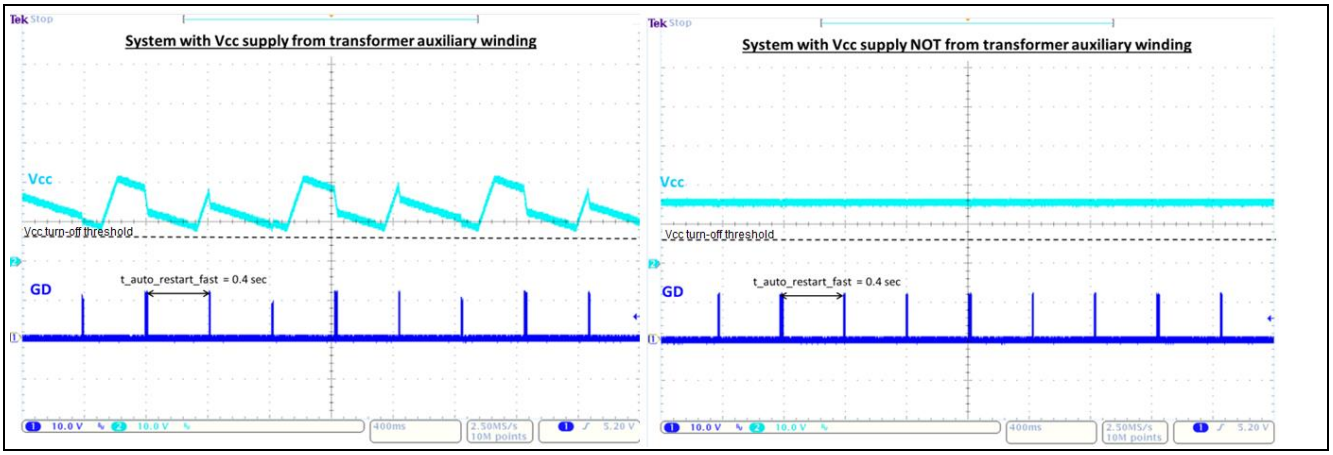


Figure 29 Waveform examples of system protection or dim-to-off with fast auto-restart reaction

In such cases, the user can burn a configuration with the parameter *EN_DIM_TO_OFF* set to “Disabled” (if the parameter *EN_DIM_TO_OFF* was set to “Enabled” before) and retest the board. If the problem of powering up or shutting down persists, it means the controller has previously encountered system protection. If the problem of powering up or shutting down disappears, it means the controller was previously in dim-to-off operation.

Scenario 3: If the GD pin signal stays low while V_{CC} stays above the turn-off threshold, e.g. 6 V, it means the controller has entered a protection state with latch-mode reaction or the configuration mode. See waveform examples in **Figure 30**.

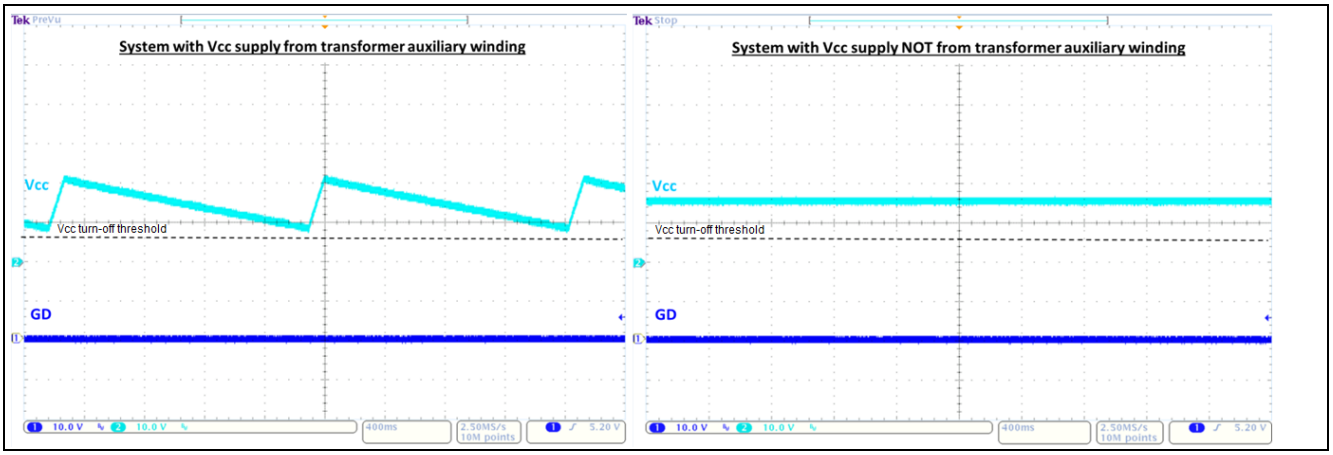


Figure 30 Waveform examples of configuration mode or system protection with latch-mode reaction

To ensure the system is not in configuration mode, please check the following:

- Always burn the first full set of parameters to the target XDPL8105 before powering up.
- Disconnect the interface board before powering up the board. The most common example of false entry to the configuration mode is to power up the board while it is connected to the .dp Interface Gen2 (with the“DP2x supply” or/and “DP2x Sync” LEDs on). If that is the case, the measured waveform will be similar to the waveform example on the right of **Figure 30**, but with a V_{CC} level of approximately 7.5 V.

Scenario 4: If the V_{CC} hits the turn-off threshold, e.g. 6 V, the IC will restart with a hardware reset using an interval based on the $V_{VCC(ON)}$ charge-up time. The typical $V_{VCC(ON)}$ level is 20.5 V. See the waveform example in **Figure 31**.

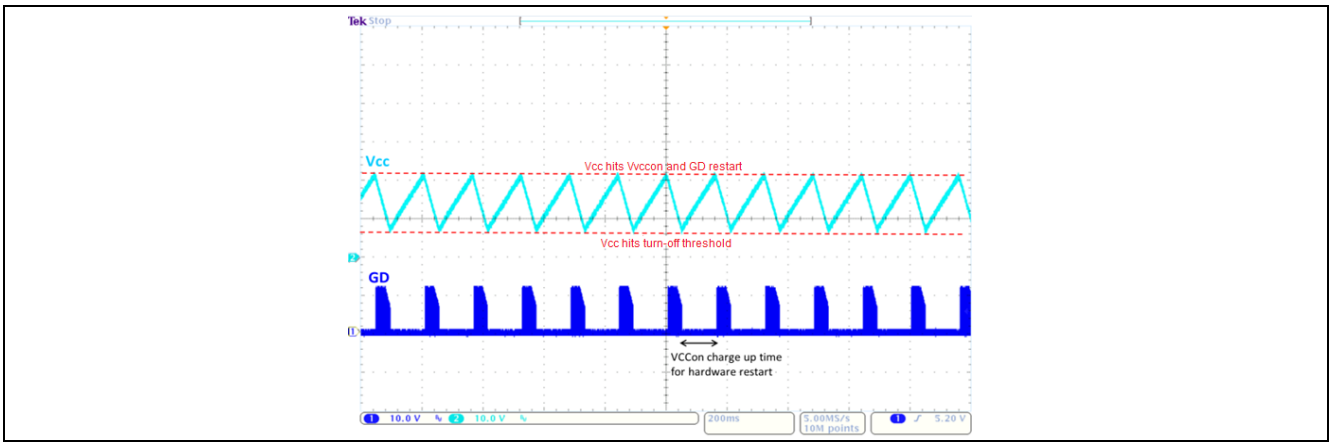


Figure 31 Waveform example of system with problems with V_{CC} supply

For scenario 4, please check your design based on the Excel tool and apply the necessary countermeasure to the V_{CC} supply circuitry and/or start-up-related parameters. Please also ensure that the parameter *Debug_mode* is configured to "disabled" so that the corresponding protection reaction which has been predefined or configured can take place and results in either scenario 1, 2 or 3 if any protection has been triggered.

For the user's easy reference, **Table 18** and **Table 19** show a summary of waveform scenarios for system protections with predefined reaction and configurable reaction respectively.

Table 18 Summary of waveform scenarios for system protection with predefined reaction

System protection	Predefined reaction	Restart interval	Waveform scenario
UV protection for V_{out}	Auto-restart	*t_auto_restart*	Scenario 1
Start-up UV protection for V_{out}			
UV protection for V_{in}			
Firmware protections (first watchdog and RAM parity)			
OV protection for V_{in}	Latch mode	Not applicable	Scenario 3
Input over-current protection level 2			
Over-temperature protection			
Under-Voltage Lockout (UVLO) of V_{CC}	Hardware restart	$V_{VCC(ON)}$ charge-up time	Scenario 4

Table 19 Summary of waveform scenarios for system protection with configurable reaction

System protection	Configurable reaction	Restart interval	Waveform scenario
OVP for V_{out}	Auto-restart[1]	*t_auto_restart*	Scenario 1
	Fast auto-restart[1]	*t_auto_restart_fast*	Scenario 2

[1] Configurable based on parameter *Speed_OVP_Vout* setting(Slow or Fast) when parameter *Reaction_OVP_Vout* is set to "Auto-Restart".

	Latch mode	Not applicable	Scenario 3
Output over-current protection	Auto-restart[1]	*t_auto_restart*	Scenario 1
	Fast auto-restart[1]	*t_auto_restart_fast*	Scenario 2
OVP for V_{CC}	Auto-restart	*t_auto_restart*	Scenario 1
	Latch mode	Not applicable	Scenario 3

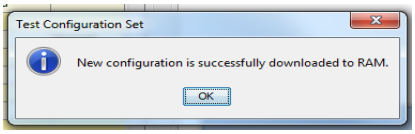
10.2.2 Debug mode

For system debugging, the user can also activate the debug mode in the XDPL8105 to read out the firmware status code. If any protection is triggered in the debug mode, the IC's GD pin stops switching and the DIM/UART pin will only function as the UART communication interface so the error code can be read out.

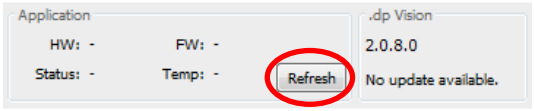
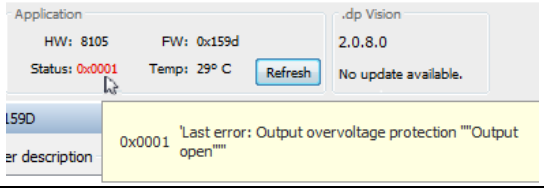
*Note: Parameter Debug_mode should only be enabled for debugging purposes along with the configuration set-up connection shown in **Figure 19**. For board testing on its own without connecting the .dp Interface Gen2, please ensure the parameter Debug_mode is set to disabled.*

Table 20 shows the recommended procedures for firmware status code read-out in debug mode.

Table 20 Recommended procedures for firmware status code read-out in debug mode

Step	Instruction
I	Open the configuration file (see the example in **Figure 20**) used in the system which has entered an unexpected protection state and set the parameter *Debug_mode* to "Enabled".
II	Ensure that the AC input to the board is switched off, that nothing is externally directly connected to the DIM/UART pin and that the hardware connection for the configuration is now connected as shown in **Figure 19**.
III	Press  to supply power and establish connection to the target XDPL8105. After this step, the XDPL8105 will be in configuration mode and the device status  should change to  .
IV	Supply the board with AC input and LED output conditons which trigger the protection. After this step, the board does not start up because the XDPL8105 is still in configuration mode.
V	Press  to test the configuration with the target XDPL8105. After this step, the IC will automatically start up in debug mode with non-dimming operation and you should see a pop-up window like the one shown below.  If any protection is triggered, the IC's GD pin will stop switching and there will be no light output.
VI	Press "OK" in the pop-up window.
VII	Press the "Refresh" button in the .dp Vision application section (as shown below) and switch off the AC input. After this step, the firmware status code is read out. If any protection has been triggered after step V, the status code will show a value in red. Otherwise, it will show 0x0000 in black.

[1] Configurable based on parameter *Speed_OCP_Iout* setting (Slow or Fast).

	
VIII	Hover the mouse over the status code (as shown below) and the description of the status code will be shown. For example, 0x0001 means output OVP. 
IX	Apply the necessary countermeasure or repeat the steps above to debug again. Otherwise, ensure the AC input is switched off before disconnecting the programming cable from the XDPL8105 board configuration connector.

11 Frequently asked questions

This section lists frequently asked questions.

11.1 Does the XDPL8105 support dim-to-off?

Yes, but it requires an active voltage source to exit the dim-to-off state. **Figure 32** shows an application example in which the XDPL8105 can support the dim-to-off feature because the DIM/UART pin has an active voltage source from a primary-side microcontroller.

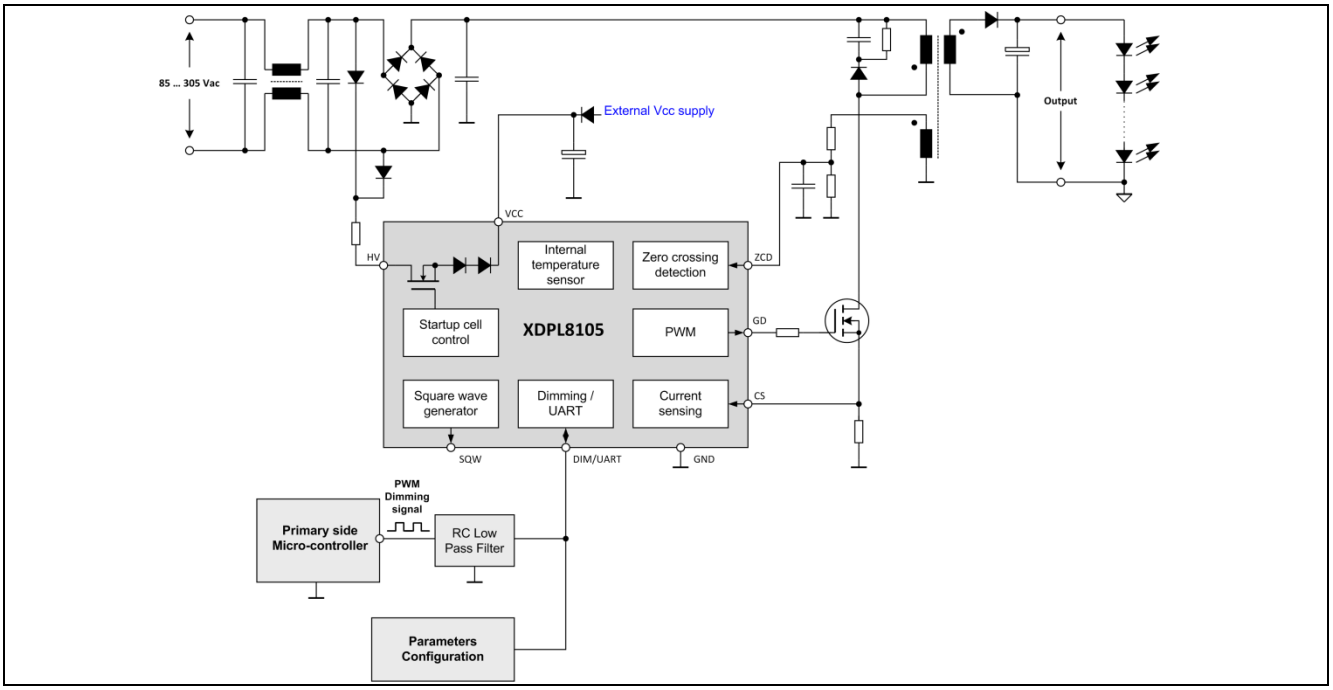


Figure 32 Application example in which XDPL8105 can support dim-to-off

Figure 33 shows an application example in which the XDPL8105 cannot support the dim-to-off feature because the secondary side 0 to 10 V dimmer is a passive voltage source.

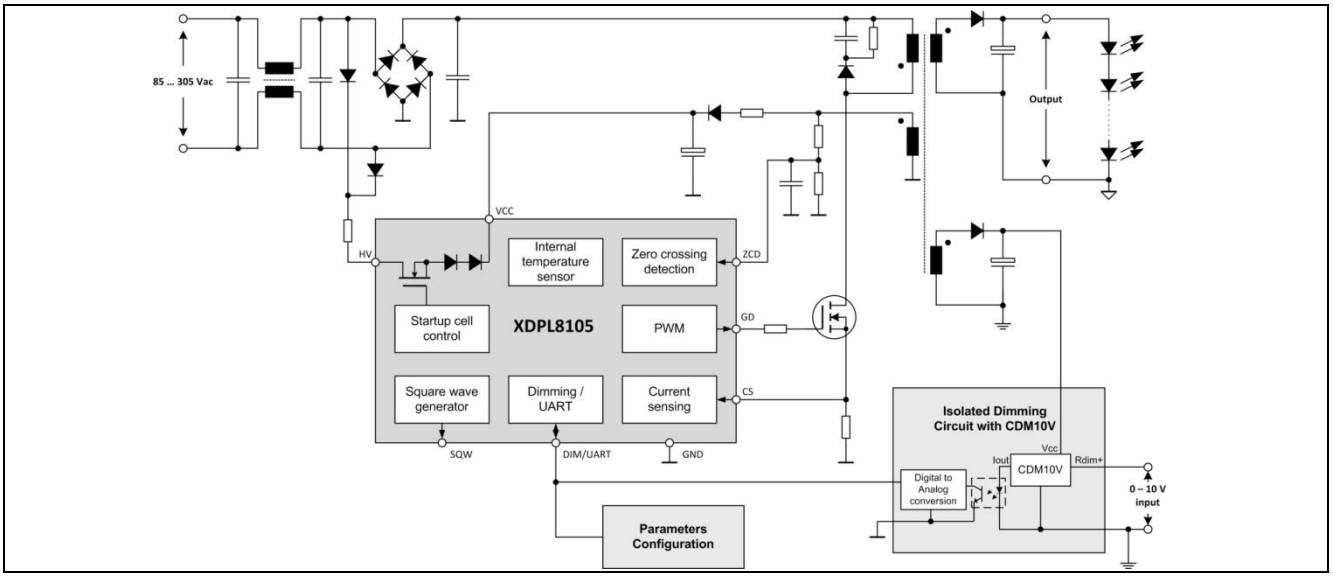


Figure 33 Application example in which XDPL8105 cannot support dim-to-off

11.2 What is the lowest possible output current with minimum dimming input?

The target output current with the minimum dimming input is based on the XDPL8105 parameter *I_out_dim_min* setting and can be configured to be as low as 10 mA. It is, however, important to note that the lower the *I_out_dim_min* value is set, the more difficult it is to achieve both good output current accuracy and short time-to-light with the minimum dimming input.

11.3 Why is the actual output current with minimum dimming input much higher than the parameter *I_out_dim_min* setting (at maximum AC input voltage and minimum LED load voltage)?

If the output current with the minimum dimming input is much higher with maximum AC input voltage and minimum LED load voltage when compared to other input-output conditions, the system has most likely reached a limit where the controller cannot reduce the output power transfer any more, based on the transformer design, controller operating mode configuration and testing conditions. As a result, the output current with the minimum dimming input cannot be properly regulated according to the target *I_out_dim_min* setting.

Therefore, it is strongly recommended to use the Excel tool to first estimate the output current with the minimum dimming input under the worst-case conditions (maximum input voltage, minimum LED voltage), before selecting the transformer design (e.g. inductance, turns ratio) and initial IC parameterization (e.g. *f_sw_min_DCM* setting).

To have reasonably good output regulation with the minimum dimming input, the actual minimum output current measurement under the worst-case conditions above should be the same or reasonably close to the *I_out_dim_min* setting. As the Excel tool only provides an estimation, the minimum output in an actual measurement could still be higher than the *I_out_dim_min* setting. In such cases, the user can further optimize the design by fine-tuning IC parameters, such as lowering the parameter *f_sw_min_DCM* setting.

Note: The parameter f_sw_min_DCM refers to the minimum DCM switching frequency.

11.4 What causes the longer time-to-light with minimum dimming input?

Primary-Side Regulation (PSR) constant current controllers, such as the XDPL8105, basically regulate the secondary output winding current, instead of the output LED current itself.

At the initial start-up stage, all secondary output winding current first flows into the output capacitor. On charging the output capacitor to the output LEDs' turn-on threshold voltage, more secondary output winding current will flow into the LED as the output capacitor voltage continues to be charged up, but at a slower rate. The steady-state is reached when all secondary output winding current flows to the LEDs.

To prevent output current overshoot during start-up, the XDPL8105 starts regulating the secondary output winding current based on the DIM/UART pin's voltage, from the initial start-up stage until the steady-state. As a result, the time-to-light with the minimum dimming input is longer than for non-dimming because the output capacitor takes more time to be charged up with the smaller regulated output current with the minimum dimming input. Therefore, the worst-case start-up time (time-to-light) always happens with the minimum AC input voltage, and maximum output LED voltage with the minimum dimming input.

11.5 How can time-to-light with minimum dimming input be improved?

There are a few possible options, but each comes with a certain trade-off or limit.

- Reduce the output capacitance, but the output current ripple will increase.
- Reduce the V_{CC} capacitance, but if reduced too much, the V_{CC} could hit UVLO during start-up and result in start-up problems or even longer start-up times.
- Reduce the HV pin's series resistor, but there is a limit based on the maximum input voltage.
- Increase the value of the parameter *I_out_dim_min*, but the output current for minimum dimming input will be higher.
- Increase the value of the parameter *V_out_start*, but it could result in output overshoot.
- Increase the value of the parameter *N_ABM_init* or *f_DCM_init*, but it could result in output overshoot.

Note: The parameter N_ABM_init is only effective if parameter control_loop_init is set to "ABM", while the parameter f_DCM_init is only effective if parameter control_loop_init is set to "DCM".

Therefore, it is strongly recommended to use the Excel tool to obtain an initial design of the board components (e.g. V_{CC} capacitance, output capacitance) and IC parameters (e.g. *I_out_dim_min* setting), based on the balanced performance of the estimated worst-case start-up time (time-to-light) and estimated maximum output ripple.

11.6 How can the output current regulation be optimized?

Please refer to **Section 10.1.3**, which describes the fine-tuning procedures of the output regulation parameters.

11.7 Why does the output LED current have high ripple?

As there is only one switching element with the single-stage PFC Flyback topology, the Flyback transformer primary winding current needs to be shaped according to the rectified input sinusoidal waveform. Since the secondary winding peak current is directly proportionate to the primary winding peak current, the output LED current will have high ripple with double line frequency (e.g. 100~120 Hz), which the output capacitors find difficult to filter.

Please also note that output ripple peak-to-peak levels (I_{pk-pk}) vary a lot based on the output LED's dynamic resistance (R_d). See examples below:

- With the same forward voltage, I_{pk-pk} becomes higher if the output load is changed to another LED type with smaller R_d, or vice-versa.
- With the same LED type, I_{pk-pk} is the maximum when the output current is at a maximum and the series LED number (voltage) is at a minimum, or vice-versa.

11.8 How can LED current ripple be reduced?

There are two possible options, as shown below, but each increases the BOM cost and comes with a certain trade-off:

- Increase the output capacitance, but this increases time-to-light, especially for minimum dimming input. Please refer to **Section 11.4** and **Section 11.5** for more details.
- Add the output ripple suppression circuitry, but this could reduce the system efficiency and output accuracy.

11.9 Why is there a light flicker when the input voltage is stepped up or down?

When the input voltage is stepped up or down, output current overshoot or undershoot could occur in the single-stage PFC Flyback because of the slow control loop speed and low loop gain of the controller, which are intended to obtain high PF and low iTHD.

To protect LEDs from being damaged by the excessive output current overshoot when input voltage is stepped up, the XDPL8105 peak output over-current protection parameter (*EN_Iout_max_peak*) can be enabled to put the system into a protection state once the estimated output current exceeds a configurable threshold (*I_out_max_peak*), and initiate an auto-restart.

There is also a configurable parameter which determines the speed of the auto-restart time (*Speed_OCP_Iout*) for this protection.

- If the parameter *Speed_OCP_Iout* is set to “Slow”, the auto restart time will be based on the configurable parameter *t_auto_restart*.
- If the parameter *Speed_OCP_Iout* is set to “Fast”, the auto restart time will be based on the configurable parameter *t_auto_restart_fast*.

One practical use case is to configure the parameter *Speed_OCP_Iout* as “Fast” so that the light output can be recovered with a shorter light-off time after the peak output over-current protection is triggered.

The first full set of working parameters burned to the 40 W reference design has the peak output over-current protection enabled. Users can choose to disable this protection by configuration if it is not desired.

11.10 What are the configurable options for the dimming curve?

Users can configure the parameter *C_DIM* to select either one of the following dimming curve shapes.

- Linear dimming curve
  Output current scales linearly with dimming voltage.
- Quadratic dimming curve
  Output current scales quadratically with dimming voltage. This provides a more evenly distributed change of brightness to the eye.

Furthermore, the voltage thresholds for deadbands at the minimum output current level (*I_out_dim_min*) can be changed by configuring the parameters *V_DIM_min* and *V_DIM_off* respectively.

*Note: The parameter V_DIM_max is non-configurable and fixed at 1.72 V. The parameter V_DIM_off is only effective when the dim-to-off feature is enabled by the parameter EN_DIM_TO_OFF (please refer to **Section 11.1** to understand the application in which dim-to-off can be supported).*

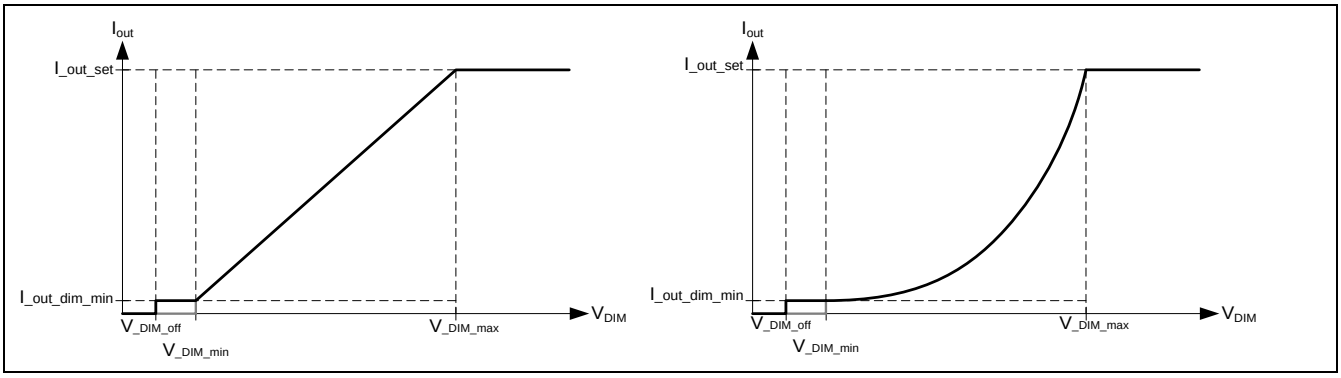


Figure 34 Configurable options for dimming curves

11.11 Can the HV series resistor be connected directly to the input filter capacitor after the bridge rectifier?

This is not recommended, because the light quality and accuracy can be degraded as the HV pin line synchronization is likely to not be as stable as connection to the X-capacitor of the AC input-line filter circuitry via the two diodes, especially with the minimum dimming input.

11.12 What is the parameter *t_min_demag* used for?

The parameter *t_min_demag* basically defines the desired minimum transformer demagnetization time. Based on the following equation, the controller dynamically calculates $t_{ON,MIN(VOUT\ SENSE)}$, which is the minimum on-time needed to secure *t_min_demag* for primary-side output voltage sensing via ZCD pin.

$$t_{ON,MIN(VOUT\ SENSE)} = \frac{N_p}{N_s} \times \frac{(V_o + V_f) \times t\_\min\_demag}{V_{IN}}$$

Where:

$\frac{N_p}{N_s}$ is the transformer primary input winding to secondary output winding turns ratio

$V_o + V_f$ is the output LED voltage plus output diode forward voltage

V_{IN} is the rectified input filter capacitor voltage.

Therefore, please note that if the calculated $t_{ON,MIN(VOUT\ SENSE}$ is higher than the configured parameter *t_on_min* value, the former will replace the parameter *t_on_min* as the effective controller minimum on-time. This typically happens when the minimum input voltage (e.g. 100 V AC) and maximum output load voltage are applied.

It is highly recommended to use the default value from the 40 W reference design configuration file, which is 3.0 µs.

11.13 How does multi-mode operation work when dimmed up or down?

Figure 35 shows the on-time and switching period changes based on the multi-mode configurable parameters when the output current (power) is dimmed up or down.

QRM delivers the highest output power of the XDPL8105 system, thus the controller should always operate in this mode at non-dimming conditions. In QRM, the on-time is controlled between the *t_on_min* and *t_on_max* parameter settings to regulate the output current when dimming, as based on the algorithm below:

- When output is dimmed down, the QRM on-time will be reduced.
- When output is dimmed up, the QRM on-time will be increased.

Typically, the QRM switching period should be based on the timing between the start of on-time and when the first QRM valley occurs (see **Figure 36** for example), but if the first QRM valley occurs before the minimum switching period (1/*f_sw_max*) is reached, the switching period will be fixed as the minimum switching period instead of switching at the first valley (see **Figure 37** and **Figure 38** for waveform examples).

When the output is dimmed down until the QRM on-time reaches slightly below the minimum on-time parameter (*t_on_min*) based on an internal predefined hysteresis, the controller will switch its operating mode from QRM on-time control to DCM period control.

In DCM, the on-time is fixed as the parameter *ton_min* setting while the switching period is maintained between the values 1/*f_sw_max* and 1/ *f_sw_min_DCM* to regulate the output current when dimming, as based on the algorithm below:

- When output is dimmed down, the DCM switching period will be increased.
- When output is dimmed up, the DCM switching period will be reduced.

Note: Under certain conditions, the t_on_min parameter value can be dynamically replaced by another internally calculated minimum on-time in order to secure the minimum demagnetization time based on the parameter t_min_demag for ZCD pin output voltage sensing. For more details, please refer to ***Section 11.12****.*

The minimum output power transfer of DCM is reached when the DCM switching period is equivalent to the maximum DCM switching period (1/*f_sw_min_DCM*) value.

If the output is dimmed down further on reaching the maximum switching period in DCM, the controller will switch its operating mode from DCM to ABM if the parameter *EN_ABM* is enabled.

In ABM, the on-time and switching frequency are fixed based on the *t_on_min* and *f_sw_min_DCM* parameter settings respectively. To regulate the output current in ABM, the number of DCM switching pulses (over the rectified input sine-wave period) is controlled, based on the algorithm below:

- When output is dimmed down, the number of DCM switching pulses is reduced.
- When output is dimmed up, the number of DCM switching pulses is increased.

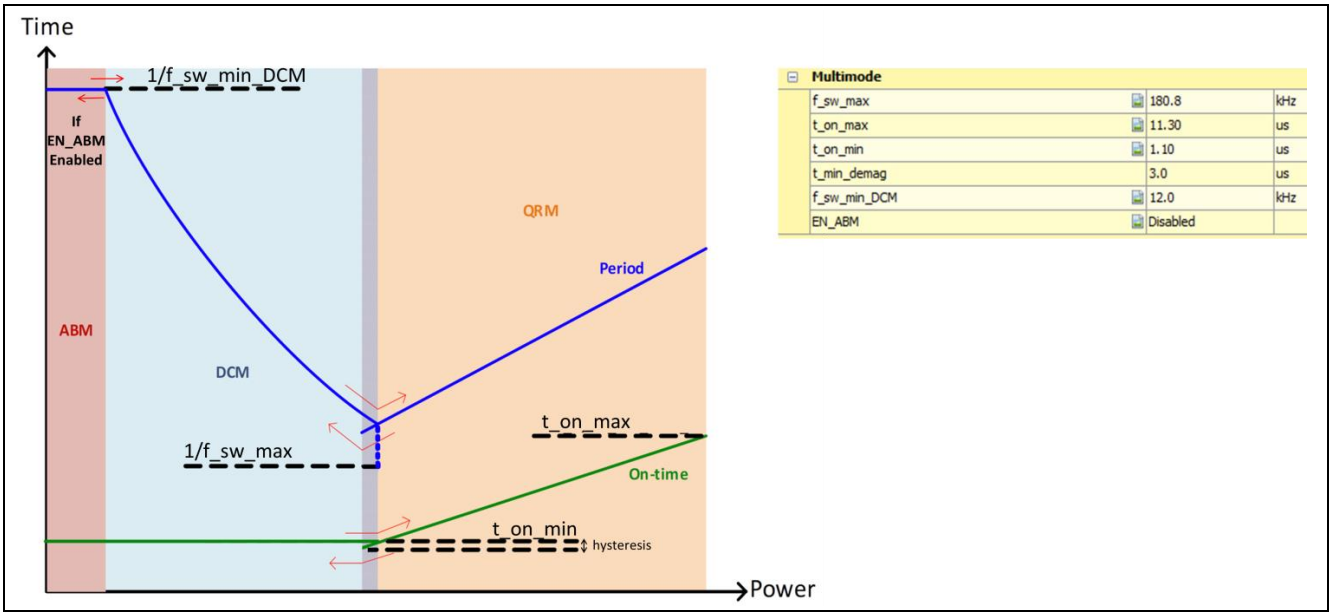


Figure 35 Multi-mode operation on-time and period changes when output is dimmed

11.14 How can the controller operating mode be identified during actual testing?

The operating mode of the controller can be identified based on the MOSFET drain voltage waveform at the peak of the rectified input sine-wave.

Please refer to the figures below for the example of waveforms taken from the XDPL8105 40 W reference design under test conditions of 230 V AC input and 36 V LED output when the secondary dimming input voltage is gradually reduced from 10 V to 0 V.

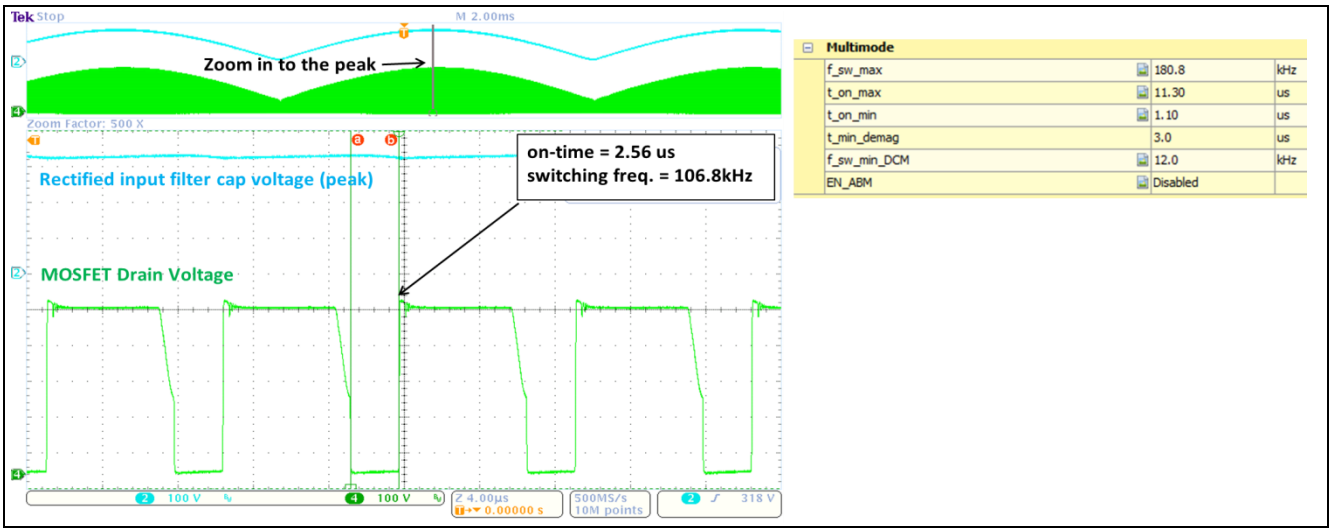


Figure 36 Example of QRM on-time control with first valley switching waveform (dimming input = 10 V)

*Note: If the QR first valley switching is not achieved under non-dimming conditions while the on-time is above the t_on_min parameter value and the switching frequency is below the f_sw_max parameter value, please refer to **Section 10.1.2** for fine-tuning the parameter t_ZCDPD.*

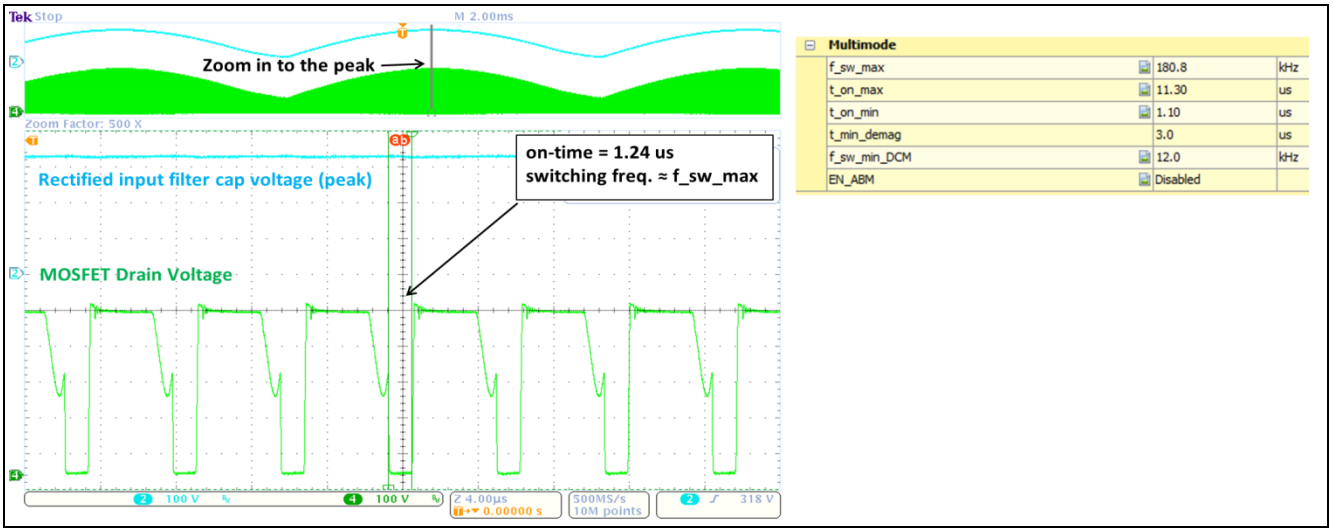


Figure 37 Example of QRM on-time control with f_sw_max waveform (dimming input = 5 V)

*Note: In **Figure 37**, the controller is in QRM on-time control operation (on-time is lower than in **Figure 36**) but the first valley switching has been blocked by the maximum switching frequency setting (f_sw_max).*

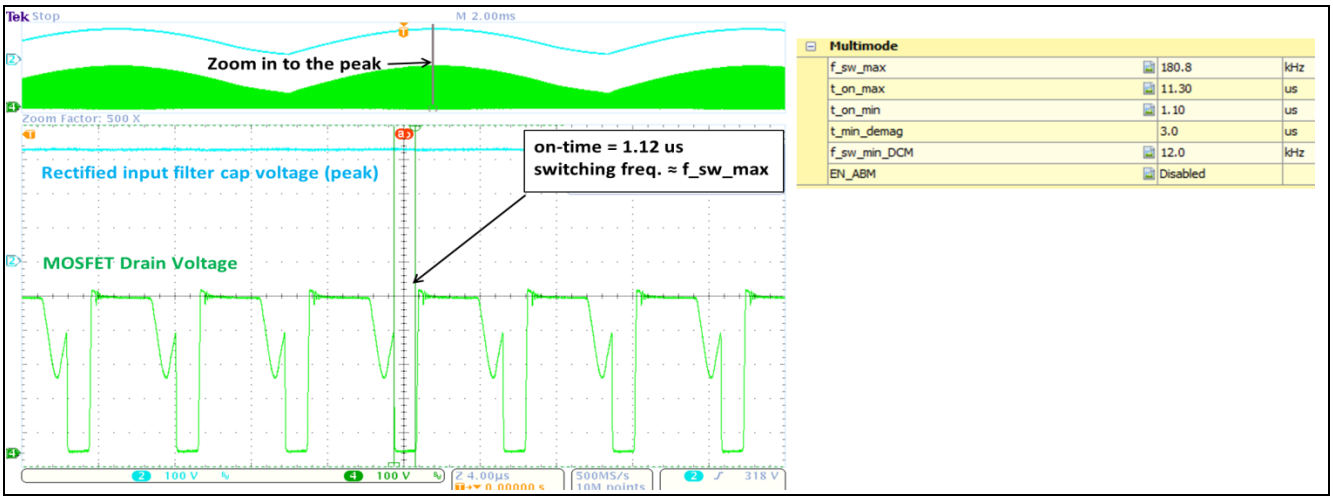


Figure 38 Example of QRM on-time control with f_sw_max waveform (dimming input = 4.7 V)

*Note: In **Figure 38**, the controller is in QRM on-time control operation (on-time is lower than in **Figure 37**) but the first valley switching has been blocked by the maximum switching frequency setting (f_sw_max).*

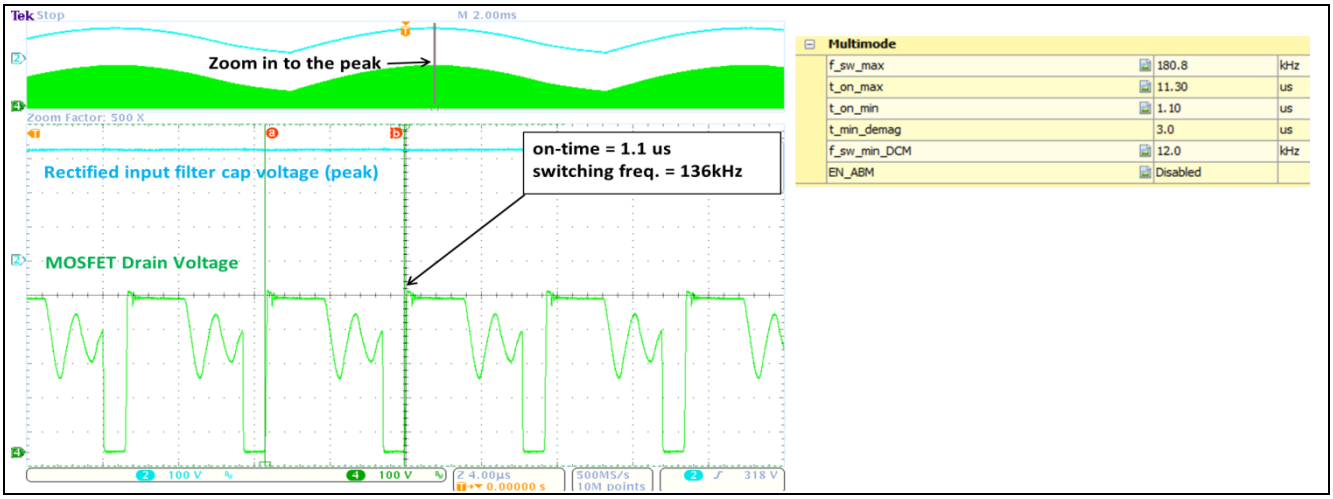


Figure 39 Example of DCM period control waveform (dimming input = 4 V)

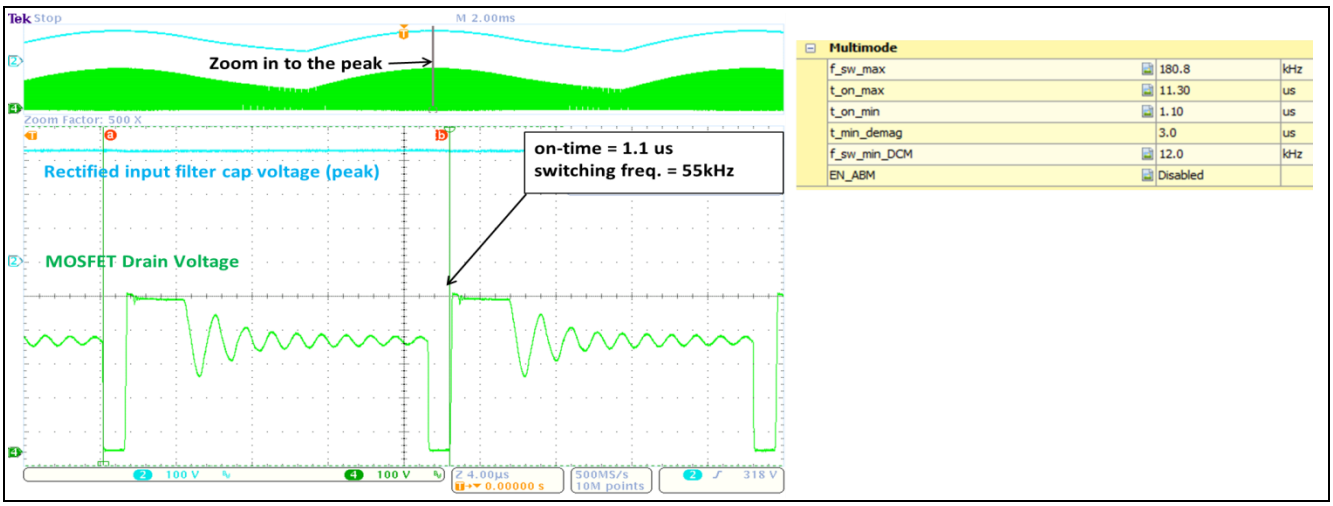


Figure 40 Example of DCM period control waveform (dimming input = 0 V)

11.15 Why is the QRM on-time or DCM switching period changing at different AC input phase angles despite having stable light output in steady-state?

In QRM, the PI regulator on-time control output is modulated based on the AC input phase angle (for PF enhancement) if the parameter *C_EMI* is configured above zero. For more details, please refer to **Section 10.1.5**.

In DCM, the PI regulator period control output is modulated based on the AC input phase angle (for light quality improvement) if the parameter *N_DCM_MOD_GAIN* is configured above zero. For more details, please refer to **Section 10.1.4**.

Apart from improving the light quality, the QRM maximum switching frequency setting is also modulated based on the AC input phase angle (for iTHD improvement) if the parameter *N_DCM_MOD_GAIN* is configured above zero. For more details, please refer to **Section 10.1.5**.

11.16 Why does the output current stay at *I_out_set* despite being dimmed down?

Please follow the troubleshooting steps below to resolve the problem.

- Test the board on its own without connecting the .dp Interface Gen2 after burning the configuration. Please note that dimming tests are not possible if the board is powered up with the test configuration function in .dp Vision.
- Ensure the target XDPL8105 has been burned with the parameter *EN_DIM* configured as “Enabled” and parameter *I_out_dim_min* configured to be reasonably below the *I_out_set* parameter setting.
- Measure the DIM/UART pin voltage to ensure it does not exceed 2.2 V at all times. This is because if 2.2 V is exceeded, the IC will stay in a non-dimming condition until reset by UVLO.
- Please ensure the DIM/UART pin voltage can be reduced to less than 1.72 V and *V_DIM_min* when the minimum dimming input signal is applied.

11.17 What could cause the start-up UVP for V_{out} to be triggered despite having the correct number of LEDs connected to the secondary output?

The start-up UVP for V_{out} can be triggered if the output voltage charging does not reach parameter *V_out_start* level within the time-out of parameter *t_start_max* on start-up, as shown in **Figure 41**. This typically happens at lower AC input voltage as the output voltage charging becomes slower.

Note: V_out_start is the start-up output voltage level which ensures V_{CC} self-supply via auxiliary winding.

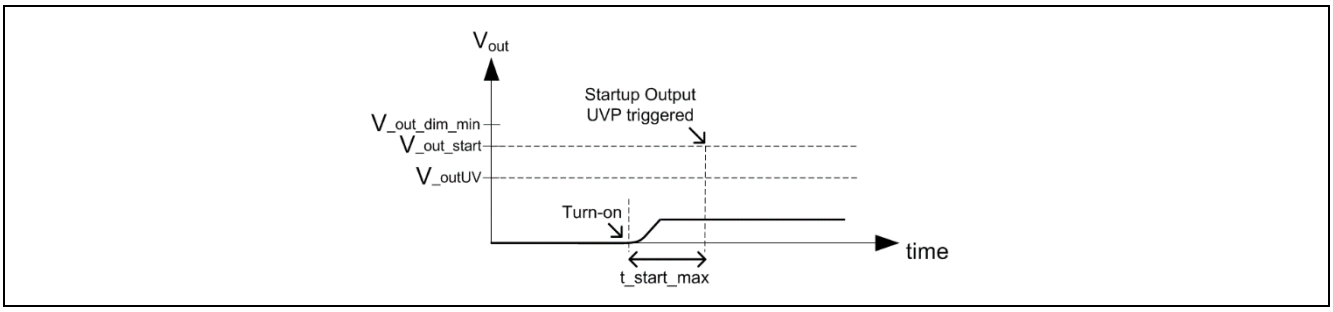


Figure 41 Start-up UVP for V_{out}

If the output capacitance is increased, the output voltage charging time becomes longer and the start-up UVP for V_{out} can also be triggered if the charging time to reach parameter *V_out_start* level becomes longer than parameter *t_start_max* setting.

To resolve the problem of mis-triggering this protection, one solution is to increase the parameter *t_start_max* value. However, it is important to ensure that the V_{CC} capacitance is sufficient to hold up the XDPL8105 operating voltage during start-up (not hitting the turn-off threshold) for at least the period based on the increased *t_start_max*. This is to ensure that an actual output short during start-up can be properly detected so that the IC can initiate the auto-restart operation based on the interval of parameter *t_auto_restart,* for low input power consumption during output short.

It is recommended to check your design based on the Excel tool and apply the necessary countermeasure to the V_{CC} supply circuitry and/or IC parameterization.

11.18 What could cause inaccuracy of the input under-voltage (brown-out) protection threshold?

The accuracy of the input UVP threshold (based on parameter *V_inUV*) very much depends on parameter *R_in*. Please refer to **Section 10.1.1** for the fine-tuning guide.

11.19 What is the main benefit of configuring the GD pin peak-source current parameter *I_GD_pk*?

To slow down the MOSFET switch-on speed for EMI improvement while having low turn-on loss, XDPL8105 GD pin peak-source current parameter *I_GD_pk* can be configured to control the gate rising slope and the MOSFET switch-on speed (configurable range: 30~118 mA), as shown in **Figure 42**.

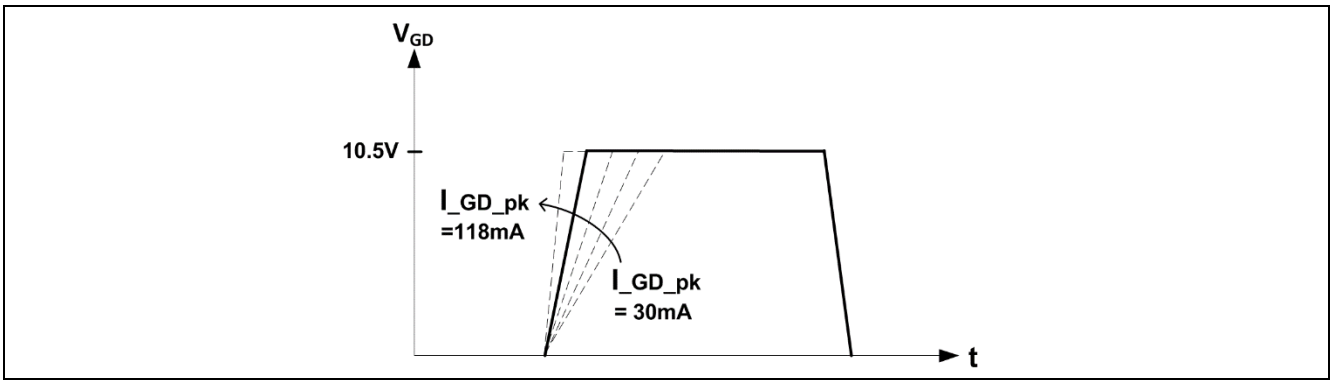


Figure 42 Gate rising slope control with parameter *I_GD_pk* configuration

This allows the user to save two external components (D-fastoff, R-slowon) in the BOM which are conventionally added to achieve the same purpose for EMI improvement, as shown in **Figure 43**.

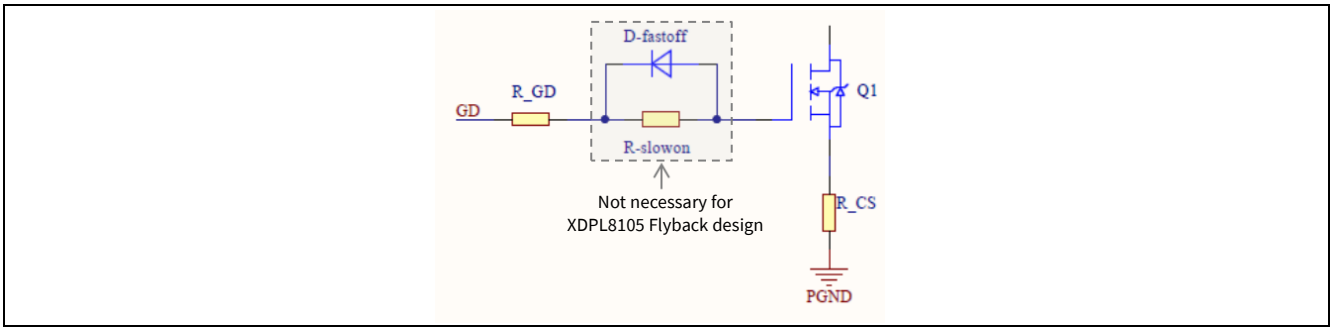


Figure 43 BOM savings with parameter *I_GD_pk* configuration

11.20 Why is the output bleeder mandatory in the design?

The output bleeder is mandatory in the design to discharge the output capacitor voltage each time after the output OVP is triggered by an output open-load (OV) condition.

Regardless of whether the reaction of the output OVP (*Reaction_OVP_Vout*) is configured as auto-restart or latch mode, the output bleeding has to be strong enough to at least nullify the output energy transfer during the interval of each restart or input voltage recycling so that the output capacitor voltage can be maintained within a safe limit based on the output overvoltage threshold (*V_outOV*).

The energy transfer to the output capacitor is required each time before the output OVP can be triggered because the primary-side output voltage sensing via the XDPL8105 ZCD pin requires the output diode to be in forward conduction.

User can select either of the output bleeder designs below:

- Active (auto-discharge circuit)
  Output bleeding happens only when transformer switching is stopped (e.g. after the protection is triggered or AC input voltage is off). The component count is higher but there is no efficiency loss during normal operation and the discharge is fast with low bleeder resistance. The schematic in **Figure 2** presents an exemplary circuitry which is formed by C10, C11, D7, Q3, Q4, R26, R27, R28, R29, R30, ZD4 and ZD5.
- Passive (dummy resistor)
  Output bleeding always happens with a dummy resistor connected in parallel with the output. The component count is the lowest with only slight efficiency loss during normal operation and the discharge is slow with high bleeder resistance.

It is strongly recommended to use the Excel tool to obtain an initial design of the circuit dimensioning (e.g. bleeder resistance) and the related IC parameterization (e.g. *Reaction_OVP_Vout, t_auto_restart*).

11.21 Can XDPL8105 be used with input voltage higher than 425 V AC or 600 V DC?

The internal HV start-up cell of the XDPL8105 can handle a maximum of 600 V. It is possible to use, for example, two Zener diodes of 270 V each to limit the voltage at the HV pin to 540 V.

If the typical single-switch Flyback design is used, the expensive 1000 V-rated MOSFET is needed to handle the very high drain voltage for such an application. Therefore, it is recommended to use the dual-switch Flyback design (with lower MOSFET voltage rating) instead. If necessary, please contact your Infineon representative for more details.

11.22 Can XDPL8105 be used as a controller of the Flyback converter that has a front-stage PFC boost converter?

It is possible but not recommended. The Flyback converter in such dual-topology stage designs is normally expected to deliver very low output current ripple (e.g. ±5 percent or below). Despite having the front-stage PFC boost converter, the PFC boost DC output voltage on the bulk capacitor has a voltage ripple which is highest when the output power reaches maximum level.

Due to the slow control loop response of the XDPL8105 for its own PFC functionality, it cannot regulate the output current while effectively suppressing its input voltage ripple from being transferred to the output. In other words, the front-stage PFC boost output bulk capacitor before the XDPL8105 Flyback converter would require a larger capacitance in order to meet the very low output current ripple requirement.

11.23 Can the Flyback transformer auxiliary winding be used to supply the microcontroller's operating voltage?

It is strongly recommended not to supply the microcontroller's operating voltage with the Flyback transformer auxiliary winding, as it will introduce an output current offset depending on the microcontroller's current consumption. As the microcontroller's current consumption is expected to change based on its operation, the output current's accuracy and stability will be affected by the changing current offset.

Furthermore, the transformer auxiliary winding is also not able to supply the microcontroller's operating voltage during dim-to-off operation, which is typically required by such applications.

12 References

[1] XDPL8105 Datasheet

[2] CDM10V Datasheet

[3] XDPL8105 Design Tool User Guide

[4] .dp Vision User Manual

Revision history

Major changes since the last revision

Page or reference	Description of change
Section 8.1	Wording update: from “project addon installer” to “.dp Vision folder setup file”
Section 8.2	Tool name and link update from “CDM10V_PRG_BOARD” to “COOLDIM_PRG_BOARD”
All sections	Font and writing style update

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