AN-REF-35W ADAPTER

35W 19V Adapter Reference Board with ICE2QS03G, IPD60R600P6 BAS21-03W & 2N7002

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Revision History

AN_201405_PL21_006

Major changes since previous revision

Date	Version	Changed By	Change Description
2 Jul 2014	1.0	Kyaw Zin Min	Release of final version

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1 Abstract

This application note is an engineering report of a very small form factor reference design for universal input 35W 19V adapter. The adapter is using **ICE2QS03G**, a second generation current mode control quasi-resonant flyback topology controller and **IPD60R600P6**, a seventh generation of high voltage power CoolMOS™. The distinguishing features of this reference design are very small form factor, best in class low standby power, high efficiency, good EMI performance and various modes of protection for high reliable system.

2 Reference board

This document contains the list of features, the power supply specification, schematic, bill of material and the transformer construction documentation. Typical operating characteristics such as performance curve and scope waveforms are showed at the rear of the report.

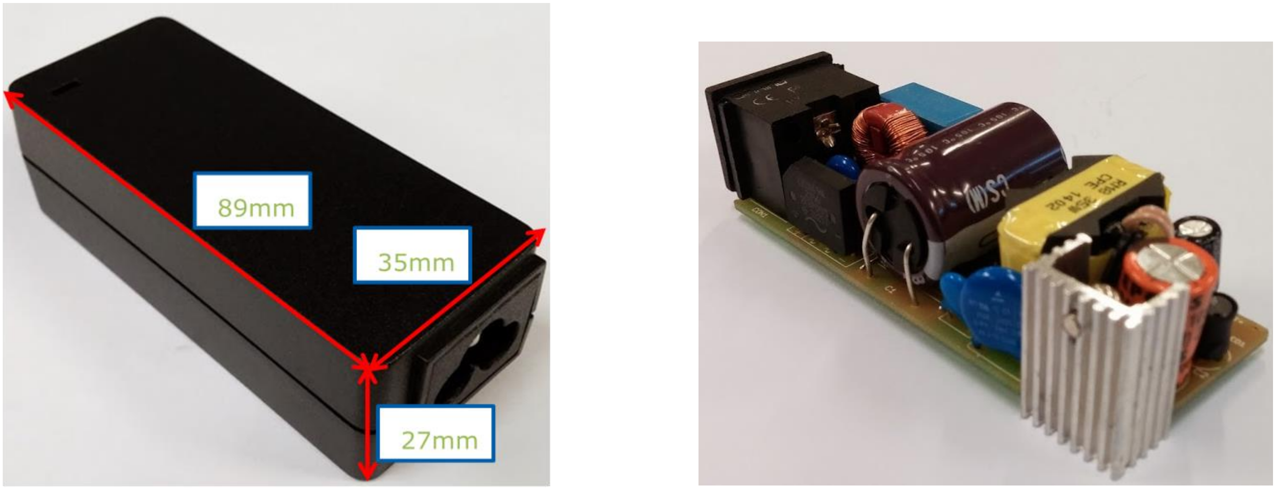


Figure 1 – REF-ICE2QSO3G & IPD60R600P6 35W ADAPTER [Dimensions L x W x H: 89mm x 35mm x 27mm]

Figure 2A – REF-ICE2QSO3G & IPD60R600P6 35W ADAPTER (Top Side)

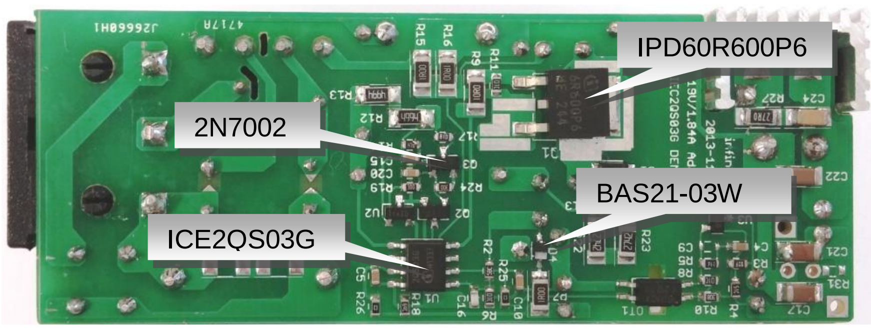


Figure 2B – REF-ICE2QSO3G & IPD60R600P6 35W ADAPTER (Bottom Side)

3 Technical specifications

Input voltage	90Vac~264Vac
Input frequency	47~63Hz
Output voltage	19V
Full load output current	1.84A
Full load output power	35W
Brownout detect/reset voltage @ full load	80/87Vac
Output over voltage protection	21~22V
Over current protection	2.3~3.3A
No-load power consumption	<75mW (comply with EU CoC Version 5, Tier 2 and EPS of DOE USA)
Active mode four point average efficiency (25%,50%,75% & 100%load) Active mode at 10% load efficiency	>88.22% (comply with EU CoC Version 5, Tier 2 and EPS of DOE USA) >78.22% (comply with EU CoC Version 5, Tier 2)
Form factor case size (L x W x H)	(89 x 35 x 27) mm^3

4 List of features (ICE2QS03G)

Quasi resonant operation till very low load
Active burst mode operation at light/no load for low standby input power (< 100mW)
Digital frequency reduction with decreasing load
HV startup cell with constant charging current
Built-in digital soft-start
Foldback correction and cycle-by-cycle peak current limitation
Auto restart mode for VCC Overvoltage protection
Auto restart mode for VCC Undervoltage protection
Auto restart mode for Overload /Openloop protection
Auto restart mode for Over temperature protection
Latch-off mode for adjustable output overvoltage protection
Latch-off mode for Short Winding

5 Circuit description

5.1 Mains Input Rectification and Filtering

The AC line input side comprises the input fuse F1 as over-current protection. The choke L2, X-capacitors C7 and Y-capacitor C11, C18 and C19 act as EMI suppressors. PCB spark gap and varistor VR1 can absorb high voltage stress during lightning surge test. After the bridge rectifier D3 and the input bulk capacitor C1, a voltage of 90 to 373 V_{DC} is present which depends on input line voltage.

5.2 PWM Control and switching MOSFET

The PWM pulse is generated by the Quasi Resonant PWM current-mode Controller **ICE2QS03G** and this PWM pulse drives the high voltage power MOSFETs, **IPD60R600P6 (**CoolMOS™ **P6)**. P6 is Infineon's seventh generation of high voltage power MOSFETs designed according to the revolutionary Superjunction (SJ) principle. The new CoolMOS™ P6 series combines our experience as the leading SJ MOSFET supplier with innovation focusing on high efficiency solutions. The resulting P6 technology is tailored to provide high performance in hard & soft switching topologies while not sacrificing the ease of use. P6 achieves extremely low conduction and switching losses especially in light load condition enabling switching applications to work more efficient and be designed more compact, lighter and cooler. The PWM switch-on is determined by the zero-crossing input signal and the value of the up/down counter. The PWM switch-off is determined by the feedback signal V_{FB} and the current sensing signal V_{CS}. **ICE2QS03G** also performs all necessary protection functions in flyback converters. Details about the information mentioned above are illustrated in the product datasheet.

5.3 Snubber Network

A snubber network R22, R23, C13 and D1 dissipate the energy of the leakage inductance and suppress ringing on the SMPS transformer. Due to the resonant capacitor (MOSFET's drain source capacitance), the overshoot is relatively smaller than fixed frequency flyback converter. Thus the snubber resistor can be used with a larger one which will reduce the snubber loss.

5.4 Output Stage

On the secondary side, 19V output, the power is coupled out via a schottky diode D2. The capacitors C2 provides energy buffering following with the LC filter L1 and C3 to reduce the output ripple and prevent interference between SMPS switching frequency and line frequency considerably. Storage capacitor C2 is designed to have an internal resistance (ESR) as small as possible. This is to minimize the output voltage ripple caused by the triangular current.

5.5 Feedback Loop

For feedback, the output is sensed by the voltage divider of R3 and R4 and compared to TL431 internal reference voltage. C4 and R5 comprise the compensation network. The output voltage of TL431 is converted to the current signal via optocoupler OT1 and two resistors R8 and R10 for regulation control.

6 Circuit Operation

6.1 Startup Operation

Since there is a built-in startup cell in the **ICE2QS03G**, there is no need for external start up resistor, which can improve standby performance significantly. When VCC reaches the turn on voltage threshold 18V, the IC begins with a soft start. The soft-start implemented in **ICE2QS03G** is a digital time-based function. The preset soft-start time is 12ms with 4 steps. If not limited by other functions, the peak voltage on CS pin will increase step by step from 0.32V to 1V finally. After IC turns on, the Vcc voltage is supplied by auxiliary windings of the transformer.

6.2 Normal Mode Operation

The secondary output voltage is built up after startup. The secondary regulation control is adopted with TL431 and optocoupler. The compensation network C4 and R5 constitutes the external circuitry of the error amplifier of TL431. This circuitry allows the feedback to be precisely controlled with respect to dynamically varying load conditions, therefore providing stable control.

6.3 Primary side peak current control

The MOSFET drain source current is sensed via external resistor R15 and R16. Since **ICE2QS03G** is a current mode controller, it would have a cycle-by-cycle primary current and feedback voltage control which can make sure the maximum power of the converter is controlled in every switching cycle.

6.4 Digital Frequency Reduction

During normal operation, the switching frequency for **ICE2QS03G** is digitally reduced with decreasing load. At light load, the CoolMOS™ **IPD60R600P6** will be turned on not at the first minimum drain-source voltage time, but on the nth. The counter is in range of 1 to 7, which depends on feedback voltage in a time-base. The feedback voltage decreases when the output power requirement decreases, and vice versa. Therefore, the counter is set by monitoring voltage V_{FB}. The counter will be increased with low V_{FB} and decreased with high V_{FB}. The thresholds are preset inside the IC.

6.5 Burst Mode Operation

At light load condition, the SMPS enters into **Active Burst Mode**. At this stage, the controller is always active but the Vcc must be kept above the switch off threshold. During active burst mode, the efficiency increase significantly and at the same time it supports low ripple on V_{out} and fast response on load jump.

For determination of entering Active Burst Mode operation, three conditions apply:

1. The feedback voltage is lower than the threshold of V_{FBEB}(1.219V). Accordingly, the peak current sense voltage across the shunt resistor is 0.1667;

2. The up/down counter is 7;

3. And a certain blanking time (t_{BEB}=24ms).

Once all of these conditions are fulfilled, the Active Burst Mode flip-flop is set and the controller enters Active Burst Mode operation. This multi-condition determination for entering Active Burst Mode operation prevents mis-triggering of entering Active Burst Mode operation, so that the controller enters Active Burst Mode operation only when the output power is really low during the preset blanking time.

During active burst mode, the maximum current sense voltage is reduced from 1V to 0.34V so as to reduce the conduction loss and the audible noise. At the burst mode, the FB voltage is changing like a sawtooth between 3.0 and 3.6V.

The feedback voltage immediately increases if there is a high load jump. This is observed by one comparator. As the current limit is 34% during Active Burst Mode a certain load is needed so that feedback voltage can exceed VLB (4.19V). After leaving active burst mode, maximum current can now be provided to stabilize V_O. In addition, the up/down counter will be set to 1 immediately after leaving Active Burst Mode. This is helpful to decrease the output voltage undershoot.

7 Protection Features

7.1 VCC over voltage and under voltage protection

During normal operation, the Vcc voltage is continuously monitored. When the Vcc voltage increases up to V_{VCCOVP} or Vcc voltage falls below the under voltage lock out level V_{VCCoff}, the IC will enter into autorestart mode.

7.2 Over load/Open loop protection

In case of open control loop, feedback voltage is pulled up with internally block. After a fixed blanking time, the IC enters into auto restart mode. In case of secondary short-circuit or overload, regulation voltage V_{FB} will also be pulled up, same protection is applied and IC will auto restart.

7.3 Auto restart for over temperature protection

The IC has a built-in over temperature protection function. When the controller's temperature reaches 140 °C, the IC will shut down switch and enters into auto restart. This can protect power MOSFET from overheated.

7.4 Adjustable output overvoltage protection

During off-time of the power switch, the voltage at the zero-crossing pin ZC is monitored for output overvoltage detection. If the voltage is higher than the preset threshold 3.7V for a preset period 100µs, the IC is latched off.

7.5 Short winding protection

The source current of the MOSFET is sensed via external resistor R15 and R16. If the voltage at the current sensing pin is higher than the preset threshold V_{CSSW} of 1.68V during the on-time of the power switch, the IC is latched off. This constitutes a short winding protection. To avoid an accidental latch off, a spike blanking time of 190ns is integrated in the output of internal comparator.

7.6 Foldback point protection

For a quasi-resonant flyback converter, the maximum possible output power is increased when a constant current limit value is used for all the mains input voltage range. This is usually not desired as this will increase additional cost on transformer and output diode in case of output over power conditions.
The internal foldback protection is implemented to adjust the VCS voltage limit according to the bus voltage. Here, the input line voltage is sensed using the current flowing out of ZC pin, during the MOSFET on-time. As the result, the maximum current limit will be lower at high input voltage and the maximum output power can be well limited versus the input voltage.

7.7 AC line under voltage protection (Brownout mode) by external circuit

When the AC line input voltage is lower than the specified voltage range, brownout mode is detected by sensing the voltage level at U2 (TL431)'s REF pin (V_{Ref_Typ} =2.5V) through the voltage divider resistors (R12, R13, R14 and R17 in Fig.3) from bulk capacitor C1. Q2 acts as a switch to enter or leave brownout mode by controlling FB pin voltage. Q3 together with R17 act as voltage hysteresis for the brownout circuit and U2 (TL431) as a comparator. The system enters the brownout mode by controlling FB pin voltage of U1 to 0V (when the voltage level at V_{Ref} drop down to 2.5V, then the MOSFET switch Q2 and Q3 on and V_{FB} drop down to 0V). It is until the input level goes back to input voltage range, V_{Ref} increase to 2.5V (then the switch Q2 and Q3 off) and the Vcc hits 18V, the brownout mode is released. The calculation for brownout circuit as below,

$$\mathrm{Vref} = 2.5\mathrm{V}$$

$$\mathrm{R12} = 4.99\mathrm{M\Omega} \qquad \mathrm{R13} = 4.99\mathrm{M\Omega} \qquad \mathrm{R14} = 301\mathrm{k\Omega} \qquad \mathrm{R17} = 681\mathrm{k\Omega}$$

$$\mathrm{Vbulkcap\_enterbrownout} = \frac{(\mathrm{R12} + \mathrm{R13} + \mathrm{R14}) \cdot \mathrm{Vref}}{\mathrm{R14}} \qquad \mathrm{Vbulkcap\_enterbrownout} = 85.39\mathrm{V}$$

$$\mathrm{Vbulkcap\_leavebrownout} = \frac{\left[\left(\frac{\mathrm{R14} \cdot \mathrm{R17}}{\mathrm{R14} + \mathrm{R17}}\right) + \mathrm{R12} + \mathrm{R13}\right] \cdot \mathrm{Vref}}{\left(\frac{\mathrm{R14} \cdot \mathrm{R17}}{\mathrm{R14} + \mathrm{R17}}\right)} \qquad \mathrm{Vbulkcap\_leavebrownout} = 122.028\mathrm{V}$$

8 Circuit diagram

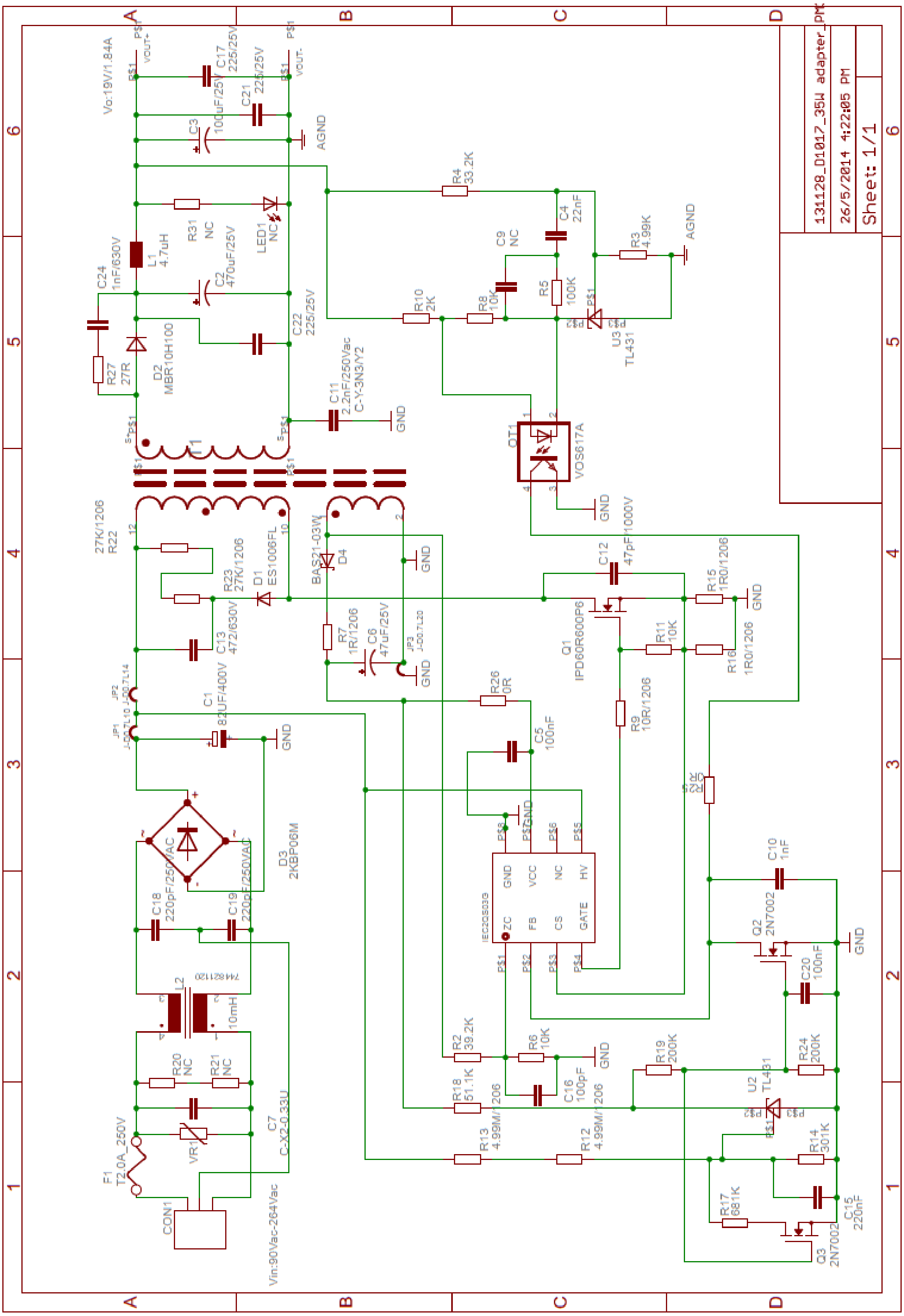


Figure 3 – 35W 19V ICE2QSO3G power supply schematic

9 PCB layout

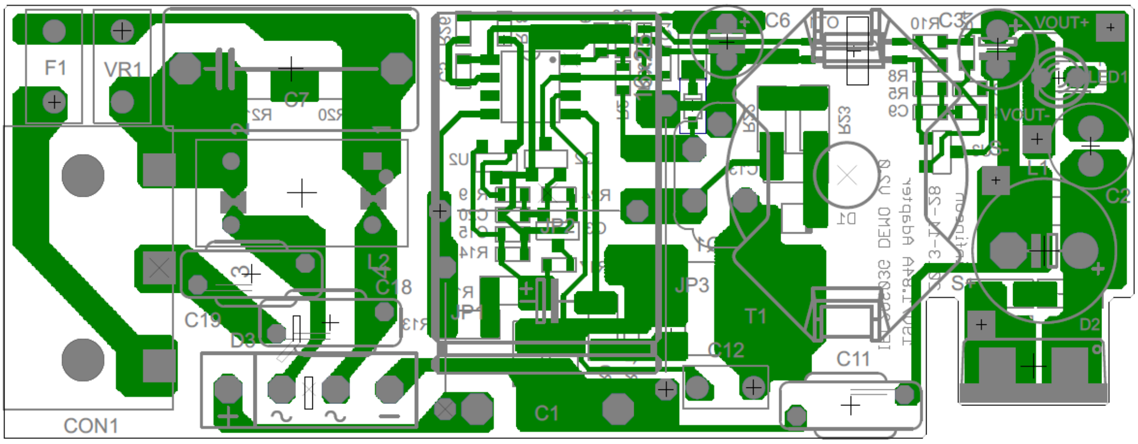


Figure 4 – Bottom side copper and component legend

9.1 Top side

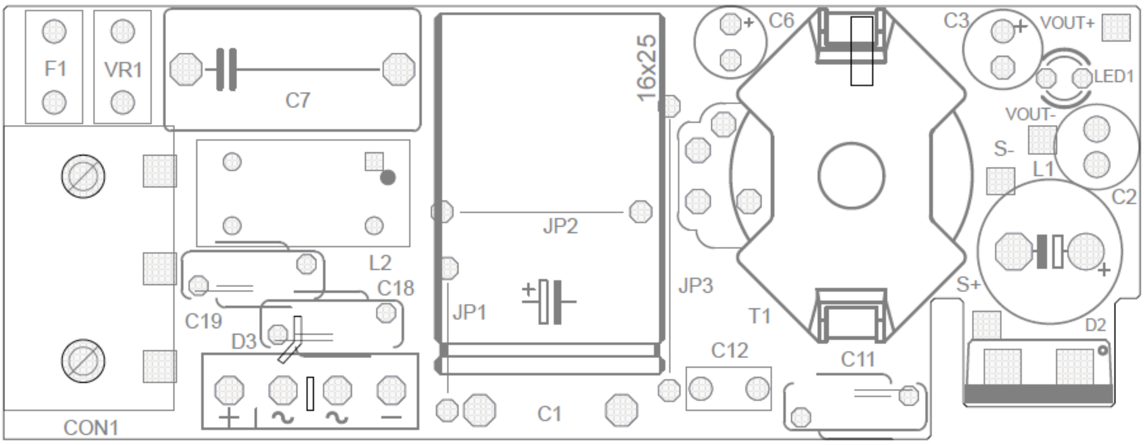


Figure 5A – Top side component legend

9.2 Bottom side

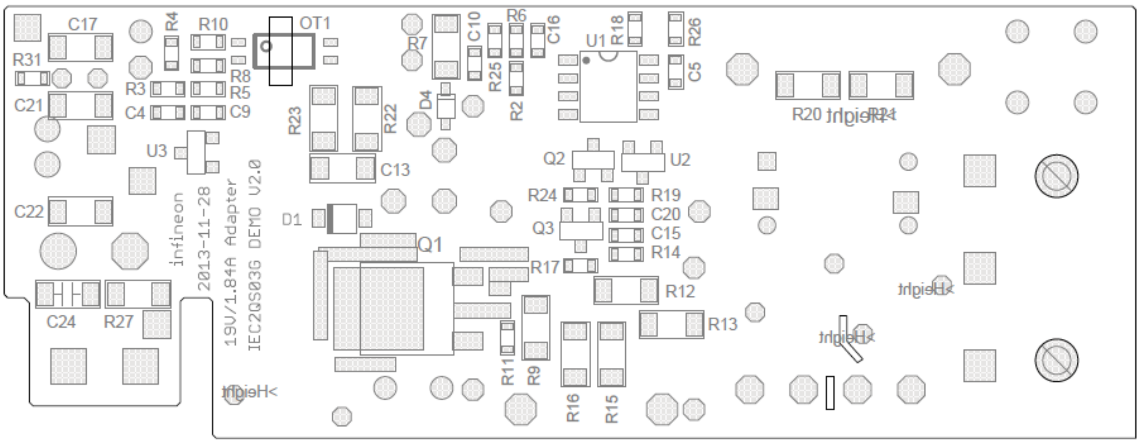


Figure 5B – Bottom side component legend

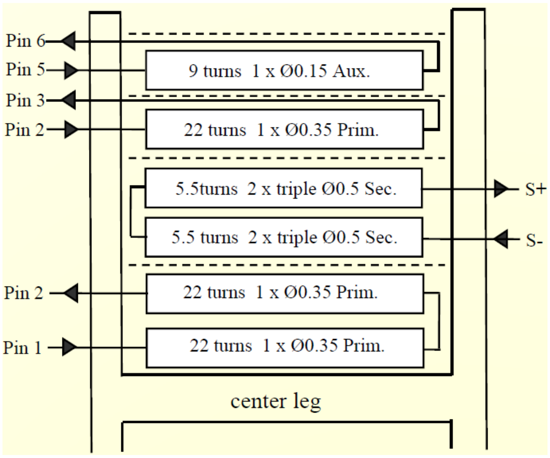
10 Component list

No.	Reference	Part value	Supplier	Description	Package
1	C1	E-CAP,82uF,400V,105℃		Electrolytic Cap	Φ18*25mm,P=10mm
2	C10	1nF/50V/X7R	MURATA	Chip Cap	0603
3	C11	Y2 Cap,2.2nF/250Vac		Ceramic Cap	9*5mm,P=10mm
4	C12	47PF/1000V		Chip Cap	6*3mm P=4mm
5	C13	4.7nF/630V/X7R	MURATA	Chip Cap	1206
6	C15	220nF/16V/X7R	MURATA	Chip Cap	0603
7	C16	100pF/50V/X7R	MURATA	Chip Cap	0603
8	C17,C21,C22	2.2uF/25V/X7R	MURATA	Chip Cap	1206
9	C18,C19	Y2 Cap,220pF/250Vac		Ceramic Cap	9*5mm,P=10mm
10	C2	E-CAP,470uF,25V	EPCOS	Electrolytic Cap	Φ10*16mm,P=5.0mm
11	C24	1nF/630V/X7R	MURATA	Chip Cap	1206
12	C3	E-CAP,100uF,25V		Electrolytic Cap	Φ6.3*11.5mm,P=5.0mm
13	C4	22nF/X7R/50V	MURATA	Chip Cap	0603
14	C5,C20	100nF/X7R/50V	MURATA	Chip Cap	0603
15	C6	47uF/25V/105℃	EPCOS	Electrolytic Cap	Φ5*10mm,P=2.5mm
16	C7	X2 CAP,0.33uF,305VAC	EPCOS	X2 CAP	6.0*12.0*13.0mm,P=10mm
17	C9	NC		Chip Cap	
18	D1	ES1006FL		Diode	SOD123
19	D2	100V,10A,0.64V		Diode	TO-220AC
20	D3	600V,2A,1.1V		Bridge Rectifier	KBPM
21	D4	200V,250mA (**BAS21-03W**)	Infineon	Diode	SOD323
22	F1	T2.0A/250V		Fuse	8*4mm,P=5mm
23	JP1	Φ0.6mm,L=10mm		Jumper wire	
24	JP2	Φ0.6mm,L=14mm		Jumper wire	
25	JP3	Φ0.6mm,L=20mm		Jumper wire	
26	L1	4.7uH/4.2A,	Wurth	Inductance	Φ6*8.5mm,P=2.5mm
27	L2	10mH,350mohm,0.7A	Wurth	Inductance	15mm*7.5mm*18mm
28	LED1	NC		LED	Φ3*mm,P=2.5mm
29	OT1	PHOTOCOUPLER,VOS617A		Optocoupler	
30	Q1	N MOSFET,600V,0.6Ohm (**IPD60R600P6**)	Infineon	MOSFET	DPAK
31	Q2,Q3	N MOSFET,60V,300mA,(**2N7002**)	Infineon	MOSFET	SOT23
32	R3	4.99K/0603, ±1%		Chip Resistor	0603
33	R10	2K/0603, ±1%		Chip Resistor	0603
34	R12,R13	4.99M/1206, ±1%		Chip Resistor	1206
35	R14	301K/0603, ±1%		Chip Resistor	0603
36	R17	681K/0603, ±1%		Chip Resistor	0603
37	R18	51.1K/0603, ±1%		Chip Resistor	0603
38	R19,R24	200K/0603, ±1%		Chip Resistor	0603
39	R2	39.2K/0603, ±1%		Chip Resistor	0603
40	R20,R21,R31	NC		Chip Resistor	0603
41	R22,R23	27.4K/1206, ±1%		Chip Resistor	1206
42	R25,R26	0/0603, ±1%		Chip Resistor	0603
43	R27	27R/1206, ±1%		Chip Resistor	1206
44	R4	33.2K/0603, ±1%		Chip Resistor	0603
45	R5	100K/0603, ±1%		Chip Resistor	0603
46	R6,R8,R11	10K/0603, ±1%		Chip Resistor	0603
47	R7,R15,R16	1R0/1206, ±1%		Chip Resistor	1206

48	R9	10R/1206, ±1%		Chip Resistor	1206
49	T1	RM-8 (N87) Lp=900 µH	EPCOS	Transformer	RM-8
50	U1	**ICE2QS03G**	Infineon	IC	SO-8
51	U2,U3	TL431		Regulator	SOT-23
52	VR1	S05K275,	EPCOS	Leaded varistors	7*4.3mm,P=5mm
53	Heatsink	22*15*10mm		heatsink	
54	PCB	80*30.5*1.6mm,one layer		PCB	
55	Case	89*35*27mm		Case	
56	Connector input	The plum blossom socket,ST-A04		socket	

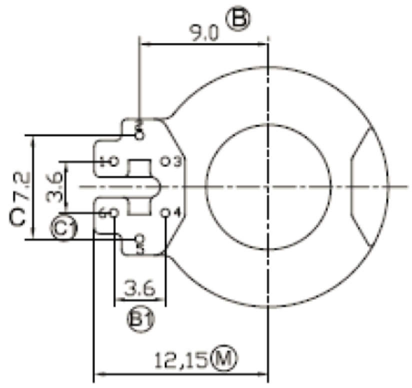
11 Transformer construction

Core and material: RM8 N87
Bobbin: RM8 with 6 pin
Primary Inductance, Lp=900 ±30 µH, measured between pin 1 and pin 3
Manufacturer and part number: EPCOS



1. S- in white teflon tube,S+ in black teflon tube
2. S- and S+ length 20mm,solder length 5mm
3. Cut pin 4 and pin 2
4. The outside of core need to parcel copper shield and connect pin 5

Winding	Start	End	No.of Turns	Wire size	Layers	Method
N1	1	2	44	1 x Ø0.35 mm	2/3 Primary	Tight
N2	S-	S+	11	2 x triple Ø0.5 mm	Secondary	Tight
N3	2	3	22	1 x Ø0.35 mm	1/3 Primary	Tight
N4	5	6	9	1 x Ø0.15 mm	Auxiliary	Tight



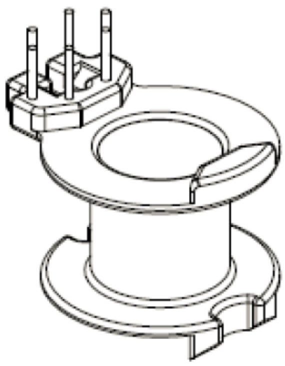


Figure 6 – Transformer structure

12 Test results

12.1 Efficiency (without 0.11Ω cable)

Vin(Vac)	Pin(W)	Vo(Vdc)	Io(A)	V_{O_ripple}(mV)	Po(W)	η(%)	Average η (%)
90	0.04360	19.03	0.000	96.40	0.00		
	4.31000	19.04	0.184	15.00	3.50	81.28	
	9.92000	19.04	0.460	27.20	8.76	88.29	88.35
	19.82000	19.04	0.920	46.30	17.52	88.38	
	29.70000	19.04	1.380	34.60	26.28	88.47	
	39.71000	19.05	1.840	72.10	35.05	88.27	
115	0.04600	19.03	0.000	99.80	0.00	0.00	
	4.34000	19.04	0.184	15.80	3.50	80.72	
	9.90000	19.04	0.460	25.40	8.76	88.47	89.09
	19.66000	19.04	0.920	49.60	17.52	89.10	
	29.48000	19.04	1.380	33.50	26.28	89.13	
	39.10000	19.05	1.840	42.70	35.05	89.65	
230	0.05938	19.03	0.000	98.00	0.00	0.00	
	4.21000	19.04	0.184	144.10	3.50	83.22	
	10.12000	19.04	0.460	22.30	8.76	86.55	88.99
	19.64000	19.04	0.920	39.60	17.52	89.19	
	29.32000	19.04	1.380	29.60	26.28	89.62	
	38.68000	19.05	1.840	32.10	35.05	90.62	
264	0.06720	19.03	0.000	100.60	0.00	0.00	
	4.21000	19.04	0.184	131.90	3.50	83.22	
	10.24000	19.04	0.460	21.80	8.76	85.53	88.49
	19.74000	19.04	0.920	39.70	17.52	88.74	
	29.42000	19.04	1.380	36.80	26.28	89.31	
	38.79000	19.05	1.840	31.10	35.05	90.36	

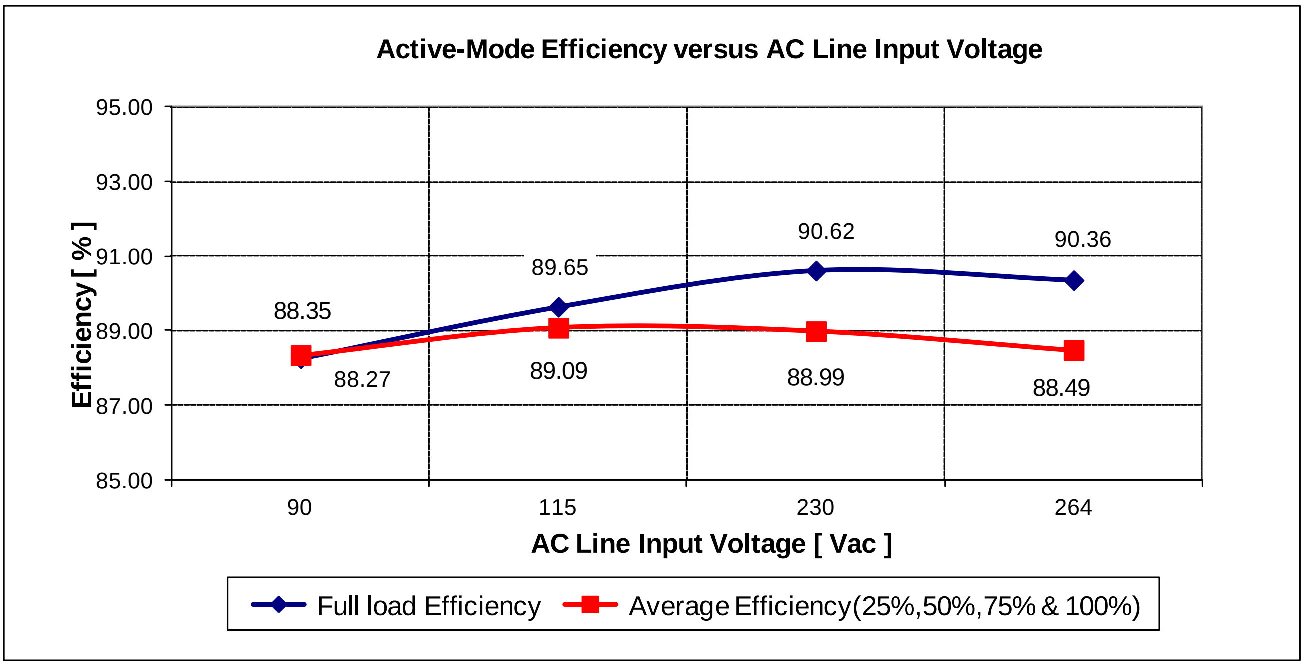


Figure 7 – Efficiency vs AC line input voltage

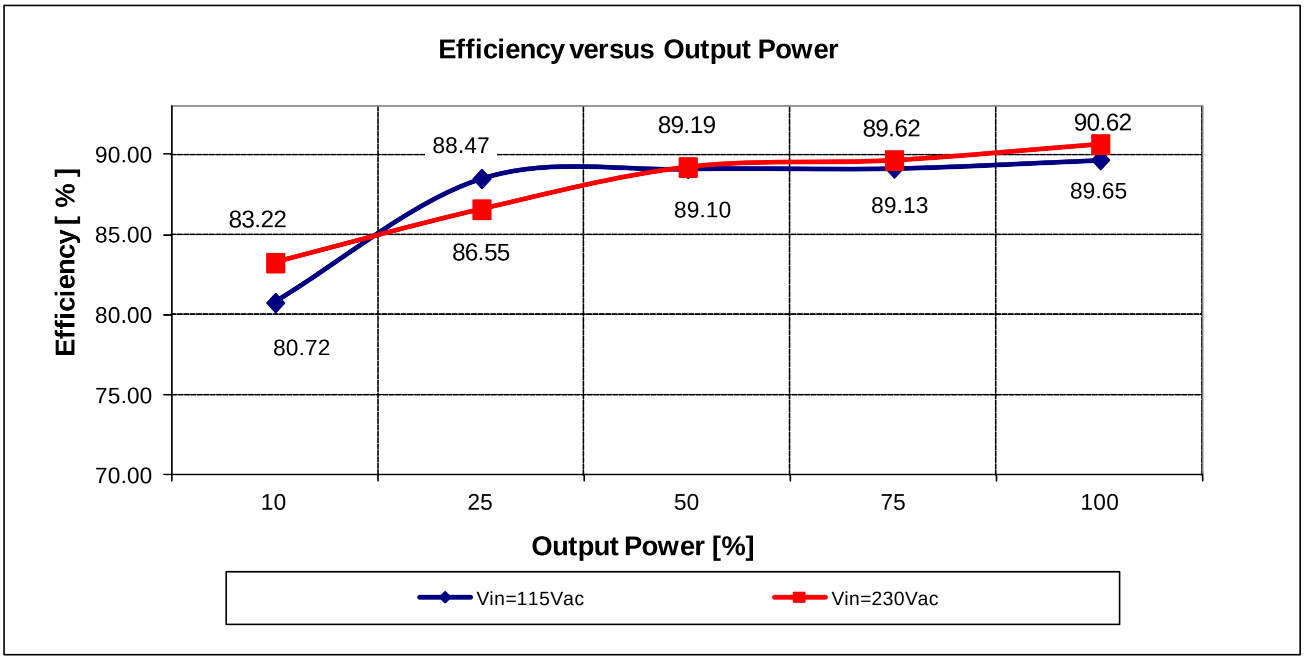


Figure 8 – Efficiency vs output power @ low and high line

12.2 Input standby power

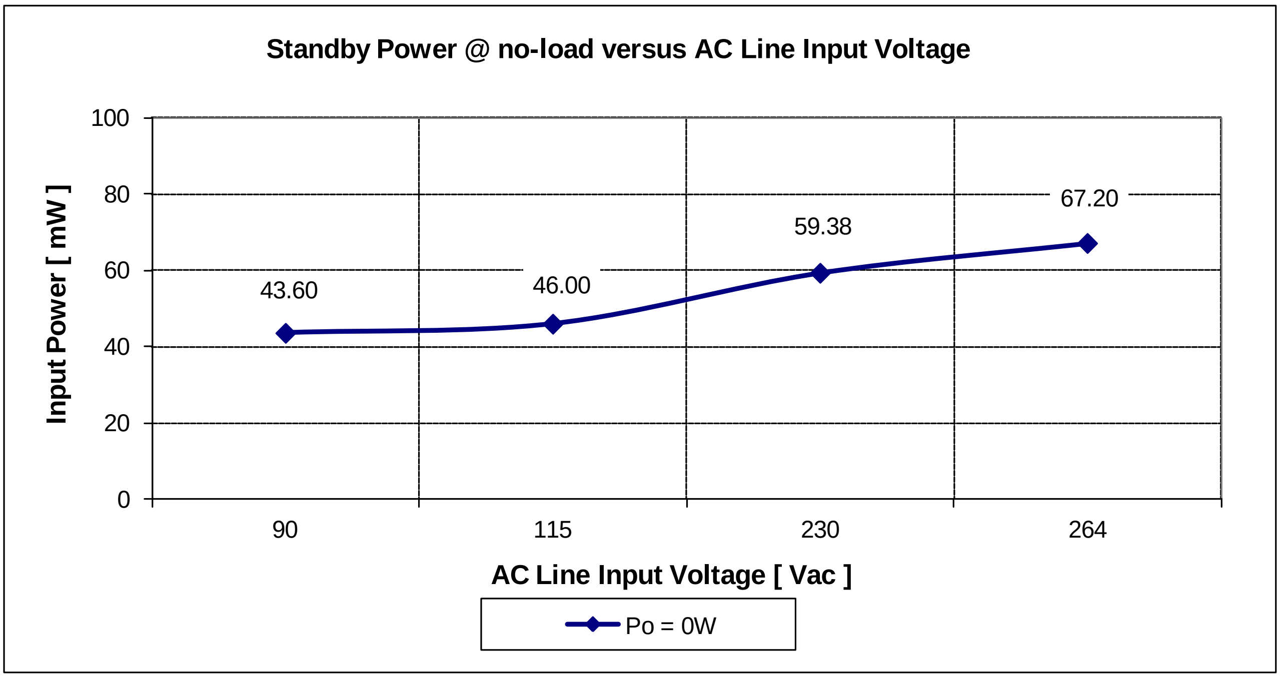


Figure 9 – Input standby power @ no load vs AC line input voltage (measured by Yokogawa WT210 power meter - integration mode)

12.3 Line regulation

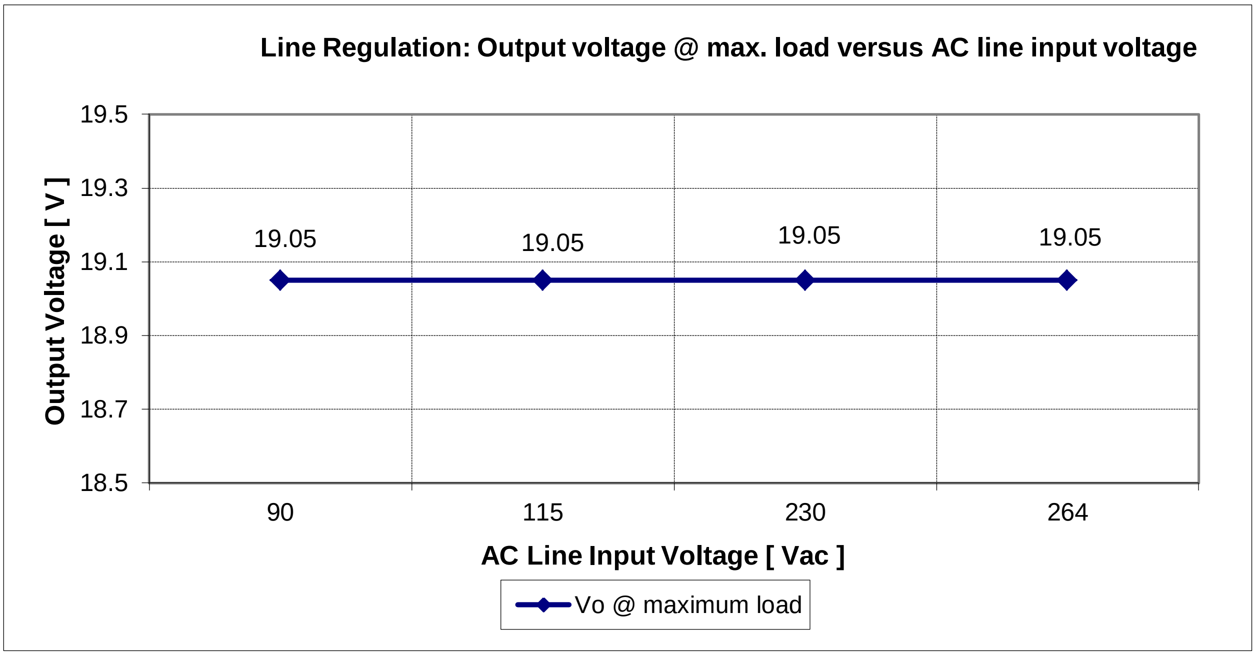


Figure 10 – Line regulation Vo @ full load vs AC line input voltage

12.4 Load regulation

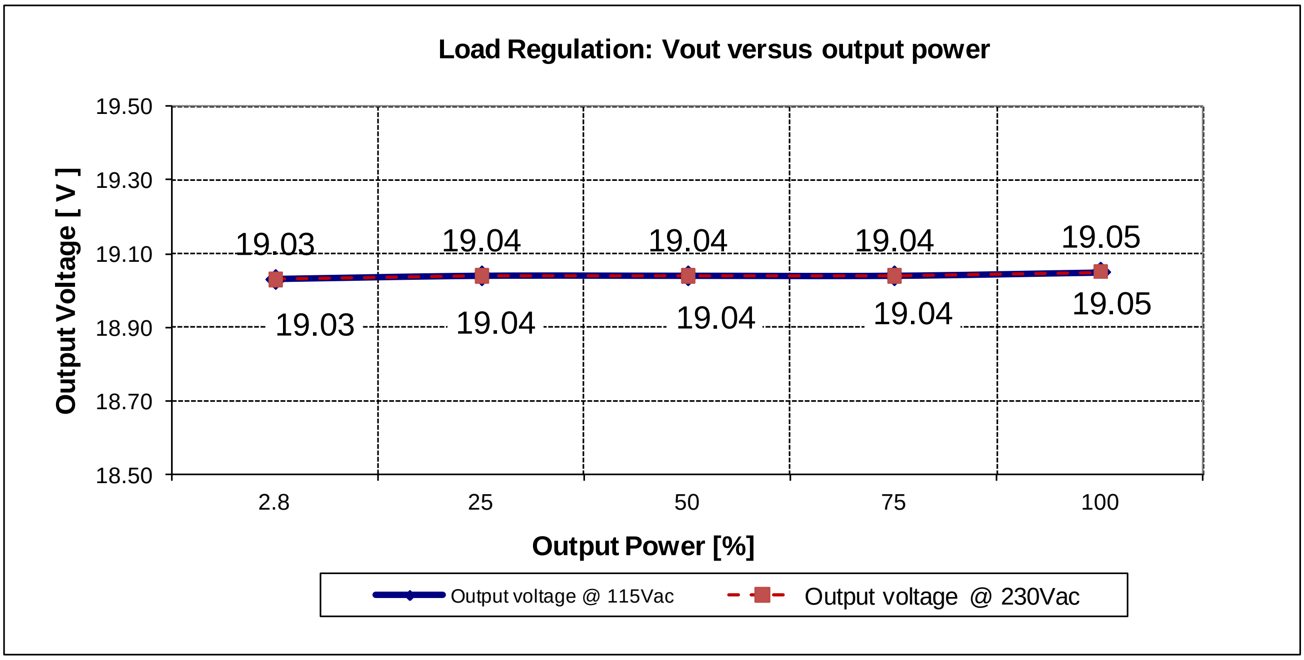


Figure 11 – Load regulation Vo vs output power

12.5 Maximum power

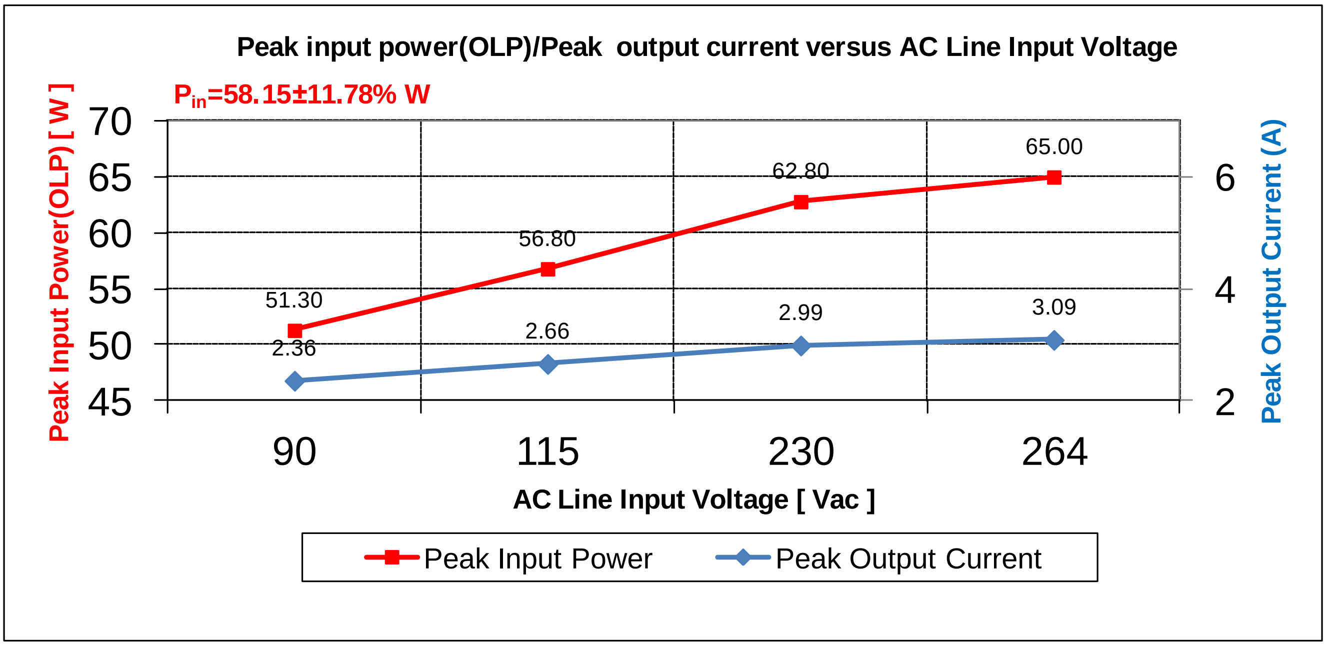


Figure 12 – Maximum output power (before over-load protection) vs AC line input voltage

12.6 ESD immunity (EN61000-4-2)

Pass EN61000-4-2 level 3 (±6kV) contact discharge

12.7 Electrical fast transient / Burst immunity (EN61000-4-4)

Pass EN61000-4-4 level 3 (±2kV)
(Note: output common is connected to ground during test)

12.8 Surge immunity (EN61000-4-5)

Pass EN61000-4-5 Installation class 3 (1kV: differential mode & 2kV: common mode)
(Note: output common is connected to ground during test)

12.9 Conducted emissions (EN55022 class B)

The conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN55022 (CISPR 22) class B. The demo board was set up at maximum load (35W) with input voltage of 115Vac and 230Vac.

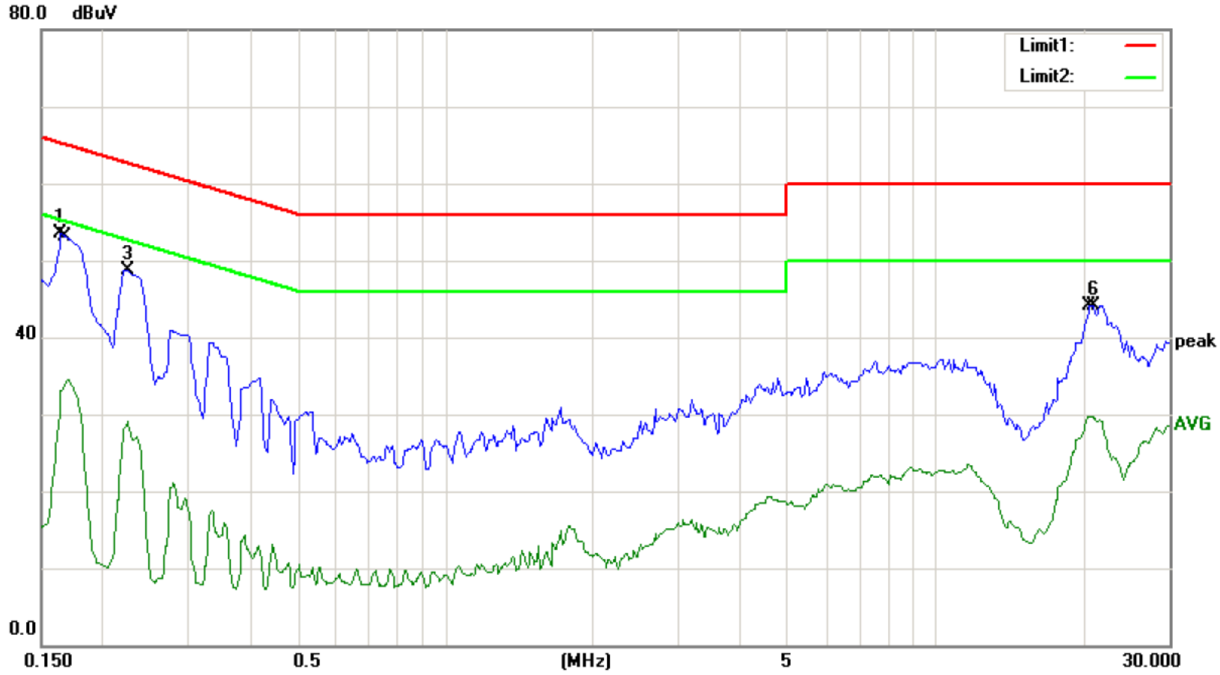


Figure 13 – Max. Load (35W) with 115 Vac (Line)

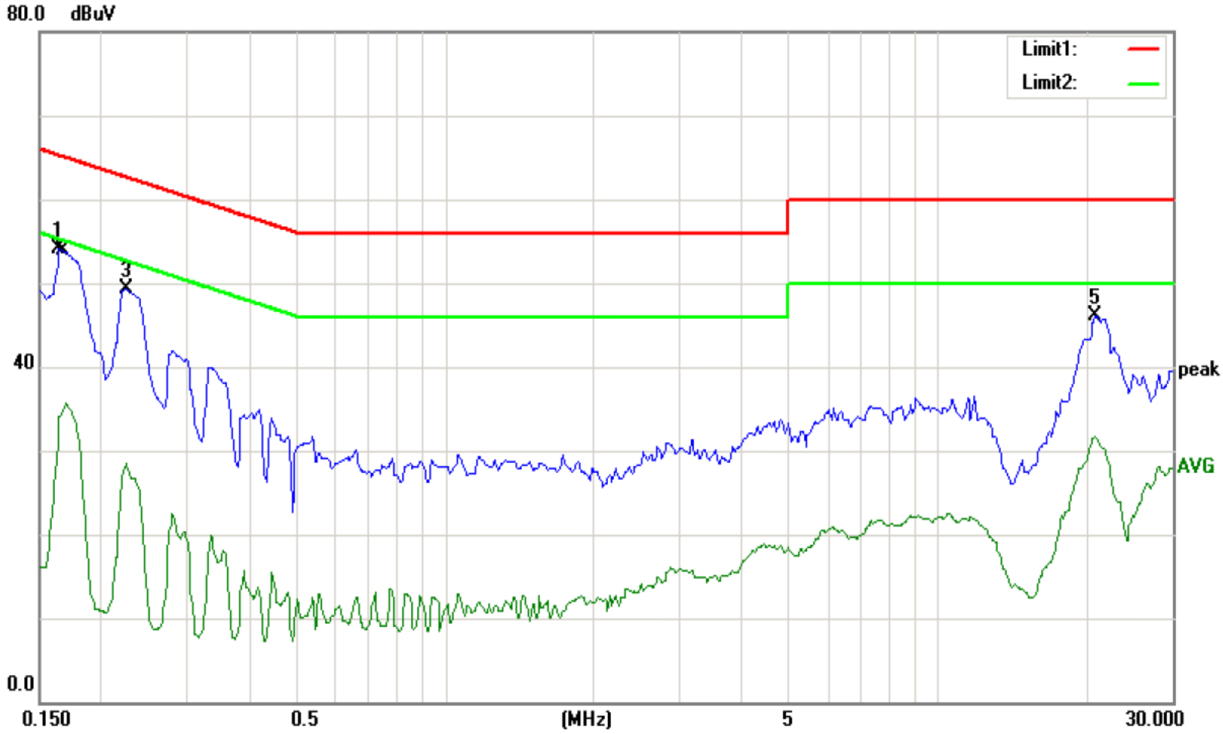


Figure 14 – Max. Load (35W) with 115 Vac (Neutral)

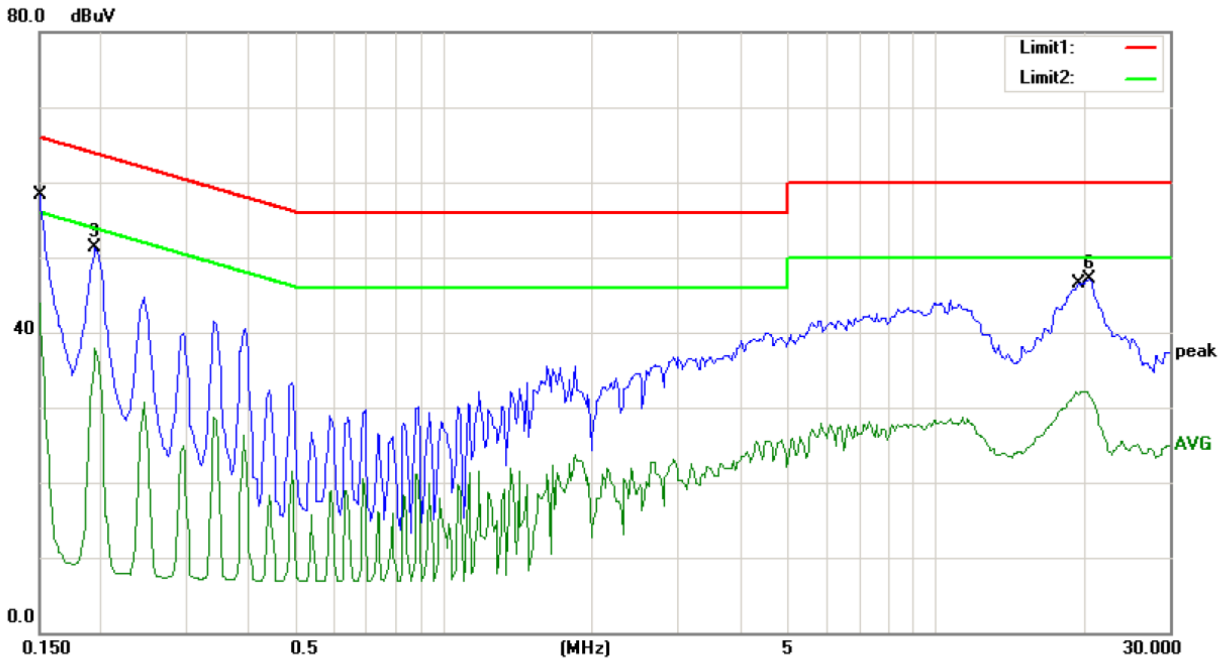


Figure 15 – Max. Load (35W) with 230 Vac (Line)

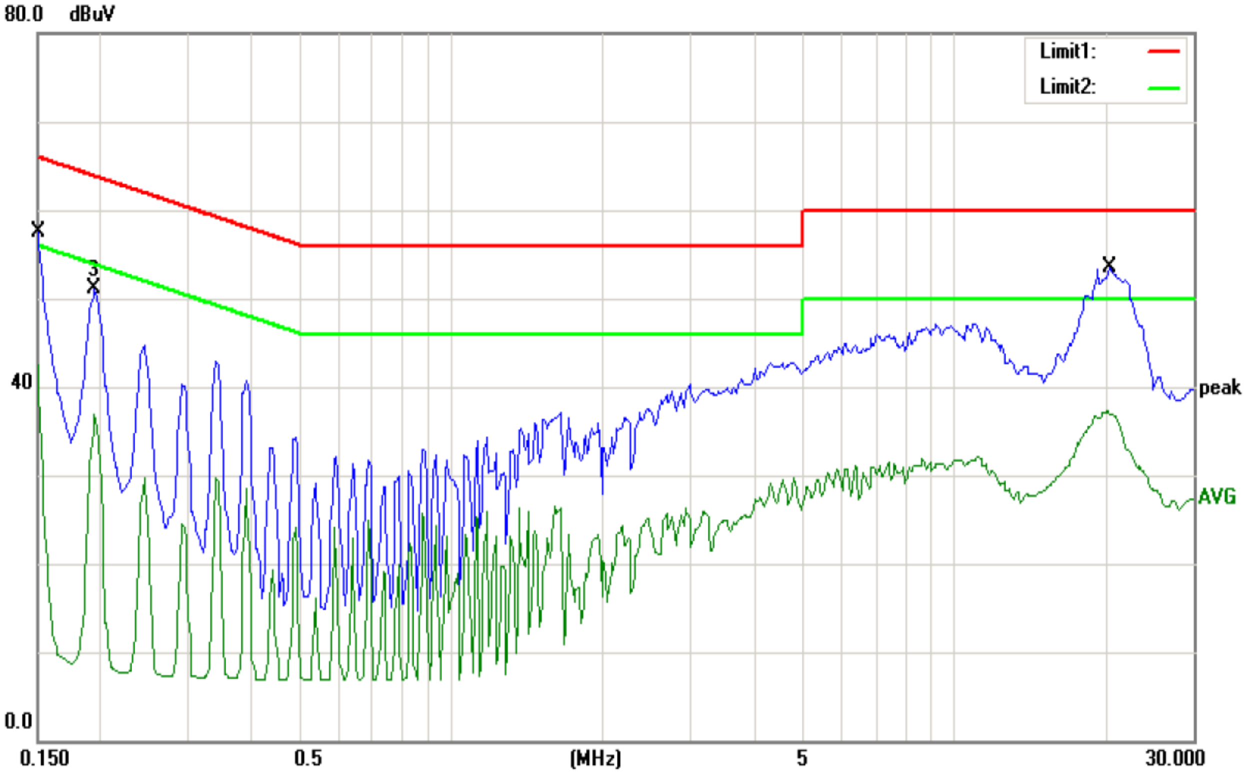


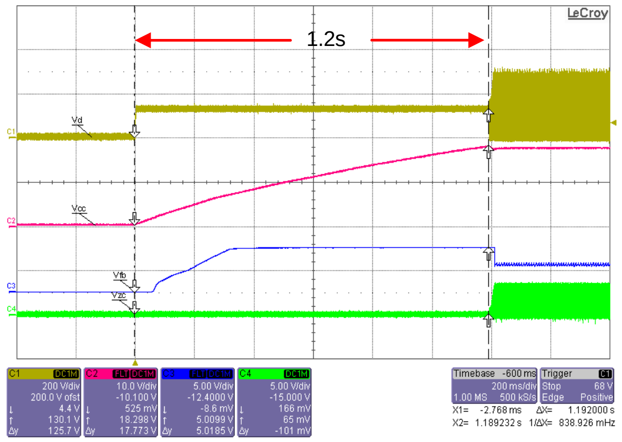
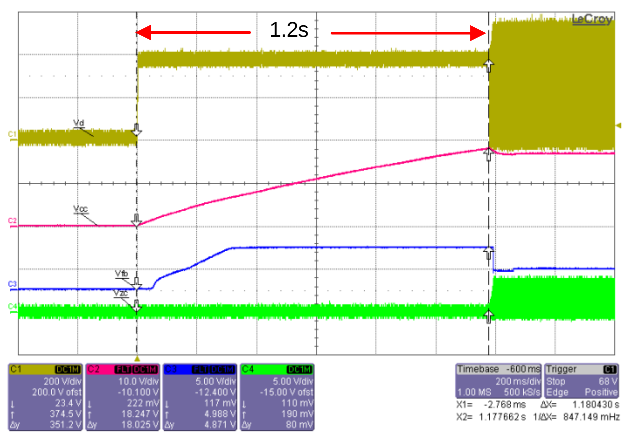
Figure 16 – Max. Load (35W) with 230 Vac (Neutral)

Pass EN55022 class B conducted emissions with > 10dB margin for QP.

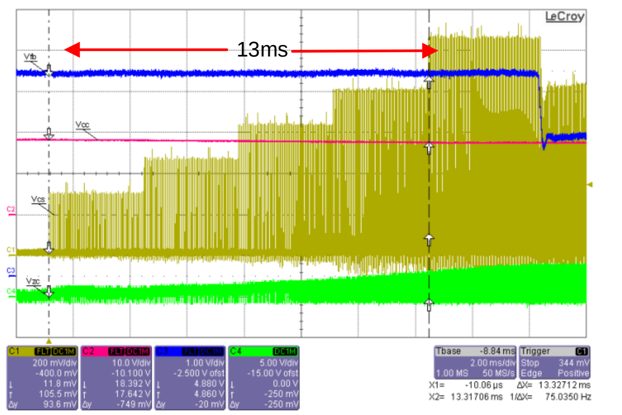
13 Waveforms and scope plots

All waveforms and scope plots were recorded with a LeCroy 6050 oscilloscope

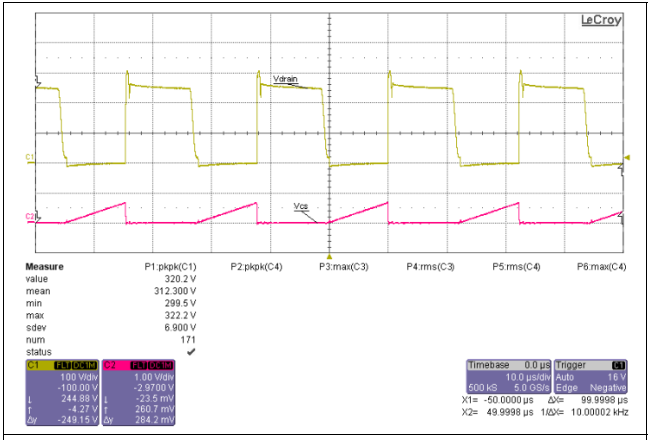
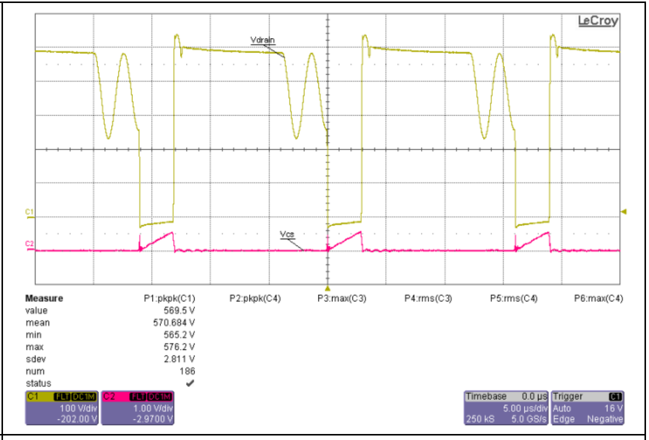
13.1 Start up at low/high AC line input voltage with maximum load

	
Channel 1; C1 : Drain voltage (V_{Drain}) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : Zero crossing voltage (V_{ZC})	Channel 1; C1 : Drain voltage (V_{Drain}) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : Zero crossing voltage (V_{ZC})
Startup time = 1.2s	Startup time = 1.2s
Figure 17 – Startup @ 90Vac & max. load	**Figure 18** – Startup @ 264Vac & max. load

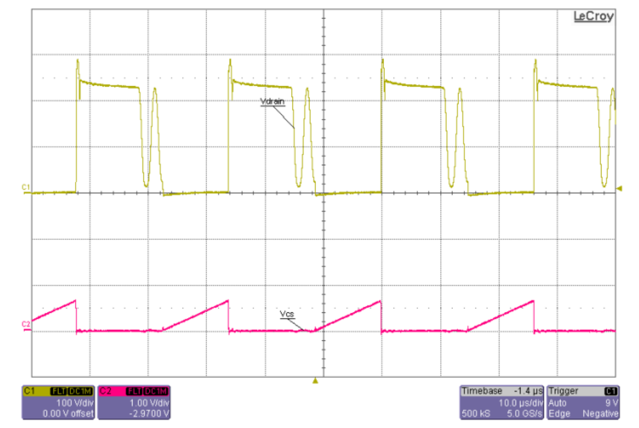
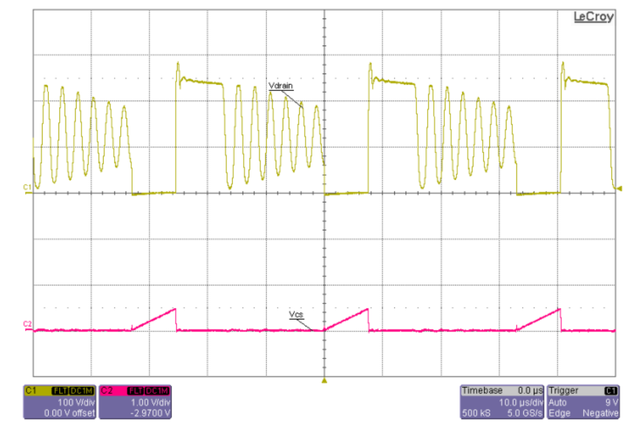
13.2 Soft start


Channel 1; C1 : Current sense voltage (V_{CS}) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : Zero crossing voltage (V_{ZC})
Soft Star time = 13ms
Figure 19 – Soft Start @ 90Vac & max. load

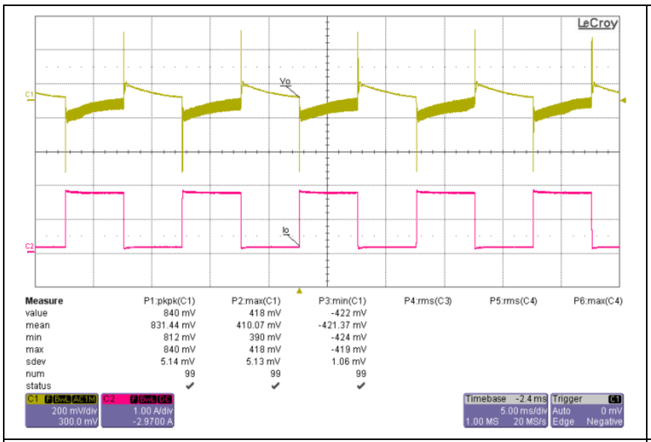
13.3 Drain voltage and current at maximum load

<table>
<tr><td>
</td><td>
</td></tr>
<tr><td>Channel 1; C1 : Drain voltage (V_{Drain})
Channel 2; C2 : Current sense voltage (V_{CS})</td><td>Channel 1; C1 : Drain voltage (V_{Drain})
Channel 2; C2 : Current sense voltage (V_{CS})</td></tr>
<tr><td>V_{Drain_peak} = 322V</td><td>V_{Drain_peak} = 576V</td></tr>
<tr><td>Figure 20 – Operation @ 90Vac and max. load</td><td>Figure 21 – Operation @ 264Vac and max. load</td></tr>
</table>

13.4 Zero crossing point during normal operation

<table>
<tr><td>
</td><td>
</td></tr>
<tr><td>Channel 1; C1 : Drain voltage (V_{Drain})
Channel 2; C2 : Current sense voltage (V_{CS})</td><td>Channel 1; C1 : Drain voltage (V_{Drain})
Channel 2; C2 : Current sense voltage (V_{CS})</td></tr>
<tr><td>Figure 22 – Operation @ 90Vac and 2nd zero crossing</td><td>Figure 23 – Operation @ 90Vac and 7th zero crossing</td></tr>
</table>

13.5 Load transient response (Dynamic load from 10% to 100%)

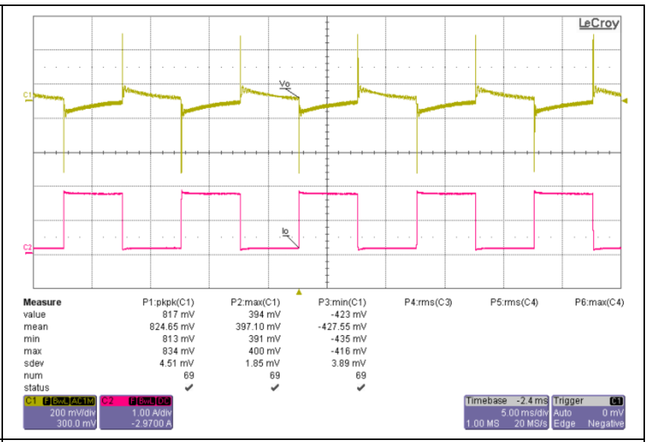


Channel 1; C1 : Output ripple voltage (Vo)
Channel 2; C2 : Output current (Io)

$V_{ripple\_pk\_pk}$=840mV (Load change from10% to 100%,100Hz,0.4A/µS slew rate)

Probe terminal end with decoupling capacitor of 0.1µF(ceramic) & 1µF(Electrolytic), 20MHz filter

Figure 24 – Load transient response @ 90Vac



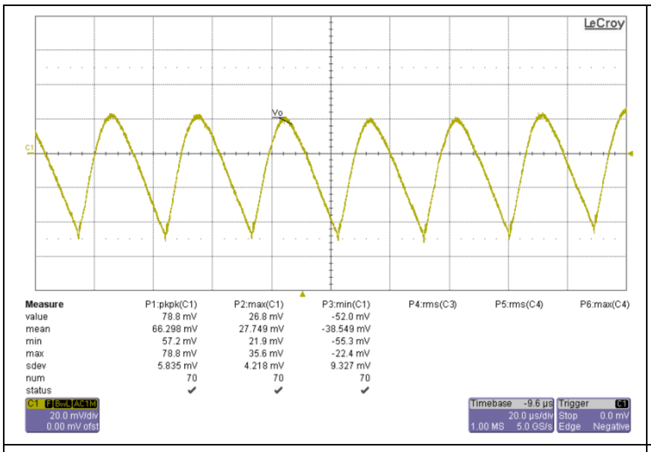
Channel 1; C1 : Output ripple voltage (Vo)
Channel 2; C2 : Output current (Io)

$V_{ripple\_pk\_pk}$=834mV (Load change from10% to 100%,100Hz,0.4A/µS slew rate)

Probe terminal end with decoupling capacitor of 0.1µF(ceramic) & 1µF(Electrolytic), 20MHz filter

Figure 25 – Load transient response @ 264Vac

13.6 Output ripple voltage at maximum load

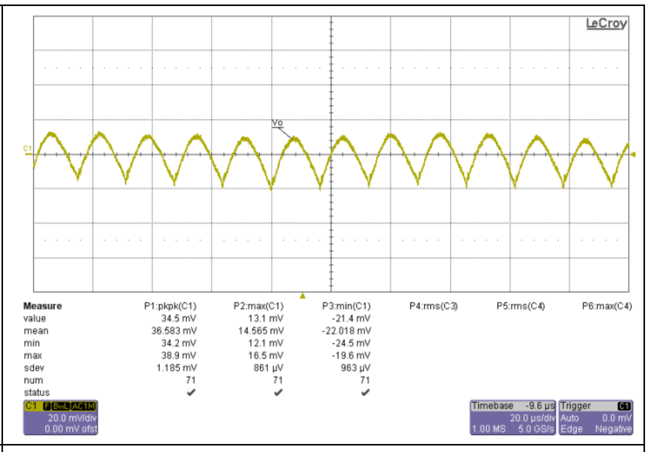


Channel 1; C1 : Output ripple voltage (Vo)

$V_{ripple\_pk\_pk}$=78.8mV

Probe terminal end with decoupling capacitor of 0.1µF(ceramic) & 1µF(Electrolytic), 20MHz filter

Figure 26 – AC output ripple @ 90Vac and max. load



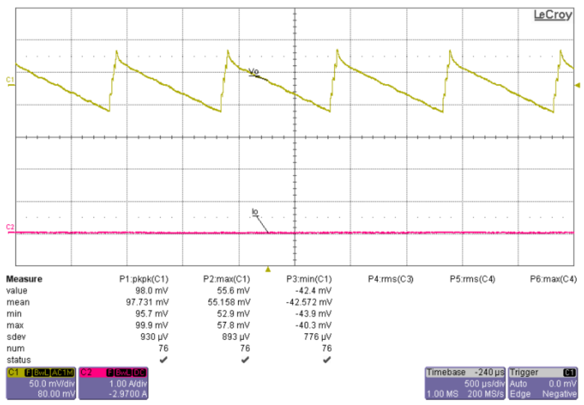
Channel 1; C1 : Output ripple voltage (Vo)

$V_{ripple\_pk\_pk}$ = 38.9mV

Probe terminal end with decoupling capacitor of 0.1µF(ceramic) & 1µF(Electrolytic), 20MHz filter

Figure 27 – AC output ripple @ 264Vac and max. load

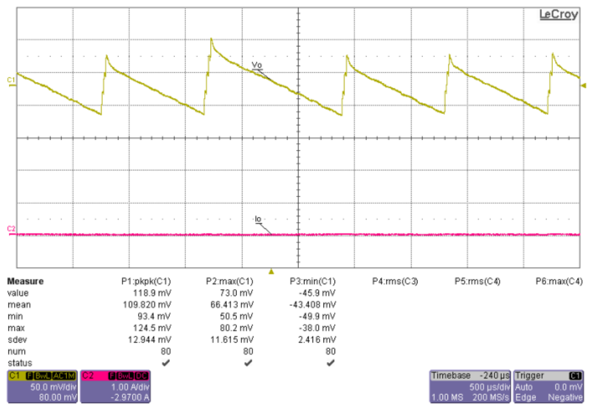
13.7 Output ripple voltage during burst mode at 1 W load



Channel 1; C1 : Output ripple voltage (Vo)

$V_{ripple\_pk\_pk}$=99.9mV
Probe terminal end with decoupling capacitor of 0.1µF(ceramic) & 1µF(Electrolytic), 20MHz filter

Figure 28 – AC output ripple @ 90Vac and 1W load

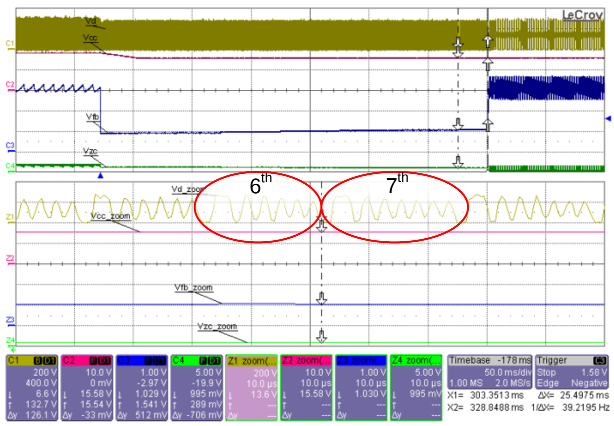


Channel 1; C1 : Output ripple voltage (Vo)

$V_{ripple\_pk\_pk}$ = 124.5mV
Probe terminal end with decoupling capacitor of 0.1µF(ceramic) & 1µF(Electrolytic), 20MHz filter

Figure 29 – AC output ripple @ 264Vac and 1W load

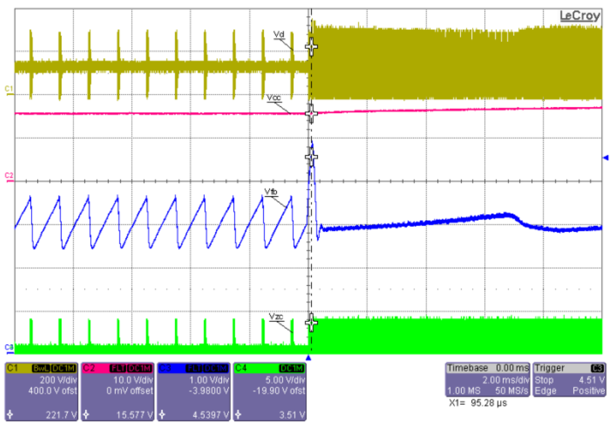
13.8 Active Burst mode operation



Channel 1; C1 : Drain voltage (V_{Drain})
Channel 2; C2 : Supply voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FB})
Channel 4; C4 : Zero crossing voltage (V_{ZC})

Condition: V_{FB}<1.219V, N_{ZC}=7 and $t_{blanking}$ =25ms
(load change form full load to 1W load)

Figure 30 – Entering active burst mode @ 90Vac

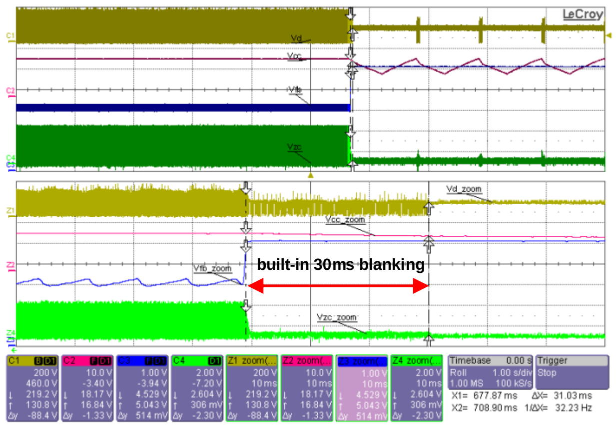


Channel 1; C1 : Drain voltage (V_{Drain})
Channel 2; C2 : Supply voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FB})
Channel 4; C4 : Zero crossing voltage (V_{ZC})

Condition: V_{FB}>4.19V
(load change from 1W to full load)

Figure 31 – Leaving active burst mode @ 90Vac

13.9 Over load protection (Auto restart mode)

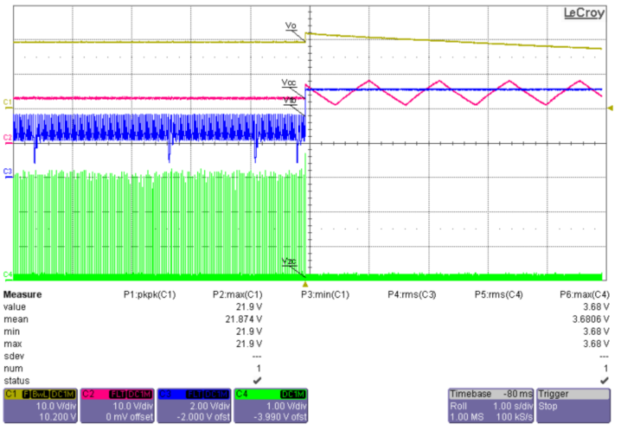


Channel 1; C1 : Drain voltage (V_{Drain})
Channel 2; C2 : Supply voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FB})
Channel 4; C4 : Zero crossing voltage (V_{ZC})

Over load protection with built-in 30ms blanking time
(output load change from full load to short load)

Figure 32 – Over load protection with extended blanking time @ 90Vac)

13.10 Output overvoltage protection (Latched off mode)

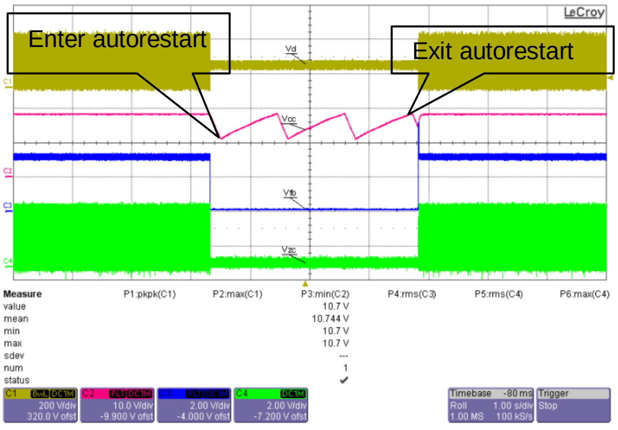


Channel 1; C1 : Output voltage (Vo)
Channel 2; C2 : Supply voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FB})
Channel 4; C4 : Zero crossing voltage (V_{ZC})

Condition: V_O >21.9V (V_{ZC}>3.7V)
(R10 disconnected during system operation at no load)

Figure 33 – Output overvoltage protection @ 90Vac

13.11 V_{CC} under voltage/Short optocoupler protection (Auto restart mode)

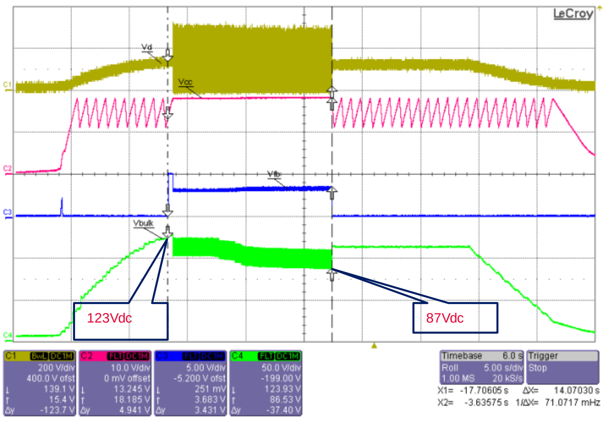
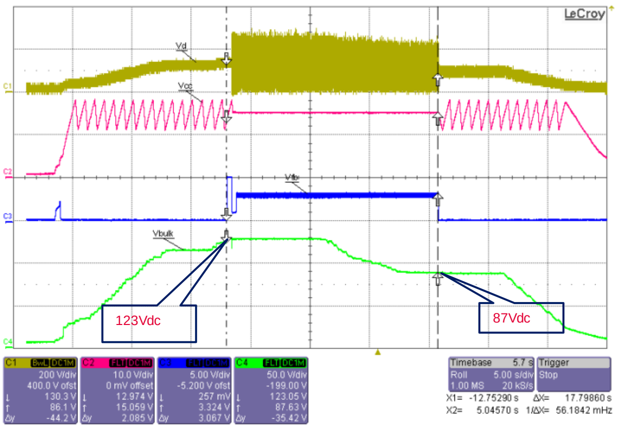


Channel 1; C1 : Drain voltage (V_{Drain})
Channel 2; C2 : Supply voltage (V_{CC})
Channel 3; C3 : Feedback voltage (V_{FB})
Channel 4; C4 : Zero crossing voltage (V_{ZC})

V_{CC} under voltage/short optocoupler protection (short the transistor of optocoupler during system operating @ full load & release)

Figure 34 – V_{cc} under voltage/short optocoupler protection @ 90Vac

13.12 Brown out protection

	
Channel 1; C1 : Drain voltage (V_{Drain}) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : Bulk voltage (V_{Bulk})	Channel 1; C1 : Drain voltage (V_{Drain}) Channel 2; C2 : Supply voltage (V_{CC}) Channel 3; C3 : Feedback voltage (V_{FB}) Channel 4; C4 : Bulk voltage (V_{Bulk})
Brownout reset: V_{bulk}= 123Vdc(87Vac) Brownout detect: V_{bulk}= 87Vdc(80Vac)	Brownout reset: V_{bulk}= 123Vdc(87Vac) Brownout detect: V_{bulk}= 87Vdc(62Vac)
Figure 35 – Brownout mode with max. load	**Figure 36** – Brownout mode with no load

14 References

[1] ICE2QS03G data sheet, Infineon Technologies AG

[2] IPD60R600P6 data sheet, 600V CoolMOS™ P6 Power Transistor

[3] BAS21-03W data sheet, Infineon Technologies AG

[4] 2N7002 data sheet, Infineon Technologies AG

[5] Converter Design Using the Quasi-Resonant PWM Controller ICE2QS01, Infineon Technologies AG, 2006. [ANPS0003]

[6] Design tips for flyback converters using the Quasi-Resonant PWM controller ICE2QS01, Infineon Technologies, 2006. [ANPS0005]

[7] Determine the switching frequency of Quasi-Resonant flyback converters designed with ICE2QS01, Infineon Technologies, 2006. [ANPS0004]

[8] ICE2QS03G design guide. [ANPS0027]

[9] 36W Evaluation Board with Quasi-Resonant PWM Controller ICE2QS03G, 2011. [AN-PS0040]

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