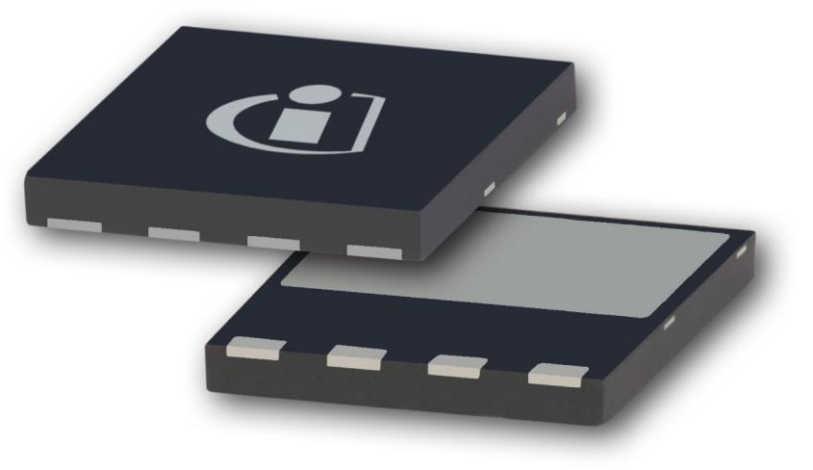
Recommendations for Printed Circuit Board Assembly of Infineon VDSON Packages (ThinPAK)



Application Note

Infineon VDSON Packages (ThinPAK)

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Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

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1. Package Description

The PG-VDSON (Plastic Green High Voltage Small Single Outline Package) is a near chip-scale plastic encapsulated package with a copper leadframe and pads at the bottom of the package to provide electrical and thermal contact to the printed circuit board.
The PG-VDSON (alias ThinPAK) is a leadless package consuming smaller area for high voltage applications compared to e.g. packages like D²PAK

Characteristics

- Small package outline 8x8 mm²
- Low profile 1 mm
- Exposed drain pad for optimized heat transfer to the PCB
- Pads with Pb-free solder plating (electroplated Sn)

Figure 1 shows a photo of PG-VDSON-4 packages (alias (ThinPAK 8x8). Visible are the 4 small Source/Gate-Pads, which show exposed copper at the package side wall (due to package singulation) and the big exposed drain pad which is fully surrounded by mold compound.

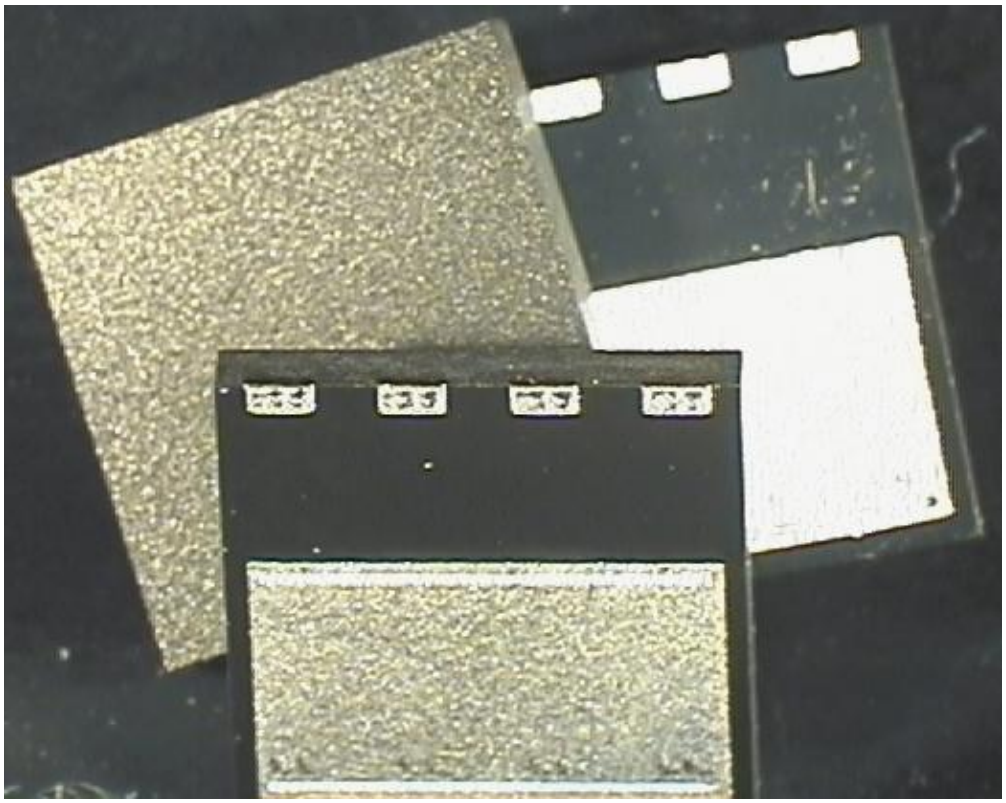


Figure 1: Top and bottom view of VDSON-4 (ThinPAK 8x8)

2. Package Handling

ESD Protective Measurement

Semiconductor devices are normally Electrostatic Discharge Sensitive Devices (ESDS devices) requiring specific precautionary measures regarding handling and processing. Discharging of electrostatically charged objects over an Integrated Circuit (IC) can be caused by human touch or by processing tools, resulting in high-current and/or high-voltage pulses that can damage or even destroy sensitive semiconductor structures. On the other hand, ICs may also be charged during processing. If discharging takes place too quickly ("hard" discharge), it may cause load pulses and damage, too. ESD protective measures must therefore prevent contact with charged parts as well as electrostatic charging of the ICs. Protective measures against ESD must be taken during handling, processing, and the packing of ESDS. A few hints are provided below on handling and processing.

i. ESD Protective Measures in the Workplace

- Standard marking of ESD protected areas
- Access controls, with wrist strap and footwear testers
- Air conditioning
- Dissipative and grounded floor
- Dissipative and grounded working and storage areas
- Dissipative chairs
- Earth ("ground") bonding points for wrist straps
- Trolleys or carts with dissipative surfaces and wheels
- Suitable shipping and storage containers
- No sources of electrostatic fields

ii. Equipment for Personnel

- Dissipative/conductive footwear or heel straps
- Suitable smocks
- Wrist straps with safety resistors
- Gloves or finger coats that are ESD-proven (with specified volume resistivity)

Regular training of staff to avoid ESD failures using this equipment is recommended.

iii. Production Installations and Processing Tools

- Machine and tool parts made of dissipative or metallic materials
- No materials having thin insulating layers or sliding tracks
- All parts reliably connected to ground potential
- No potential difference between individual machine and tool parts
- No sources of electrostatic fields

Detailed information on ESD-protective measures may be obtained from the ESD Specialist through Area Sales Offices. Our recommendations are based on the internationally applicable standards IEC 61340-5-1 and ANSI/ESD S2020.

Packing of Components

Different packings such as fixtures for feeding components in an automatic pick&place machine (tape&reel, trays,...) and surrounding bags and boxes to prevent damage during transportation or strorage are available depending on component and customer needs. Please refer to product and package specifications (on the IFX homepage) and our sales department to get information about what packing is available for a given product.
Generally the following list of standards dealing with packing should be considered if applicable for a given package and packing:
IFX packings according to the IEC 60286-* series

IEC 60286-3	Packaging of components for automatic handling – Part 3: Packaging of surface mount components on continuous tapes.
IEC 60286-4	Packaging of components for automatic handling – Part 4: Stick magazines for dual-in-line packages.)
IEC 60286-5	Packaging of components for automatic handling – Part 5: Matrix trays

Moisture-sensitive Surface Mount Devices (SMDs) are packed according to IPC/JEDEC J-STD-033*: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

Detailed Packing Drawings ⇨ Packing Information (Internet)

Other References:

ANSI/EIA-481-*	Standards Proposal No. 5048, Proposed Revision of ANSI/EIA-481-B "8mm through 200mm Embossed Carrier Taping and 8mm & 12mm Punched Carrier Taping of Surface Mount Components for Automatic Handling (if approved, to be published as ANSI/EIA-481-C).
EIA-783	Guideline Orientation Standard for Multi-Connection Package (Design Rules for Tape and Reel Orientation)

Moisture-sensitive Components (MSL Classification)

For moisture-sensitive packages, it is necessary to control the moisture content of the components. Penetration of moisture into the package molding compound is generally caused by exposure to ambient air. In many cases, moisture absorption leads to moisture concentrations in the component that are high enough to damage the package during the reflow process. Thus it is necessary to dry moisture-sensitive components, seal them in a moisture-resistant bag, and only remove them immediately prior to assembly to the Printed Circuit Board (PCB). The permissible time (from opening the moisture barrier bag until the final soldering process) that a component can remain outside the moisture barrier bag is a measure of the sensitivity of the component to ambient humidity (Moisture Sensitivity Level, MSL). The most commonly applied standard IPC/JEDEC J-STD-033* defines eight different MSLs (see
Table 1). Please refer to the "Moisture Sensitivity Caution Label" on the packing material, which contains information about the moisture sensitivity level of our products. IPC/JEDEC-J-STD-20 specifies the maximum reflow temperature that shall not be exceeded during board assembly at the customer's facility.

Table 1: Moisture Sensitivity Levels (acc. to IPC/JEDEC J-STD-033*)

Level	Floor Life (out of bag)	
	Time	Conditions
1	Unlimited	≤30°C/85% RH
2	1 year	≤30°C/60% RH
2a	4 weeks	≤30°C/60% RH
3	168 hours	≤30°C/60% RH
4	72 hours	≤30°C/60% RH
5	48 hours	≤30°C/60% RH
5a	24 hours	≤30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤30°C/60% RH

If moisture-sensitive components have been exposed to ambient air for longer than the specified time according to their MSLs, or the humidity indicator card indicates too much moisture after opening a Moisture Barrier Bag (MBB), the components have to be baked prior to the assembly process. Please refer to IPC/JEDEC J-STD-033* for details. Baking a package too often can cause solderability problems due to oxidation and/or intermetallic growth. In addition, packing material (e.g. trays, tubes, reels, tapes,…) may not withstand higher baking temperatures. Please refer to imprints/labels on the respective packing to determine allowable maximum temperature.

For Pb-free components, two MSLs can be given: One for a lower reflow peak temperature (Pb-containing process) and one for a higher reflow peak temperature (Pb-free). Each one is valid for the respective application.

Storage and Transportation Conditions

Improper transportation and unsuitable storage of components can lead to a number of problems during subsequent processing, such as poor solderability, delamination, and package cracking effects.

These standards should be taken into account:

IEC 60721-3-0	Classification of environmental conditions: Part 3: Classification of groups of environmental parameters and their severities; introduction.
IEC 60721-3-1	Classification of environmental conditions: Part 3: Classification of groups of environmental parameters and their severities; Section 1: Storage
IEC 60721-3-2	Classification of environmental conditions: Part 3: Classification of groups of environmental parameters and their severities; Section 2: Transportation
IEC 61760-2	Surface mounting technology – Part 2: Transportation and storage conditions of surface mounting devices (SMD) – Application guide.
IEC 62258-3	Semiconductor Die Products – Part 3: Recommendations for good practise in handling, packing and storage
ISO 14644-1	Clean rooms and associated controlled environments Part 1: Classification of airborne particulates

General storage conditions – overview:

Product	Condition for storage
Wafer/die	N2 or MBB (IEC 62258-3)
Component – moisture-sensitive	MBB (JEDEC J-STD-033*)
Component - not moisture-sensitive	1K2 (IEC 60721-3-1)

(MBB = Moisture Barrier Bag)

Maximum storage time:
The conditions to be complied with in order to ensure problem-free processing of active and passive components are described in standard IEC 61760-2.

Internet Links to Standards Institutes:

American National Standards Institutes (ANSI)

Electronics Industries Alliance (EIA)

Association Connecting Electronics Industries (IPC)

Handling Damage and Contamination

Automatic or manual handling of components in or out of the component packing may cause mechanical damage to package leads and/or body.
VDSON components in the packing are ready to use.

Any contamination applied to component or packing may cause or induce processes that (together with other factors) may lead to a damaged device. The most critical issues are:

- Solderability problems
- Corrosion
- Electrical shorts (due to conductive particles)

Component Solderability

The sufficiently thick and wettable metal surfaces (final plating) or solder depots/balls of most semiconductor packages assure good solderability, even after a long storage time. **Note that the cut edges of the pins should be ignored in any assessment of solderability.** Suitable methods for the assessment of solderabiltiy can be derived from JESD22B 102 or IEC60068-2-58.

VDSON components are tin-plated and are compatible with Pb-containing and Pb-free soldering.

3. Printed Circuit Board

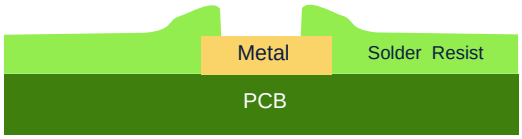
Routing

The PCB design and construction are key factors for achieving highly reliable solder joints. For example, VDSON packages should not be placed at the same opposite locations on either side of the PCB (if double-sided mounting is used), because this results in a stiffening of the assembly with earlier solder joint fatigue compared to a design in which the component locations are offset. Furthermore, it is known that the board stiffness itself has a significant influence on the reliability (temperature cycling) of the solder joint interconnect, if the system is used in critical temperature cycling conditions.

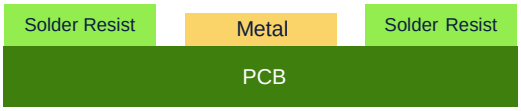
PCB Pad Design

The solder pads have to be designed to assure optimum manufacturability and reliability. Two basic types of solder pads are commonly used:

- „Solder Mask Defined“ (SMD) pad: The copper pad is larger than the solder mask opening above this pad. Thus the land area is defined by the opening in the solder mask.



- „Non-Solder Mask Defined“ (NSMD) pad: Around each copper pad there is solder mask clearance. It is necessary to specify the dimensions and tolerances of the solder mask clearance so that no overlapping of the solder pad by solder mask occurs (depending on PCB manufacturers’ tolerances, 75 µm is a widely used value).



A VDSON package features a metallic drain-pad at the bottom side, which serve to conduct a large amount of heat into the PCB to achieve higher thermal performance and therefore has to be completely soldered to the PCB. The drain pad can be soldered 1:1 by area or split by rectangular solder mask openings, so-called “pockets” which can serve to reduce solder joint voiding. In any case, the stencil aperture size under the drain pad has to be reduced to avoid device tilting.
In high-current applications or those having high thermal dissipation, source pads also require highest possible contact area to the PCB.

In case of VDSON package, SMD pads are the preferred solution. In applications in which high currents in combination with high temperatures can occur, large conductor cross-sections are preferable to avoid electro migration.

Internal studies have demonstrated that VDSON packages show good self-alignment during reflow soldering process using the following recommended layout for reflow soldering. For a suitable wave soldering for VDSON package, please refer to chapter 5

Figure 2 shows the recommended PCB pad design for reflow soldering of VDSON-4, including appropriate dimensions.
Please note that the recommendations can only give dimensions for the solder mask openings. Generally the copper dimensions depend on the capability of the board manufacturer. For high current applications the copper dimensions for drain and source pads should be chosen as big as possible to enlarge the conductor cross-sections. These also serve for heat dissipation.
Please note that there is no exact congruency of PCB pads and package pads.

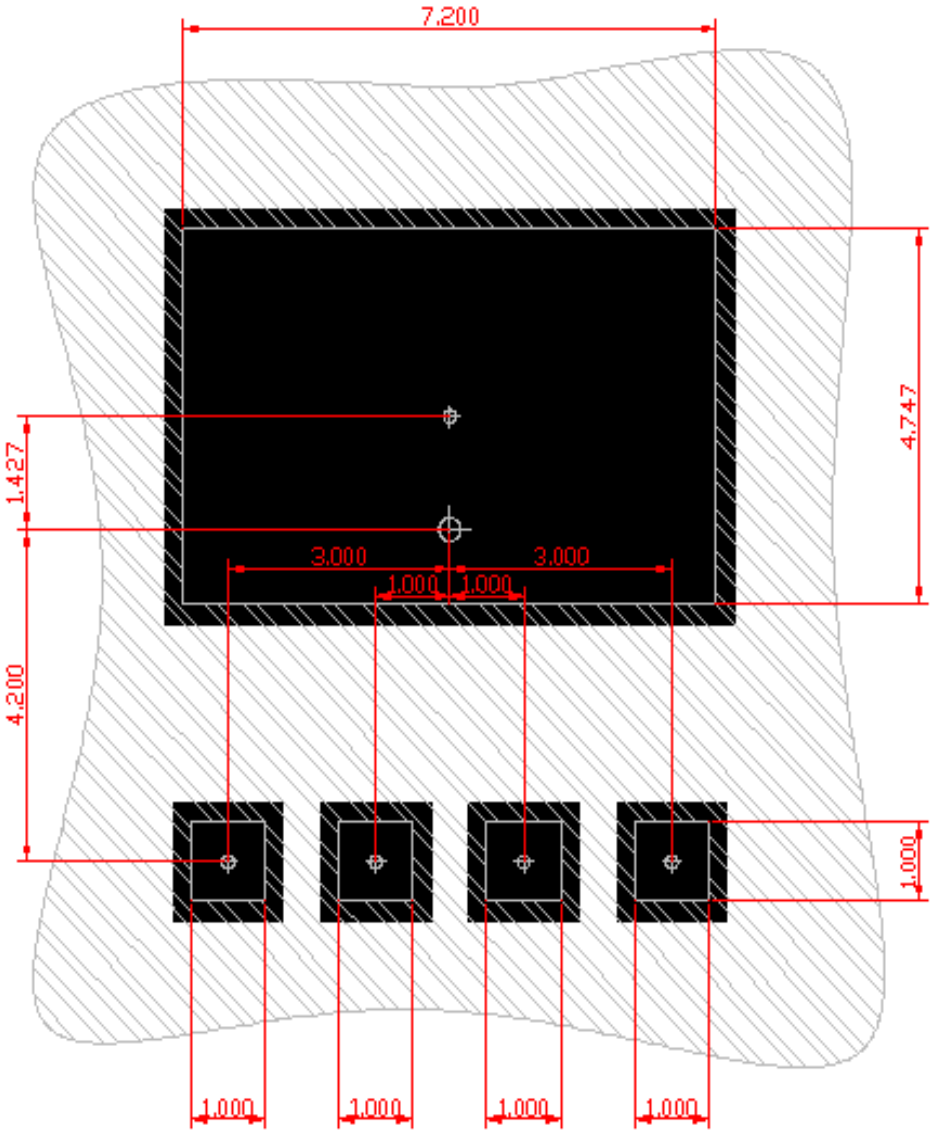


Figure 2: Recommended PCB pad design for reflow soldering of VDSON-4

To connect the exposed die pad thermally and electrically directly to inner and/or bottom copper planes of the board, plated through-hole vias are used. They help to distribute the heat into the board area, which spreads from the chip over the package die pad and the solder joint to the thermal pad on the board.
A typical hole diameter for such thermal vias is 0.2 to 0.4 mm. This diameter and the number of vias in the thermal pad depend on the thermal requirements of the end product, the power consumption of the product, the application and the construction of the PCB. However, an array of thermal vias with pitch 1.0-1.2 mm can be a reasonable starting point for further optimization of most products/applications. Thermal and electrical analysis and/or testing are recommended to determine the minimum number needed.

If the vias remain open during board manufacturing, solder may flow into the vias during board assembly ("solder wicking"). This results in lower stand-off (which is mostly controlled by the solder volume between the package die pad and thermal pad on the PCB), and/or solder protruding from the other side of the board, which may interfere with a second solder paste printing process on this opposite board side. To prevent solder beading, a wettable surface surrounding these vias at the opposite board side should be provided to act as a buffer for the surplus solder (decreasing of solder paste amount may prevent this effect, but can also lead to an increased voiding rate).
Under certain conditions (e.g. insufficient wetting of copper plated vias), open vias could have the effect of large voids in the "thermal" solder joint under the die pad, but in general the open vias serve as venting holes for gas in the solder joint.

If necessary, solder wicking can be avoided by plugging (filling with epoxy) and overplating the vias. With very small vias, so-called "microvias" (approx. 100 µm), it is generally sufficient to overplate the via and get a filling by copper. In both cases, it is necessary to specify a planar filling. However, flat dents tend to increased voiding. They serve as traps for voids forming during reflow soldering.
Another method is called "tenting." The vias in this case are covered with solder mask (e.g. dry-film solder mask). Via tenting must be done from top, because when via tenting is done only from the bottom side, the voiding rate could be significantly higher. Combined with an intelligent solder mask layout for the thermal pad, this method leads to good processability and balanced solder joints.

If it is not necessary to have a direct connection from the solder pad under the exposed die pad to the inner layers of the PCB, the vias should be placed near the package and covered with solder mask.

Pad Surfaces

The solder pads have to be easy for the the solder paste to wet. In general, all finishes are well-proven for Surface Mount Technology Assembly (SMTA). Using a Hot Air Solder Leveling (HASL) finish (Pb-free or Pb-containing HASL), a certain unevenness has to be taken into account. Other platings are completely "flat" (e.g. Cu-OSP, electroless Sn or NiAu) and therefore are preferred when fine-pitch components are used on the PCB.
From a package point of view, it is difficult to recommend a certain PCB pad finish that will always meet all requirements. The choice of finish also depends strongly on board design, pad geometry, all components on the board, and process conditions, and must be chosen accordingly to the specific needs of the customer.
Infineon's internal tests have shown that Cu-OSP and NiAu are quite effective platings. Due to the higher cost of NiAu, Cu-OSP is recommended for mass production.

Table 2: Typical PCB pad finishes

Finish	Typical Layer Thickness [µm]	Properties	Concerns
HASL (SnAg) (*Hot Air Solder Leveling*)	› 5	Low cost, widely used, well known in fabrication	Uneven surface, formation of humps, flatness of single pads has to be good for fine-pitch applications
Electroless Tin	0.3 – 1.2	Solder joint consists only of copper and solder, no further metal is added to the solder joint	Long-term stability of protection may be a concern, baking of PCB may be critical
Electroless Silver	0.2 - 0.5	Solder joint consists only of copper and solder, no further metal is added to the solder joint	Long-term stability of protection may be a concern, baking of PCB may be critical
Electroless Ni / Immersion Au (*ENIG*)	3 – 7 / 0.05 – 0.15	Good solderability protection, high shear force values	Expensive, concerns about brittle solder joints
Galvanic Ni / Au	› 3 / 0.1 – 2	Only for thicker layers, typically used for connectors	Expensive, not recommended for solder pads
OSP (*Organic Solderability Preservatives*)	Typical 1	Low cost, simple, fast and automated fabrication	Must be handled carefully to avoid damaging the OSP; not as good long-term stability as other coatings; in case of double-sided assembly only suitable with inert gas during reflow

4. PCB Assembly using solder paste printing and reflow soldering (SMT)

SMDs are typically used in so-called Surface Mount Technology. Used processes are solder paste printing, pick-and-place and reflow soldering.
Internal investigations have shown that the VDSON can also be suitable for wave soldering, which is typically used in Through Hole Technology (THT).
Chapter 4 is only dealing with SMT. For wave soldering of VDSON please refer to chapter 5

Solder Stencil

The solder paste is applied onto the PCB metal pads by stencil printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. Too much solder paste will cause solder bridging, whereas too little solder paste can lead to insufficient solder wetting between all contact surfaces. In most cases the thickness of a stencil has to be matched to the needs of all components on the PCB. For VDSON packages, 100- to 150-µm thick stencils are recommended. To ensure a uniform and high solder paste transfer to the PCB, laser-cut stencils (mostly made from stainless steel) should be preferred.
The apertures in general should be of the same size and shape as the metal pads on the PCB. However, different sizes of board pads result in device tilting. Therefore the amount of solder/solder paste on the exposed pad has to be reduced. Furthermore the squeegee bends down into larger openings so that a thinner solder paste layer is deposited. To reduce this effect, the stencil opening for the exposed drain pad can be segmented into smaller areas ("pockets").
Infineon's internal investigations showed that the ratio between stencil openings and drain pad can vary between 40% and 80%. The ideal amount of solder depends on stencil thickness, PCB pad finish, via layout, and solder paste.
The best results were achieved with a PCB having no vias in pad, a stencil thickness of 120 µm and the stencil apertures given in Figure 3.

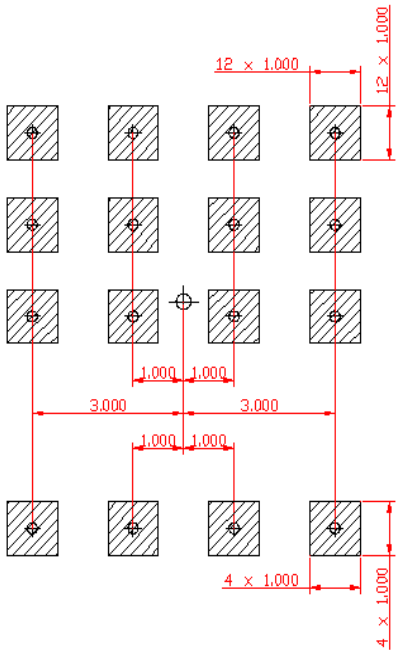


Figure 3: Recommended dimensions of solder paste stencil for VDSON-4

Solder paste consists of solder alloy and a flux system. Normally the volume is split into about 50% alloy and 50% flux and solvents. In term of mass, this means approximately 90 wt% alloy and 10 wt% flux system and solvents. The flux system has to remove oxides and contamination from the solder joints during the soldering process. The capacity for removing oxides and contamination is given by the respective activation level.
The contained solvent adjusts the viscosity needed for the solder paste application process. The solvent has to evaporate during reflow soldering.
The metal alloy in Pb-containing solder pastes is typically eutectic SnPb or nearly eutectic SnPbAg. Pb-free solder pastes contain so-called SAC-alloys (typically 1-4% Ag and <1% Cu). A "no-clean" solder paste is preferred for packages such as VDSON where cleaning below the component is difficult.
The paste must be suitable for printing the solder stencil aperture dimensions; type 3 paste is recommended.
Solder paste is sensitive to age, temperature, and humidity. Please follow the handling recommendations of the paste manufacturer.

Component Placement

Although the self-alignment effect due to the surface tension of the liquid solder will support the formation of reliable solder joints, the components have to be placed accurately according to their geometry. Positioning the packages manually is not recommended but is possible, especially for packages with big terminals and pitch. An automatic pick&place machine is recommended to get reliable solder joints, .
Component placement accuracies of +/-50 µm are obtained with modern automatic component placement machines using vision systems. With these systems, both the PCB and the components are optically measured and the components are placed on the PCB at their programmed positions. The fiducials on the PCB are located either on the edge of the PCB for the entire PCB or additionally on individual mounting positions (local fiducials). These fiducials are detected by a vision system immediately before the mounting process.
Recognition of the packages is performed by a special vision system, enabling the complete package to be centered correctly.

The maximum tolerable displacement for a VDSON is high. Typically 20% to 30% of the PCB pad width are acceptable. For a VDSON this would mean 200 to 300 µm which is far more than typical placement accuracies of pick-and-place systems.

The following factors are important:

- Especially on large boards, local fiducials close to the device can compensate for PCB tolerances.
- The lead recognition capabilites of the placement system should be used rather than the outline centering. Outline centering can only be used for packages where the tolerances between pad and outline are small compared to the placement accuracy needed. In case of VDSON also outline recognition is suitable

- To ensure the identification of the packages by the vision system, adequate lighting as well as the correct choice of measuring modes is necessary
- Too much placement force can squeeze out solder paste and cause solder shorts. On the other hand, not enough placement force can lead to insufficient contact between package and solder paste and may result in insufficient sticking of the component on the solder paste, which may then lead to shifted or dropped devices
- A pick-up nozzle suitable for the package body size should be used. The nozzle should be slightly smaller than the package body. A bigger nozzle may lead to an irregular force distribution, especially to increased forces at the edges of the package body. On the other hand, a nozzle that is too small may lead to increased forces in the package center. Package bodies that are divided into different areas that have different heights require special care when choosing the nozzle. Nozzle shape and size are probably more critical in these cases. In case of VDSON nozzles can be rectangular or round. Their size should be between 4 and 7 mm. Please take into account that smaller nozzle may give insufficient vacuum values

Reflow Soldering

Soldering determines the yield and quality of assembly fabrication to a very large extent. Generally all standard reflow soldering processes have these features:

- Forced convection (max. qualified profile given by the JEDEC MSL classification)
- Vapor phase
- Infrared (with restrictions)

and typical temperature profiles are suitable for board assembly of the VDSON packages.

During the reflow process, each solder joint has to be exposed to temperatures above the solder melting point or “liquidus” for a sufficient time to get the optimum solder joint quality, whereas overheating the PCB with its components has to be avoided. Please refer to the bar code label on the packing for the peak package body temperature. When using infrared ovens without convection, special care may be necessary to assure a sufficiently homogeneous temperature profile for all solder joints on the PCB, especially on large, complex boards with different thermal masses of the components. The recommended type of process is forced convection reflow. Using a nitrogen atmosphere can generally improve solder joint quality, but is normally not necessary for soldering tin-lead metal alloys.

The temperature profile of a reflow process is one of the most important factors of the soldering process. It is divided into several phases, each with a special function. Figure 4 shows a general forced convection reflow profile for soldering VDSON packages. Table 3 shows an example of the key data of such a solder profile that has been used for the Sn-Pb and for the Pb-free alloy listed above. Individual parameters are influenced by various facts, not only by the package. It is essential to follow the solder paste manufacturer’s application notes, too. Additionally, most PCBs contain more than one package type and therefore the reflow profile has to be matched to all components’ and materials’ demands. We recommend measuring the solder joints’ temperatures by thermocouples beneath the respective packages. Consider that components with large thermal masses do not heat up at the same speed as lightweight

components, and the position and the surrounding of the package on the PCB as well as the PCB thickness can also influence the solder-joint temperature significantly. Therefore, these reflow profiles should serve as guidelines, but have to be further adjusted to each actual application.

Because the thermal impact of reflow is critical for Pb-free solder pastes, linear temperature profiles can be applied to achieve a shorter reflow time in total. When reducing the soaking time, it is very important to ensure a homogeneous temperature distribution on the PCB; in this case, a convection oven is recommended.

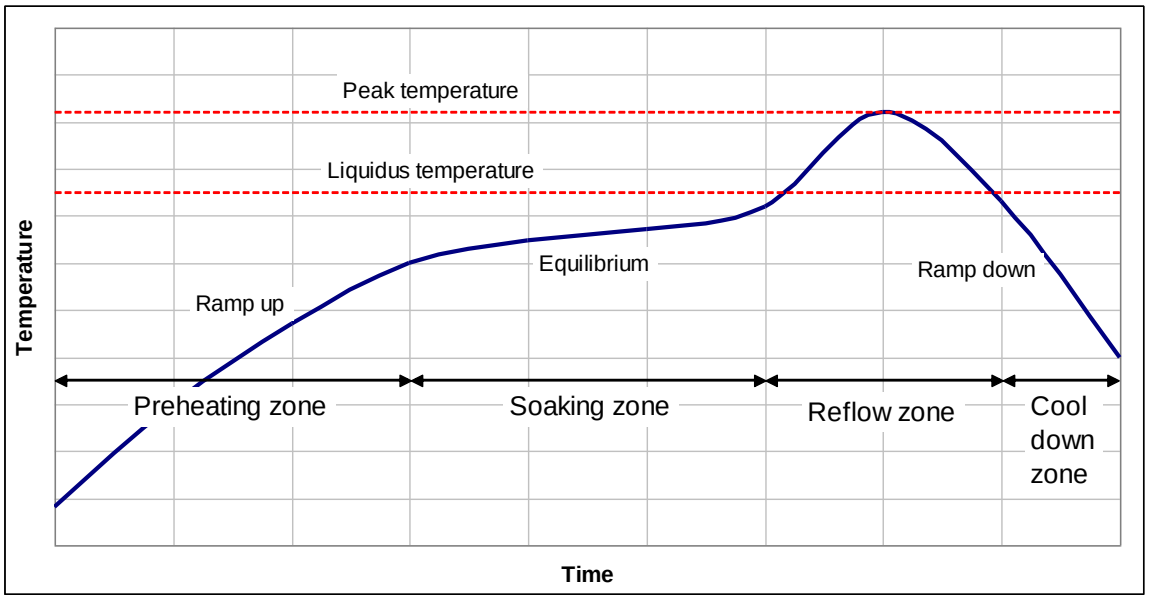


Figure 4: General forced-convection reflow solder profile

Table 3: Example of the key data of a forced-convection reflow solder profile

Parameter	Tin-lead alloy (SnPb or SnPbAg)	Pb-free alloy (SnAgCu)	Main influences coming from …
Preaheating rate	2.5 K/s	2.5 K/s	Flux system (solder paste)
Soaking temperature	140-170°C	140-170°C	Flux system (solder paste)
Soaking time	80 s	80 s	Flux system (solder paste)
Peak temperature	225°C	245°C	Alloy (solder paste)
Reflow time above melting point (liquidus)	60 s	60 s	Alloy (solder paste)
Cool-down rate	2.5 K/s	2.5 K/s	

Double-Sided Assembly

VDSON packages are generally suitable for mounting on double-sided PCBs. First, the board assembly is done on one side of the PCB (including soldering). Afterwards, the second side of the PCB is assembled.
If the solder-joint thickness is a critical dimension, please be aware that solder joints of components on the first side will be reflowed again in the second reflow step. In the reflow zone of the oven (i.e. where the solder is liquid), the components are only held by wetting forces from the molten solder. Gravity acting in the opposite direction will elongate the solder joints, unlike joints on the top side, where gravity forces the components nearer to the PCB surface). This shape will be frozen at temperatures below the melting point of solder and therefore result in a higher stand-off on the bottom side after the reflow process. Heavy vibrations in a reflow oven may cause devices to drop off the PCB.

5. Wave soldering

Wave soldering of VDSON is possible, but the position of the SMD glue has to be chosen carefully. Internal investigations have proven that a proper pad layout and glue dispensing pattern can be found to have a good processability of VDSON prior and during wave soldering.

Regarding the ability of a given product in VDSON to be wave soldered, please refer to the product data sheet or ask your local IFX-sales, marketing or application engineer.

Process Flow for SMDs with wave soldering

Before SMD packages can be wave soldered, they have to be attached to the PCB by glue. The sequence for this is showing in (Figure 5: Attachment of SMDs prior to wave soldering.):

1. Setting of glue dots
2. Placement of SMDs
3. Curing of adhesive
4. Turning PCB
5. Double wave soldering of SMDs

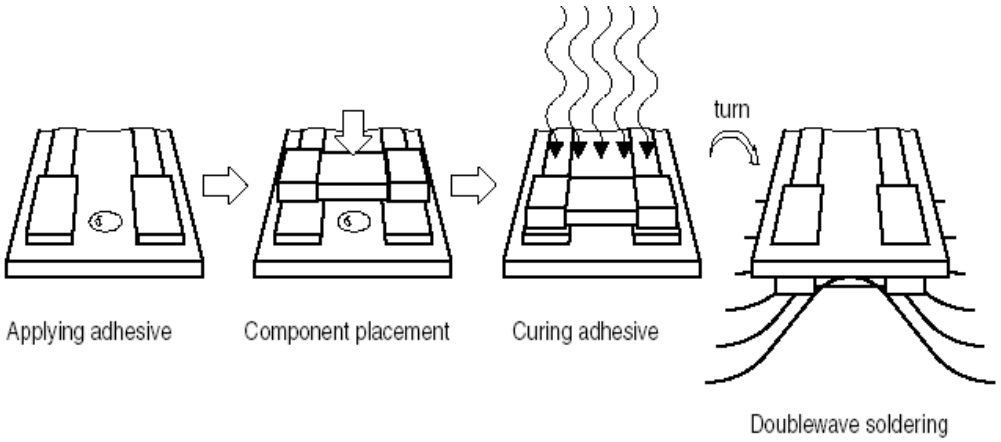


Figure 5: Attachment of SMDs prior to wave soldering.

PCB design and SMT-glue dot application for wave soldering

A special PCB design is needed to give good soldering results in terms of wetting behaviour, voiding rate and co-planarity of the device.
The PCB pad design in Figure 6 provides two positions/areas for application of SMT-glue dots, which should be located half underneath the package and half protruding to have on one side optimum adhesion. On the other side the protruding glue dot supports visual inspection.
The glue should not spread over the wettable surface of pads. Even if the surface seems to be free of glue a so-called bleading can contaminate the surface and may lead to non-wetting.
The glue dot volume has to be chosen accordingly. A too small volume may lead to poor adhesion, a too big volume may spread too much and contaminates PCB or component pads.

After SMT-glue dispensing the component has to be assembled onto the PCB (please refer to section o). During touchdown placement force has to be controlled in order to prevent too much squeeze-out of the SMT-glue.
Subsequently the SMT-glue has to be cured. Typically THDs are assembled afterwards and the PCB is ready for wave soldering.
Please note that the given board pad layout is suitable and tested for a transport direction given in Figure 6.

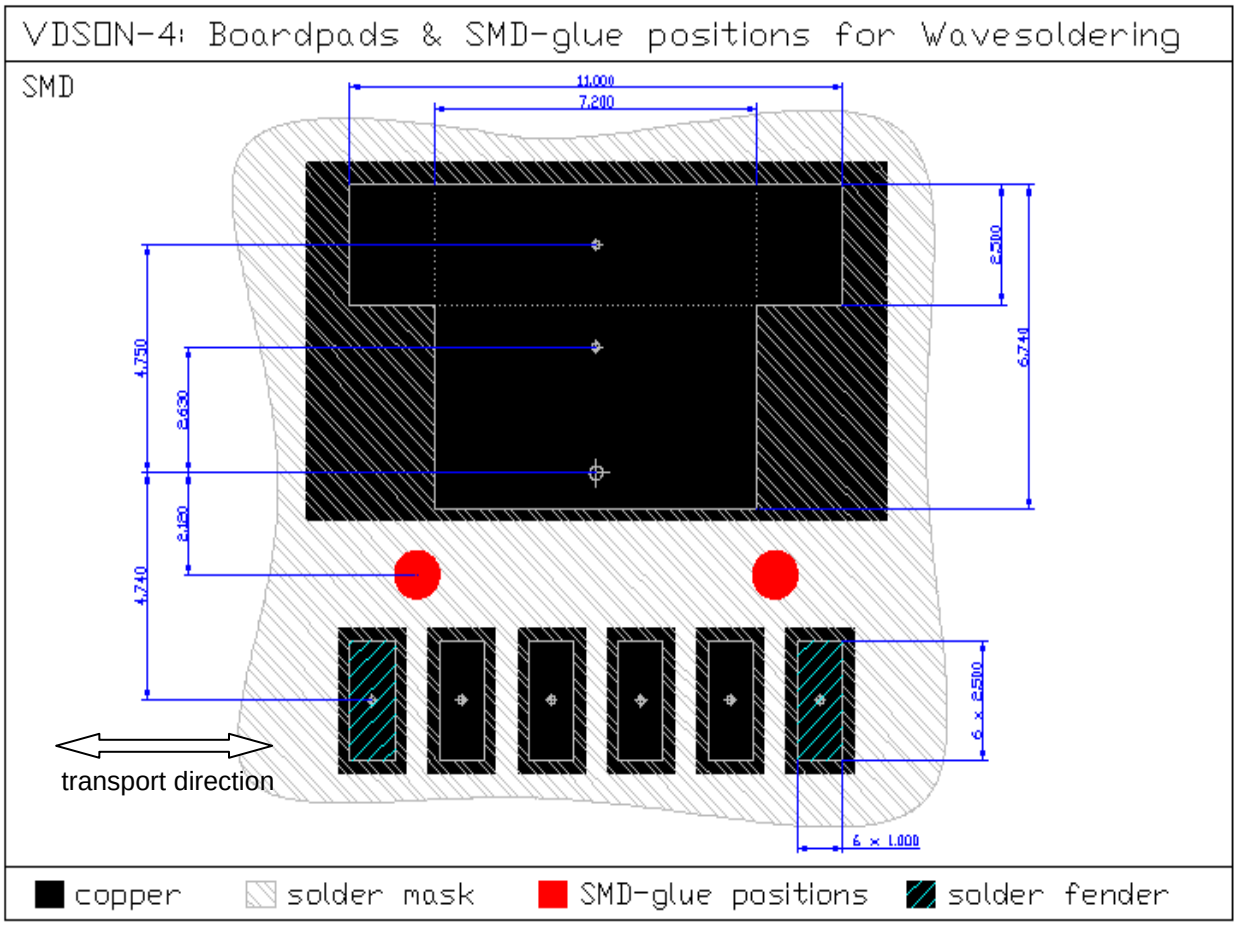


Figure 6: PCB pad design for wave soldering of VDSON-4 with SMD-glue positions and solder fender

Wave soldering profile

There are many types of wave soldering machines. However, the basic components and principles of these machines are the same. A standard wave solder machine consists of three zones: the fluxing zone, the preheating zone, and the soldering zone. An additional fourth zone is used for the cleaning of the board, depending on the used flux type..

Dual-wave soldering is the most commonly used method. Figure 7 shows a typical temperature profile. The peak temperatures, ramp rates, and times depend on the materials and the wave soldering equipment used.

The first wave has a turbulent flow and therefore guarantees wetting of nearly all shapes of leads and board pads, but also creates some solder bridges. These solder bridges have to be removed by the second wave, which has a laminar flow.
When using lead-free solder alloys, a nitrogen atmosphere is recommended.

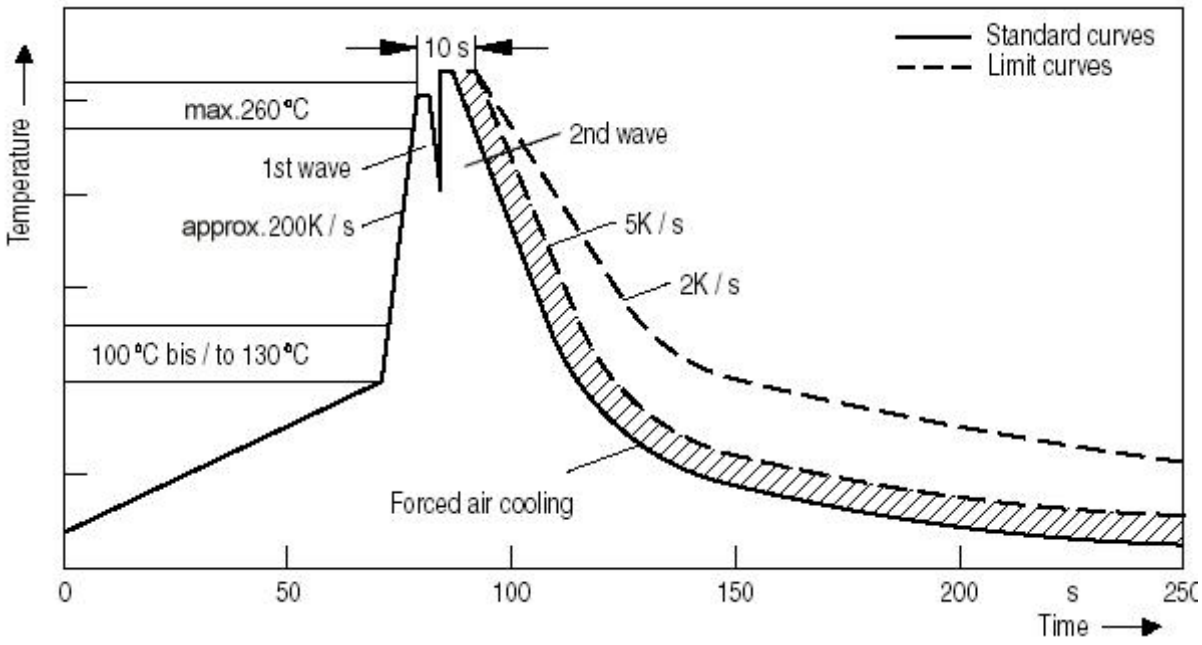


Figure 7: Typical dual-wave soldering profile

6. Cleaning

After the reflow soldering process, some flux residues can be found around the solder joints. If a “no-clean” solder paste has been used for solder paste printing, the flux residues usually do not have to be removed after the soldering process. Be aware that cleaning beneath a VDSON package is difficult because of the small gap between package substrate and PCB and is therefore not recommended. If the solder joints have to be cleaned, the cleaning method (e.g. ultrasonic, spray or vapour cleaning) and solution have to be selected in consideration of the packages to be cleaned, the flux used in the solder paste (rosin-based, water-soluble, etc.), and environmental and safety aspects. Even small residues of the cleaning solution should be removed/dried very thoroughly. Contact the solder paste manufacturer for recommended cleaning solutions.

7. Inspection

Compared to typical SMD components that have gullwing leads the solder joints of VDSON packages are mainly formed underneath the package. The leads end directly at the component body edge. A visual inspection of the solder joints with conventional Automatic Optical Inspection (AOI) systems is limited to the outer surface of the solder joints. Since the non-wetting of the package lead front-side walls is not a reject criteria, the significance of an optical inspection is limited. Figure 8 shows solder joints of a VDSON-4. For the gate and source pads the visibility is limited because the leads do not protrude beyond the package body. The drain solder joint (= exposed pad) is fully covered by the package body and therefore not visible anyway. For the acceptability of electronic assemblies inspected optically, please refer also to the IPC-A-610 standard. Please note that VDSON packages are not included up to now in this standard and that therefore the specifications have to be taken more as a general guideline for solder joint inspection, than as specific rules for VDSON.

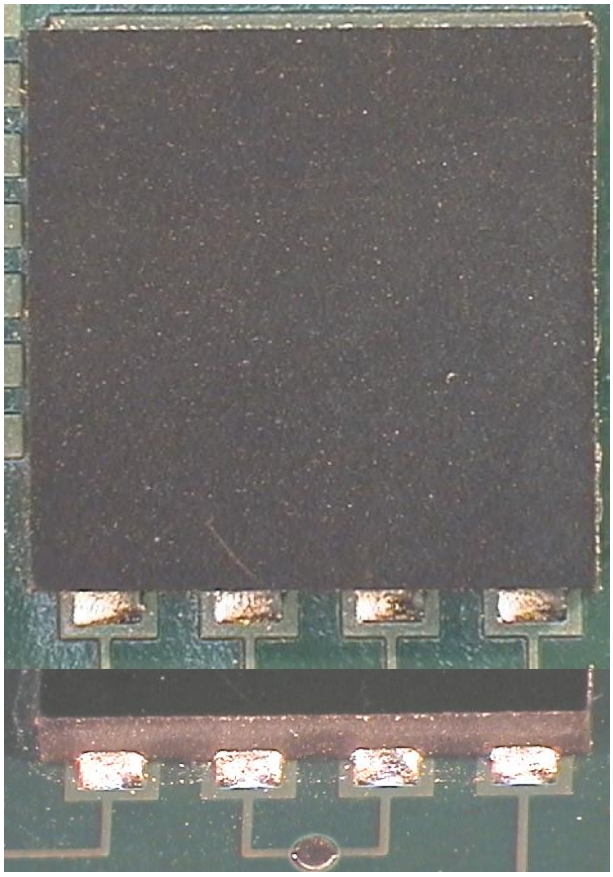


Figure 8: Typical optical photos of VDSON soldered on a PCB. The left photos shows an overview. Solder joints of gate and source can be seen on the right side. The drain pad solder joint is fully covered by the package body.

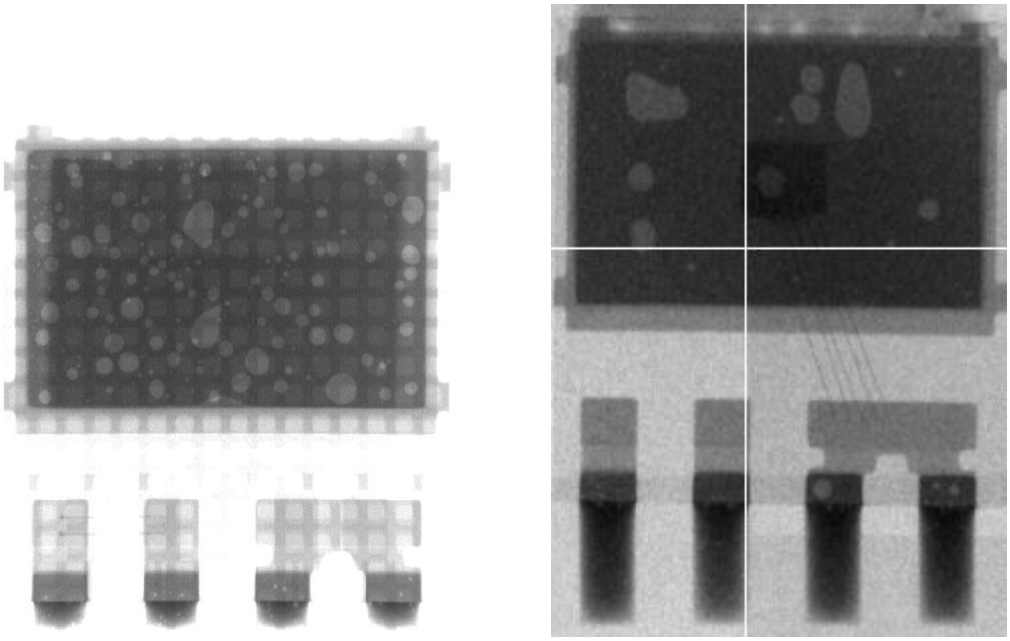


Figure 9: X-ray photos of a reflow soldered VDSON-4 (left) , and a wave soldered VDSON-4 (right).

Automatic X-ray Inspection (AXI) systems are appropriate for efficient inline control. AXI systems are available as 2D and 3D solutions. They usually consist of an X-ray camera and the hardware and software needed for inspection, controlling, analysing and data transfer routines. These reliable systems enable the user to detect soldering defects such as poor soldering, bridging, voiding and missing parts. However, other defects such as broken solder joints are not easily detectable by X-ray.
Fig. 9 shows an example of a typical X-ray photo of VDSON. Silicon die, wirebonds, leadframe, and the solder joints that connect the package to the PCB are visible. The voids in the solder joints formed during soldering can easily be seen and are mainly caused by the flux system of the solder paste.
As a rule-of-thumb, a 25% maximum voiding rate (X-ray inspection top-down view) for the perimeter pads is a starting point. The bigger exposed pad may tend to more or less voiding, depending on board pad size, via and stencil layout, solder paste, and reflow profile. Generally such big solder pads do not provide enough surface for gas to escape, which generates during reflow. Therefore solder joints of big pads generally tend to show more voiding.

Cross-sectioning of a soldered package as well as dye penetrant analysis can serve as tools for sample monitoring only, because of their destructive character. Nonetheless, these analysis methods must be used during engineering of new products at customers' production sites to get detailed information about the solder-joint quality. **Figure 10** shows typical cross-sections through solder joints. The photo at the left side shows the solder joint of a small gate or source pad with meniscus reaching up to the top of the initially exposed copper at the package side wall (wetting not necessary according to IPC-A-610). The photo at the right side shows the right side of the drain pad (exposed pad).

Pb-free solder joints look different from tin-lead (SnPb) solder joints. SnPb solder joints typically have a bright and shiny surface. Lead-free (SnAgCu) solder joints typically do not have this bright surface. Pb-free solder joints are often dull and grainy. These surface properties are caused by the irregular solidification of the solder, as the solder alloys are not exactly eutectic (like the 63Sn37Pb solder alloy). This means that SnAgCu-solders do not have a melting point but a melting range of several degrees. Although Pb-free solder joints have this dull surface, this does not mean that Pb-free joints are of lower quality or weaker than the SnPb joints. It is therefore necessary to teach the inspection staff what these Pb-free joints look like, and/or to adjust optical inspection systems to handle Pb-free solder joints.

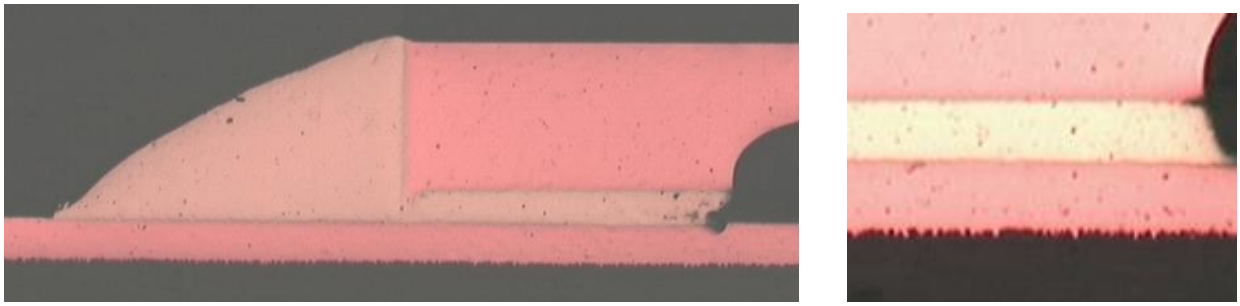


Figure 10: Cross-section views of a mounted VDSON package. The left photo shows a SAC305 solder joint of a small pad (gate/source). The right photo shows the outer edge of a drain pad which in case of VDSON is comparable to the inner edge.

8. Rework

If a defective component is detected after board assembly, the device can be removed and replaced by a new one. Due to possible damage while removing the component, a desoldered component should not be reused. Nevertheless, desoldering the old component (if analysis afterwards is planned) and resoldering of the new component has to be done very thoroughly.
Repair of single solder joint is not recommended. Soldering of single pads may lead to mechanical damage or inhomogeneous heating / thermal overstress.

Tooling

The rework process is commonly done on special rework equipment. There are a lot of systems available on the market, and for processing these packages the equipment should fulfill the following requirements:

Heating: Hot air heat transfer to the package and PCB is strongly recommended. Temperature and air flow for heating the device should be controlled. With freely programmable temperature profiles (e.g. by PC controller), it is possible to adapt the profiles to different package sizes and thermal masses. PCB preheating from the underside is recommended. Infrared heating can be applied, especially for preheating the PCB from the underside, but infrared heating should be used only for augmenting the hot air flow from the upside. Nitrogen can be used instead of air.

Vision system: The bottom side of the package as well as the site on the PCB should be observable. For precise alignment of package to PCB, a split optic should be used. Microscope magnification and resolution should be appropriate for the pitch of the device.

Moving and additional tools: The device should be relocatable on the whole PCB area. Placement accuracy better than +/-50 µm is recommended. The system should have the capability of removing solder residues from PCB pads (special vacuum tools).

Device Removal

If a defective component is going to be sent back to the supplier, no further defects must be introduced to the device during its removal from the PCB, because this may hinder the supplier's failure analysis. The following recommendations should be followed:

Moisture: Depending on its MSL, the package may have to be dried before removal. If the maximum storage time out of the dry pack (see label on packing material) is exceeded after board assembly, the PCB has to be dried according to the recommendations (Section o); otherwise too much moisture may have been accumulated and damage may occur (popcorn effect).

Temperature profile: During the soldering process, it should be assured that the package peak temperature is not higher and temperature ramps are not steeper than for the standard assembly reflow process (Section o).

Mechanics: Be careful not to apply high mechanical forces for removal. Otherwise, failure analysis of the package can be impossible, and/or the PCB can be damaged. For large pack-

ages, pipettes (vacuum nozzles) can be used. Pipettes are (implemented on most rework systems).

Site Redressing

After removing the component, the pads on the PCB have to be cleaned of solder residues. Don't use steel brushes because steel residues can lead to bad solder joints.
Before placing a new component on the PCB, solder paste should be applied to each PCB pad by printing (special micro stencil) or dispensing. No-clean solder paste is recommended.
Using only flux without applying additional solder is not recommended because the resulting solder joints will be thinner and their reliability will differ from that of a standard PCB assembly.

If a desoldered component has to be resoldered, the component has to be cleaned and old solder and flux have to be removed first. This has to be done with special care so that the package is not harmed by mechanical or thermal stress, or material such as flux, solder, and cleaning solvents that may penetrate into the package through the optical window and/or vent holes.

Reassembly and Reflow

After preparing the site, the package can be placed onto the PCB. The maximum applied pick&place force should not exceed the force applied during standard board assembly.
It is also possible to position the package exactly above the PCB pads, at a height just above the pads so that there is no contact between the package and the PCB. The package is then dropped into the printed or dispensed solder paste depot (zero-force placement).
During the soldering process, it should be assured that the package peak temperature is not higher and temperature ramps are not steeper than for the standard assembly reflow process (Section o). Investigation has shown that if distance, time, and airflow are properly controlled, a hot air temperature of 300°C can be used, for example, without violating the maximum allowed reflow profile.