MOSFET fast switching: motivation, implementation, and precautions

About this document

Scope and purpose

This application note provides a brief introduction to MOSFET fast switching in hard-switched applications, discusses its motivation, benefits, key aspects, how to implement it and, finally, addresses some common difficulties when using MOSFET fast switching.

Intended audience

SMPS design engineers.

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1 Introduction

Efficiency and power density are key trends in modern switched-mode power supplies (SMPS) in several applications. Energy conversion efficiency impacts the electricity bill in two ways: firstly, losses are turned into heat, and secondly this heat loads the cooling system that is required to keep the facility temperature controlled. High power density is highly appreciated, since it defines the equipment footprint and that is relevant to the real-estate cost, especially in telecom and datacom applications, for example. Therefore, high conversion efficiency and power density help to reduce the total cost of ownership of such installations. These requirements guide the selection of all system parts, including the power MOSFETs. To address the above-mentioned requirements, Infineon has recently released new MOSFET technologies (OptiMOS™ 6 80 V and 100 V) that are based on the advantages of a revolutionary new cell design combined with the benefits of advanced manufacturing technologies. This combination brings together the benefits of exceptionally low conduction losses, superior switching performances, improved safe operating area (SOA) and good ruggedness. These features make it the best fit for high-switching-frequency applications, fulfilling the requirements of high efficiency while enabling designs for higher power densities and cost-effectiveness [1]. Moreover, Infineon's innovative and improved PQFN package concept with source-down and source-down dual-cooled package technologies complements the advances in technology, yielding products with superb features to aid the SMPS designer to fulfill the toughest design requirements. Although the SMPS designer can use fast switching to advantage to fulfill these requirements, for example high efficiency, some caution must be exercised when using it. Fast switching may cause drain-source and gate-source voltage overshoots and unwanted induced turn-on of the switch if not properly applied. This document will give some guidance to the designer on how best to implement fast switching without incurring the issues mentioned.

2 Fast switching in high-frequency hard-switched topologies

High-efficiency DC-DC converters, powering systems with large load variations and wide input-voltage range, such as telecom and datacom systems, can only be implemented if the converter is of the switched-mode type [2]. Such converters use semiconductor switches that are turned on and off conveniently with the aid of a pulse-width modulation (PWM) technique to regulate the output voltage, wherever required. In hard switching, every time a switch changes its status from off to on, and vice versa, there is an overlap between the voltage across the switch and the current through it. This overlap between voltage and current causes losses, which are referred to as switching losses. These losses grow proportionally with the increase in the switching frequency, because the switching frequency is the repetition rate of the switching events. The size of the converter inductor, capacitor and transformer is highly dependent on the converter switching frequency: the sizes are reduced as the switching frequency increases [3]. If, on the one hand, the switching frequency is increased in order to reduce the converter volume and increase power density, which is one of the key requirements of the design, on the other hand this will increase switching losses, which will harm the converter efficiency, affecting the other key requirement of the converter design.

Resonant converters have been shown in the literature to solve the issue of these conflicting requirements [4] [5]. These converters use the oscillation created by one inductor and one capacitor to achieve soft-switching of the switching device, where it then operates in either zero-voltage switching (ZVS), zero-current switching (ZCS) or both to eliminate the switching losses – and thus the dilemma is removed. A point to mention, though, is that generally, the major disadvantage of resonant-type converters is the increased current and/or voltage stresses on semiconductors compared to the corresponding PWM topology. In addition, most ZVS converters circulate significant amounts of energy and require a relatively large resonant inductor to create ZVS conditions. Therefore, there is a strong trade-off between the switching-loss savings and increased conduction losses. This trade-off may result in a lower efficiency and/or larger size of a high-frequency resonant-type converter compared to a PWM converter operating at a lower frequency. This is especially true for applications with wide input-voltage and load ranges, as in telecoms and datacoms. In addition, variable-frequency operation is often perceived as a disadvantage of resonant converters [5]. This application note will focus on hard switching only.

2.1 Achieving fast switching in high-frequency hard-switched topologies

In this section, contributing factors to fast switching are discussed.

2.1.1 Influence of MOSFET parameters on switching times

Figure 1 and Figure 2 show the simplified MOSFET–driver connections (a) along with relevant ideal waveforms and time events during the turn-on and turn-off transitions (b). These figures also show the MOSFET parasitic capacitances and internal gate resistance (Rg_{int}). As can be seen in both figures, the overlap between the drain-source voltage (V_{DS}) and the drain current (I_D) occurs between times t1 and t3, the so-called switching time (t_{sw}). This overlap generates switching losses and occurs twice in a switching period: during the turn-on and turn-off transitions. Because switching losses are inevitable in hard-switched topologies, they ought to be minimized if high system efficiency is to be attained. To do this, t_{sw} is the only parameter that can be minimized, because the system voltage and power are defined design inputs that are non-negotiable. V_{DS} depends on the system voltage (V_{bus}) and topology and I_D depends on the system power and on whether paralleling of devices is required. t_{sw} can be reduced if either the V_{DS} voltage or the I_D current transition times are decreased. These transition times are highly dependent on the following MOSFET parameters: gate charge (Q_g), gate-drain charge (Q_{gd}), internal gate resistance (Rg_{int}), transconductance (g_{fs}) and package source (Ls) and drain (Ld) inductances. The gate-driver integrated circuit (IC) also contributes to defining t_{sw} with its output-stage pull-up and pull-down resistances, along with the respective saturation currents (driver peak sink and source currents). Finally, a last contributor impacting t_{sw} is the printed circuit board (PCB) layout and its loop inductance.

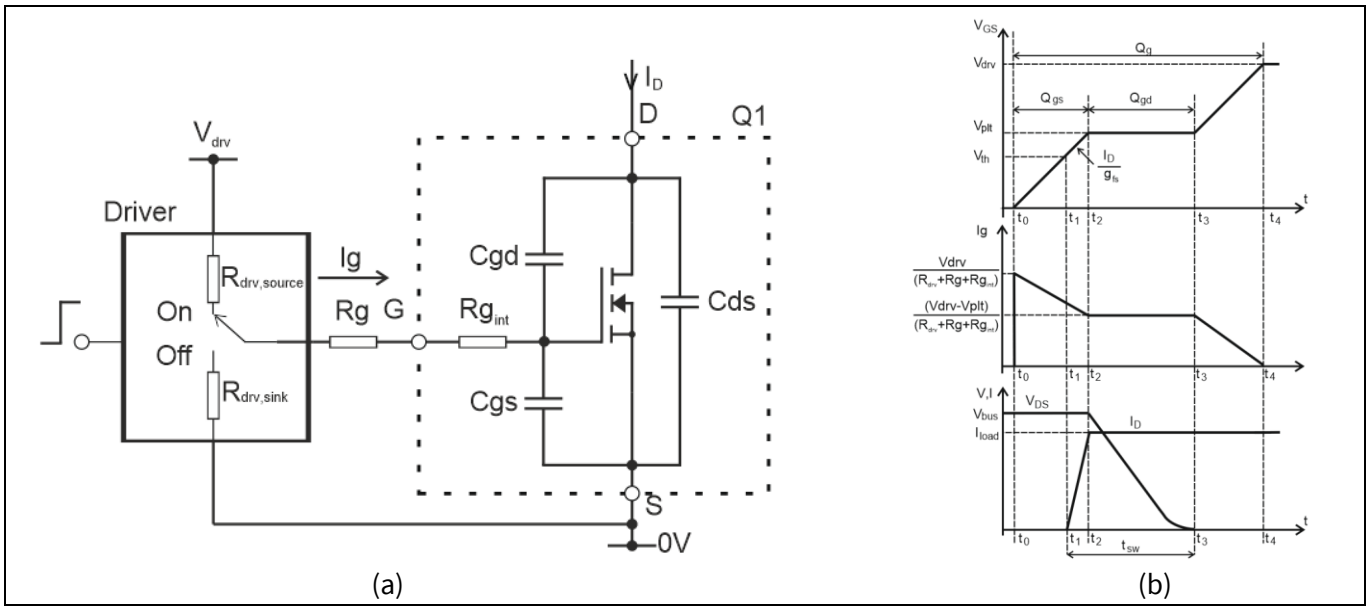


Figure 1 **(a) Simplified circuit diagram of the MOSFET–driver connection for the turn-on transition; (b) V_{DS}, V_{GS}, Ig, and I_D ideal waveforms during the turn-on transition**

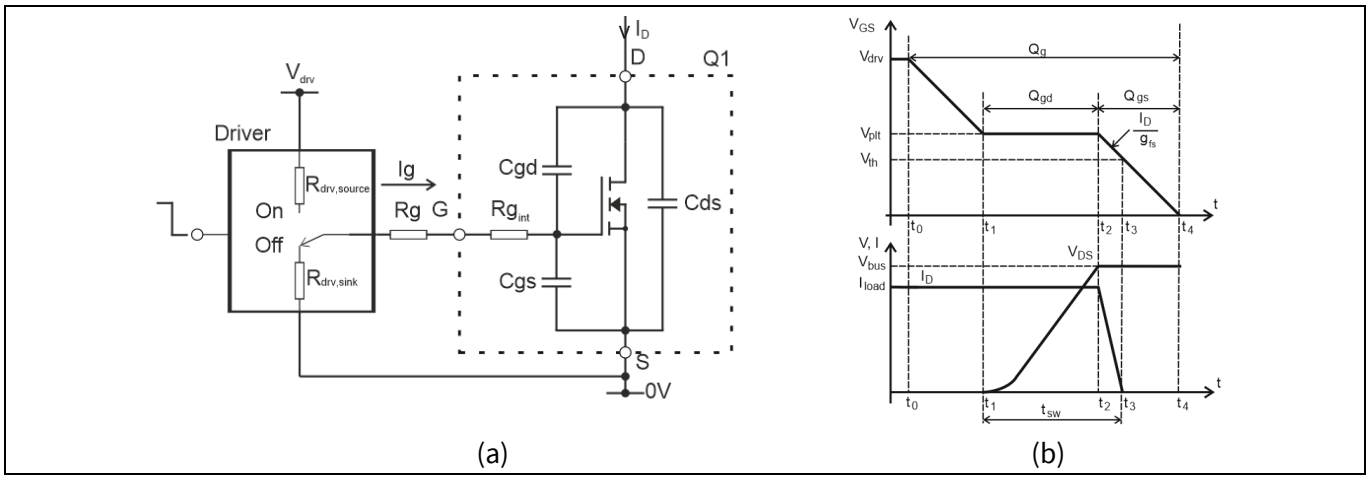


Figure 2 **(a) Simplified circuit diagram of the MOSFET–driver connection for the turn-off transition; (b) V_{DS}, V_{GS}, Ig, and I_D ideal waveforms during the turn-off transition**

Figure 1 (b) shows that the turn-on V_{DS} transition occurs between times t2 and t3, and during this period the gate current is constant. This figure also shows that the constant gate current supplies an amount of charge equal to the MOSFET Q_{gd}, in the time interval t2 to t3. The gate current (Ig) level depends on the driving voltage (V_{drv}), the MOSFET plateau voltage (V_{plt}) and the equivalent series-connected resistances in the path between the driver power supply and the MOSFET gate capacitances. In general, the V_{DS} transition time is the major portion of t_{sw} and, therefore, if it is reduced, t_{sw} and the switching losses are greatly reduced as well. The designer then has the obvious choice of selecting a MOSFET with low Q_{gd}, low Rg_{int}, and low V_{plt}. Figure 1 (b) shows that V_{plt} is equal to the MOSFET threshold voltage (V_{th}) plus I_D divided by the MOSFET transconductance (g_{fs}) and, therefore, low V_{plt} is achieved if the MOSFET g_{fs} is high. g_{fs} is the second important parameter in reducing t_{sw}, as can be seen in Figure 1 (b), because it impacts the other portion of t_{sw}, period t1 to t2: the I_D rise time. The higher the g_{fs} value is, the shorter the time interval t1 to t2 will be and the faster I_D will rise, reducing its overlap time with V_{DS} and hence losses. The above-mentioned MOSFET parameters also play the same relevant role in the turn-off event, seen in Figure 2 (b). The gate-source (Cgs) and the gate-drain (Cgd) capacitances, along with Rg, Rg_{int}, and R_{drv}, define the time constant that governs the speed of the turn-on and turn-off events: the lower Cgs and Cgd are, the faster the MOSFET will switch.

2.1.2 MOSFET package and PCB layout contributions to the switching times

Figure 3 (a) shows the MOSFET–driver connection with the PCB traces parasitic inductance Lgate, for the gate loop, Ldrain for the drain loop, and Lsource for the source connection to the ground; the MOSFET internal capacitances and package inductances (Lg, Ls, and Ld) are also displayed. Figure 3 (b) shows the impact of the parasitic inductances on the turn-on waveforms, highlighting especially the difference of the V_{GS} waveform when compared to the idealized waveform seen in Figure 1 (b), when Q1, acting as high-side switch in a buck converter, for example, blocks a freewheeling diode not shown in Figure 3 [6].

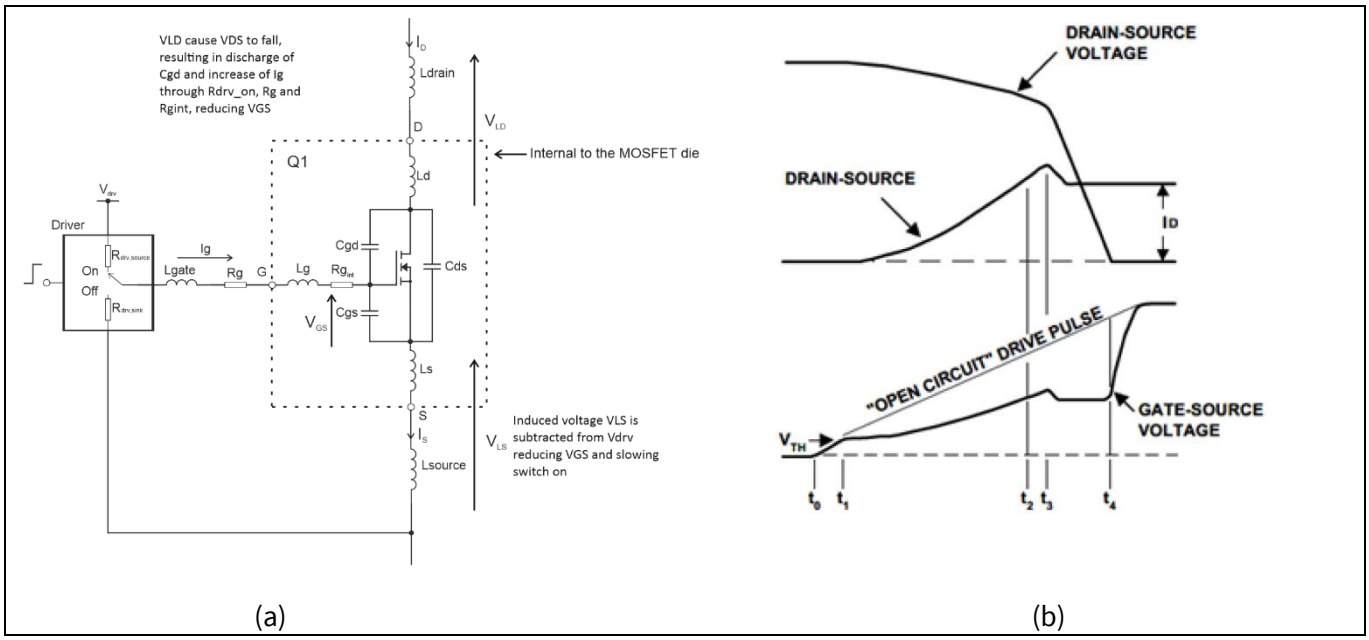


Figure 3 (a) Circuit diagram of the MOSFET–driver connection showing the MOSFET internal parasitic inductances (Lg, Ld, and Ls) and the circuit parasitic inductances Lgate, Ldrain, and Lsource [6]; (b) turn-on waveforms showing the effects of parasitic inductances [6]

Referring to the gate-source voltage V_{GS}, seen in Figure 3 (a), at time t0 this voltage starts to rise until at t1 it reaches the threshold voltage of the MOSFET and the drain current starts then to increase. At this point two things happen, which make the V_{GS} waveform deviate from its original linear rise. First, inductances Ls and Lsource, in series with the source, which is common to the gate circuit (“common source inductance”), develop an induced voltage V_{LS} as a result of the increasing source current. This voltage counteracts the applied V_{drv} voltage and slows down the rate of rise of V_{GS} measured directly across the gate and source terminals. This acts to reduce the rate of rise of the source current, creating a negative feedback effect such that increasing current in the source produces a counteractive voltage at the gate, which tends to resist the change of I_D. The second factor that influences the gate-source voltage is the Miller effect. During the period t1 to t2 some voltage is dropped across the unclamped stray circuit inductances in the drain (Ld in series with Ldrain), causing a reduction in the drain-source voltage V_{DS} appearing directly across the MOSFET. The decreasing value of V_{DS} is reflected across Cgd, drawing a discharge current Igd through it, and thereby increasing the effective capacitive load being driven by the drive circuit. This, in turn, increases the voltage drop across the output impedance of the gate drive circuit (Lgate, Rg, Lg, and Rg_{int}) and decreases the rate of rise of V_{GS}. This is another negative feedback effect, in which increasing I_D results in a reduction in the rise of V_{GS} resisting the increase of I_D. This behavior continues throughout the period t1 to t2, as I_D rises to the current flowing in the freewheeling rectifier before switch-on, and it continues into the next period t2 to t3 when the freewheeling diode goes into reverse recovery. At time t3 the diode starts to block reverse conduction and V_{DS} starts to fall. The rate of decrease of V_{DS} is now determined by the Miller effect and an equilibrium condition is reached under which V_{DS} falls at the rate

necessary for V_{GS} to satisfy the level of I_D, as explained previously. V_{GS} falls as the diode reverse recovery current drops and remains at the Miller plateau level corresponding to I_D, as V_{DS} transitions to zero, while I_D is constant. Finally, at time t4, the MOSFET is switched fully on, allowing V_{GS} to rise to V_{dr}. Similar considerations apply to the turn-off interval [6]. The SMPS designer needs to minimize Lsource + Ls in order to reduce its impact on the switching speed. Infineon aids the designer in minimizing such inductance offering devices in source-down PQFN packages with very low Ls value [9]. This package offers additional features such as a reduction of up to 25 percent in $R_{DS(on)}$ and superior thermal performance with decreased R_{thJA} and R_{thJC}. These combined features allow the device to yield the same performance as that of the industry standard drain-down PQFN-5x6 packaged device but in a smaller package: PQFN 3x3. The smaller package gives the extra benefit of more optimized layout designs, especially if device parallelization is required.

A PCB layout with low commutation-loop inductance is another relevant contributor to fast switching. Figure 4 (a) shows the simplified circuit diagram of a buck converter, (b) the top view of the placement of its decoupling capacitors (C15 to C18), and (c) MOSFETs (Q1 and Q2) and its commutation loop with the high-frequency displacement current highlighted by the curved arrow seen in the PCB top layer. This L-shaped layout yields an approximately 2 nH loop inductance, which is very low. Figure 5 shows a recommended commutation-loop layout with 750 pH loop inductance. Figure 6 shows a comparison of the synchronous rectifier (SR) MOSFET V_{DS} voltage rise times, in a buck converter, for the two different layout options: the L-shaped and the recommended layouts. The graph shows that the recommended layout yields 42 percent faster turn-on transition time than the L-shaped one.

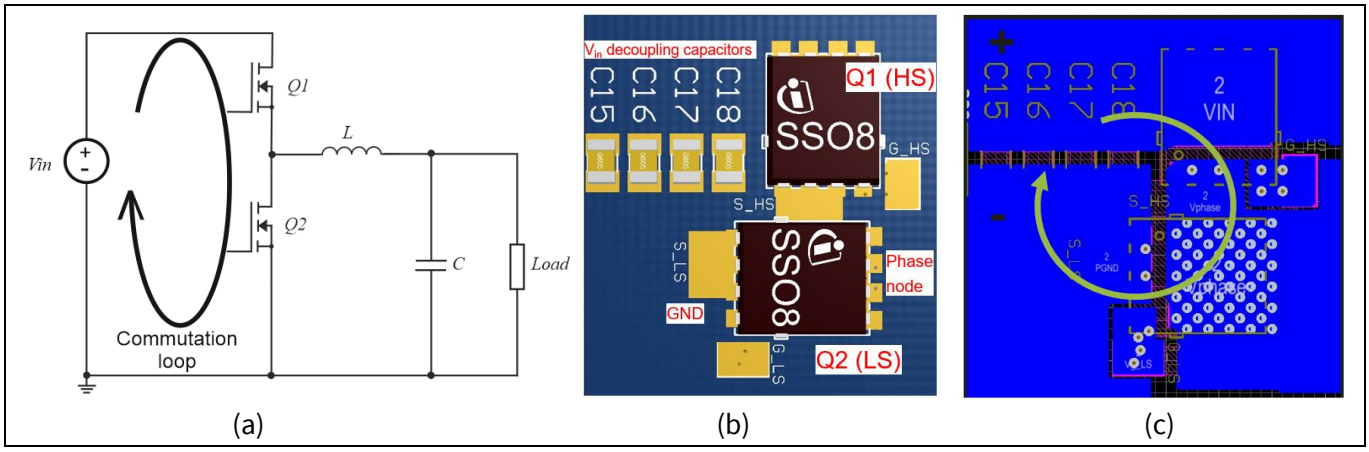


Figure 4 **(a) Simplified circuit diagram of a buck converter and its commutation loop; (b) top view of the placement of the buck converter decoupling capacitors C15 to C18 and MOSFETs Q1 and Q2 (mirrored L-shape); (c) view of the PCB top-layer traces with the high-frequency displacement current highlighted by the curved arrow**

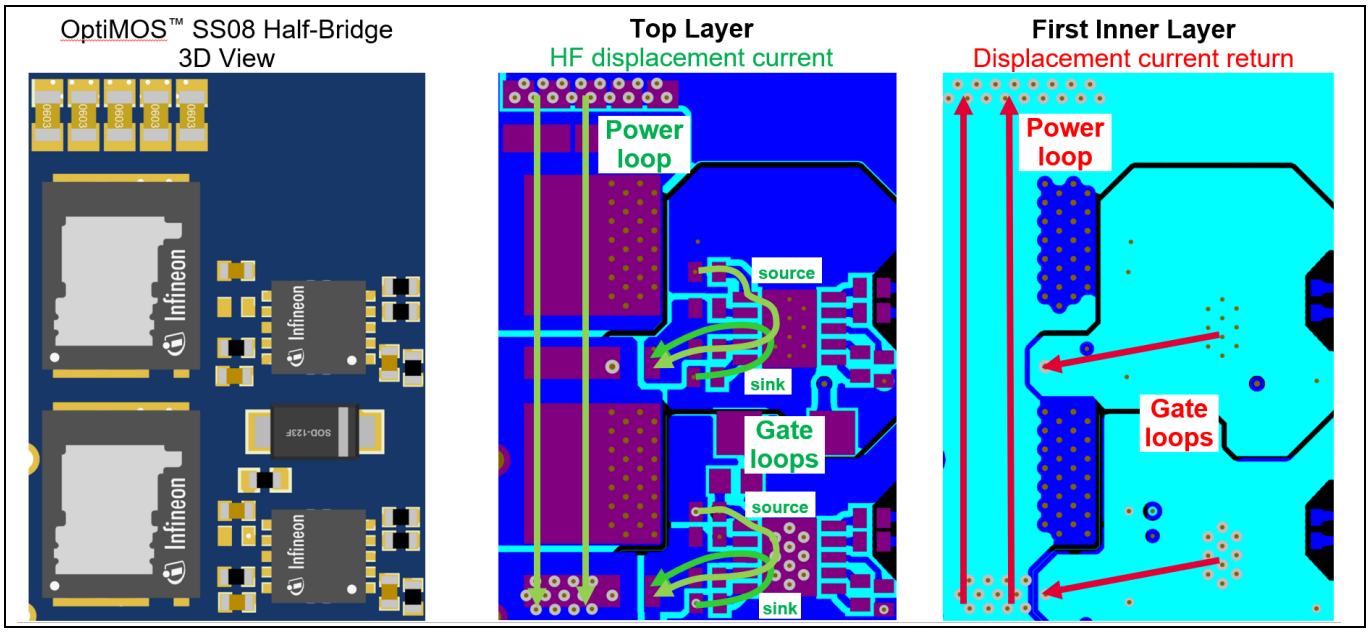


Figure 5 **Recommended commutation-loop layout for lowest inductance (750 pH)**

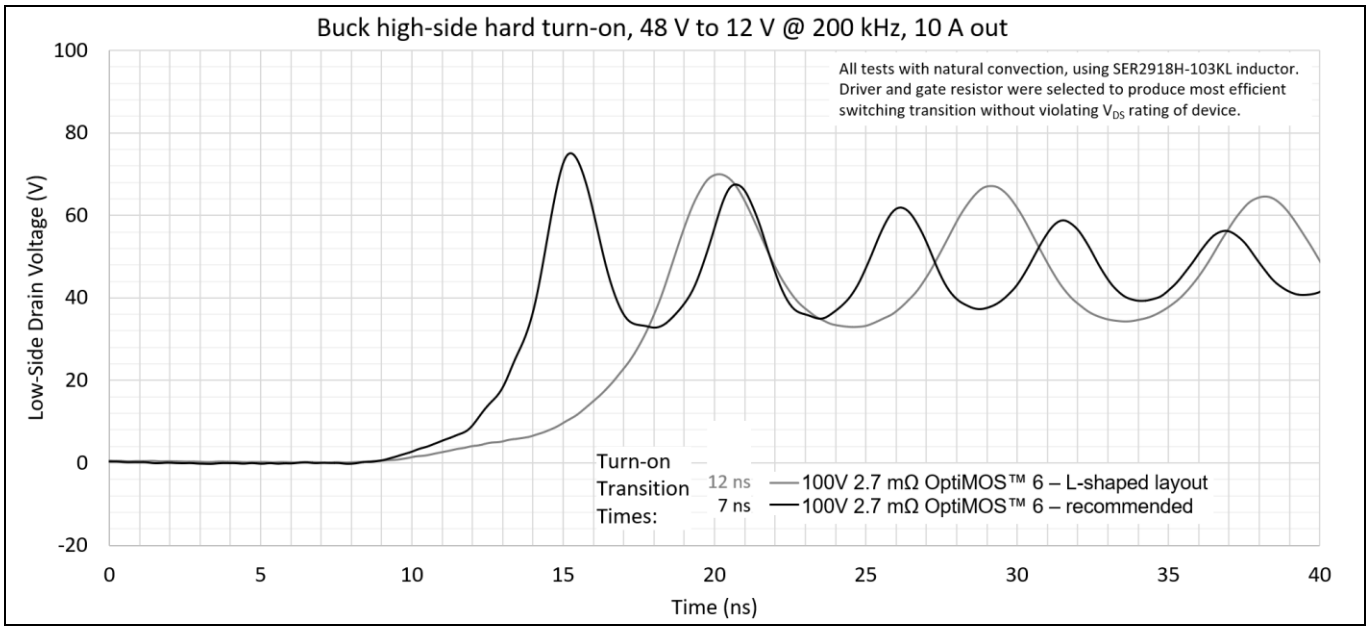


Figure 6 **Comparison of the turn-on transition times for the L-shaped and recommended layouts in a buck converter**

2.2 Precautions when using fast switching

In this section, some common issues arising with fast switching are discussed.

2.2.1 Source inductance

The common-source inductance (Lsource + Ls) is an active player in fast switching, impacting the switching speed negatively and, therefore, should be kept to a minimum. Figure 7 shows the circuit diagram of the MOSFET–driver connection for the switch-on event (a) and the switch-off event (b) and their parasitic inductance voltage drops. During turn-on, the common-source inductance voltage V_{CS} appears as a reaction to the increasing change in the source current (positive di/dt). The same effect is seen in the gate-loop inductance, where a voltage V_{LG} appears as a reaction to the change of Ig. V_{GS} and V_{LG} reduce the effective voltages on Rg and Rg_{int}, reducing the magnitude of Ig, and also reducing the turn-on switching speed. On the other hand, during turn-off, the V_{CS} voltage changes direction, because the drain-current fall time has a negative di/dt, and causes the MOSFET internal source connection voltage to become negative ($-V_{CS}$); the net voltage in the gate loop will then be $V_{GS}-(V_{LG}+V_{CS})$, which again reduces the magnitude of Ig, slowing down the turn-off event. Therefore, care with the gate and source-loop layouts is highly recommended in order to enable fast switching and good efficiency.

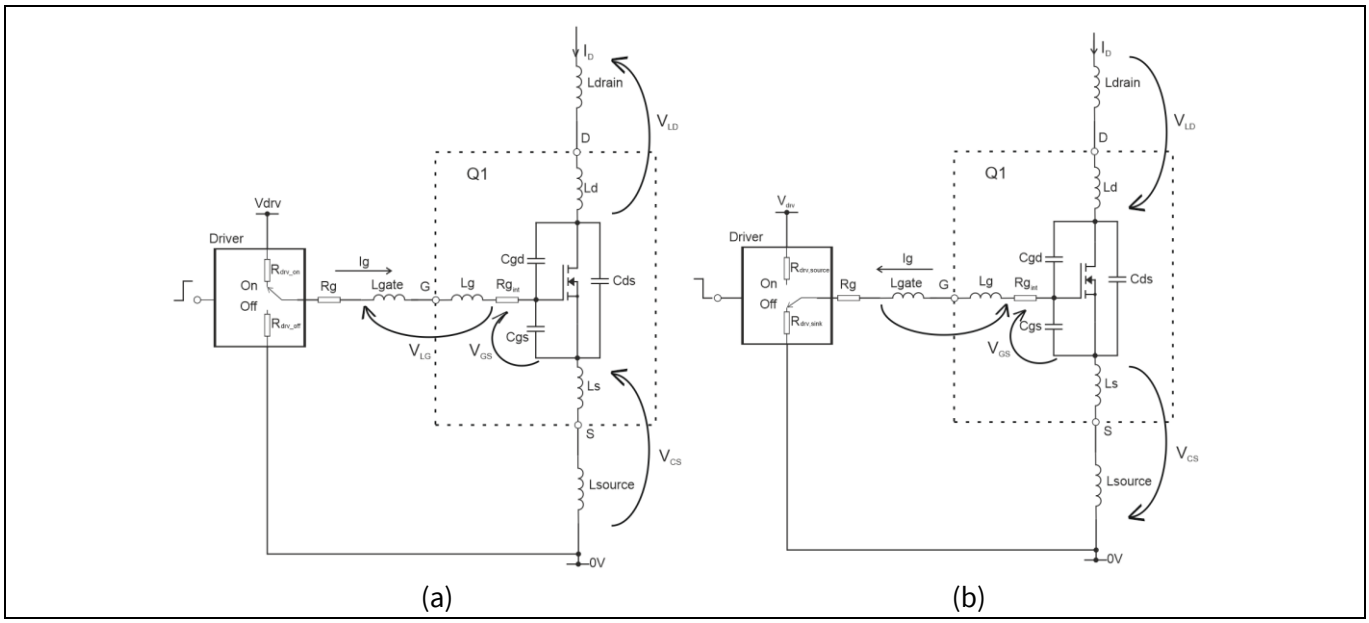


Figure 7 (a) Circuit diagrams of the MOSFET–driver connections and their parasitic inductance voltage drops for the switch-on event; (b) the switch-off event

The common-source inductance plays a particular role when the MOSFET is used as a SR, especially during the dead time period, when the MOSFET channel is blocked and V_{LG} is equal to zero [10]. In this mode of operation, the current flow direction is from the source to the drain and the current flows through the MOSFET body diode. It can be seen in Figure 8 (a) that, as the drain current magnitude is reduced (negative dI_D/dt), the induced voltage in the circuit inductances reverts and V_{CS} becomes positive. The net effect for the MOSFET gate is that a negative V_{GS} voltage equal to $-V_{CS}$ is applied to it, as seen in this figure. This negative gate voltage is useful because it helps to prevent the MOSFET from suffering induced turn-on. Induced turn-on is a phenomenon that can occur when MOSFETs are used in fast-switching applications where high dV_{DS}/dt transitions appear at the drain while the device is in the off-state. This is typically the case in hard-switching applications such as SMPS and motor drive inverters, where two MOSFETs are used in a half-bridge configuration. Figure 8 (b) shows how “CdV/dt” causes a current pulse to couple through Cgd to the gate, which

is pulled to 0 V through Rg and $R_{drv,sink}$. This current pulse can be sufficient to induce a voltage spike at the gate. It is important to remember that the MOSFET may also have a significant internal gate resistance Rg_{int}, so that the induced gate spike appearing at the silicon chip may be larger than that observed at the gate terminal. If the induced turn-on spike exceeds the MOSFET V_{th} then the device will partially turn on for a brief time before the high-side MOSFET has fully turned off. With both devices partially on, a high current can flow through the half-bridge, which can violate SOA limits and destroy one or both devices [11].

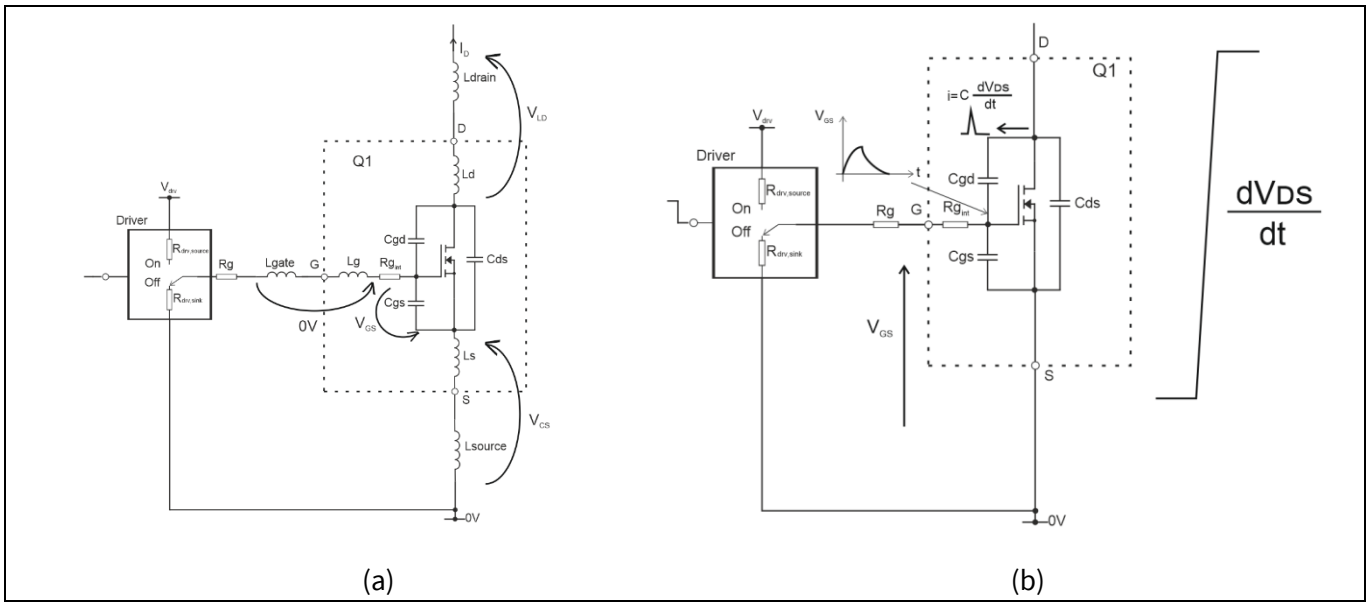


Figure 8 **(a) Circuit diagram of the MOSFET–driver connection for the MOSFET operating as SR during the dead time; (b) induced turn-on mechanism [11]**

2.2.2 Gate-loop impedance

The gate-loop inductance, formed by Lgate, the device internal inductances Lg, Ls, and the common-source inductance Lsource, along with the gate capacitances Cgs and Cgd and its internal and external gate resistances, Rg_{int} and Rg, respectively, form an RLC circuit. The series combination of the resistance values in the gate loop sets the damping of the RLC circuit [7]. As mentioned in Section 2.1.1, the equivalent loop resistance value negatively impacts the switching speed and should be kept as low as possible. However, this equivalent resistance value also controls the V_{GS} overshoot, as seen in Figure 9, and therefore a compromise between switching speed and maximum values of V_{GS} voltage overshoot and undershoot has to be made. The designer ought then to pay attention to the PCB layout, reducing the gate-loop parasitic inductance to a minimum, if the V_{GS} overshoot and undershoot voltages are to be tamed to an acceptable level and yet design in a rather low loop resistance in order to still attain fast switching. Reference [8] shows that gate driver ICs are sensitive to negative voltages (-1 V absolute maximum rating) at their phase node and therefore the gate voltage undershoot has to be controlled. Reference [7] shows that if the series resistance is equal to the circuit critical resistance (yields critical damping), the V_{GS} voltage waveform will be maximally flat (no overshoot), and if it is less than the critical value, the V_{GS} voltage waveform will show overshoot and finally if the series resistance is higher than the critical value, the V_{GS} voltage waveform will be overdamped and the MOSFET switching will be slower. Figure 9 illustrates the V_{GS} voltage waveforms for these three cases of series resistances yielding two underdamped waveforms, a critically damped waveform and an overdamped waveform. One particular case of the series resistance being less than the critical value is the one where the overshoot equals 10 percent of the V_{GS} voltage (10 V in the figure). This case is borderline for the driver because this resistance yields an undershoot of – 1 V, which is already the driver IC absolute maximum value; therefore,

the optimum selection for fast switching lies between the 10 percent overshoot voltage and the maximally flat one. According to reference [7], the critical resistance is given by: $R_{loop} = 2 \cdot \sqrt{\frac{L_{loop}}{(Cgs+Cgd)}}$.

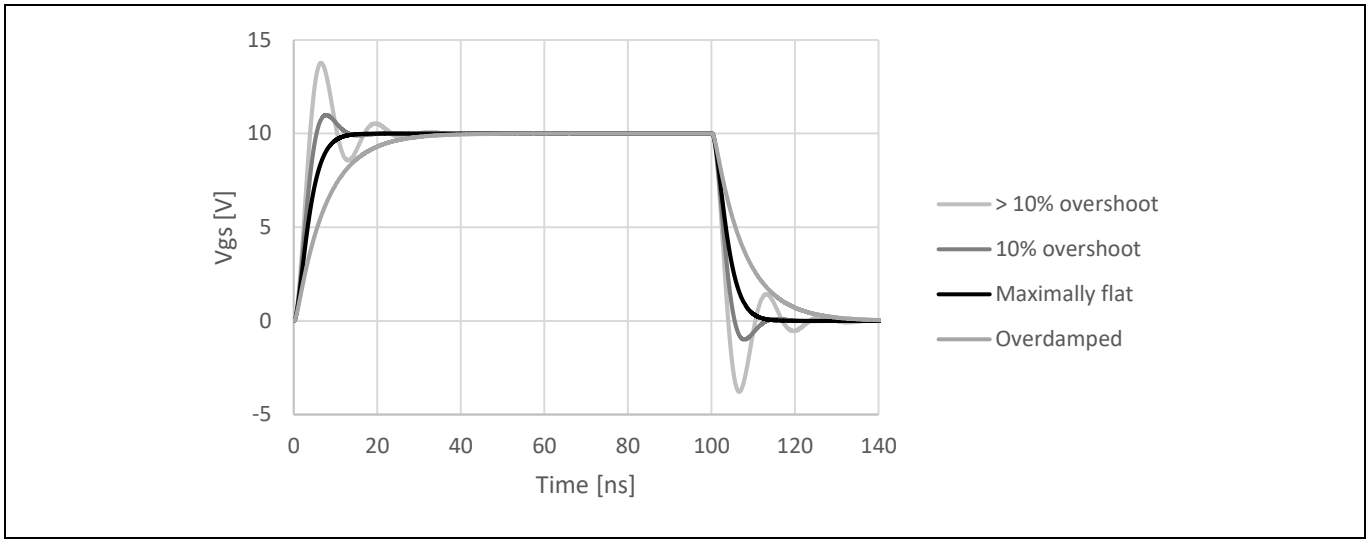


Figure 9 **Gate-source voltage waveforms for different gate-loop resistances, showing two underdamped, a critically damped and an overdamped waveform**

2.2.3 MOSFETs with low charges

As mentioned in Section 2.1, MOSFETs with low charges, such as the new OptiMOS™ 6 80 V and 100 V MOSFETs, are the perfect choice for fast switching, since their low Qgd enables fast V_{DS} transitions. This new technology uses a revolutionary new cell design combined with the benefits of an advanced manufacturing technology, which brings together the benefits of exceptionally low conduction losses, superior switching performances, improved SOA and good ruggedness. This new concept has a built-in snubber with low-resistance field plates [13]. This built-in snubber is a structure present in all MOSFETs that use the field-plate trench structure, which utilizes oxide charge balance and two-dimensional (or three-dimensional as with OptiMOS™ 6 80 V and 100 V) depletion effect from the field plate electrode [14]. Figure 10 (a) illustrates the built-in snubber composed of the field-plate resistance (R_{OSS}) and the field-plate capacitance (C_{OSS} = Cfp + Cgd, with Cfp >> Cgd). The advantage of a low R_{OSS} is that less losses occur in the MOSFET while charging and discharging C_{OSS} in normal operation. The drawback of it is that, for turn-off events, the V_{DS} voltage overshoot could be high and its ringing will be less damped, as seen in Figure 10 (b) [13]. An additional feature of the OptiMOS™ 6 80 V and 100 V technologies is that they have a metal gate structure, which yields a so-far unmatched switching uniformity over the whole die area. This metal gate structure yields a much-improved gate resistance uniformity across the chip compared to the commonly used polysilicon gates [13]. Along with a direct connection of the field plates to the source metal, a device setup is realized that not only ensures a very fast and homogeneous transition at turn-on and turn-off that minimizes switching losses, but also reduces the risk of an unwanted dV_{DS}/dt induced turn-on of the MOSFET.

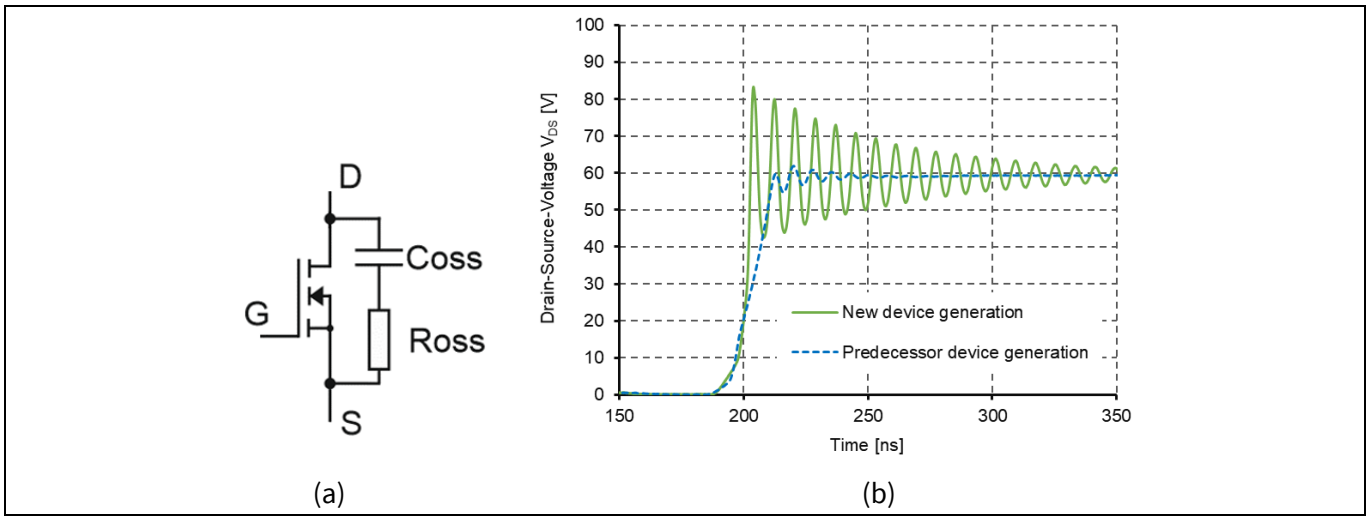


Figure 10 **(a) Simplified MOSFET equivalent circuit showing the internal built-in snubber; (b) comparison of the drain-source voltage behaviors for the two device generations OptiMOS™ 5 and 6 100 V**

2.3 Mitigation of common issues when using fast switching

In this section, some recommendations to keep unwanted effects while using soft switching to a minimum are presented.

2.3.1 Low source inductance

As discussed in Section 2.2.1, low common-source inductance is beneficial to fast switching and can be implemented on the one hand by design, with the reduction of the PCB-related inductances to a minimum, and on the other by the choice of high-performance packages. Infineon's OptiMOS™ low- and medium-voltage power MOSFETs present an innovative and improved PQFN package with the source-down concept. In this concept, the orientation of the silicon chip source is toward the bottom side of the package, which yields devices with low $R_{DS(on)}$ and very low source package inductance. The chip drain is connected to the package pins through a reinforced clip placed on top of the silicon chip. This combination of source-down chip with the clip on the drain yields significantly reduced package parasitics on all terminals and the thermal performance is pushed to the next level. The OptiMOS™ power MOSFET 3.3 x 3.3 mm^2 source-down package is now available in 25 V to 150 V in bottom-side cooling (BSC) and in dual-side cooling (DSC). This new concept comes in two different footprint versions: a source-down standard gate version and a source-down center-gate version, seen in Figure 11, which is specifically optimized for parallelization. Compared to alternative solutions, source-down offers benefits such as low source inductance, low $R_{DS(on)}$ and improved thermal performance [9].

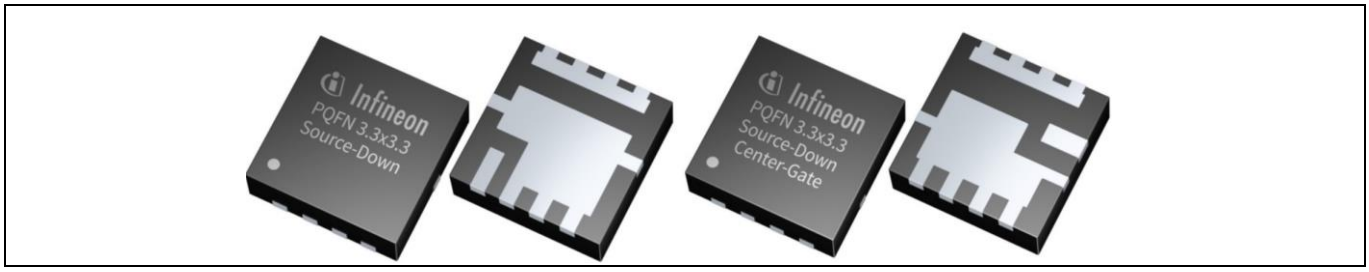


Figure 11 **The OptiMOS™ power MOSFET 3.3 x 3.3 mm^2 in source-down and source-down center-gate versions**

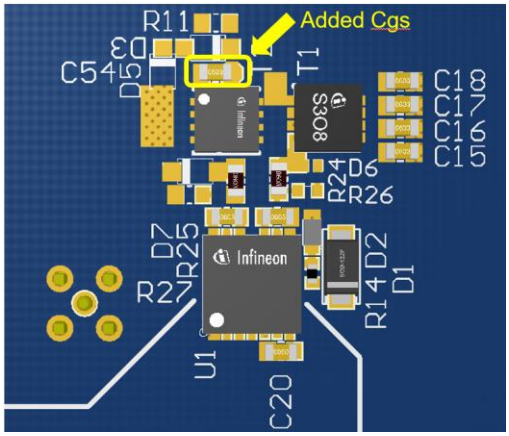
Fast switching in high-frequency hard-switched topologies

As described in Section 2.2.1, low common-source inductance reduces the immunity to induced turn-on: MOSFETs with relatively high Qgd may suffer induced turn-on when using the source-down packages because the gate negative voltage provided by the source inductance is dramatically reduced and the relatively high Cgd of these devices increases the Cgd x dV_{DS}/dt current that charges Cgs, raising the V_{GS} voltage.

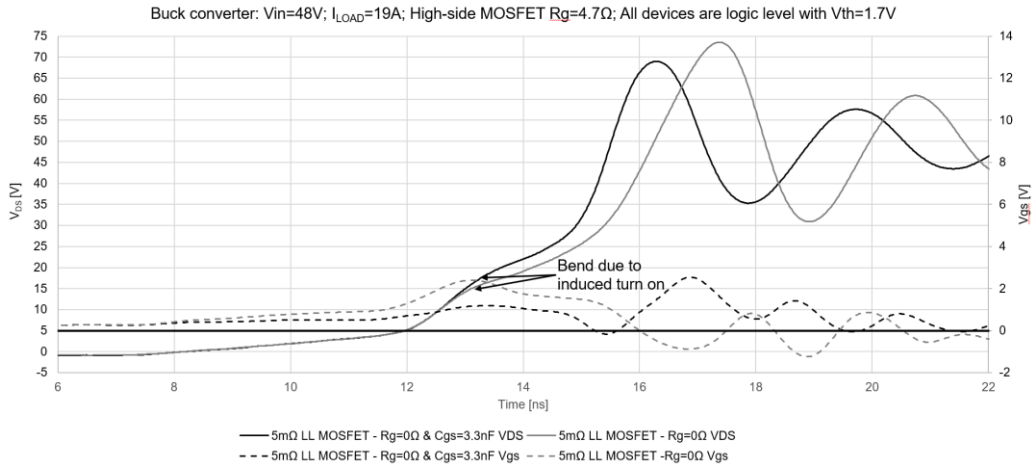
In order for the SMPS designer to prevent induced turn-on, the preferred option would be the selection of MOSFETs with low Qgd, like the new OptiMOS™ 6 80 V and 100 V MOSFETs, in source-down packages. These devices are more immune to induced turn-on, due to their low Qgd, and thus can fully reap the benefits of the low source-inductance packages, achieving fast switching. Additionally, the new OptiMOS™ 6 80 V and 100 V MOSFETs, with their low internal gate resistance, realized with the novel metal gate technology, enable a very homogeneous switching, preventing areas of the die parasitically turning on because of an inferior gate connection.

For MOSFETs with rather high Qgd, the first remedy the designer can use is to reduce the value of the external Rg, paying attention to the resulting negative voltage that the driver might experience (see Section 2.2.2), in order to have a low-ohmic turn-off impedance in the gate loop; this yields a lower induced voltage at the MOSFET gate pin. If that is not enough to prevent the induced turn-on, an external Cgs capacitor added to the MOSFET gate terminal will further lower the gate impedance to the ground and reduce the magnitude of the induced voltage in the gate, as seen in the PCB layout shown in Figure 12 (a), where an 80 V logic-level MOSFET with relatively high Qgd has been used in a buck converter as an example case. The logic-level MOSFET has a typical V_{th} of 1.7 V, which is less than the induced voltage seen at its gate: more than 2 V (Figure 12 (b), grey dashed line). As a result, one can see that the V_{DS} voltage upswing bends to the right, meaning that the MOSFET conducts for a short time, causing the V_{DS} voltage to bend to the right. A V_{DS} voltage bend to the left comes from the C_{OSS} value reduction with the increase in the V_{DS} voltage. The same figure shows that the bending is much less pronounced when a 3.3 nF external capacitor is added to the MOSFET gate-source pins (black curves). When an external Cgs capacitor is added to the MOSFET gate-source pins, the total equivalent capacitance is increased, resulting in a lower induced voltage in the gate (dashed black curve Figure 12). Moreover, the V_{DS} voltage bend has also been reduced, and more importantly the buck converter efficiency has been improved with the added Cgs capacitor, as seen in Figure 12 (c), despite the extra gate losses generated by the added gate capacitor. This figure also shows that the overshoot voltage level is reduced when the external capacitor is used; this happens because the induced turn-on current traps some energy in the commutation-loop inductance, which is later diverted to the MOSFET C_{OSS}, causing its V_{DS} voltage to overshoot to higher levels than those seen when the external capacitor is used. A point to mention is that V_{th} decreases with the increase in temperature and hence this must be considered when selecting the right Cgs capacitor value in the design (design for the worst case!).

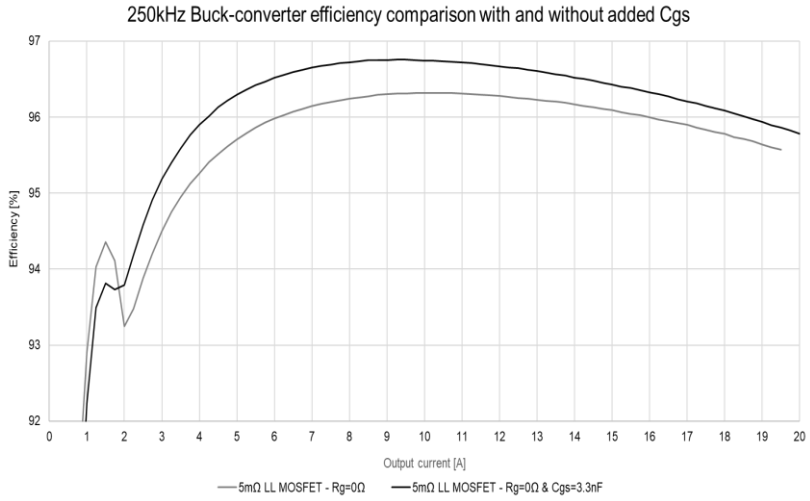
Figure 13 shows the V_{DS} voltage waveform for a normal level (V_{th} = 2.8 V) 5.7 mΩ OptiMOS™ 6 100 V device, in a source-down package, which has reduced Qgd. One can see that there are no bends (leaning to the right) in the V_{DS} waveform, meaning that induced turn-on does not occur for this device in that particular design.



(a)



(b)



(c)

Figure 12 **(a) Buck converter layout with the added Cgs capacitor; (b) buck converter SR MOSFET V_{DS} and V_{GS} voltage waveforms; (c) buck converter efficiency curves comparison with and without an added external Cgs**

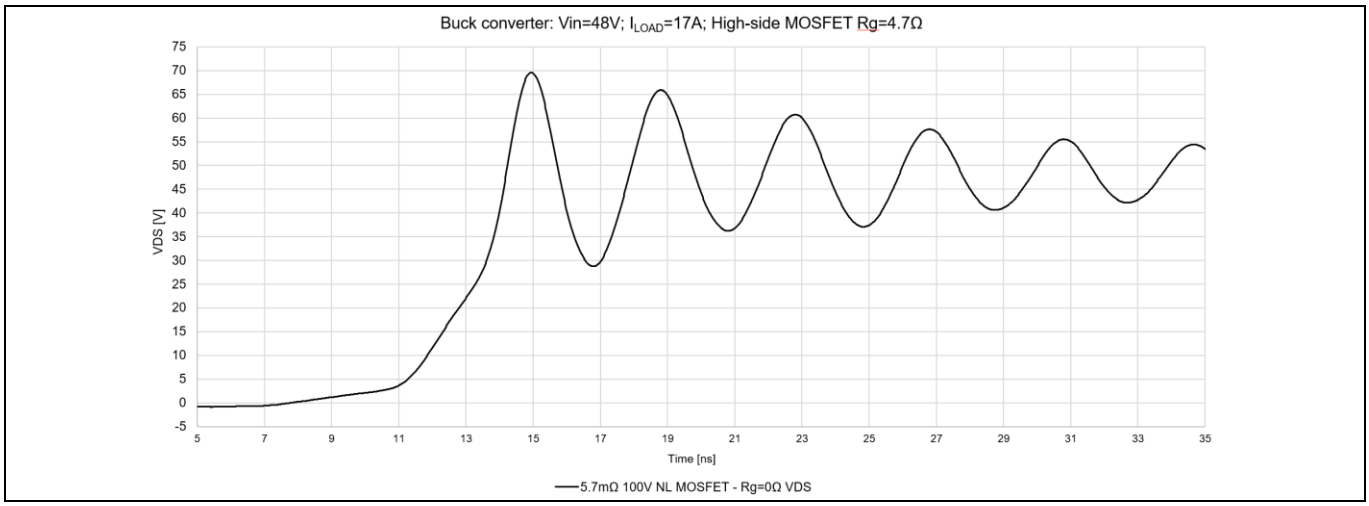


Figure 13 Buck converter SR MOSFET V_{DS} voltage waveform for a normal-level OptiMOS™ 6 100 V

2.3.2 Negative phase-node voltage spike

Another phenomenon associated with the commutation-loop inductance is the negative phase-node voltage spike observed in buck converters (see Figure 14 (b)). This issue has been raised and addressed in reference [15]. Figure 14 (a) shows the buck converter simplified diagram with the commutation-loop inductance split into two portions, L1 and L2. Figure 14 (b) shows the measured buck converter phase-node voltage undershoot. According to reference [15], the voltage undershoot is highly dependent on the input voltage V_{in} and on the ratio of one portion of the computation-loop inductance (L2) and the total commutation-loop inductance L1+L2: $\frac{L2}{(L1+L2)}$. The only design variables that reduce the negative spike lie within the board layout and package choice for the MOSFETs and capacitors, as the choice of package will influence the commutation-loop inductance and its distribution. In order to reduce the undershoot voltage, the ratio L2/(L1+L2) should be small. This should be accomplished by reducing L2 instead of enlarging L1, since it would lead to more dynamic power losses. The only way to achieve the goal of reduced undershoot without sacrificing efficiency is by shifting the existing loop inductance so that L2 is minimized. In practice, this is rather straightforward. Primarily a low inductive advanced package such as SuperSO8, S3O8 or DirectFET should be chosen. The lowest value for L2 is achieved when:

- the GND return path from the load is entering the source of the low side MOSFET before reaching the closest input decoupling capacitors and
- the inductor is connected as close as possible to the LS MOSFET drain terminal. These measures ensure lowest undershoot without sacrificing efficiency. Connecting the driver should follow the above reasoning and also take the reference potential directly from the source of the LS MOSFET.

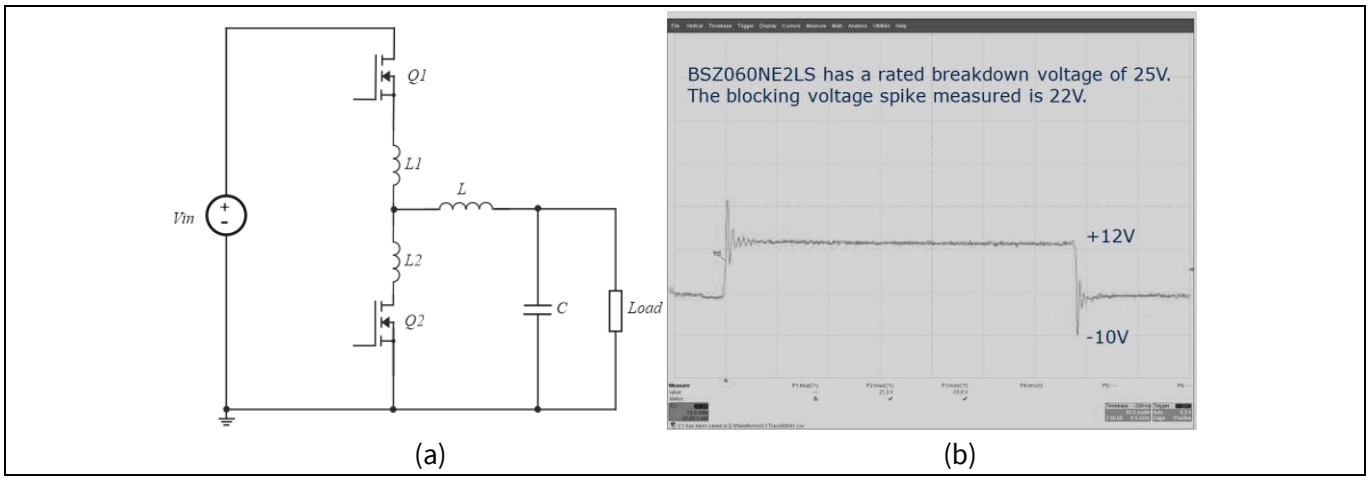


Figure 14 (a) Buck converter simplified diagram showing the commutation-loop inductance (L1 + L2); (b) measured buck converter phase-node voltage undershoot [15]

2.3.3 Low-damped V_{DS} voltage

As mentioned in Section 2.2.3, such fast-switching MOSFETs could have low R_{OSS}, which causes the natural V_{DS} voltage ringing to be low damped.

MOSFETs with low R_{OSS} are versatile and can be used either in resonant converters, where the low R_{OSS} value yields less loss, or in hard-switched applications with the aid of some snubber network that could be dissipative or non-dissipative. Next, some examples of the applications of such networks are shown.

There are a variety of solutions typically adopted to keep SR MOSFET V_{DS} voltage overshoot under control. Among them, it is possible to distinguish between passive snubbers (made up of passive components only) and active voltage clamps making use of controlled switches. Among the passive solutions, both dissipative (simple and polarized RC) and resonant snubbers are used.

2.3.3.1 Non-dissipative snubber networks

Two examples of commonly used non-dissipative snubber networks will be shown to illustrate how the overshoot at SR MOSFETs can be controlled in telecom DC-DC converters. In such converters, the SR commutation is inductively limited, with a large power loop inductance dominated by the transformer leakage inductance. The loop inductance stores high energy, and in most cases this high energy is enough to drive the SR MOSFETs into avalanche. The use of an active clamp is one of the most effective and efficient ways to keep drain-source voltage overshoot under control and within prescribed derating according to regulations. The adoption of such a concept can be extended to different applications as well, to keep MOSFETs' V_{DS} voltage overshoot within acceptable values and keep the SR MOSFET voltage class as low as possible, so that more cost-effective MOSFETs may be used in the application.

Active-clamp network

The first application example is an isolated DC-DC converter targeting radio frequency power amplifier (RFPA) applications that are powered off a DC bus with input voltage ranging from -60 V to -36 V and delivering a regulated +50 V output to power such amplifiers [16]. In this application, the active-clamp network is used on the secondary side, in the SR stage; Figure 15 illustrates the full-bridge rectifier part of the secondary side of the aforementioned converter, including the active-clamp network ($Q_{clamp,1\&2}$ + $C_{clamp,1\&2}$).

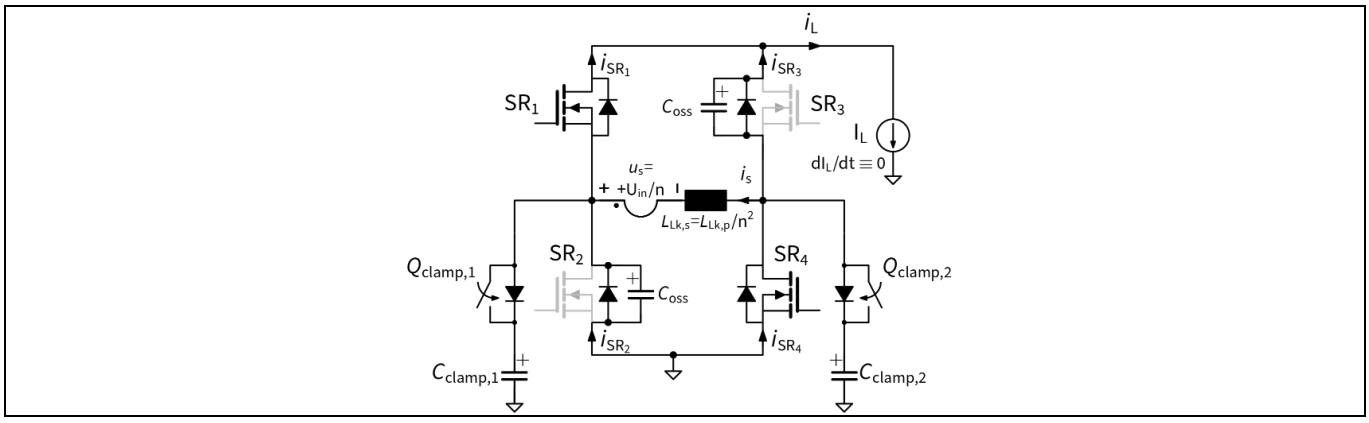


Figure 15 Telecom DC-DC converter SR stage (SR1 to SR4) with one active-clamp cell (Q_{clamp} + C_{clamp}) per SR node phase [16]

The motivation for the active clamp can be summarized as follows. During the dead time, SR_1 and SR_4 are turned on simultaneously while SR_2 and SR_3 are kept off. The SR_1 to SR_2 phase-node voltage rises up to the voltage level imposed by the transformer secondary winding. During this phase, the SR_2 and SR_3 body diodes recover and the energy trapped in the commutation-loop inductance is dumped into their output capacitances, C_{oss}, causing the phase-node voltage to overshoot.

The insertion of the active-clamp circuit curbs this voltage overshoot, clamping the phase node at the steady-state voltage across the clamp capacitor itself. The clamp capacitors are chosen to be large (i.e., 50 to 100 times larger than the SR C_{oss}, acting almost as voltage sources) and their steady-state voltages should be as close as possible to the transformer secondary voltage U_s. During the turn-off transient of the body diodes, the clamp is effectively in parallel with their output capacitances, through the body diode of Q_{clamp}, and must be realized with a switch able to operate over two quadrants, as the current must be able to reverse in order to reset (charge balance) the clamp capacitor at each cycle, through a resonance realized with the secondary-side referred leakage inductance. Such resonance is also responsible for recovering part of the energy associated with the turn-off of the SR rectifier, which otherwise would be lost.

More details on the operation modes of this snubber can be found in [16]. Figure 16 shows 150 V SR MOSFET V_{DS} voltage waveforms without and with the use of the active-clamp snubber. It can be seen that without the clamp the 150 V SR-MOSFET goes into avalanche and the voltage ringing is very pronounced. With the clamp, on the other hand, it can be seen that the overshoot is greatly reduced and the prescribed derating on the peak overshoot (90 percent of $V_{(BR)DSS}$, according to IPC-9592B) can be achieved.

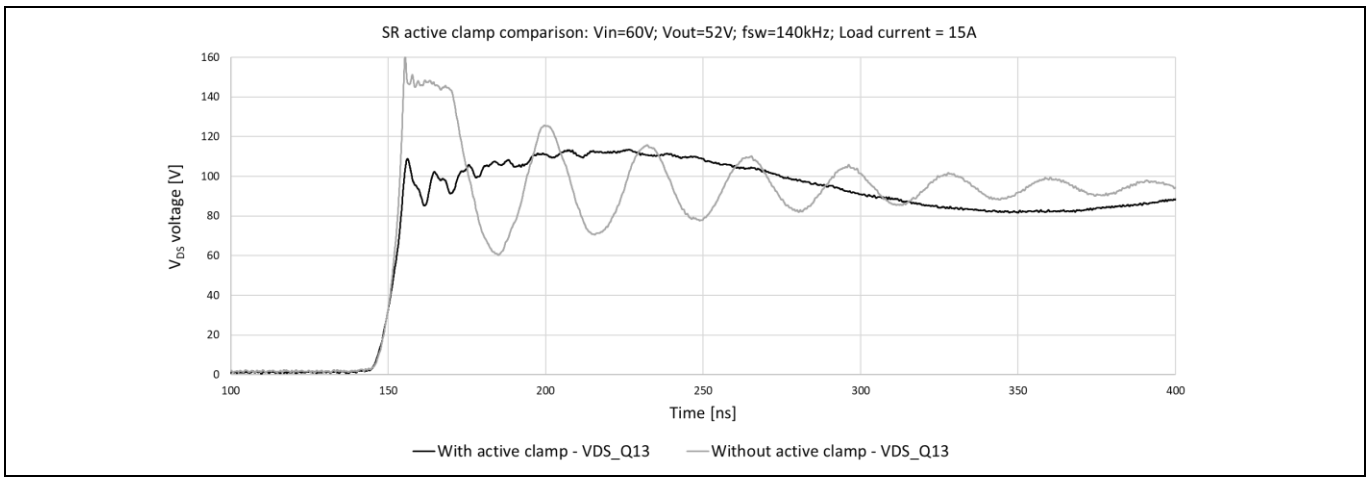


Figure 16 SR phase-node waveforms comparison with and without the SR active-clamp snubber

Capacitance-diode-lossless turn-off snubber

Another SR lossless snubber is the capacitance-diode-lossless (CDL) turn-off snubber, introduced in [17], which recycles the energy trapped in the transformer leakage inductance during the body-diode reverse recovery phase of the SR switches. This snubber is illustrated in Figure 17 in a center-tapped full-bridge DC-DC converter with one CDL snubber per SR MOSFET; the detailed information on how to design it can be found in [17] and therefore it is not discussed further here.

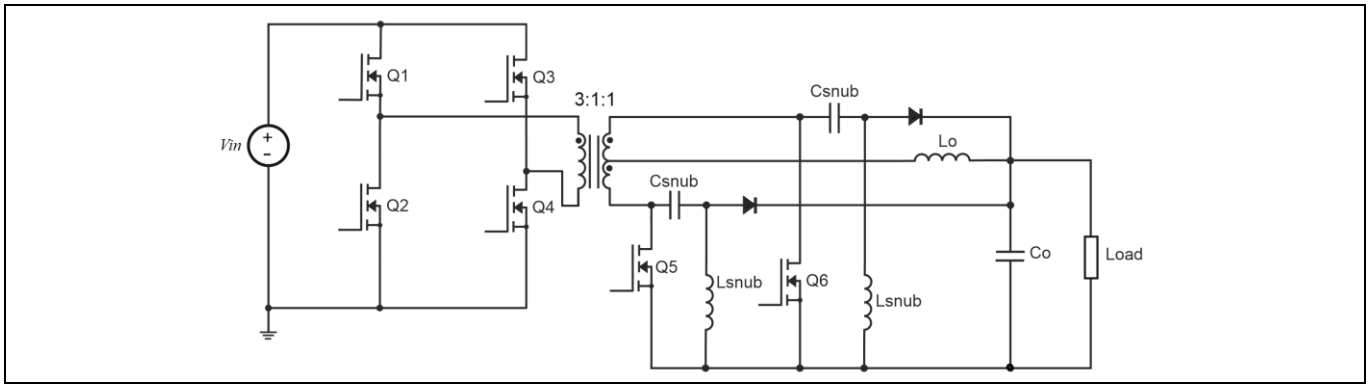


Figure 17 A center-tapped full-bridge DC-DC converter with one CDL snubber per SR MOSFET [17]

2.3.3.2 Phase-node voltage clamp network

The RCD voltage clamp network is another cost-effective solution to limit the MOSFET V_{DS} voltage overshoot. This network is illustrated in Figure 18, where it is used to limit the phase-node voltage overshoot on the primary side of a center-tapped full-bridge DC-DC converter commonly used in telecom applications. As the SR MOSFETs' body diodes have their reverse recovery charges recovered, the energy trapped in the commutation-loop inductances is dumped into the Q2 and Q4 C_{OSS} capacitors and the excess is diverted by diodes Dcla1 and 2 into the clamp capacitor Ccla. Ccla should be large enough to absorb the charge delivered during the clamping interval with little rise in voltage, which should be kept equal or slightly higher than the voltage level of V_{in} [18]. The loop formed by the protected MOSFET, the clamp diode and the clamp capacitor should be the smallest possible in order to minimize this loop inductance and reduce the MOSFET V_{DS} voltage overshoot. If the PCB layout makes it difficult to have a single clamp capacitor with two small commutation loops, one should consider splitting Ccla in two, as seen in Figure 19. The clamp diode must also be selected carefully: its breakdown voltage should be as low as possible in order to minimize its forward recovery time. Schottky diodes could also be used since they have no forward recovery time and will yield low clamped voltage. The bleeder resistor Rcla is selected to maintain the voltage in Ccla at a safe level for the MOSFET under the worst-case operating conditions. A design criterion can be obtained by equating the average current input to Ccla via diodes Dcla1 and Dcla2 to the average current output from Ccla via Rcla, as explained in [18]. Figure 20 shows a comparison of the phase-node voltages of a 600 W telecom DC-DC brick converter with and without the clamp network in the corner case of highest input voltage (72 V) and maximum load current; it can be seen that the phase-node voltage overshoot has been reduced by at least 14 V with the aid of this network. Figure 19 illustrates the clamp-network component values used in the experiment. Figure 21 shows the comparison of the system efficiency of this converter with and without the clamp network for 48 V and 60 V input voltages; it can be seen that, at 48 V, in the half-to-full load range, there is a mild efficiency gain. At 60 V input voltage, there is a mild drop in efficiency throughout the load range, showing that it has not been optimized for this corner case.

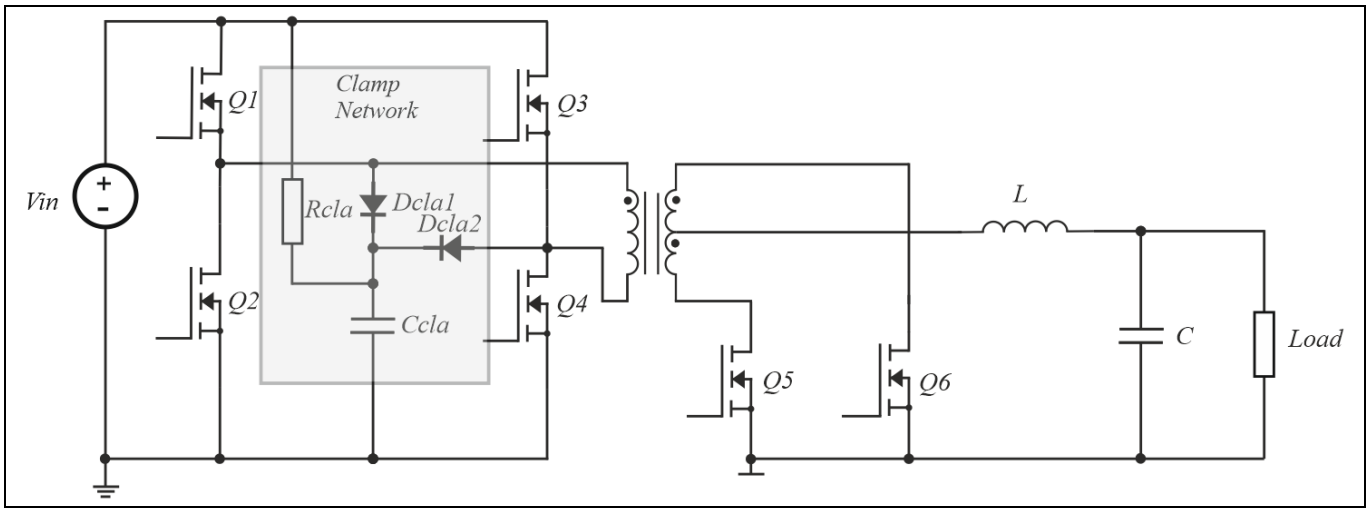


Figure 18 **A full-bridge DC-DC converter with center-tapped SR stage using a clamp network on the primary side to limit the phase-node voltage overshoot**

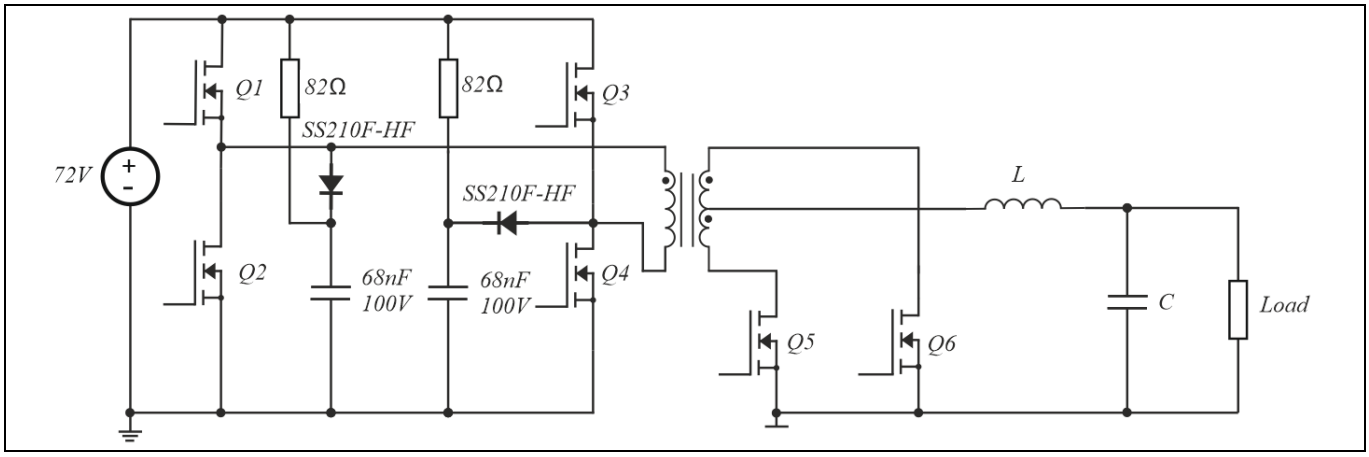


Figure 19 **A full-bridge DC-DC converter using one clamp network per phase node to ease layout and reduce the clamp network commutation-loop inductance**

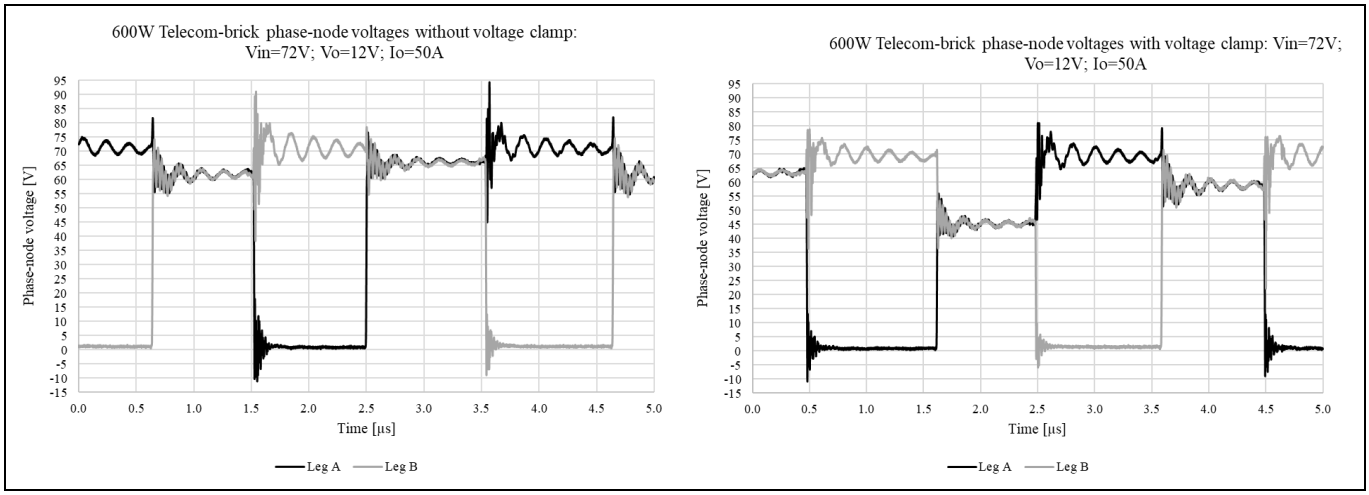


Figure 20 **Comparison of the phase-node voltages of a 600 W telecom DC-DC brick converter with and without the clamp network in the corner case of highest input voltage (72 V) and maximum load current**

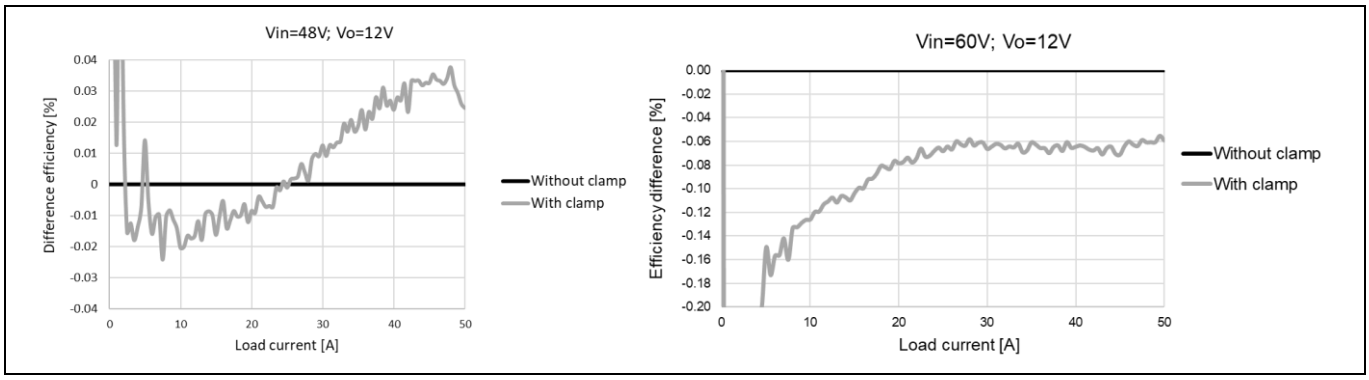


Figure 21 **System efficiency comparison of the 600 W telecom DC-DC brick converter with and without the clamp network for V_{in} = 48 V and 60 V**

3 Summary

A brief introduction to MOSFET fast switching in hard-switched applications has been given here, highlighting its motivation, benefits, key aspects to take full advantage of it and mitigation measures to deal with possible difficulties.

Infineon's new OptiMOS™ 6 80 V and 100 V technologies, combined with the PQFN package concept with source-down and DSC technologies, yield very fast-switching devices that facilitate SMPS designs with exceptionally good layout and thermal management.

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