

Low-cost heatsinking of SMD power MOSFETs on a single-layer PCB

Wave-soldered SuperSO8 cooled by a through-hole heatsink

About this document

Heatsinking Surface Mount Devices (SMDs) is a challenging task, especially in low-cost applications.

This application note describes the thermal management of a SMD together with a cost-optimized through-hole heatsink on a single-layer, wave-soldered PCB, with an additional focus on solder voids.

Intended audience

Power supply designers.

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1 Introduction

1 Introduction

The thermal management of Through Hole Devices (THDs) is a well-known topic.

Cooling SMDs is not easy, but there are still many ways to solve this problem in applications.

Typically two different solutions are used. A small heatsink could be mounted on top of the device, or the heat could be transferred through the PCB to the other side using thermal vias. A combination of both methods increases the possibility of reducing the chip temperature, and sometimes even more exotic (and more expensive) solutions are used.

The situation becomes more tricky if thermal vias are not possible, as on a single-sided PCB, as used in many consumer products. In several of these low-cost solutions a combination of SMDs and THDs on one single PCB will be necessary. The SMDs are positioned and glued first, and the THDs are assembled before finally the wave-soldering is done. One solution to cool the SMD is to glue a small heatsink on top, but in most cases this is not easy for mechanical reasons.

This application note shows another solution: using SMDs and THDs together on a wave-soldered, single-sided PCB with a cheap THD heatsink. The influence of solder voids (due to wave-soldering) and different chip sizes is also shown. Using forced air-cooling optimizes thermal management. This is shown in [Chapter 3.2](#).

2 Set-up description

2 Set-up description

Figure 1 shows a cheap L-shaped metal profile forming the heatsink for the SMD (SuperSO8). The SMD is positioned on the bottom (solder) side and the thermal connection between both devices is provided by the copper tracks of the PCB.

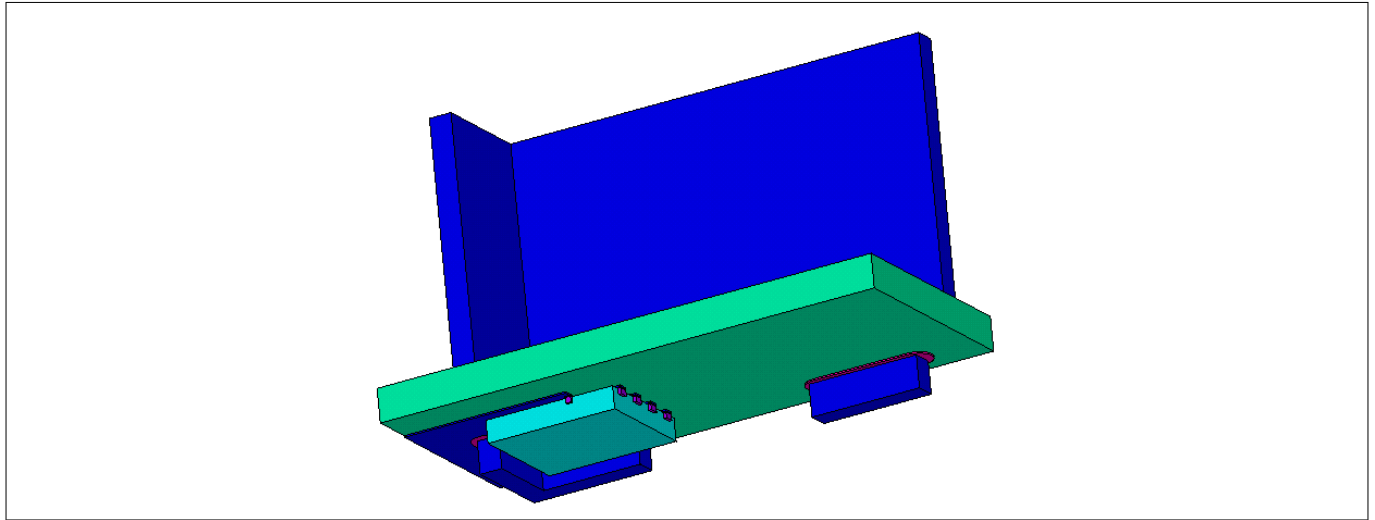


Figure 1 3D image of the simulated arrangement

Figure 2 shows the mechanical drawings including different shapes of solder voids. The thermal connection between the SuperSO8 and the heatsink on the top side is provided by a copper area of 8 mm × 7.5 mm (70 μm/ 2 oz. copper thickness). The SuperSO8 is positioned very close to the solder connections of the heatsink.

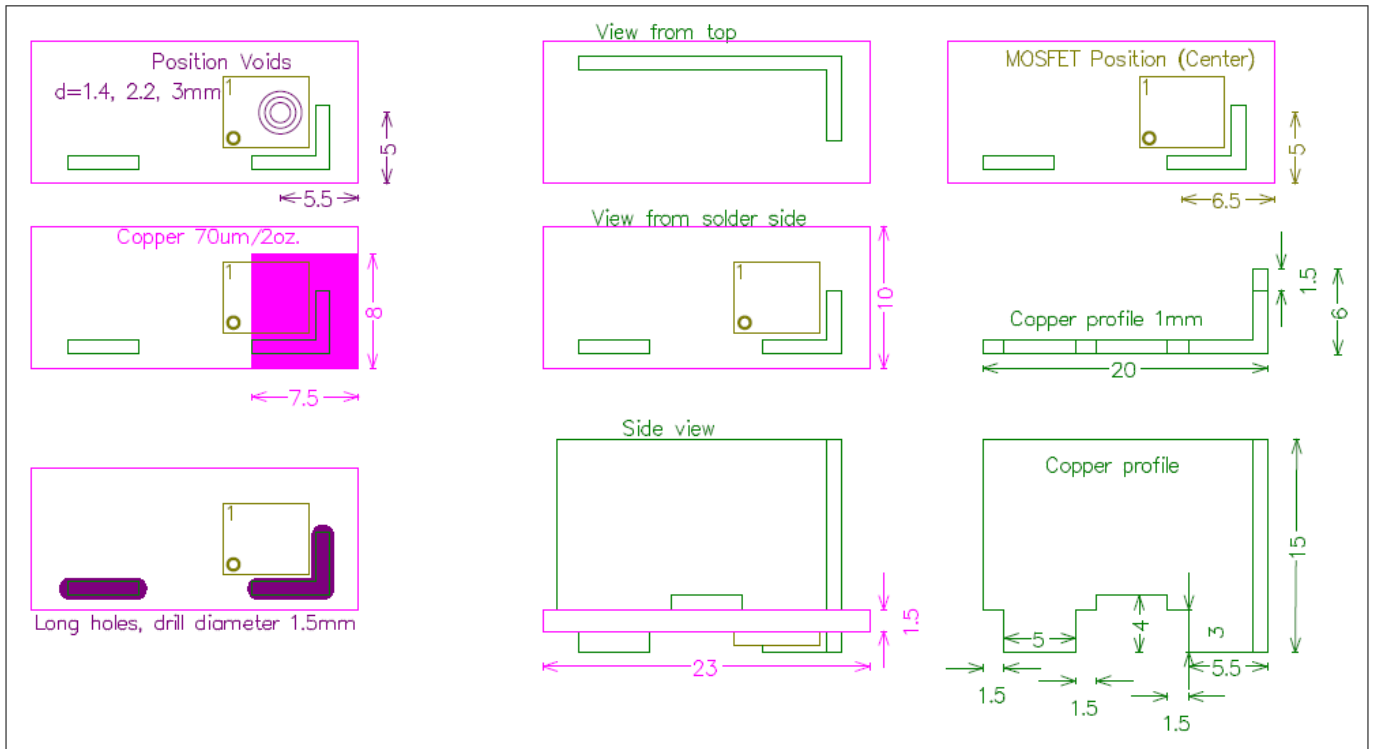


Figure 2 Mechanical drawings of simulated set-up

Figure 3 shows the simulated MOSFETs. On the left the bottom view of the packaged part is shown with the copper lead-frame in purple. The light green area in the middle and right images represents the corresponding chips.

2 Set-up description

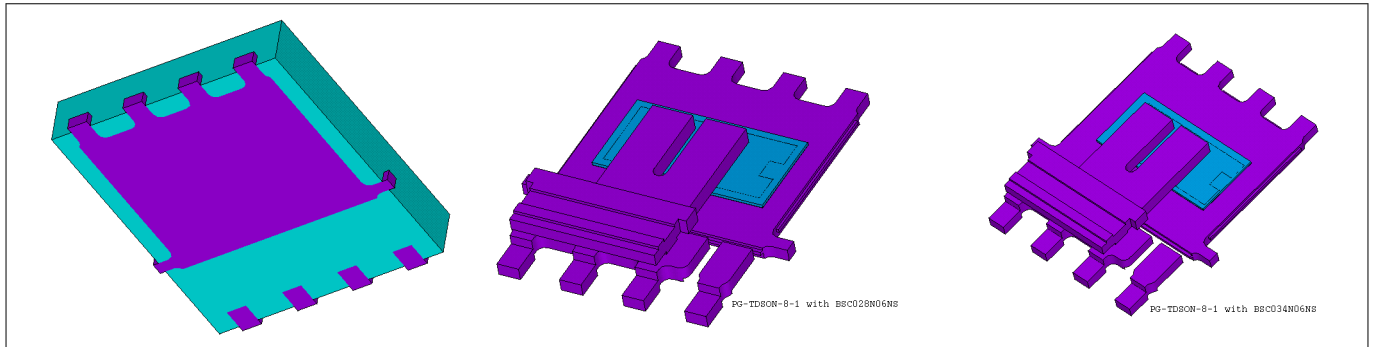


Figure 3 SuperSO8 with two different chip sizes

Wave-soldering SMDs can lead to solder voids, i.e. gas bubbles between the part and the PCB. These voids increase the thermal resistance from case to PCB by acting as a thermal insulator.

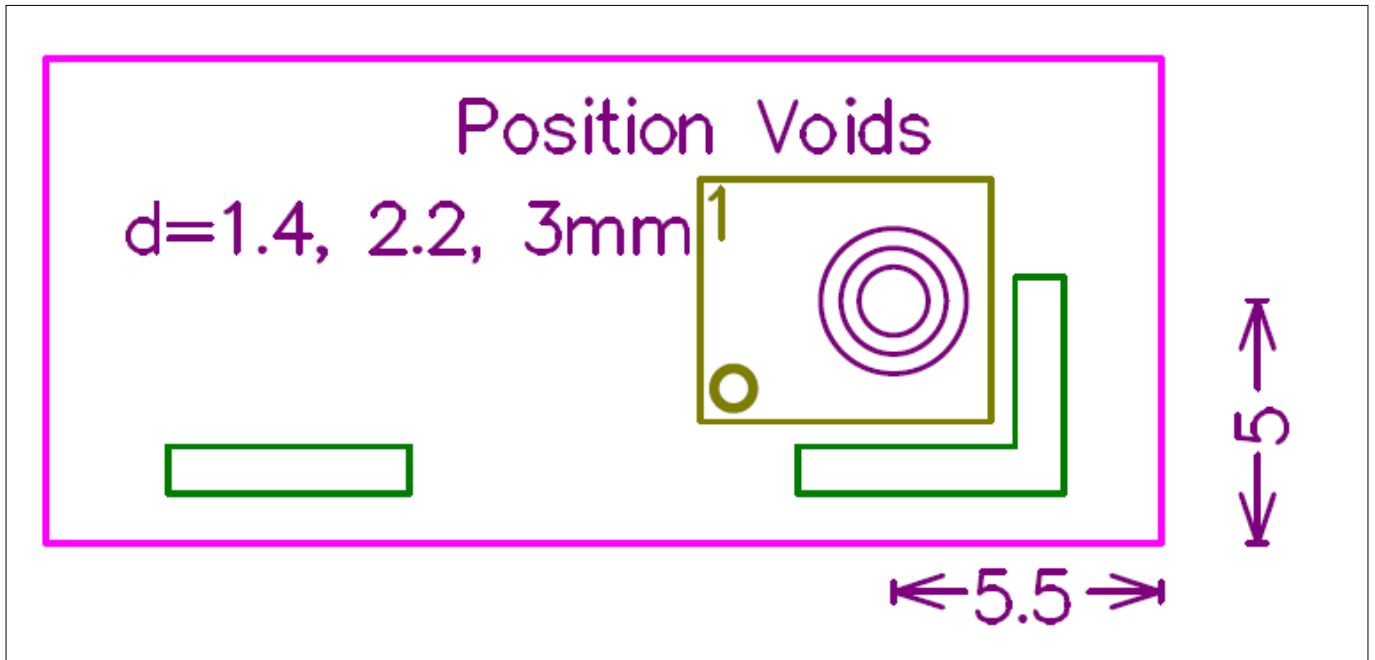


Figure 4 Position of simulated solder voids

3 Simulation results

3 Simulation results

3.1 Results “free convection” without voids over the full power range 0.5 W to 7 W

For the boundary condition “free convection/radiation on whole system” the power range from 0.5 W to 7.0 W was simulated and the thermal resistance junction to ambient R_{thJA} was calculated. The calculations showed that the impact of the void size was negligible. So only the cases “no void” and “maximum void” (diameter 3 mm) are shown in the following diagrams. All simulated voids have a circular shape.

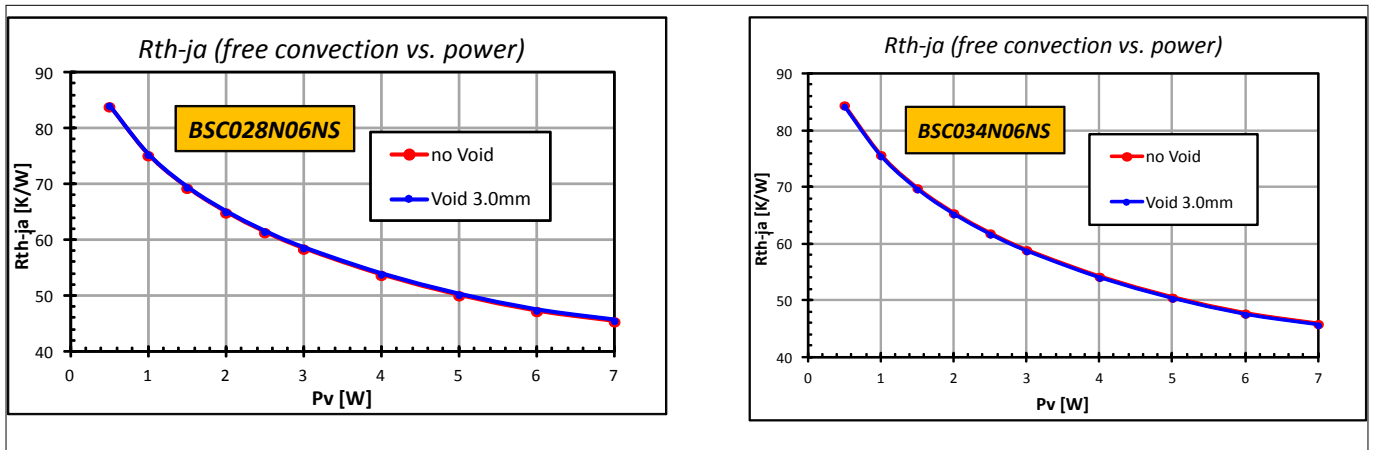


Figure 5 R_{thJA} for BSC028N06S (left) and BSC034N06NS (right), full power range and free convection

3.2 Results “forced convection 1 m/s” 0.5 W to 2.5 W

In case of additional forced convection around the heatsink the thermal behavior is much better, resulting in a lower R_{thJA} .

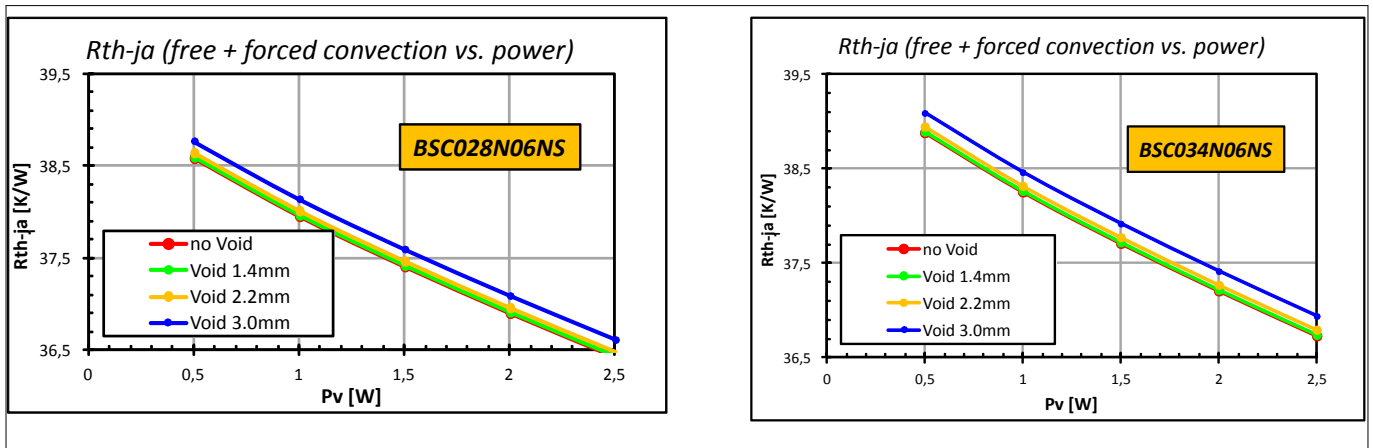


Figure 6 R_{thJA} for BSC028N06S (left) and BSC034N06NS (right), 2.5 W with forced convection

3.2.1 Temperature distribution in thermal pictures

For this boundary condition the temperature distributions are shown for the power of 2 W (no void/max. void).

3 Simulation results

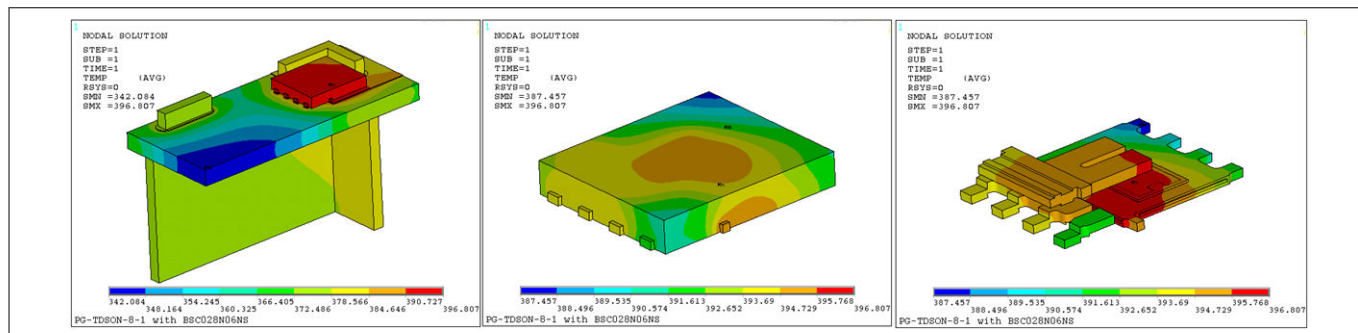


Figure 7 Temperature distribution “forced convection 1 m/s, no void” for BSC028N06NS

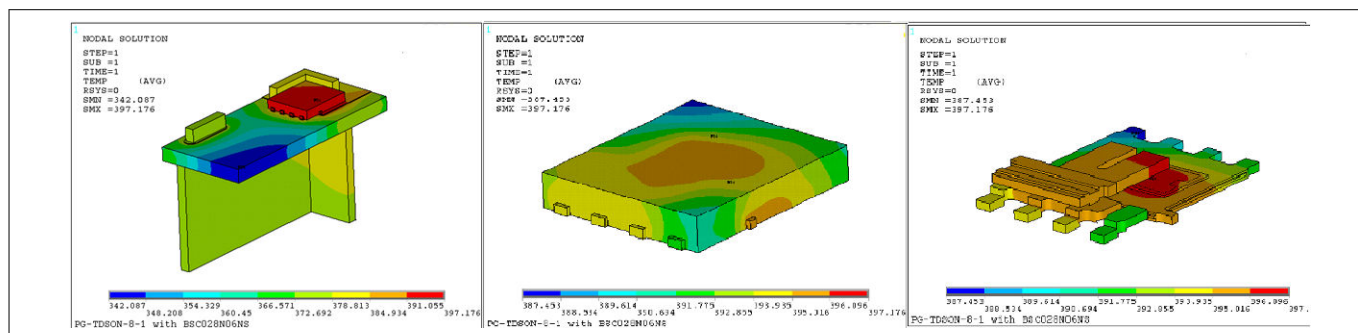


Figure 8 Temperature distribution “forced convection, max. void (d = 3 mm)” for BSC028N06NS

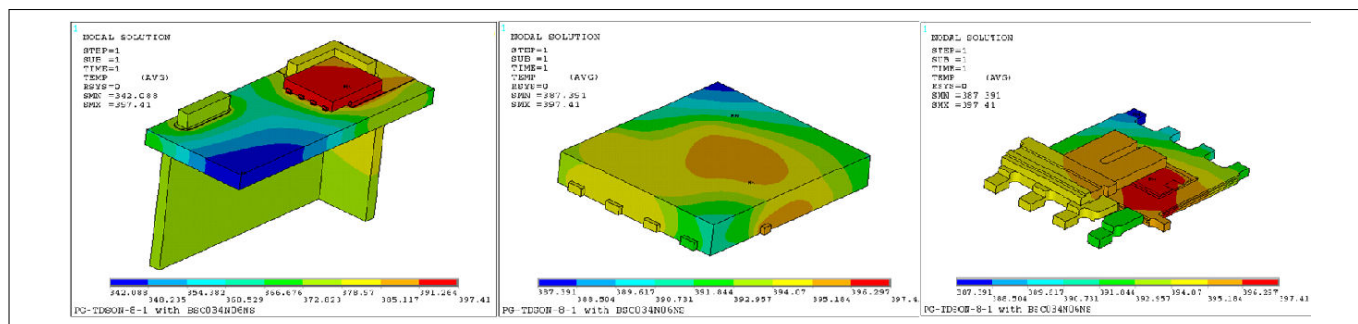


Figure 9 Temperature distribution “forced convection, no void” for BSC034N06NS

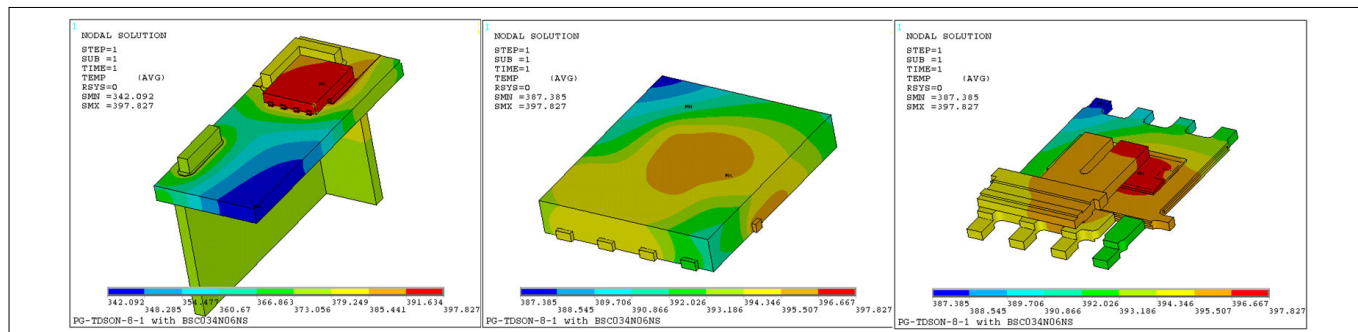


Figure 10 Temperature distribution “forced convection, max. void (d = 3 mm)” for BSC034N06NS

3 Simulation results

3.2.2 Temperature distribution tables

Void	Pv [W]	Tj [°C]	Tpcb [°C]	Ttop [°C]	Rth-ja [K/W]	Void	Pv [W]	Tj [°C]	Tpcb [°C]	Ttop [°C]	Rth-ja [K/W]
0 mm	0.5	91.99	91.87	91.58	83.98	0 mm	0.5	92.14	91.98	91.68	84.27
	1	125.22	124.95	124.37	75.22		1	125.51	125.18	124.57	75.51
	1.5	154.05	153.63	152.75	69.37		1.5	154.49	153.98	153.07	69.66
	2	179.90	179.33	178.15	64.95		2	180.50	179.79	178.57	65.25
	2.5	203.52	202.77	201.29	61.41		2.5	204.26	203.35	201.82	61.70
	3	225.37	224.44	222.66	58.46		3	226.27	225.14	223.30	58.76
	4	265.02	263.74	261.33	53.75		4	266.23	264.67	262.18	54.06
	5	300.45	298.85	295.78	50.09		5	301.96	300.01	296.84	50.39
	6	333.55	331.63	328.06	47.26		6	335.39	333.06	329.36	47.57
	7	367.96	365.72	361.67	45.42		7	370.07	367.34	363.15	45.72
1.4mm	0.5	92.00	91.87	91.59	83.99	1.4mm	0.5	92.14	91.98	91.70	84.28
	1	125.22	124.95	124.40	75.22		1	125.52	125.18	124.61	75.52
	1.5	154.06	153.63	152.80	69.37		1.5	154.50	153.98	153.12	69.67
	2	179.92	179.33	178.21	64.96		2	180.52	179.79	178.64	65.26
	2.5	203.54	202.77	201.37	61.41		2.5	204.29	203.35	201.90	61.71
	3	225.39	224.44	222.75	58.46		3	226.30	225.14	223.40	58.77
	4	265.05	263.74	261.45	53.76		4	266.27	264.67	262.32	54.07
	5	300.49	298.85	295.93	50.10		5	302.01	300.02	297.01	50.40
	6	333.61	331.64	328.24	47.27		6	335.46	333.07	329.57	47.58
	7	368.02	365.73	361.88	45.43		7	370.14	367.35	363.39	45.73
2.2mm	0.5	92.02	91.85	91.62	84.04	2.2mm	0.5	92.17	91.97	91.73	84.34
	1	125.27	124.92	124.46	75.27		1	125.57	125.15	124.68	75.57
	1.5	154.13	153.59	152.90	69.42		1.5	154.58	153.94	153.23	69.72
	2	180.01	179.27	178.34	65.01		2	180.62	179.73	178.79	65.31
	2.5	203.65	202.69	201.54	61.46		2.5	204.42	203.27	202.10	61.77
	3	225.53	224.35	222.95	58.51		3	226.46	225.05	223.63	58.82
	4	265.23	263.62	261.72	53.81		4	266.48	264.55	262.63	54.12
	5	300.72	298.71	296.27	50.14		5	302.28	299.86	297.39	50.46
	6	333.89	331.47	328.66	47.31		6	335.79	332.89	330.04	47.63
	7	368.34	365.53	362.35	45.48		7	370.52	367.14	363.93	45.79
3.0mm	0.5	92.08	91.82	91.68	84.17	3.0mm	0.5	92.24	91.93	91.79	84.48
	1	125.40	124.85	124.57	75.40		1	125.71	125.07	124.80	75.71
	1.5	154.32	153.49	153.06	69.55		1.5	154.80	153.82	153.41	69.86
	2	180.27	179.13	178.56	65.13		2	180.91	179.58	179.02	65.45
	2.5	203.97	202.53	201.80	61.59		2.5	204.78	203.08	202.39	61.91
	3	225.91	224.15	223.28	58.64		3	226.89	224.81	223.98	58.96
	4	265.74	263.35	262.15	53.94		4	267.05	264.24	263.09	54.26
	5	301.35	298.37	296.80	50.27		5	302.99	299.47	297.96	50.60
	6	334.66	331.08	329.31	47.44		6	336.65	332.44	330.75	47.78
	7	369.24	365.06	363.11	45.61		7	371.52	366.60	364.75	45.93

Figure 11 Temperature distribution BSC028N06NS (left) and BSC034N06NS (right)

Void	Pv [W]	Tj [°C]	Tpcb [°C]	Ttop [°C]	Rth-ja [K/W]	Void	Pv [W]	Tj [°C]	Tpcb [°C]	Ttop [°C]	Rth-ja [K/W]
0 mm	0.5	69.29	69.17	69.00	38.58	0 mm	0.5	69.44	69.29	69.11	38.88
	1	87.95	87.70	87.35	37.95		1	88.25	87.95	87.56	38.25
	1.5	106.11	105.72	105.18	37.41		1.5	106.56	106.09	105.50	37.71
	2	123.81	123.27	122.53	36.90		2	124.41	123.76	122.97	37.21
	2.5	141.07	140.38	139.44	36.43		2.5	141.82	140.99	139.99	36.73
1.4mm	0.5	69.30	69.17	69.01	38.59	1.4mm	0.5	69.45	69.29	69.12	38.89
	1	87.96	87.70	87.38	37.96		1	88.26	87.95	87.60	38.26
	1.5	106.13	105.73	105.22	37.42		1.5	106.58	106.10	105.56	37.72
	2	123.82	123.28	122.59	36.91		2	124.43	123.77	123.04	37.21
	2.5	141.09	140.39	139.52	36.43		2.5	141.85	141.00	140.07	36.74
2.2mm	0.5	69.32	69.16	69.05	38.64	2.2mm	0.5	69.47	69.29	69.16	38.95
	1	88.01	87.69	87.45	38.01		1	88.32	87.93	87.68	38.32
	1.5	106.19	105.70	105.33	37.46		1.5	106.66	106.07	105.68	37.77
	2	123.92	123.24	122.74	36.96		2	124.54	123.73	123.20	37.27
	2.5	141.20	140.34	139.69	36.48		2.5	141.98	140.95	140.27	36.79
3.0mm	0.5	69.38	69.14	69.10	38.77	3.0mm	0.5	69.54	69.26	69.22	39.09
	1	88.14	87.65	87.56	38.14		1	88.46	87.88	87.80	38.46
	1.5	106.39	105.64	105.50	37.59		1.5	106.88	105.99	105.86	37.92
	2	124.18	123.15	122.96	37.09		2	124.83	123.62	123.44	37.41
	2.5	141.53	140.23	139.97	36.61		2.5	142.34	140.81	140.58	36.94

Figure 12 Temperature distribution BSC028N06NS (left) and BSC034N06NS (right); 2 W situation is highlighted in yellow

4 Conclusion

4 Conclusion

The simulated low-cost solution (single-sided, SuperSO8 with THD heatsink, wave-soldered) can easily handle 2 W or slightly more with a forced convection of 1 m/s.

The influence of solder voids and different chip sizes on the R_{thJA} and chip temperature is negligible.

The bottleneck of the thermal path is the thermal resistance of the connection between the device and the heatsink.

5 Revision history

5 Revision history

Document version	Date of release	Description of changes

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