CoolMOS™

Primary Side MOSFET Selection for LLC Topology

Application Note

About This Document

This application note introduces the key factors of power MOSFETs in Zero Voltage Switching (ZVS) operation and provides the methods for improving reliability and efficiency of a primary side MOSFET in LLC topology.

Scope and Purpose

Guide the users how to select the proper MOSFET in LLC topology.

Intended audience

Experienced power supply designers who want to optimize their system for reliability and efficiency

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1 Introduction

Over the past several years, energy efficiency and power density have become the major challenges for power conversion. Rising energy leads to a higher cost of delivering power. In the meantime, the demand for compact power supplies grows significantly. It requires power supplies with high performance, low profile and high power density. LLC resonant converters are widely adopted due to the advantages such as high efficiency, high power density, and low electromagnetic interference in power supply applications among the various power converter designs. It is important to select the right and suitable MOSFET not only for the efficiency but also the reliability of a LLC resonant converter. In addition to the basic criteria such as package, drain-source voltage rating, drain current rating and on state resistance as written in Ref. [1], two considerations are required for power MOSFET selection and driving signal design in an LLC resonant converter: (a) maintenance of Zero Voltage Switching (ZVS) operation of the power MOSFET; (b) avoidance of system reliability issues due to incomplete body diode reverse recovery in the power MOSFET. Based on these two directions, this application note discusses the key factors of power MOSFETs in ZVS operation and provides the methods for improving reliability and efficiency of a primary side MOSFET in LLC topology.

2 Zero Voltage Switching of LLC

One of the advantages of the LLC resonant converter is its ability to achieve zero voltage switching over its entire load range. With zero voltage switching, turn on loss for the primary side devices is eliminated. For primary side MOSFET to achieve ZVS in LLC topology, there are three considerations as below: (a) inductive load of LLC power stage; (b) complementary control signal for high/low side switch. It means the duty of high/low side gate signals are 50% and with 180° phase difference; (c) suitable dead time to sustain ZVS; Figure 1(a) shows the circuit diagram of a half bridge LLC resonant converter and Figure 1(b) shows the inductive load causing voltage leading the current for achieving ZVS. For achieving ZVS operation at the primary side of this converter at “turn-on time”, the circuit should operate in the inductive region and the resonant inductor current must be high enough to discharge the voltage of effective capacitance appearing in parallel with drain-sources of the power MOSFETs.

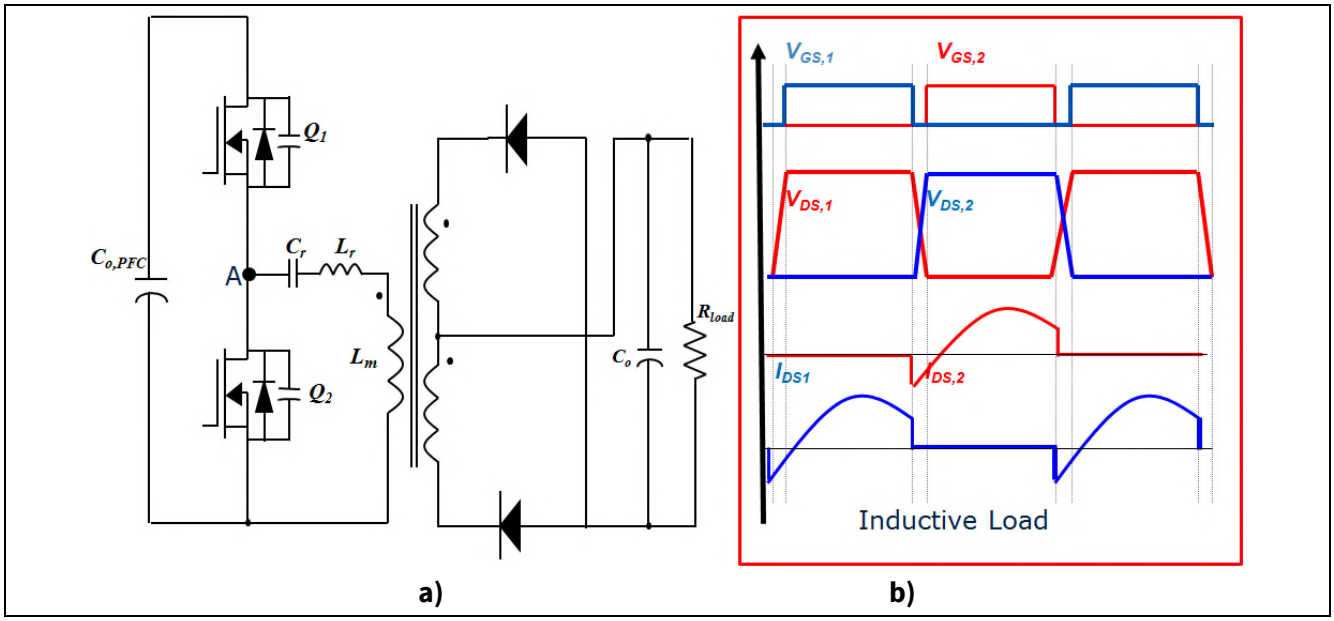

Figure 1 LLC resonant converter (a) and waveforms of inductive load (b)

2.1 The effect of MOSFET Output Capacitance (C_{oss})

When both the primary sides MOSFETs are off, the circulating current in the resonant tank will charge and discharge the output capacitances of the switches. The equivalent circuit of a half-bridge LLC resonant converter in dead time when both Q_1 and Q_2 are turned off is as shown in Figure 2, wherein node A is the center point between power MOSFETs Q_1 and Q_2. Based on the resonant equation of the L-C switching circuit, the voltage at node A is obtained as:

$$V_A = (V_{in} - V_c) + I_{D,off}\sqrt{\frac{L_{eq}}{C_{eq}}}\sin\omega_r t \quad (1)$$

Wherein, V_{in} is the voltage on $C_{O,PFC}$,Vc is the voltage on C_r, L_{eq} is the sum of L_r and L_m, C_{eq} is the equivalent capacitance in the equivalent circuit and $\omega_r = \frac{1}{\sqrt{L_{eq}C_{eq}}}$.

For ZVS before Q_1 turns on, the voltage at node A must satisfy:

$$(V_{in} - V_c) + I_{D,off}\sqrt{\frac{L_{eq}}{C_{eq}}}\sin\omega_r t \geq V_{in} \quad (2)$$

Since the maximum value for a sinusoidal wave is 1, the conditions of the switching voltage from equation (2) are given as:

$$L_{eq}I_{D,off}^2 \geq C_{eq}V_c^2 \quad (3)$$

Wherein, $I_{D,off}$ is the initial current level on the inductor when the power MOSFET is turned off.

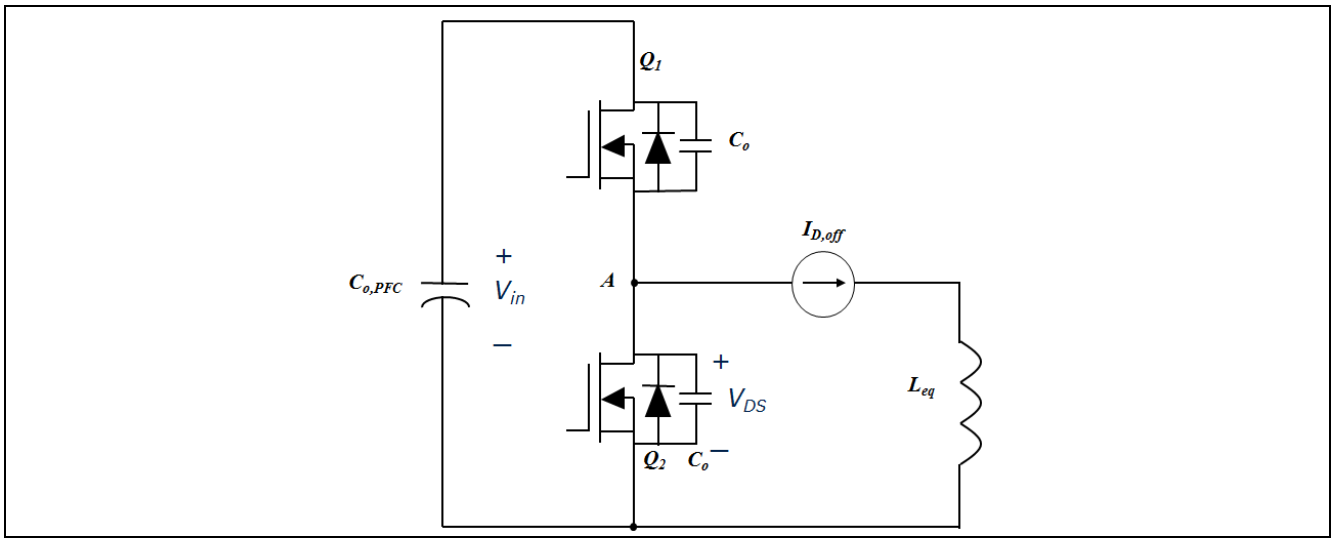

Figure 2 Equivalent circuit of the half- bridge LLC resonant converter during dead time

Equation (3) as defined appears to formulate the condition for ZVS from the perspective of resonant energy. However, the fact is that equation (3) is derived from the voltage equation of node A and more importantly, the charging/discharging time for the output capacitance of the power MOSFET in the dead time are decided by the L_{eq} and C_{eq} resonant frequency. Furthermore, C_{eq} varies with the D-S voltage drop V_{DS} and is not a constant value as shown in Figure 3. This is due to the fact that the output capacitance of the power MOSFET is a main contributing component that either increases or decreases in relation to V_{DS}, wherein the characteristics of the charge distribution in the power MOSFET varies with V_{DS}. As a result, variations in C_{eq} must also be taken into account when considering the ZVS conditions, as the discharge time of the power MOSFET output capacitance is also affected by C_{eq}.

A question that might arise at this point is, what is the real-world equivalent capacitance to design for? As shown in the equivalent circuit in Figure 2, the output capacitances of the two power MOSFETs in the half-bridge circuit are connected in parallel with regards to the equivalent inductance. When taking the effects of V_{DS} into account, the sum of the two V_{DS} from both power MOSFETs connected in series equals the PFC voltage. As a result, the equivalent capacitance from the power MOSFET in regards to the equivalent inductance in the half-bridge LLC circuit is as shown in Figure 3(b), wherein the equivalent capacitance increases exponentially for V_{DS}＜50V or V_{DS} >350V.

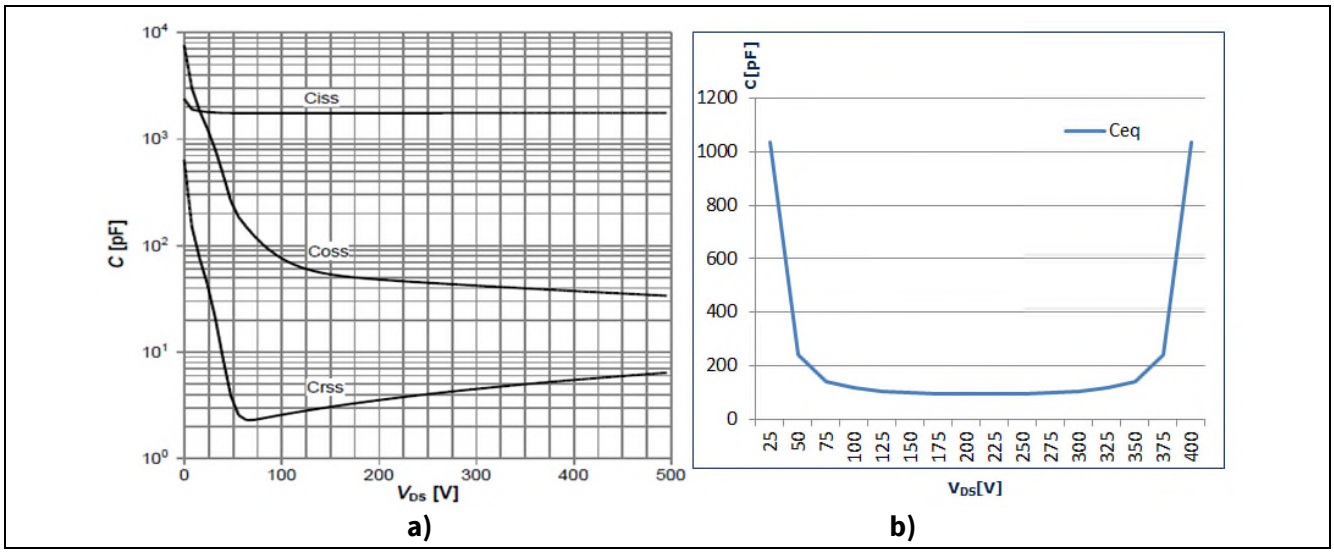

Figure 3 a) Parasitic capacitance distribution in power MOSFET (CoolMOS™ IPP60R190P6)
b) C_{eq} of LLC equivalent circuit (CoolMOS™ IPP60R190P6)

The discharging V_{DS} voltage in the half-bridge LLC power MOSFET is sectioned into four parts as shown in Figure 4(I) 380V→300V; (II) 300V→200V; (III) 200V→100V; and (IV)100V→0V. Even though there is an 80V drop in section (I), the total time in sections (I) and (IV) is two-thirds of the full discharge time under the condition of identical voltage drops and constant inductor current. This is due to the fact that the power MOSFET output capacitance increases exponentially when V_{DS} approaches 0V, thus it is harder to discharge the output capacitance resulting in a longer L-C resonant period and longer discharge time.

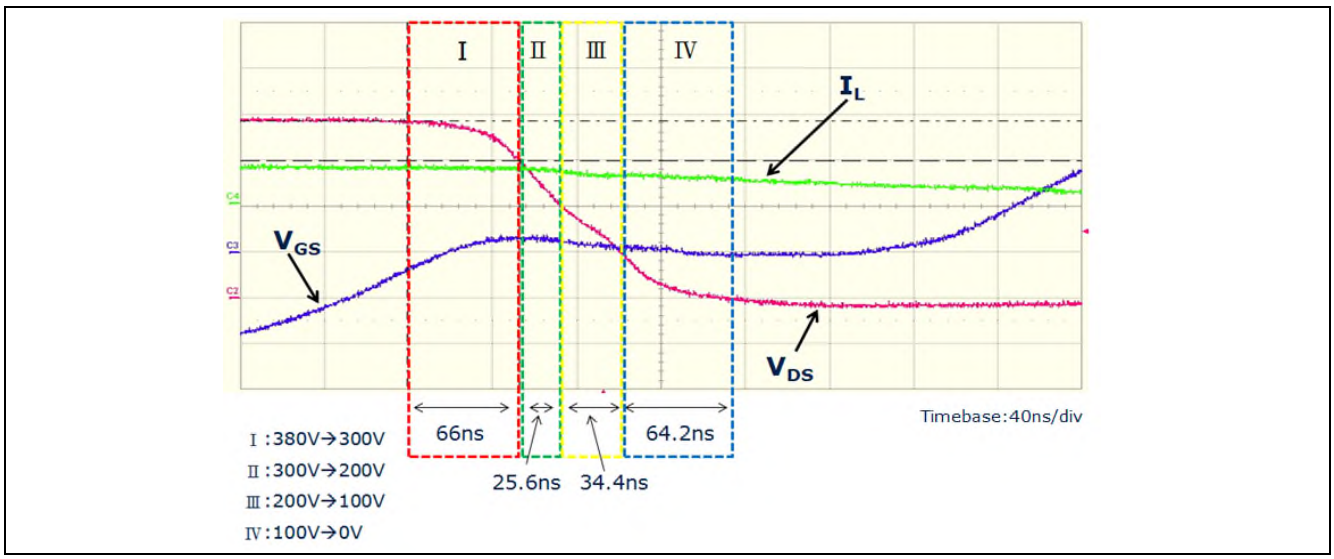

Figure 4 Discharging the C_{oss} of half-bridge LLC power MOSFET

For the consideration of the power MOSFET in the half-bridge LLC resonant converter, selecting a power MOSFET with low output capacitance at lower V_{DS} voltages can achieve ZVS more easily under identical inductor current conditions. In addition, efficiency can also be improved through reducing dead time.

2.2 The effect of dead time

Dead time is required to discharge completely the effective capacitance appeared in parallel with drain–sources of the power MOSFETs to realize the ZVS operation at the worst-case conditions applied to the

converter. For identifying the required dead time, two important limitations must be considered. One of them depends on the power MOSFET's minimum required dead time, which can be obtained from the datasheet easily, by considering MOSFET parameters such as body diode reverse recovery time, turn-on and -off delay times, rise, and fall times. Another is related to the minimum necessary dead time for achieving ZVS operation even under the worst-case conditions, i.e., when maximum input voltage is applied to the converter and the output voltage is adjusted at minimum value under light or no load conditions. In the situations that ZVS operation needs longer dead time than that of the power MOSFET's necessary value, the greater value can be used for satisfying both cases, but this approach will sacrifice the converter efficiency.

There are three kinds of C_{OSS} values in datasheets of CoolMOS™: C_{OSS} at specified V_{DS} value, $C_{o(er)}$ and $C_{o(tr)}$. $Co_{(tr)}$ is an equivalent fixed capacitance of MOSFET to determine the charging/discharging time of C_{OSS} of MOSFET regardless of topology. The dead time selection should ensure ZVS of two primary side MOSFET at maximum switching frequency, where the magnetizing current to charge and discharge MOSFET C_{OSS} is the minimum. Equation (4) shows the relation of dead time and MOSFET $C_{O(tr)}$.

$$t_{dead} = \frac{2 * C_{O(tr)} * V_{in}}{I_{mag\_min}} \tag{4}$$

Wherein, I_{mag_min} is the minimum magnetizing current to charge and discharge C_{oss}.

The four most common waveforms and solutions for ZVS power MOSFETs are as shown in Figure 5, where modification of the circuit for optimal efficiency can be carried out according to the instructions given. Figure 5(a) illustrates the perfect ZVS diagram. In Figure 5(b), V_{DS} cannot fully discharge to 0V before the control signal V_{GS} is sent, thus it is recommended to reduce the magnetizing inductance value in the transformer, slightly increase the dead time or replace the power MOSFET wiSth a higher $R_{DS(on)}$. In Figure 5(c), the power MOSFET achieves ZVS, but the inductance current is insufficient to continually forward bias the body diode; thus it is recommended to slightly reduce dead time. ZVS is achieved in Figure 5(d), but the excessive dead time results in reduced efficiency; thus, it is recommended to reduce dead time.

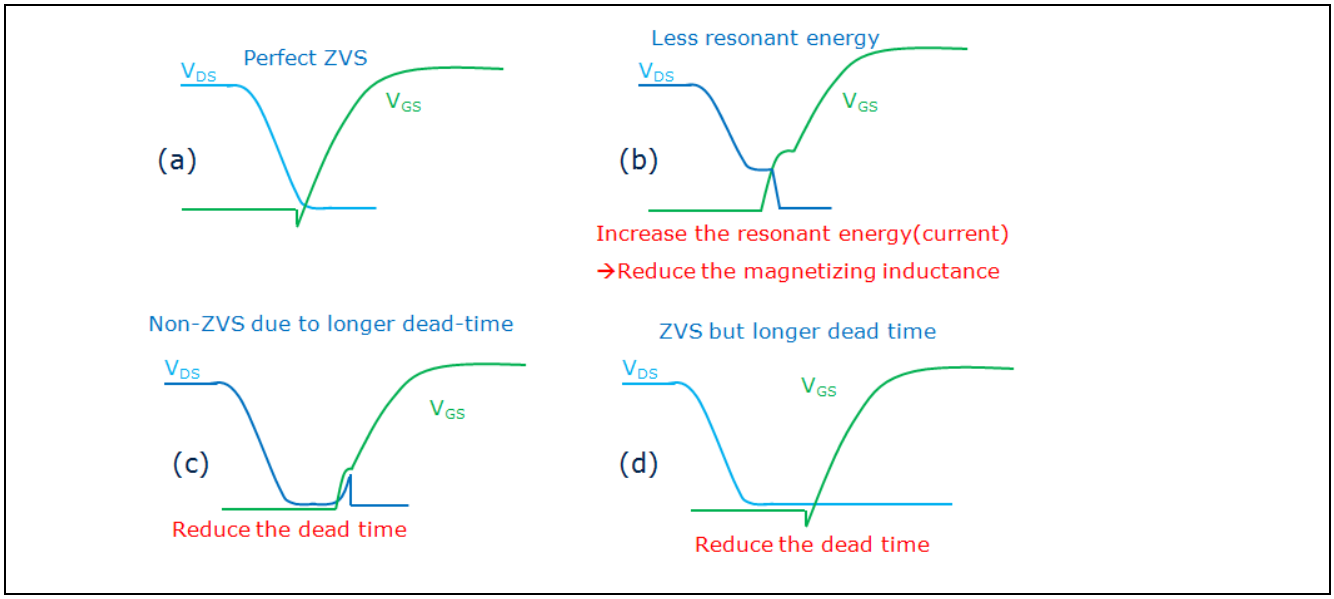

Figure 5 Waveforms for ZVS power MOSFET and solutions

3 Incomplete Reverse Recovery of the MOSFET Body Diode

Since the body diode of the primary side MOSFET in the LLC resonant converter must conduct to achieve ZVS, it is necessary to observe the conditions under which the body diodes conduct. An LLC resonant converter is a load resonant converter that easily achieves high energy conversion efficiency with the ZVS power MOSFET. Design considerations of the power MOSFET in the primary side LLC resonant converter are relatively simple compared to a phase-shifted full-bridge converter, as it is not affected by leading or lagging waveforms with regards to the power MOSFET. With the exception of the capacitive load resulting from overload or short-circuit conditions, during startup only system reliability issue caused by incomplete body diode reverse recovery of the power MOSFET need to be considered. The following would discuss the issue of system reliability during startup caused by incomplete body diode reverse recovery of the power MOSFET and the recommended solutions.

3.1 Structural view of incomplete reverse recovery of MOSFET body diode

Due to the structure of a conventional MOSFET, the incomplete reverse recovery of the primary side MOSFET's body diode would cause a failure. Figure 6(a) shows a cross sectional view of a conventional power MOSFET. Figure 6(b) shows the destruction mechanism by lateral hole currents below the n+-region. The hole current flowing through the n--drift region enters the p-well from the side thus flowing laterally through the p-well towards the metal contact (shown in grey). The current will cause a voltage drop along its way towards the contact. This voltage drop tends to forward bias the pn-junction formed by the p-well and the n+-region, if the reverse current through the device is large enough, a voltage can develop across the base resistance causing the turn-on of the intrinsic bipolar transistor. As this bipolar current has a positive temperature coefficient, the total current through the transistor is likely to form a filament at one or few cells, driving the transistor locally into thermal destruction.

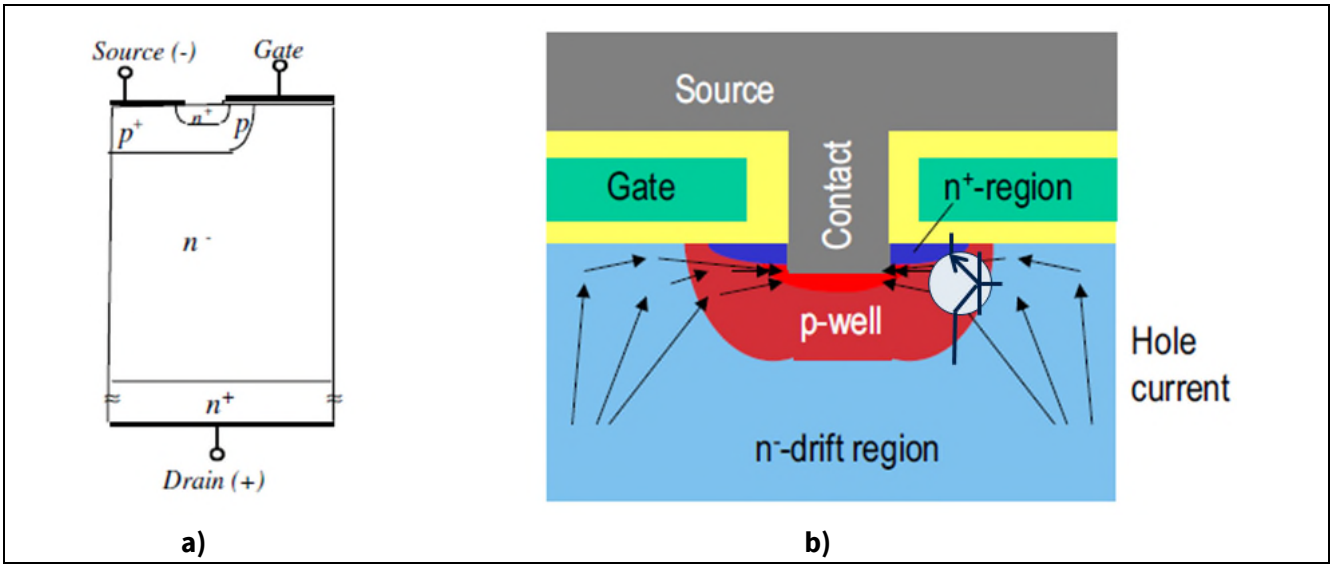

Figure 6 a) Cross Section of a Conventional Power MOSFET cell
b) Detailed view of a conventional power MOSFET cell, illustrating the destruction mechanism by lateral hole currents below the n+-region

Figure 7(a) shows a cross section of CoolMOS™ Cell. There is only one distinctive difference to Figure 6(a) of the conventional MOSFET: the p-column reaching deep into the active area of the device.

The p-column acts to balance out the charge in the conduction channel and allow for the device to have a higher doping concentration while still maintaining the same blocking voltage.

As shown in Figure 7(b), the hole current is not focused in the curvature of the p-well like in a conventional MOSFET cell, but comes up straight towards the metal contact. The reason for this behavior is that the p- and n-column create a horizontal electric field deep inside the MOSFET, which separates electrons and holes. Therefore the device is not subjected to lateral hole currents below the n+-source region, which are supposed to ignite the parasitic npn-bipolar transistor. Thus the CoolMOS™ transistor does not suffer from therefore mentioned root cause for the failures of the ZVS converter.

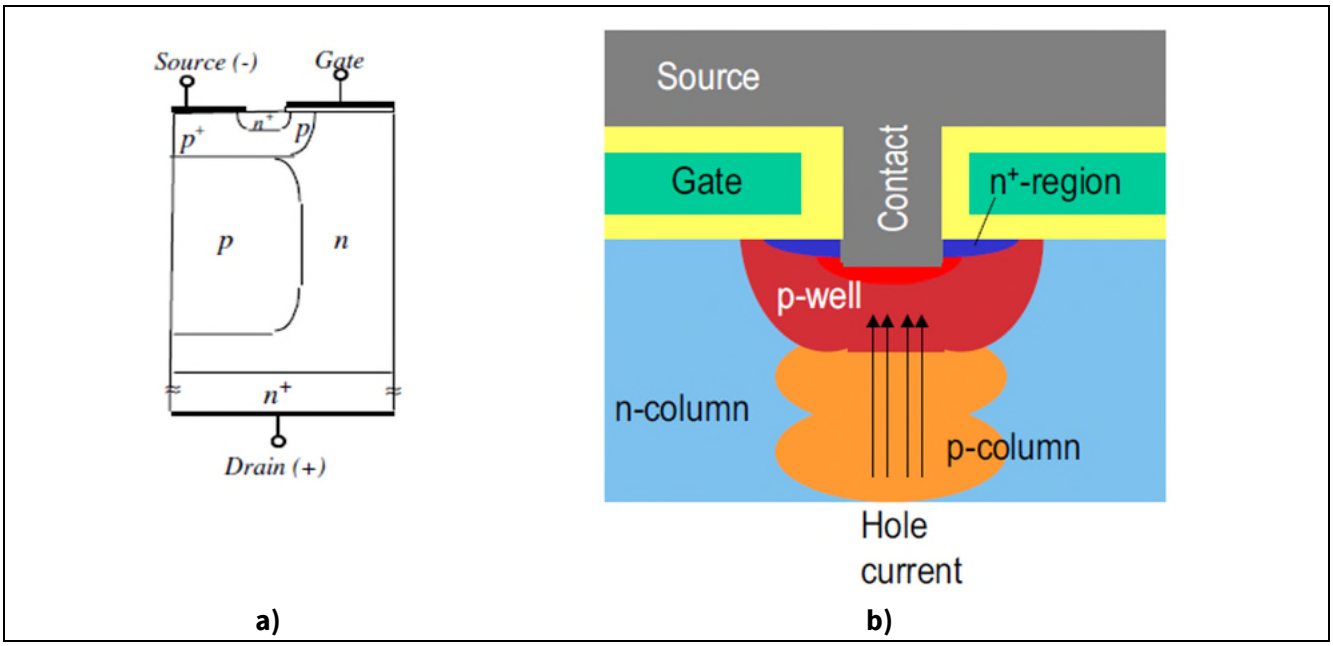

Figure 7 a) Cross Section of CoolMOS™ Cell
b) Detailed view of a CoolMOS™ transistor cell, illustrating the focused hole current flowing vertically upward towards the metal contact

3.2 Issue of incomplete reverse recovery of MOSFET body diode

Figure 8 illustrates the four modes of ZVS power MOSFET for the LLC resonant converter: (I) When the driving signal V_{GS} is LOW, the primary side equivalent inductor current discharges the output capacitance (C_{oss}) of the power MOSFET completely and the body diode is forward biased with a reverse current (S→D); (II) When the driving signal is HIGH, the body diode is forward biased and the power MOSFET is turned on with a reverse current (S→D); (III) When the driving signal is HIGH, the power MOSFET is turned on with a forward current (D→S); (IV) When the driving signal is LOW, the primary side equivalent inductance charges the output capacitance of the power MOSFET.

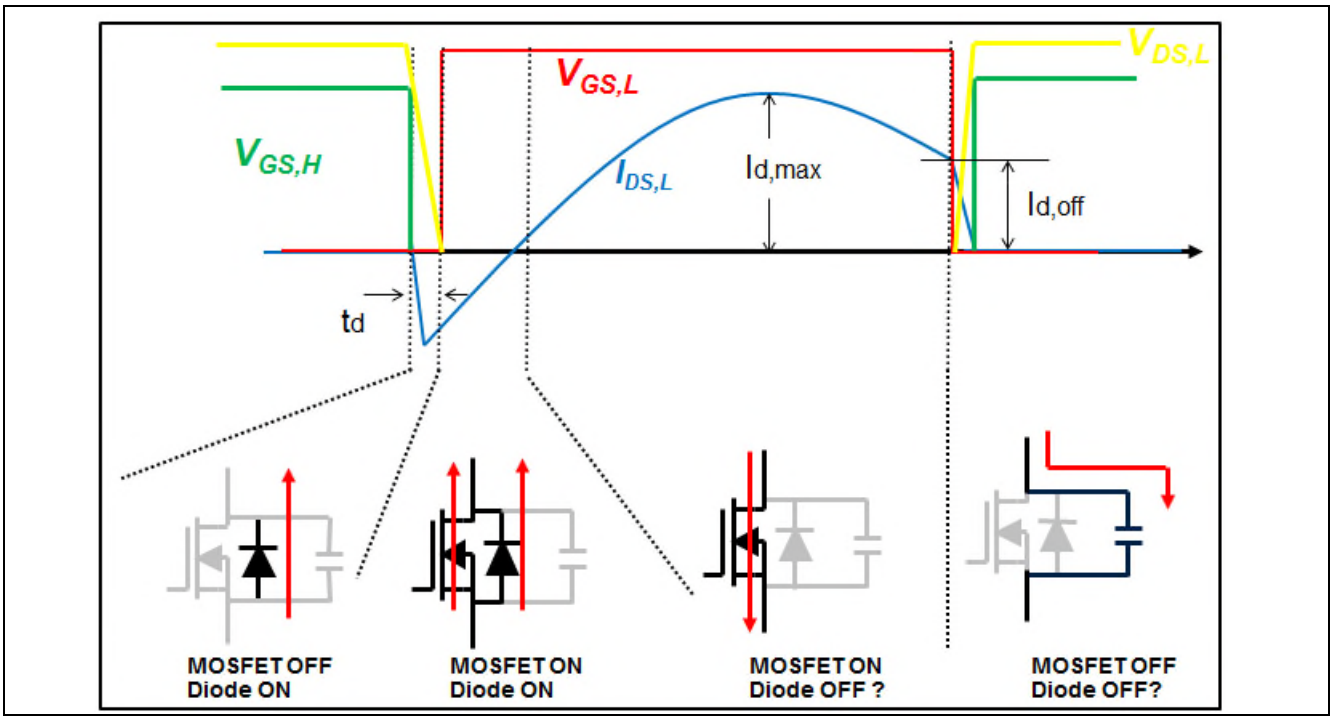

Figure 8 Four modes of the ZVS power MOSFET for the half-bridge LLC resonant converter

The three parameters to take note of are: dead time (t_d), terminal turn-off current ($I_{d,off}$) of the power MOSFET, and maximum current ($I_{d,max}$) of the power MOSFET when turned on, wherein the dead time and terminal turn-off current of the power MOSFET are the key to achieve ZVS. According to prior experiments, the product of the maximum turn-on current and turn-on resistance of the power MOSFET ($I_{d,max} \times R_{DS(on)}$) is the maximum reverse bias voltage of the body diode when the power MOSFET is turned on. If this is too low or the forward (D→S) current is not present, the body diode cannot completely reverse recovery or enter reverse recovery when the power MOSFET turns on. When the matching power MOSFET in the half-bridge circuit turns on, the circuit generates a reverse recovery current with very steep slew rate (di/dt) and very high peak voltage in order to turn off the body diode, thus possibly damage the power MOSFET. It is worth noting that the condition for achieving ZVS in the power MOSFET is not the same as the condition for the body diode reverse recovery.

As shown in Figure 9(a), even though the power MOSFET has achieved ZVS with the higher magnetizing inductance value in the half-bridge LLC circuit, the reverse recovery current with very steep slew rate still flows through the matching power MOSFET when it is turned on. This is due to the insufficient maximum turn-on current in the power MOSFET. In identical experiments, lowering the magnetizing inductance value for higher maximum turn-on current in the power MOSFET will result in higher reverse voltage in the body diode when the power MOSFET turns on. The body diode naturally cuts off and the reverse recovery current diminishes as shown in Figure 9(b).

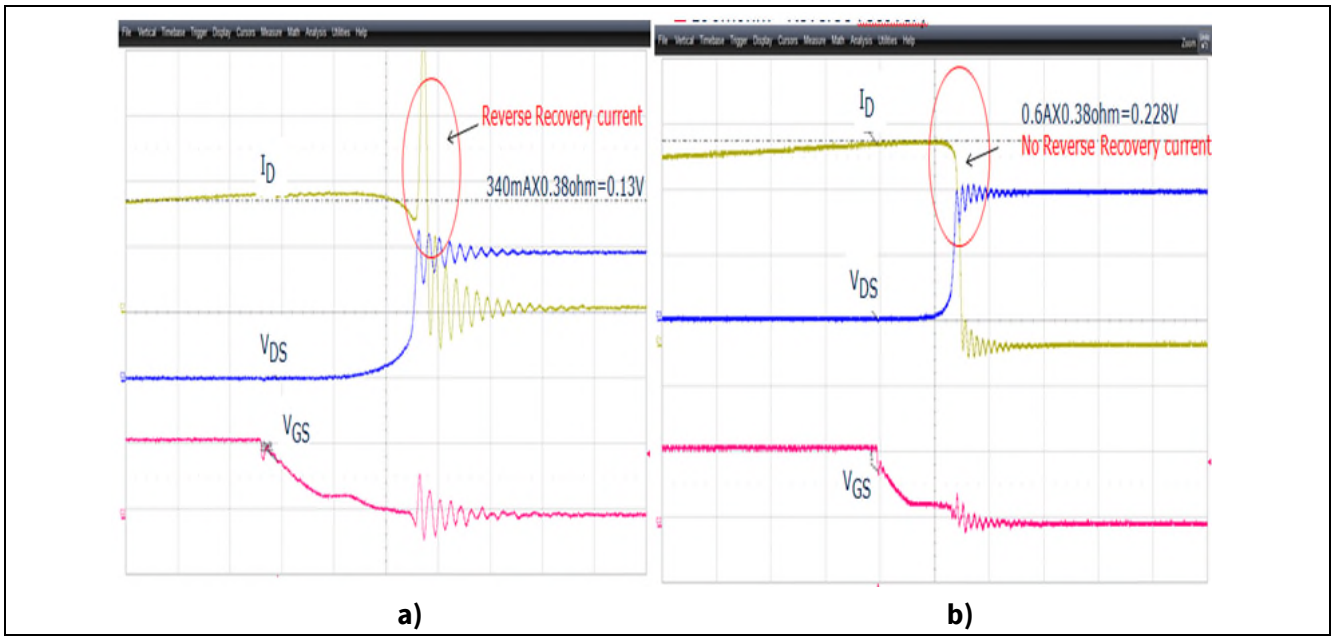

Figure 9

a) Reverse recovery current in matching power MOSFET when body diode is not completely reverse recovery

b) Reverse recovery current not shown in matching power MOSFET when body diode is completely reverse recovery

In the traditional half-bridge LLC resonant converter and asymmetric half-bridge converter architecture, the resonant capacitance C_r, resonant inductance L_r, and transformer are connected in series, and then connected to the power MOSFET in half-bridge form, as shown at the right hand side of Figure 10.

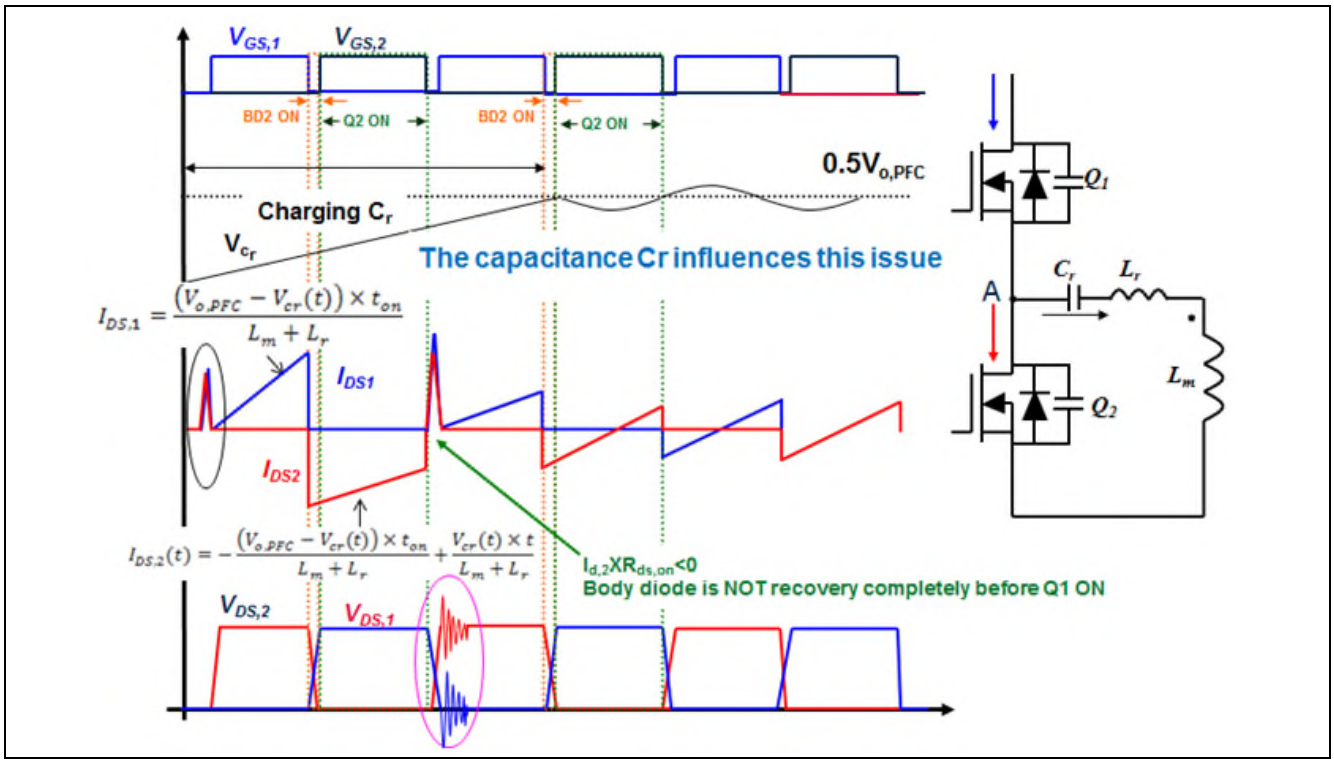

Figure 10 Possible damage to the power MOSFET during startup of the half-bridge LLC converter due to incomplete body diode reverse recovery

In this circuit, the high side power MOSFET Q_1 turns on to instantaneously set the voltage of node A and charges the output capacitance of Q_2. During the start of the first cycle when Q_1 turns on, a large current flows through these two power MOSFETs to set the voltage at node A. The current equation flowing through Q_1 is then $\frac{V_{PFC}-V_{cr}(t)}{L_r+L_m} \times t$. After a period of t_{on}, the inductance current at the first-stage is therefore $\frac{V_{PFC}-V_{cr}(t)}{L_r+L_m} \times t_{on}$. This inductance current is then the initial current to the body diode of the bottom power MOSFET Q_2 when Q_1 turns off. When Q_2 turns on, the primary side inductance current increases from an initial value of $-\frac{V_{PFC}-V_{cr}(t)}{L_r+L_m} \times t_{on}$ with charging slew rate of $\frac{V_{cr}(t)}{L_r+L_m}$. As a result, the current equation for Q_2 turning on is given as:

$$i_2(t) = -\frac{V_{PFC}-V_{cr}(t1)}{L_r+L_m} \times t_{on} + \frac{V_{cr}(t)}{L_r+L_m} \times t \quad (5)$$

Hence, the slew rate of Q_1 current is inversely proportional to the voltage $V_{cr(t)}$ across the resonant capacitor. After a period of t_{on}, the higher Q_1 current results in a higher absolute value of the Q_2 initial current. The flatter the slew rate of Q_2 current is, the harder it is for Q_2 current to return to zero and enter the positive (D flowing into S as positive) region even before Q_2 turns off and Q_1 turns on. As a result, the voltage at node A remains at 0V due to the fact that the body diode of Q_2 is still not completely reverse recovery. At the second cycle when Q_1 turns on to set the node A voltage, a reverse recovery current is applied to the body diode of Q_2 to remove its clamping voltage and then charge the output capacitance of Q_2. However, currents with high slew rate cannot be avoided in this process of reverse recovery generated by Q_1 on the body diode of Q_2 through a high peak voltage to Q_2. Sometimes this peak will exceed the maximum breakdown voltage of the power MOSFET and thus directly damage the transistor, as shown in Figure 11.

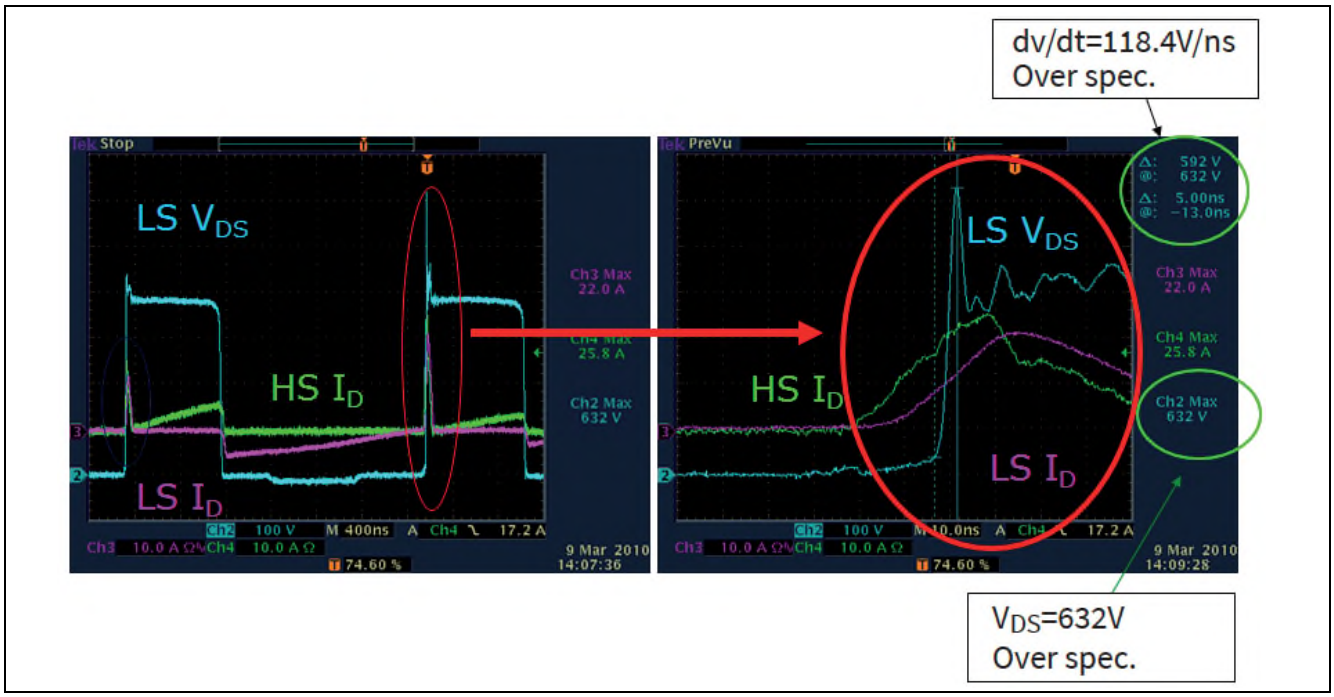

Figure 11 During startup, excessive peak voltage caused by reverse recovery current flowing to power MOSFET

3.3 Solution for the issue of incomplete reverse recovery of MOSFET body diode

In real-world applications designing for higher output capacity, a power MOSFET with higher resonant capacitance and lower turn-on resistance will further exacerbate this situation. In this case, using the quick reverse recovery body diode of the power MOSFET with low Q_{rr} flattens out the peak voltage but cannot fully eliminate the voltage peak. In practice, the most effective solutions are as shown in Figure 12.

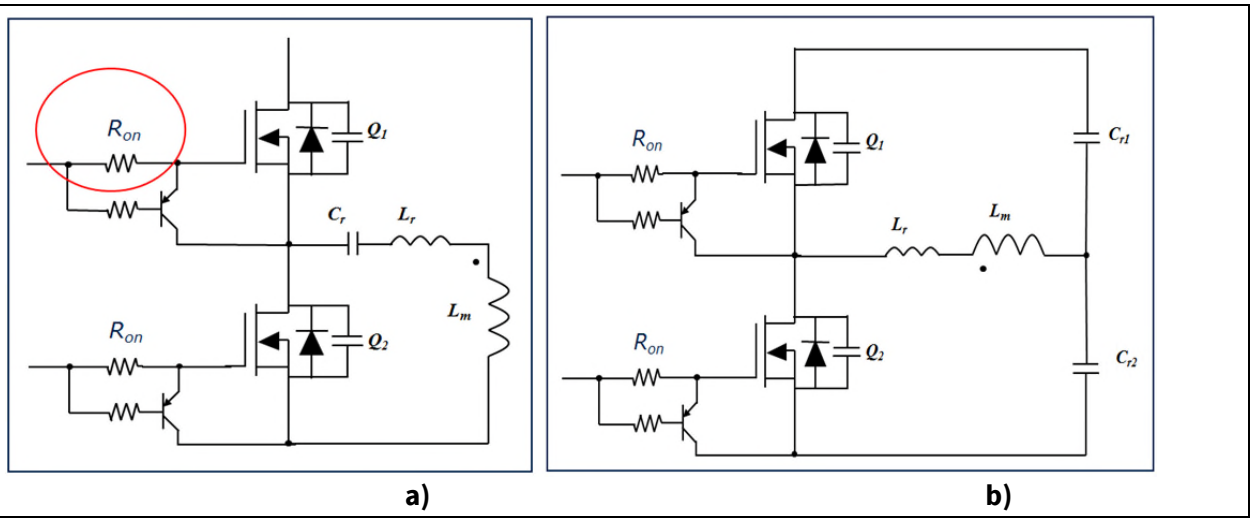

Figure 12 Solutions to eliminate the high voltage peak caused by incomplete body diode reverse recovery during startup of the LLC resonant converter
(a) Increase turn-on driving resistance $R_{g,on}$ of high side power MOSFET
(b) Separated resonant capacitor

Wherein, increasing the turn-on driving resistance $R_{g,on}$ of the high side power MOSFET effectively limits the reverse recovery current slew rate of the low side power MOSFET, thus reducing the possible peak voltage. In Figure 12(b) direct coupling of the discrete resonant capacitor to the output of the PFC eliminates the need to be charged through the high side power MOSFET. In addition, voltage across the resonant capacitor can be charged at the same time as the PFC output voltage. The unbalanced slew rate of the primary side charging current no longer occurs. System reliability is thus improved when the body diode can completely turn-on and reverse recovery.

The other common example occurs in using the PWM mode controller. Because the high side and low side MOSFET turn-on time was inconsistent or one end may have a MOSFET turn-on signal while the other end did not, the MOSFET turn-on and turn-off current values become inconsistent during the first few turn-on cycles during start-up. This leads certain MOSFET body diodes to become unable to turn-off and causes the overcurrent phenomenon.

Figure 13 shows the MOSFET overcurrent phenomenon that occurred because the low side MOSFET gate signal did not appear.

The recommended solutions for the above described phenomenon are to (a) reduce the resonant capacitor C_r value when possible; (b) use a symmetric drive waveform controller; and (c) to resolve asymmetric high side and low side drive signal waveform phenomenon, to use a MOSFET with fast body diode because its low reverse recovery charge as well as recovery time. This can reduce the large current caused by the high reverse recovery charge and the MOSFET burning incidence.

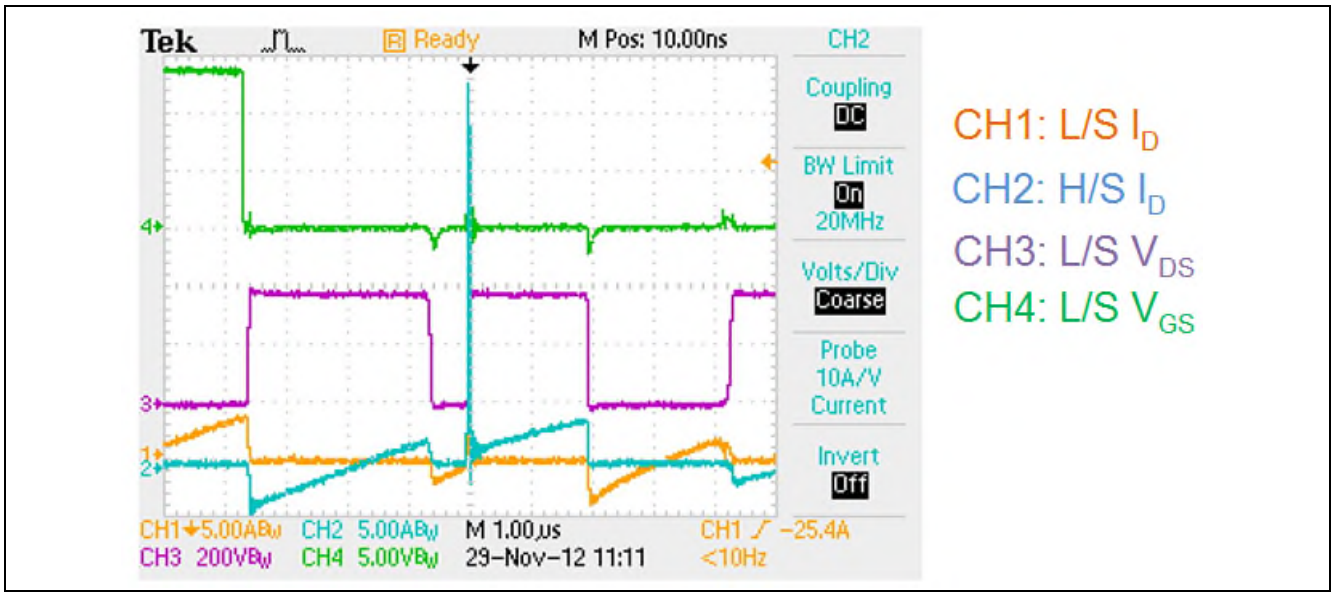

Figure 13 MOSFET overcurrent caused by half-bridge asymmetric drive signal

4 MOSFET Selection Criteria for LLC Topology

According to the above description, two key factors are most important to consider for selecting the MOSFET for LLC topology: ZVS of MOSFET and body diode reverse recovery

4.1 Q_g and C_{oss} of MOSFET

A rule-of-thumb for selecting suitable MOSFETs based on ZVS point of view is to select a MOSFET with lower $C_{O(tr)}$ in the same $R_{DS(on)}$ device which determines the charging/discharging time during the dead-time in LLC topology. The lower the $C_{O(tr)}$ value, the shorter the discharging time of the MOSFETs. However, $C_{O(tr)}$ is just a simple index to compare the charging/discharging time of MOSFETs. The most important factor to determine the discharging time is the C_{OSS} at V_{DS}<50V. Refer to Figure 3(b), it shows the equivalent C_{OSS} of MOSFET versus V_{DS} of MOSFET. It is obvious that the equivalent C_{OSS} value of MOSFET as V_{DS}<50V or V_{DS}>350V is much higher than C_{OSS} at V_{DS}=100V~300V.

From the viewpoint of MOSFET ZVS and efficiency, the selection criteria MOSFETs for LLC topology are:

(a) Lower Q_g for faster switching transient time and lower switching off losses.

(b) Lower $C_{O(tr)}$ and lower C_{OSS} as V_{DS}<50V can reduce the need of magnetizing current, less dead time and further body diode conduction time.

From an efficiency point of view, with some LLC controllers or digital ICs that guarantee the body diode of MOSFETs can be reverse recovery completely, CoolMOS™ CP and CoolMOS™ P6 series are best choices for LLC topology with the lowest Q_g , $C_{o(tr)}$ and the lower C_{OSS} value @V_{DS}<50V.

4.2 Body diode reverse recovery

The body diode reverse recovery issue in LLC topology comes from the charging speed of the resonant capacitance C_r during startup. In fact, with higher resonant capacitance and higher initial startup switching frequency, it is more difficult to make the body diode reverse recovery completely. In several applications, like higher power range power supply, LED lighting and charger, the higher voltage gain of resonant tank within operation frequency is necessary. In other words, the higher resonant capacitance (more than 330nF) is selected in LLC topology to increase the voltage gain.

The recommended solution to resolve the body diode hard commutation issue is demonstrated in the previous section. The di/dt of reverse recovery current of low side body diode and the V_{DS} of low side MOSFET can be suppressed by the high side MOSFET with higher turn-on gate resistor. However, under extremely high reverse recovery current, the turn-on gate resistance may be increased to a higher value, maybe more than 100Ω which would be a trade-off of efficiency in the meantime.

On the other hand, the discrete resonant capacitance is a good solution to resolve this issue, however, under a high power density requirement it is not easy to use the separated resonant capacitance due to the space constraint. It is recommended to select the CoolMOS™ CFD series with the extremely low reverse recovery charge to resolve this issue thoroughly.

5 Conclusion

This application note has presented the conditions for ZVS in a half-bridge LLC resonant converter, a real-world application to observe waveform, discharge time of the power MOSFET and output capacitance as a factor of variable V_{DS}. From viewpoint of efficiency, with some controllers which guarantee the body diode of MOSFET can be reverse recovery completely, CoolMOS™ CP, CoolMOS™ P6 series with the lowest Q_g and $C_{o(tr)}$ are the best selections for LLC topology. Furthermore, the reverse recovery condition for the body diode is decided by the product of the max turn-on current and turn-on resistance $R_{DS(on)}$ of the power MOSFET. In the half-bridge LLC resonant conversion, the incomplete body diode reverse recovery of the power MOSFET is highly likely to result in excessive peak voltages and damage during the initial ON-OFF cycles at startup. A high side power MOSFET with higher driving resistance $R_{g,on,}$ such as higher than 68 ohm and discrete resonant capacitor can effectively resolve the issue of system reliability in half-bridge LLC resonant converters. CoolMOS™ CFD series can overcome this issue in most of the conditions due to the extremely low reverse recovery charge.

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Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office. Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.