600 V CoolMOS™ P7

Infineon's most well-balanced high voltage MOSFET technology

Author: Alois Steiner

About this document

Feedback

Scope and purpose

This document describes Infineon's latest high voltage (HV) superjunction (SJ) MOSFET technology, the new 600 V CoolMOS™ P7. The electrical characteristic of 600 V CoolMOS™ P7 provides all the benefits of a fast switching SJ MOSFET combined with low conduction losses while keeping the oscillation tendency low, giving ease-of-use. To avoid failures during assembly 600 V CoolMOS™ P7 offers an ESD robustness greater than 2 kV (HBM) for all products. This feature enables design engineers to easily design power converters with high efficiency, high power density, high levels of robustness and cool thermal behavior. 600 V CoolMOS™ P7 is a price/performance competitive solution, replacing 600 V CoolMOS™ P6 and is universally applicable, including being suitable for hard and soft switching topologies such as power factor correction (PFC) and LLC.

The intention of this application note is to describe technical benefits of 600 V CoolMOS™ P7 compared to 600 V CoolMOS™ P6 and competitor devices based on characterization data and application measurements.

Finally, a simple design-in guideline will be summarized for a smooth design-in of 600 V CoolMOS™ P7 for a standard hard switching SMPS topology and a standard soft switching LLC SMPS topology.

Intended audience

This document is intended for design engineers who want to improve their HV power conversion applications.

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1 Introduction

This application note describes the characteristics of 600 V CoolMOS™ P7, the newest HV SJ MOSFET technology from Infineon, which features major advances in achievable application efficiency in combination with "ease-of-use" (ease-of-use or easy to design-in requirements include high robustness in ESD, extremely low oscillation tendency, excellent robustness of the body diode against destruction in hard commutation), representing an attractive cost/performance solution for different applications.

1.1 Target applications

As already mentioned, 600 V CoolMOS™ P7 is universal applicable, and suitable for hard and soft switching topologies such as PFC and LLC. For cost reasons, this feature is a significant advantage, especially in the cost sensitive market segments where 600 V CoolMOS™ P7 will be positioned.

Table 1 Target applications

Application	PFC	PWM
Server	Boost stage	LLC
Telecom	Boost stage	LLC
PC power	Boost stage	TTF
		LLC
TV	Boost stage	LLC

1.2 Features and benefits

The 600 V CoolMOS™ P7 is the next step in MOSFET silicon improvement based on the 600 V CoolMOS™ C7. As C7 continues the strategy to increase the switching performance in order to enable highest efficiency in all target applications including PFC and HV DC-DC stages such as LLC (a DC-DC stage with a resonant tank in order to maintain ZVS), the P7 will balance the fast switching behavior combined with "ease-of-use" requirements to enable a fast and easy design-in, even in plug and play situations.

This plug and play situation is more common in consumer markets such as the TV market and PC power market. In a standard TV board there is plenty of space available on the PCB; to save costs a combo IC is widely used to control the PFC stage and the LLC stage. By placing this combo IC between the two stages there is a compromise regarding distances to the MOSFET. As a result the parasitic inductances and capacitances of the PCB layout are enlarged thereby approaching the critical level to force the oscillations (for example, at the gate of the MOSFET).

In order to maintain control of the application designers must select a device that is not overly affected by oscillation. If used in an LLC stage, the MOSFET must be able to handle a hard commutation on the body diode without any damage. Based on this example, it is obvious that the "ease-of-use" requirement is important. On the other hand, in the TV market power density is more and more in focus and therefore a higher efficiency is a requirement to implement a smaller cooling area or to move to surface-mount devices (SMD).

In exactly this way, optimization was realized with a 600 V CoolMOS™ P7, achieving "ease-of-use" in combination with very high efficiency and the possibility to offer SMD devices in the lowest $R_{DS(on)}$ ranges.

Table 2 Features and benefits

Product features	Customer benefits
Optimized integrated R_g P7 is designed for low oscillation sensitivity and low losses	Easy for customer to balance ease of use against efficiency by controlling switching behavior using external components
Integrated ESD diode where applicable P7 offers ESD robustness greater than 2 kV (HBM) for all products	Ensures high quality in customer's manufacturing environment
Rugged body diode P7 offers good hard commutation ruggedness	Same part suitable in both hard switching and soft switching topologies within the PSU (i.e., PFC and LLC circuits)
Wide $R_{DS(ON)}$ portfolio including both through hole and SMD packages available	Suitable for many different applications both consumer and industrial
Balanced features for performance/ease-of-use/price	Suitable for many different applications both consumer and industrial

1.3 SJ principle

For conventional HV MOSFETs (Figure 1), the voltage blocking capability in the drain drift region is developed through the combination of a thick epitaxial region and light doping. This results in about 95 percent of the device resistance being in the drain region, which cannot be improved by the approaches used for LV transistors (trench cells with smaller cell pitch); where only about 30 percent of the transistor resistance is in the drain drift region.

The intrinsic resistance of a conventional epitaxial drift region of optimum doping profile for a given blocking voltage class is shown in Figure 2 as the "silicon limit line," which, in the past, has been a barrier to improved performance in HV MOSFETs. Chen and Hu theoretically derived this limit line in the late 1980s [1]. This aspect of MOSFET design and physics limited achievable performance until the introduction of CoolMOS™ by Siemens (now Infineon), the first commercially available SJ MOSFETs [2], [3].

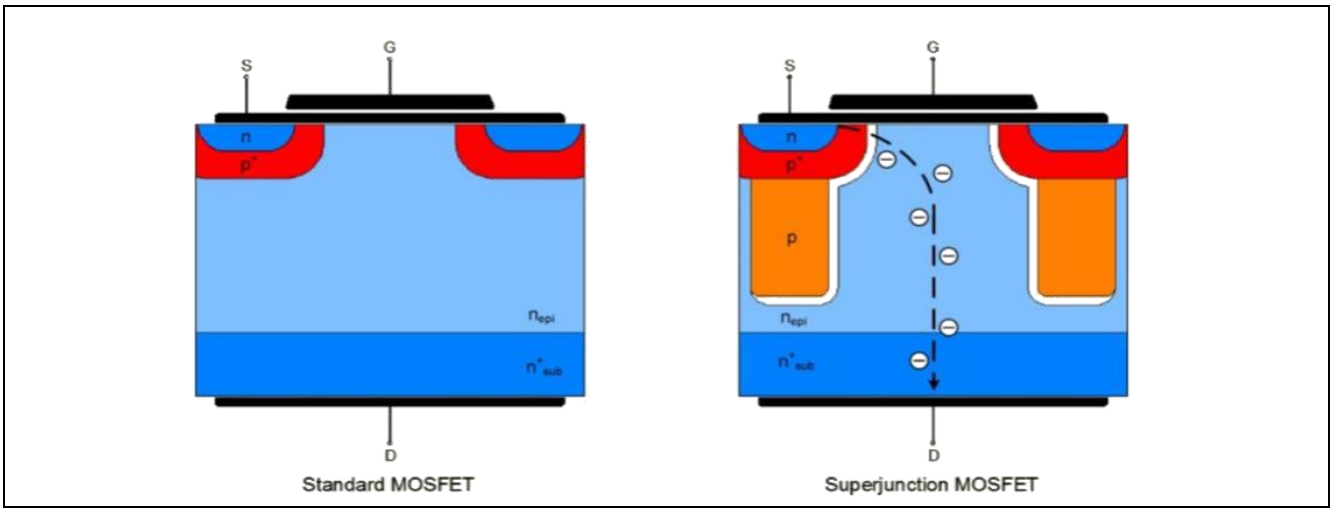


Figure 1 Schematic drawing of conventional HV planar MOSFET and SJ MOSFET

In 1999, CoolMOS™ first employed a novel drain structure employing the SJ concept (Figure 1). There are two key principles employed in this transistor design. First, the main current path is much more heavily doped than for a conventional HV MOSFET. This lowers the on-state resistance. But without the p-columns forming a charge compensation structure below the cell structure, the transistor would have a much lower blocking voltage capability due to the highly doped n-region. The precisely sized and doped p-columns constitute a "compensation structure", which balances the heavily doped current path and supports a space charge region with zero net charge supporting high blocking voltage.

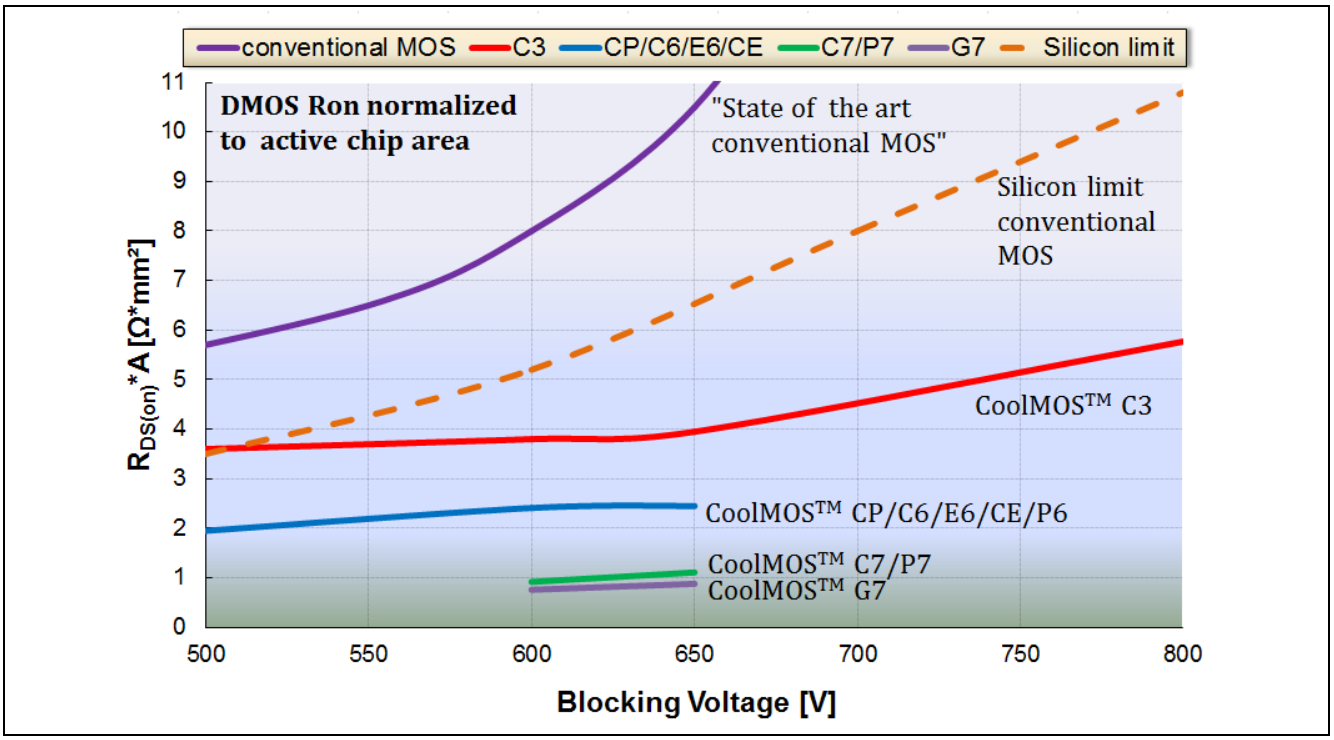


Figure 2 Silicon limit line of area specific $R_{DS(on)}$ over blocking voltage capabilities of conventional MOS versus CoolMOS™ generations

This construction enables a reduction in area specific resistance that has obvious conduction loss benefits - the attendant remarkable reduction in chip area for the first generation of CoolMOS™ technology lowered capacitance and dynamic losses as well. The SJ technology made it possible to "beat" the silicon limit line (Figure 2) and, with a new finer pitch generation in CoolMOS™ P7, to further improve all aspects of losses [4],[5].

This MOSFET technology approach has now been further extended with the development of 600 V CoolMOS™ P7, which reduces the typical area specific $R_{DS(on)}$ down below the 1 Ω*mm² level. Together with several cell geometry considerations, this reduces all device capacitances, thus improving the switching related figures of merit (FOM) and application performance characteristics substantially as described in the next chapters. [5]

Figure 3 shows the schematic cell cross-section and compensation structure comparison between P6 (left) and P7 (right). This configuration poses significant manufacturing challenges and drew upon process technology experience from a number of areas at Infineon in developing a new approach for this generation of CoolMOS™ but brings considerable technological benefits that are described below.

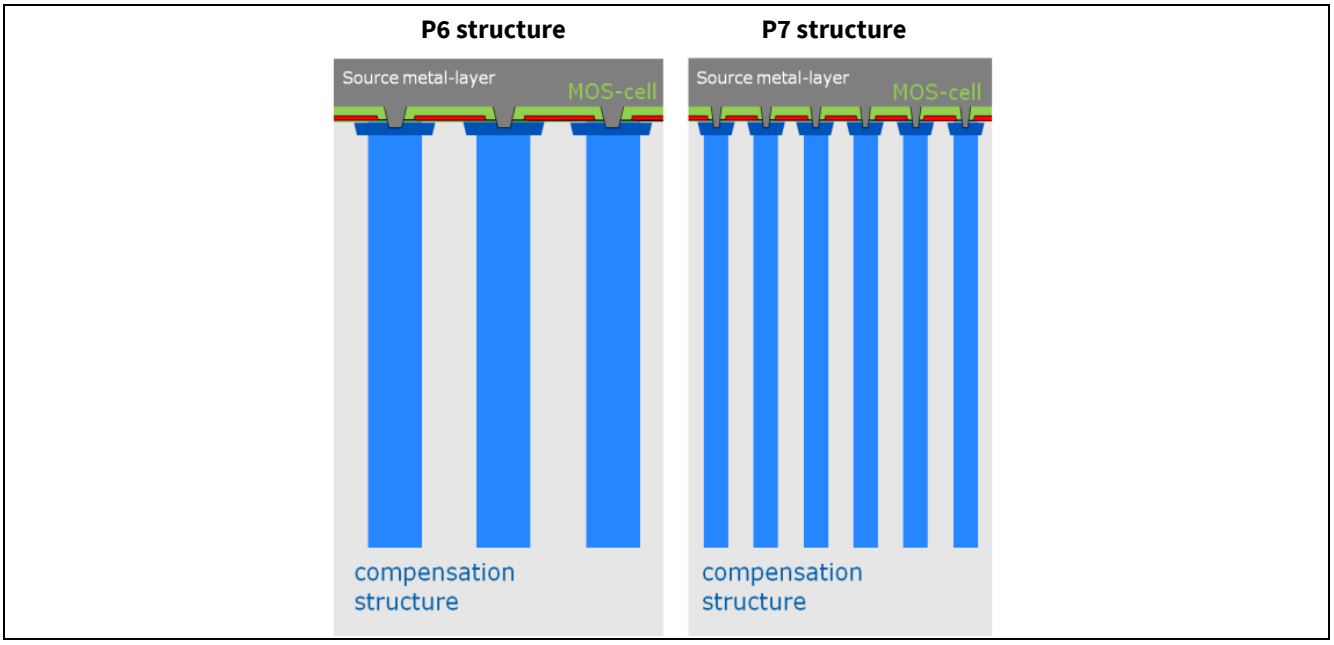


Figure 3 Schematic comparison of 600 V CoolMOS™ P6 and P7 cross section concepts showing the high aspect ratio compensation structure for performance increase

2 Technology parameter comparison of 600 V CoolMOS™ P6, P7 and competition

2.1 Technology description

To make an optimum MOSFET selection for the application and apply it successfully, it is necessary to first have a clear understanding of the technology differences to its predecessors. The most obvious advantage of 600 V CoolMOS™ P7 is the substantially improved area specific $R_{DS(on)}$ (Table 3), the 600 V P7 active chip area is reduced compared to previous generations to achieve a given $R_{DS(on)}$ class.

The benefits include possible lower $R_{DS(on)}$ ratings in the new package, for example 60 mΩ in TO-220/ TO-220FP or 65 mΩ in ThinPAK 8x8. On the other hand, by offering smaller packages, the parasitic inductances will also be reduced, such as with TO-220 compared to TO-247, which for previous technologies were not possible due to their larger silicon sizes. The reduction of the parasitic inductance in the gate driver loop reduces switching losses. These product features are absolutely necessary to achieve new power density levels.

Table 3 Comparison of CoolMOS™ P6, P7, Competitor 1 and Competitor 2 in the 190 mΩ $R_{DS(on)}$ class

Specification	Unit	Symbol	Comp. 1	Comp. 2	P6 190 mΩ	P7 180 mΩ
Max on-state resistance 25°C	mΩ	$R_{DS(on)}$	190	190	190	180
I_D current rating at 25°C	A	$I_{D, cont}$	15.8	18	17.5	18
I_D pulse rating	A	$I_{D, pulse}$	63.2	72	57	53
Typical gate to source, gate to drain, gate charge total	nC	Q_{GS} Q_{GD} Q_G	9 16 38	6 12 29	11 13 37	6 8 25
Typical C_{iss} at 400 V	pF	C_{iss}	1350	1060	1750	1081
Typical C_{oss} at 400 V	pF	C_{oss}	35	55	76	19
E_{oss} energy stored in the output capacitance	µJ	E_{oss}	4.5	4.7	4.9	2.7
Typical effective output capacitance energy related	pF	$C_{o(er)}$	55	258	61	33
MOSFET dv/dt ruggedness	V/ns	dv/dt	50	50	100	80
Reverse diode dv/dt	V/ns	dv/dt	15	15	15	50
Maximum diode commutation speed	A/µs	di_F/dt	-	400	500	900
Reverse recovery charge (typical)	µC	Q_{rr}	2.9	4	4	1.3
Peak reverse recovery current	A	I_{rrm}	23	24	25	15

2.2 Low Q_G, Q_{GD}

One of the most important improvements of CoolMOS™ P7 is in the device gate charge. P7 will offer a 30 percent Q_g reduction in comparison to P6 over the whole $R_{DS(on)}$ range which mainly comes from the reduction of the gate drain charge Q_{GD} in the much shorter length of the Miller plateau. The Q_g reduction enables better efficiency, especially in light load conditions due to reduced driving losses ($P_{driv}=2xQ_gxU_gxf_{sw}$) and enables a very fast switching perfomance for turn-on and turn-off. Furthermore, low Q_g allows reducing the driver circuit current capability for the driver. Figure 4 shows Q_g in nC for P7 against P6, competitor 1 and competitor 2 at 180 mΩ.

The key message of the graph below: P7 offers 30 percent lower driving losses compared to P6

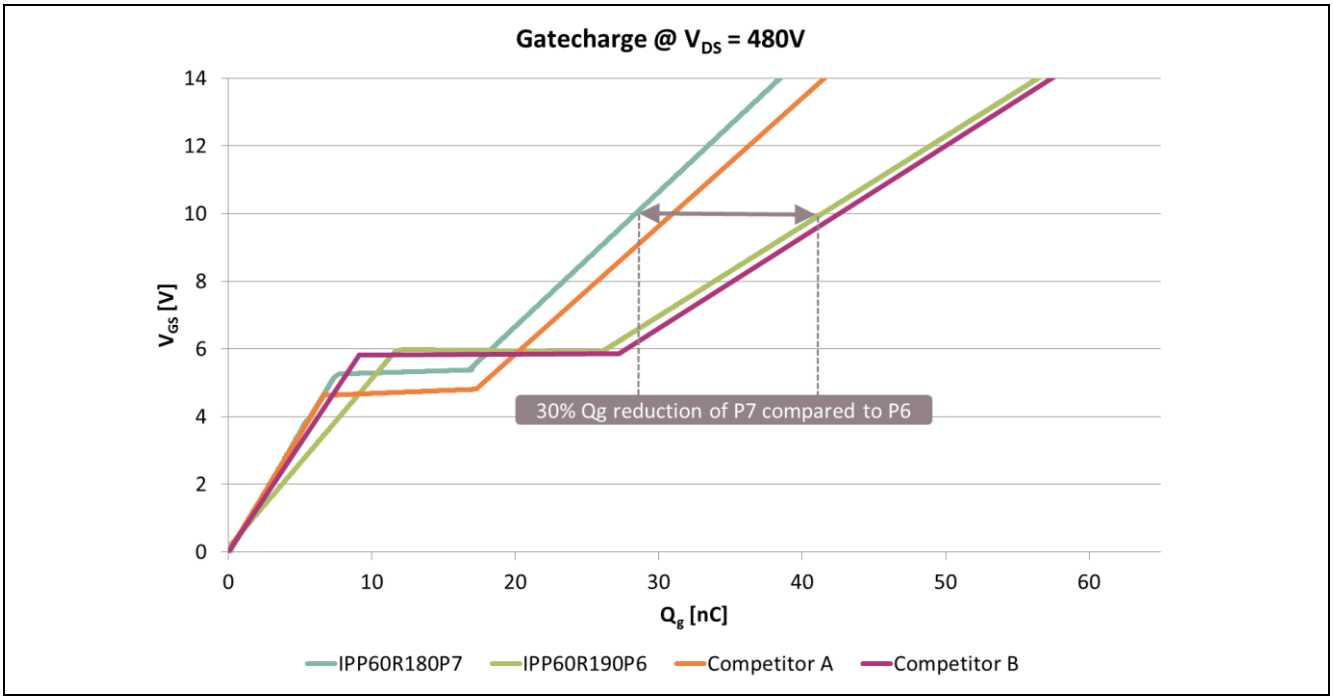


Figure 4 Gate charge comparision of CoolMOS™ P7, P6 and competitors

Q_{GD} is a significant parameter related to switching transition times and losses. Figure 5 shows simplified switching waveforms; the voltage transition takes place during the Miller plateau region, or Q_{GD}.

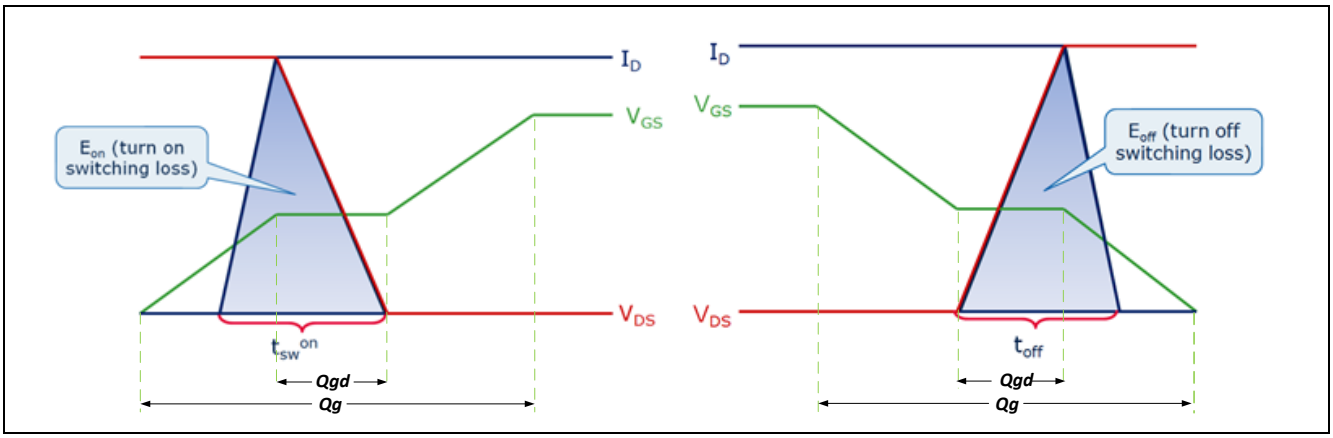


Figure 5 Simplified turn-on and turn-off waveforms

Above is the "classic" format for calculating turn-off time and loss. The actual turn-off losses with fast switching can be up to 50 percent lower than calculated, due to the high Q_{oss} of SJ MOSFETs, and because the C_{oss} acts like a nonlinear capacitive snubber. The current flow through the drain during turn-off under these conditions is non dissipative capacitive current, and with a fast drive, the channel may be completely turned-off by the onset of drain voltage rise. The nonlinear shape of the C_{oss} capacitance varies from one CoolMOS™ family to another. Consequently the shape and the snubbing of the voltage transition, which in turn affects switching losses, as explained in the following subsection. [5]

2.3 Tuned C_{oss} curve

SJ output capacitance acts like a nonlinear capacitive snubber. Figure 6 shows the C_{oss} capacitance curves as function of the drain to source voltage (V_{DS}). In general, SJ has a relatively high capacitance in the LV range (less than 50 V). The figure below compares the C_{oss} for CoolMOS™ P7 and P6. It is clear that P7 has higher C_{oss} values in the LV region, but lower values in the HV region. Both of these attributes affect the time domain voltage transition in terms of snubbing and dv/dt during turn-off.

The key message of the graph below: P7 offers lower switsching losses compared to P6

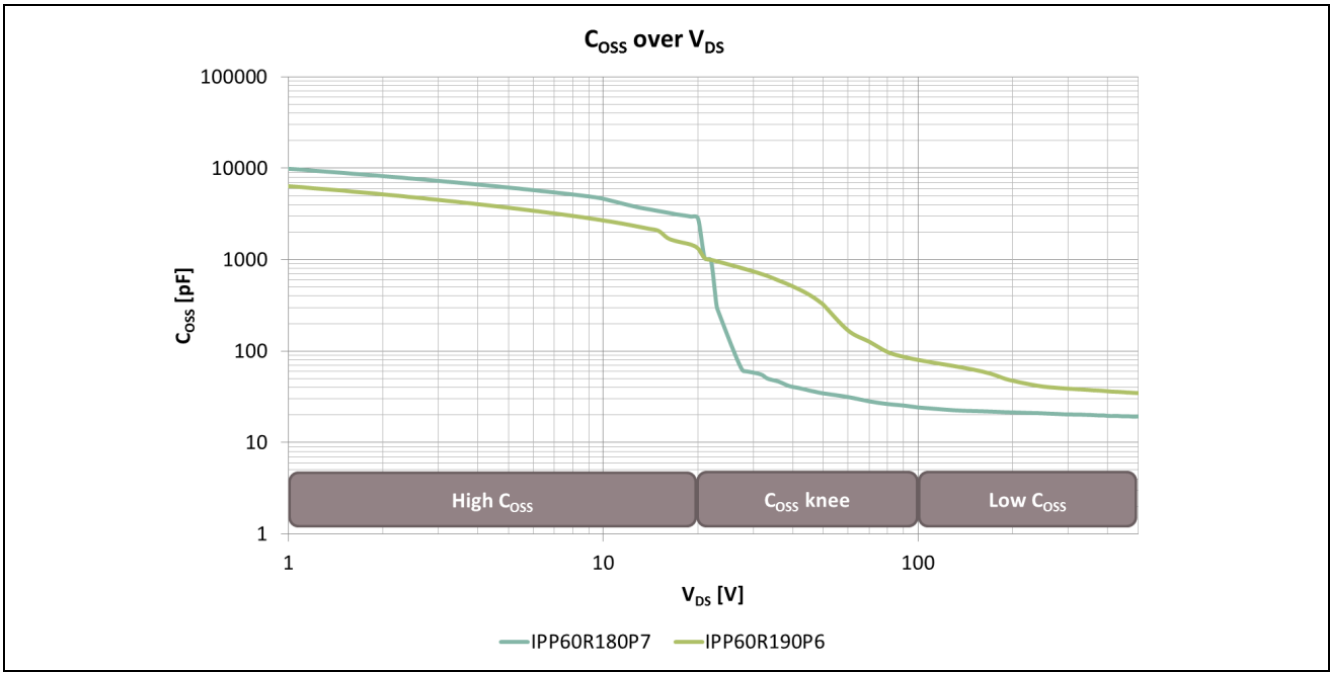


Figure 6 C_{oss} curve comparison for CoolMOS™ P7 and P6

2.4 Smooth fast switching transition (dv/dt)

Figure 7 shows the turn-off switching waveform comparison between 600 V CoolMOS™ P6 and 600 V CoolMOS™ P7 at R_g, ext=1.8 V, I_D=5 A and V_{GS}=13 V. Even for this extremely low external R_g one can see a very similar smooth switching behavior from 600 V CoolMOS™ P7 compared to 600 V CoolMOS™ P6. In these application conditions dV/dt reaches 55 V/ns with a maximum V_{DS} voltage overshoot up to 450 V.

The key message of the graph below: P7 offers simmilar smooth switching behavior and simmilar dv/dt compared to P6.

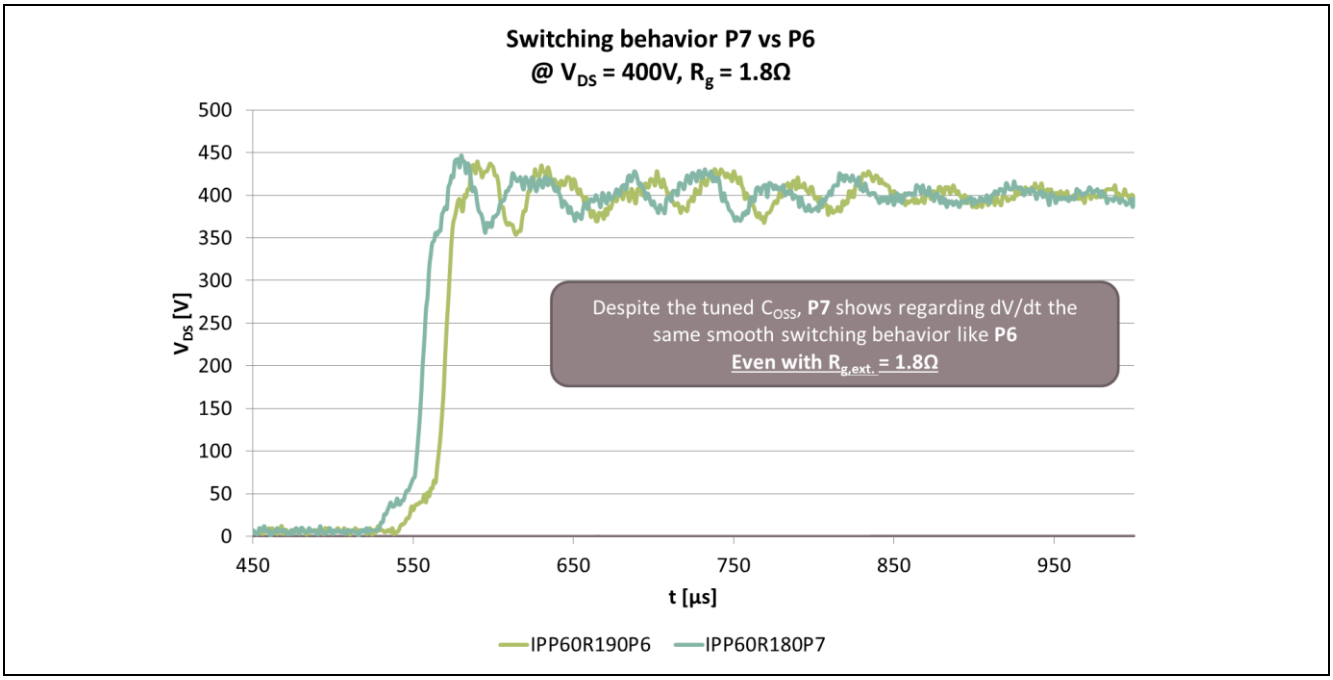


Figure 7 dV/dt comparison of CoolMOS™ P7 and P6

2.5 Low E_{oss}

As already discussed for the output capacitance (C_{OSS}), the capacitance drop for P7 takes place at lower voltage levels when compared to previous generations. This, combined with a remarkable reduction of the C_{OSS} level at high voltages, which dominates the overall value of the energy stored in the output capacitance, brings the E_{OSS} at typical DC link voltages of 400 V down to roughly one half of the previous generations, as shown in Figure 8.

The key message of the graph below: P7 offers ~50 percent lower E_{oss} losses compared to P6.

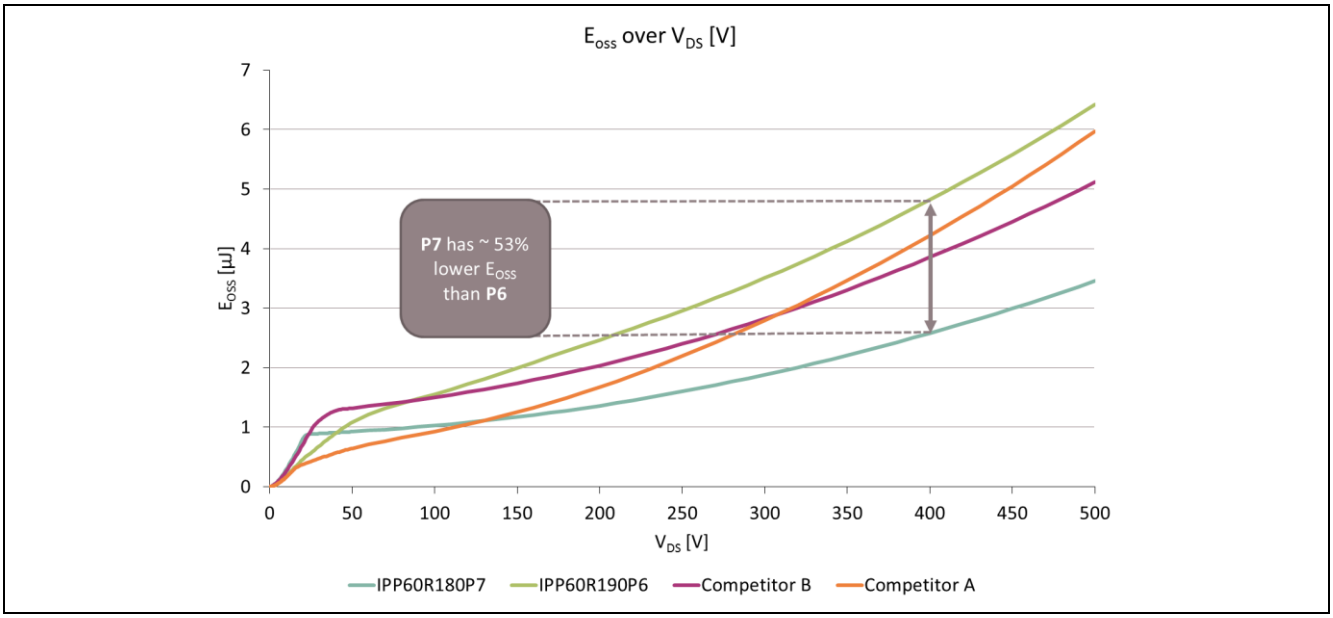


Figure 8 E_{OSS} comparison of CoolMOS™ P7, P6 and competitors

In hard switching applications, this energy is a fixed loss. E_{OSS} is stored in the C_{OSS} during the turn-off phase; then it is dissipated in the MOSFET channel in the next turn-on transient, as shown in simplified format in Figure 9.

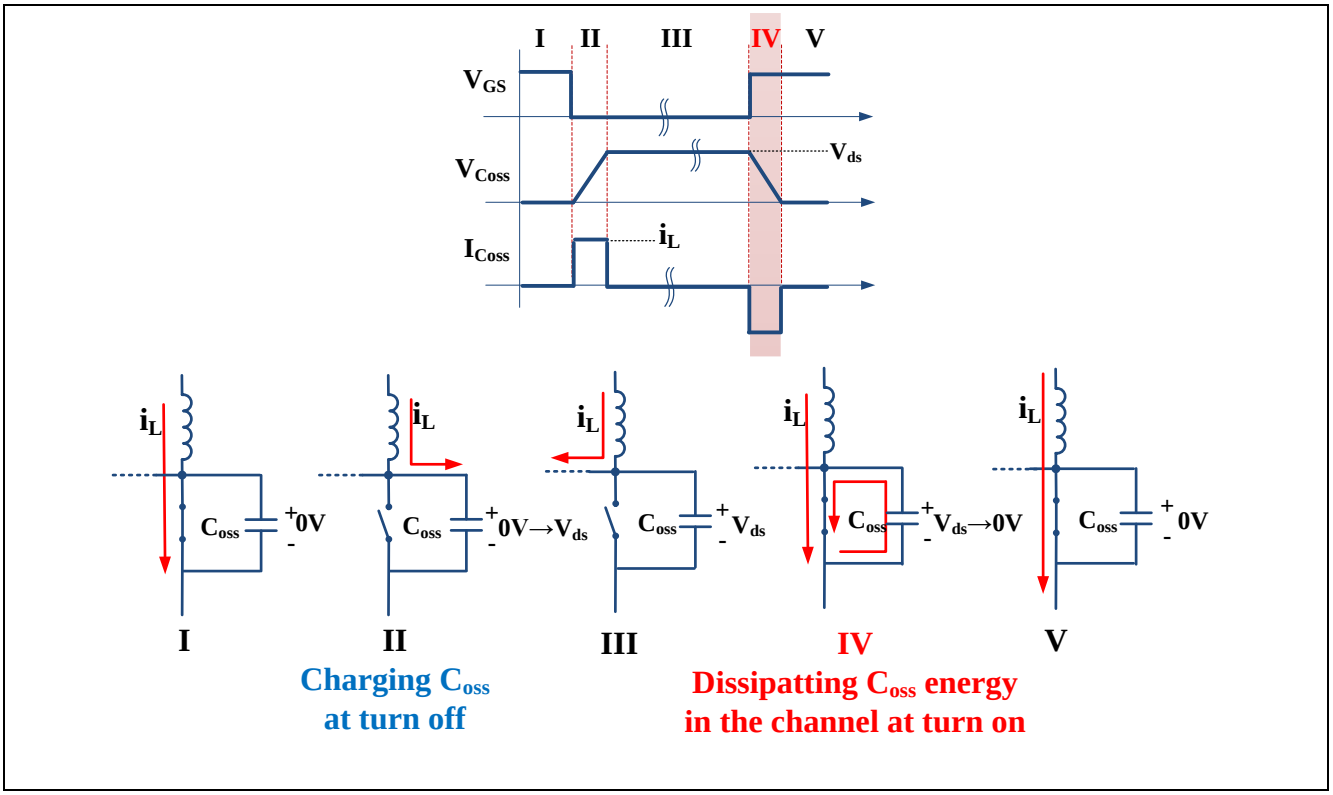


Figure 9 Simplified E_{oss} dissipation mechanism in hard switching

This loss can be significant at light load condition because most of the other losses are load dependent and decrease considerably at light load, thus, the E_{oss} reduction contributes to an improvement of the light load efficiency. Figure 10 illustrates the contribution of E_{oss} loss to the total MOSFET losses in a CCM PFC boost application, showing that E_{oss} loss is two thirds of the total losses at 20 percent load condition.

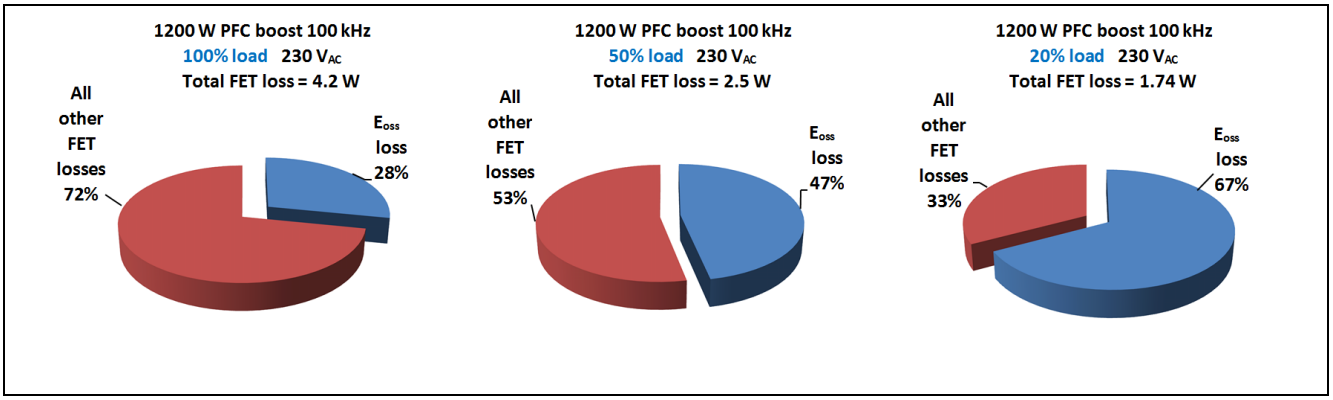


Figure 10 E_{oss} contribution to total FET losses in PFC boost at different load conditions

In soft switching applications, with zero voltage turn-on, this energy is recycled back to the circuit (before the turn-on) rather than dissipated, as simplified in Figure 11.

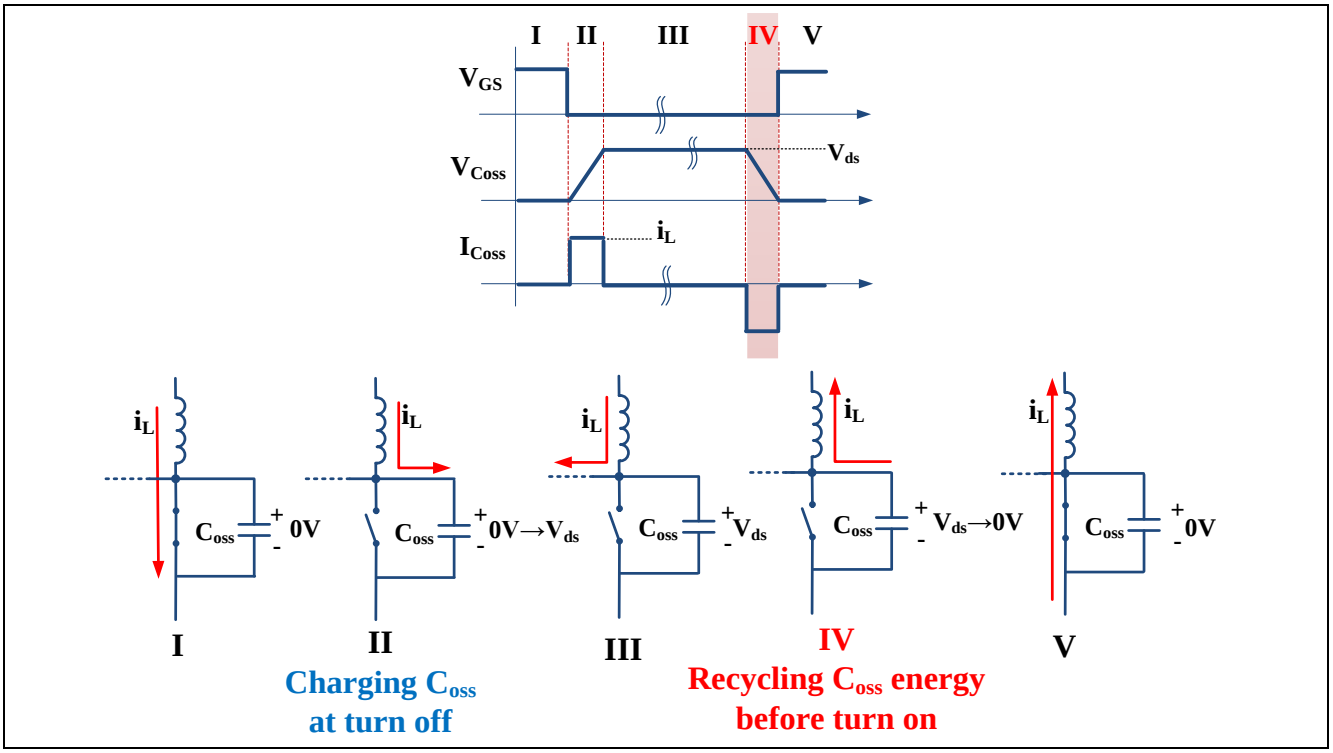


Figure 11 Simplified E_{oss} recycling mechanism in soft switching

Although E_{oss} is assumed to be recycled in ZVS applications, it is still desirable to have lower E_{oss}. In topologies such as resonant LLC or phase-shift full-bridge, the designer must ensure proper sizing of the primary inductance and its stored energy that is required to complete recycling of E_{oss} and reach complete ZVS.

ZVS may be lost partially or completely if the inductive energy available in the circuit is not sufficient to charge and discharge the output capacitance of the two MOSFETs in the same bridge leg.

The energy condition for achieving ZVS is given by:

$$Inductive\ Energy \geq Capacitive\ Energy$$

$$0.5 \cdot L_{eq} \cdot {I_L}^2 \geq 0.5 \cdot (2 \cdot C_{o(er)}) \cdot {V_{in}}^2$$

$$0.5 \cdot L_{eq} \cdot {I_L}^2 \geq 2 \cdot E_{oss}$$

Where $C_{o(er)}$ is the MOSFET's equivalent energy related output capacitance as shown in the datasheet. Figure 12 shows an example from the IPP60R180P7 datasheet to show the $C_{o(er)}$ parameter and its definition, which is used for energy calculation purposes. [5]

Effective output capacitance, energy related[1)]	$C_{o(er)}$	-	33	-	pF	V_{GS}=0V, V_{DS}=0...400V

[1)] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

Figure 12 Datasheet snapshot of the $C_{o(er)}$ capacitance and its definition

Therefore, the tuned C_{oss} curve for 600 V CoolMOS™ P7 results in lower $C_{o(er)}$ and E_{oss}, makes it easier for the designer to optimize efficiency without sacrificing ZVS. For example, in a resonant LLC, the magnetizing inductance can be increased to reduce the poor circulating primary side current. In phase-shifted full-bridge, the ZVS will extend to a lighter load point, otherwise the external primary side inductor used to increase the inductive energy might not be required.

2.6 Tuned Q_{oss}

Due to the non-linear capacitance of SJ MOSFETs, the stored charge in the output capacitance is mostly concentrated in the low voltage region. Nearly 90 percent of the Q_{oss} charge will be generated between 0 V and 20 V, 10 percent from 20 V up to 400 V.

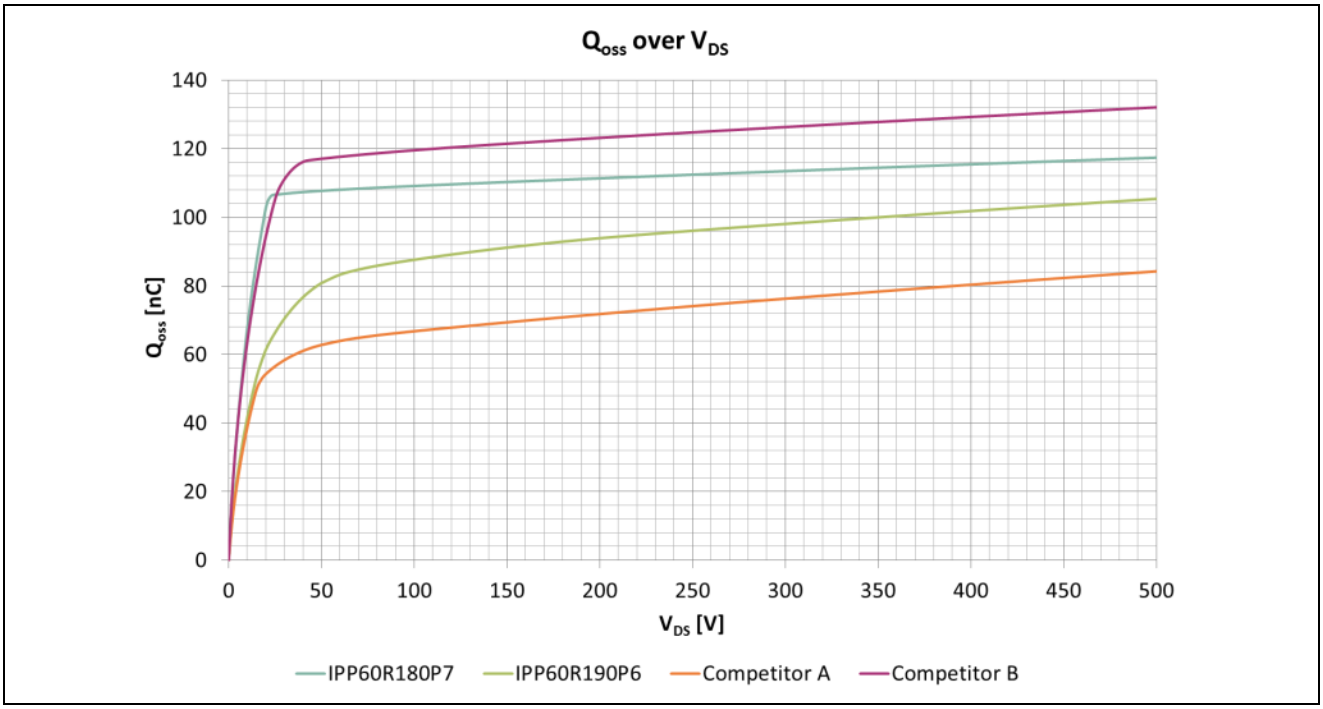


Figure 13 Q_{oss} comparison of CoolMOS™ P7, P6 and competitors

The reduction in Q_{oss} is also advantageous in ZVS applications; apart from having sufficient energy to achieve ZVS as discussed in the section above, the dead time between the two MOSFETs in the switching leg must also be long enough to allow the voltage transition.

The time condition for achieving ZVS is given by:

$$Deadtime \geq ZVS\ transition\ time$$

$$Deadtime \geq 2 * C_{o(tr)} * \frac{V_{DS}}{I}$$

$$Deadtime \geq 2 * \frac{Q_{OSS}}{I}$$

Where I is the current used to charge and discharge both FETs in the switching leg.

V_{DS} is the FET voltage, typically 400 V.

$C_{o(tr)}$ is the MOSFET's equivalent time related output capacitance as shown in the datasheet. Figure 14 shows an example from the IPP60R180P7 datasheet of the $C_{o(tr)}$ parameter and its definition, which is used for time calculation purposes.

Effective output capacitance, time related[2)]	$C_{o(tr)}$	-	314	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
$C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V						

Figure 14 Datasheet snapshot of the $C_{o(tr)}$ capacitance and its definition

Therefore, the Q_{OSS} and $C_{o(tr)}$ reductions facilitate completing the ZVS transition within the dead time period.

2.7 Low turn-on and turn-off losses

Figure 15 and Figure 16 show the result of E_{on} and E_{off} characterization measurements for P6 and P7. We can assume that a typical application condition for a PFC will be a 10 Ω external R_g and 5 A maximum drain current. P7 offers approximately 20 percent lower turn-off losses and approximately 15 percent lower turn-off losses when compared to P6. This improvement in P7 is based on reduced C_{rss} and the reduced total Q_g.

Due to the improved turn off losses, P6 is a good fit for discontinuous conduction mode PFC and soft switching topologies such as LLC where the turn-off losses are dominant.

The key message of the graph below: P7 offers ~20 percent lower E_{off} losses compared to P6.

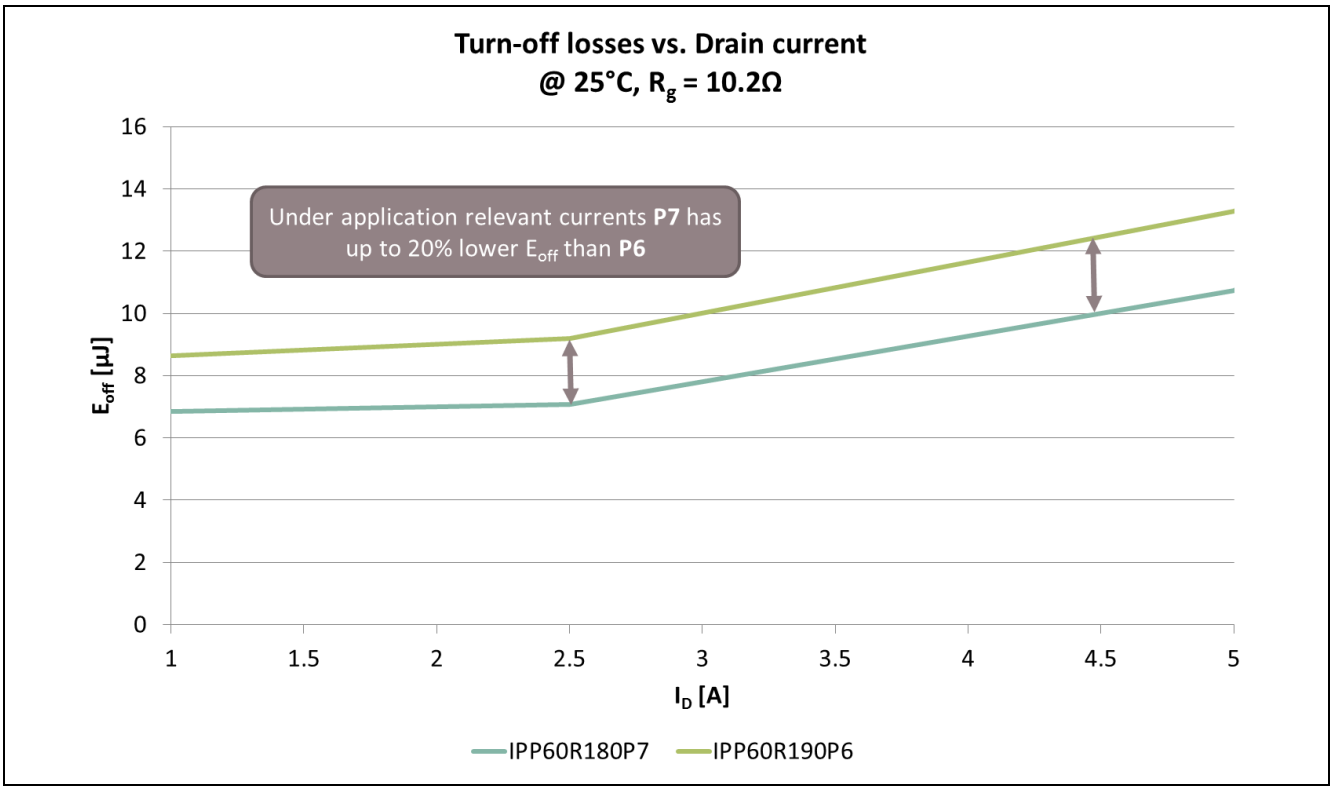


Figure 15 Turn-off comparison of CoolMOS™ P7 and P6

The key message of the graph below: P7 offers ~15 percent lower E_{on} losses compared to P6.

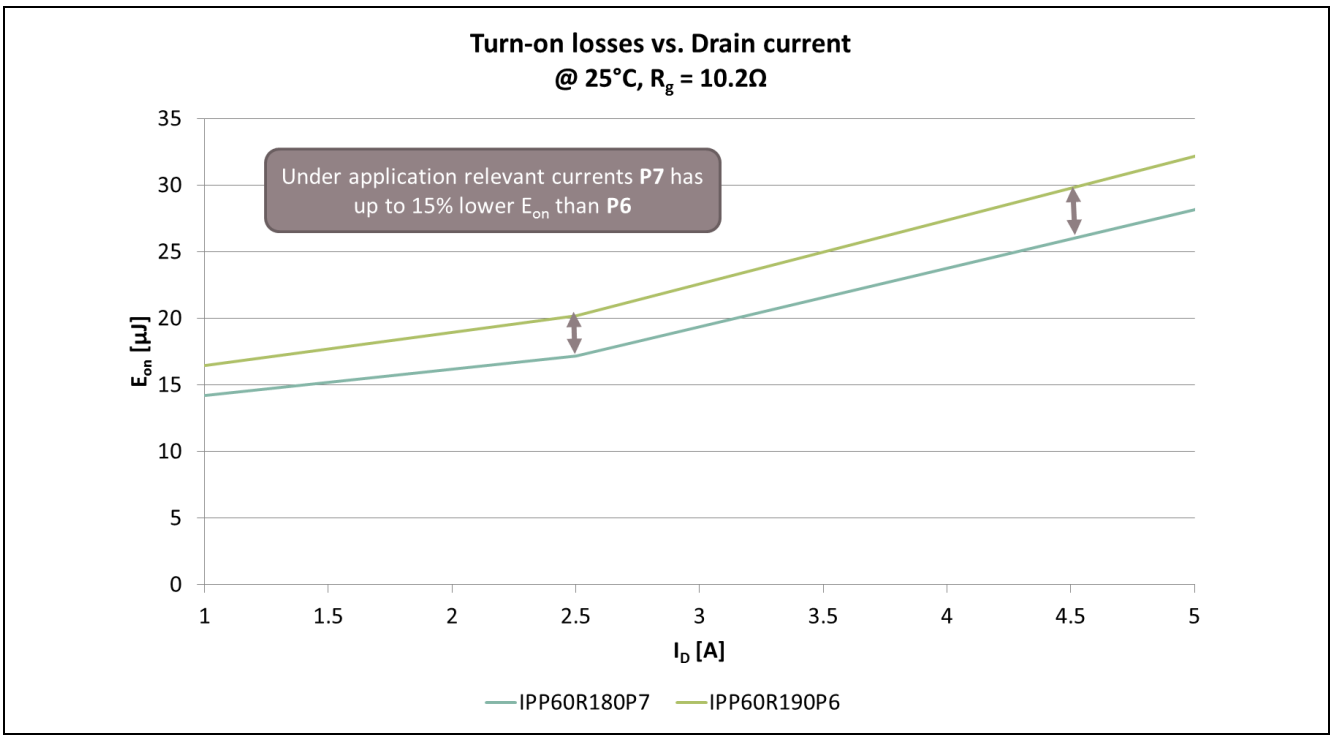


Figure 16 Turn-on comparison of CoolMOS™ P7 and P6

2.8 Integrated gate resistor

600 V CoolMOS™ P7 includes an integrated gate resistor, $R_{g,int}$, in order to achieve self-limiting di/dt and dv/dt characteristics. Figure 17 shows different values of integrated R_g against $R_{DS(on)}$ defined according to the different application conditions and the trade-off between efficiency and ease-of-use requirements.

$R_{DS(on)}$ classes from 37 mΩ up to 180 mΩ are mostly used in CCM PFC, whereas low external R_g's (e.g 5…20 Ω) will be selected according to the efficiency requirements. Values of $R_{DS(on)}$ higher than 180 mΩ will be widely used in DCM PFC where the EMI requirement is more dominant than the efficiency.

To enable low EMI, high external R_g's will be used (e.g 20…100 Ω). The integrated R_g allows fast turn-on and turn-off at normal operating current conditions but limits di/dt and dv/dt in the case of abnormal conditions. For device values from 37 mΩ up to 180 mΩ, the integrated R_g scales inversely with the gate charge and device capacitances. Devices higher than 180 mΩ have a minimum integrated R_g to enable safe smooth switching even in worst case conditions.

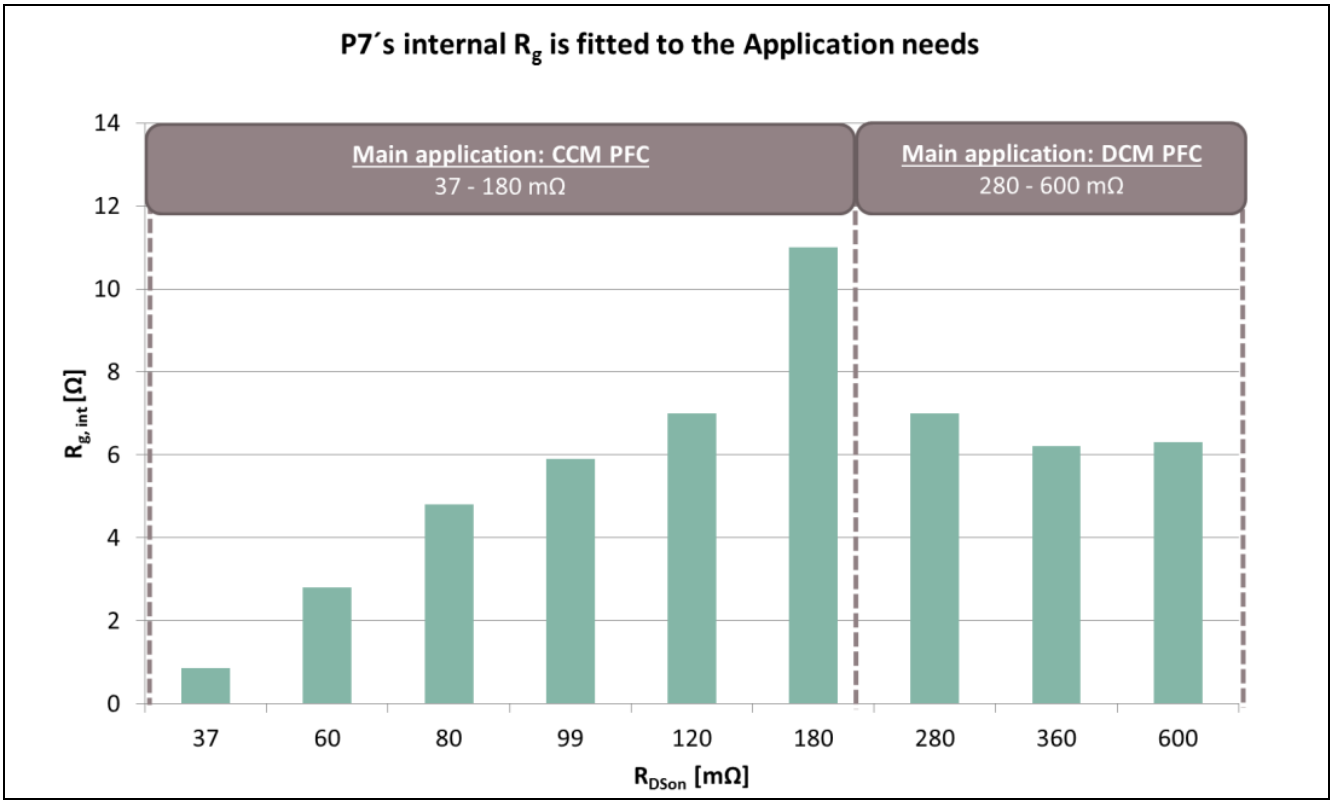


Figure 17 Integrated $R_{g,int}$ comparison of CoolMOS™ P7 in CCM and DCM PFC

2.9 ESD protection

As already mentioned in the introduction, in some application segments such as TV, the robustness of the MOSFET is a very crucial point. To make the design-in and the manufacturing process easier and more reliable for customers, the 600 V CoolMOS™ P7 is designed to enable a very high ESD robustness. This robustness is a function of the chipsize.

The preferred values of $R_{DS(on)}$ in the TV segment start from 190 mΩ up to 600 mΩ. With high values of $R_{DS(on)}$ and the smaller chip size, ESD levels are typically around 500 V. To overcome this, we implement an internal bipolar Zener diode between the gate and source for devices with $R_{DS(on)}$ values higher than 100 mΩ. With this, all 600 V CoolMOS™ P7 products will be able to survive an ESD level higher than 2 kV according to the HBM, thereby enabling up to two levels better ESD clasification levels compared to older CoolMOS™ generations.

2.10 Rugged body diode

One of the greatest achievementsents during the 600 V CoolMOS™ P7 developments was the improvement of the body diode ruggedness against destruction in hard commutation.

2.10.1 When is a rugged body diode needed?

In soft switching applications, such as resonant LLC and ZVS full-bridge converters, some circuit operations may include hard commutation on the MOSFET's body diode. In general, when a reverse current flows in the body diode, some charge (Q_{rr}) is stored in the FET's parasitic diode structure. If the external voltage then changes direction, a high dv/dt voltage is applied to the diode before this charge is completely removed; the residual charge will dissipate very quickly causing a high di/dt current, hence causing a high voltage overshoot.

Hard diode commutation can occur due to several circuit operations, including:

- Capacitive mode operation, Figure 18 shows the MOSFET operation in both inductive and capacitive modes. In the latter, the current is leading the voltage, and reverses its direction before the half period has ended. The negative current flows in the body diode; when the next half period is initiated by the turn on of the other MOSFET in the switching bridge. This exposes the diode to high dv/dt, and a high reverse recovery current spike is seen, as shown in Figure 18.

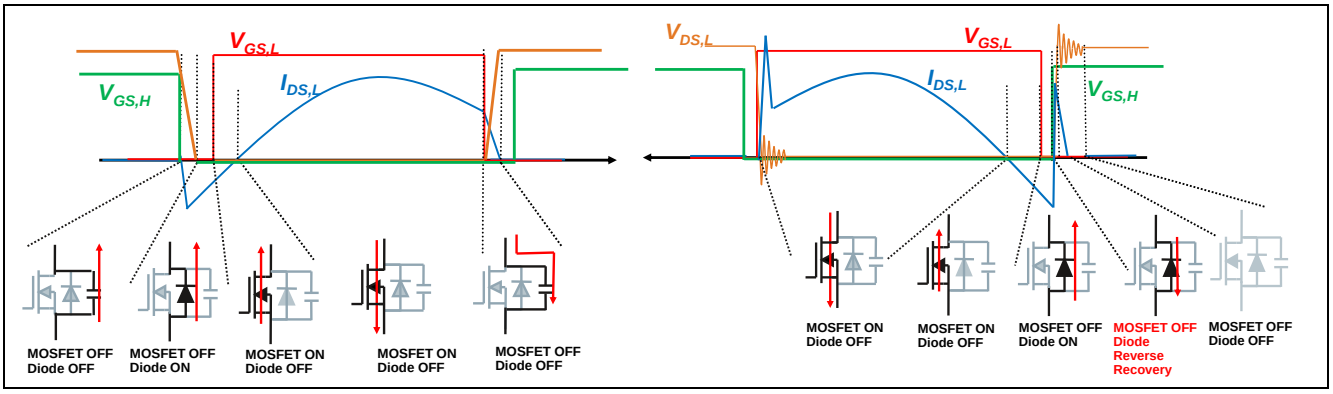


Figure 18 MOSFET operation in LLC circuit: Inductive mode (left), capacitive mode (right)

- At light load or no load operation, hard commuttion can occur in both LLC and ZVS full-bridges. When the diode conducts and stores Q_{rr} charge during the dead time, the following period of the on-time should generate a voltage drop across the diode. At light load this voltage drop can be insufficient to recover all of the Q_{rr} stored in the p-n region, hence the residual Q_{rr} charge will cause hard commutation of the body diode once the other bridge MOSFET is turned on, as can be seen in Figure 19.

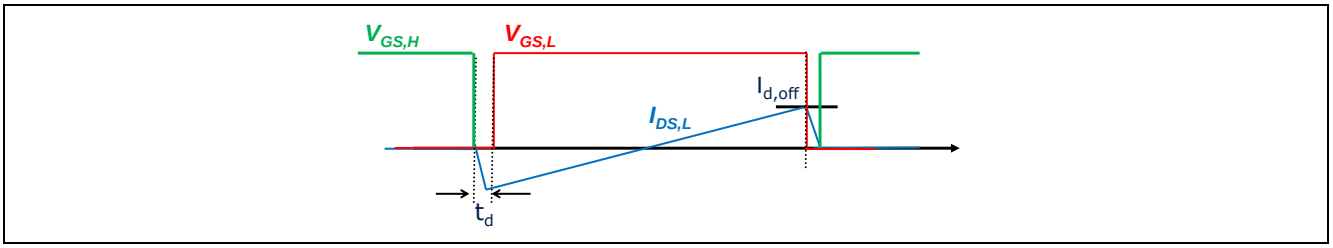


Figure 19 MOSFET operation in light load

- Also at short circuit, load transient and start-up, hard commutation can happen depending upon the reaction speed of the control circuit. Although the steady-state regulation curves were designed to avoid the capacitive mode, these are transition modes that could force the operation to pass through several cycles of capacitive mode and hard commutation, until the controller and resonant tank settle to the steady state again. Figure 20 is an illustration of the operational transition during a short circuit, until detected and protected by the controller. [5]

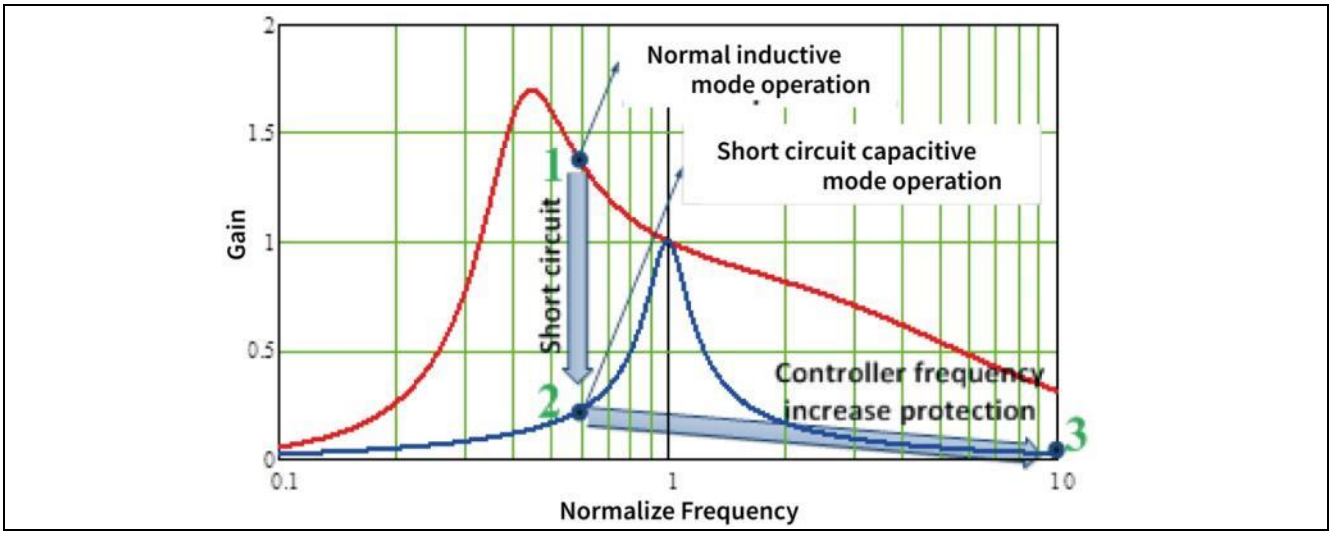


Figure 20 Short circuit operation in LLC an circuit

2.10.2 How to test the body diode ruggedness?

To test the body diode, we need a flexible and simple setup that allows for testing the device in different application conditions by using variations of $R_{g,ext}$ or variations of forward currents. These requirements are able to be realized in the double pulse test setup that is described in Figure 21.

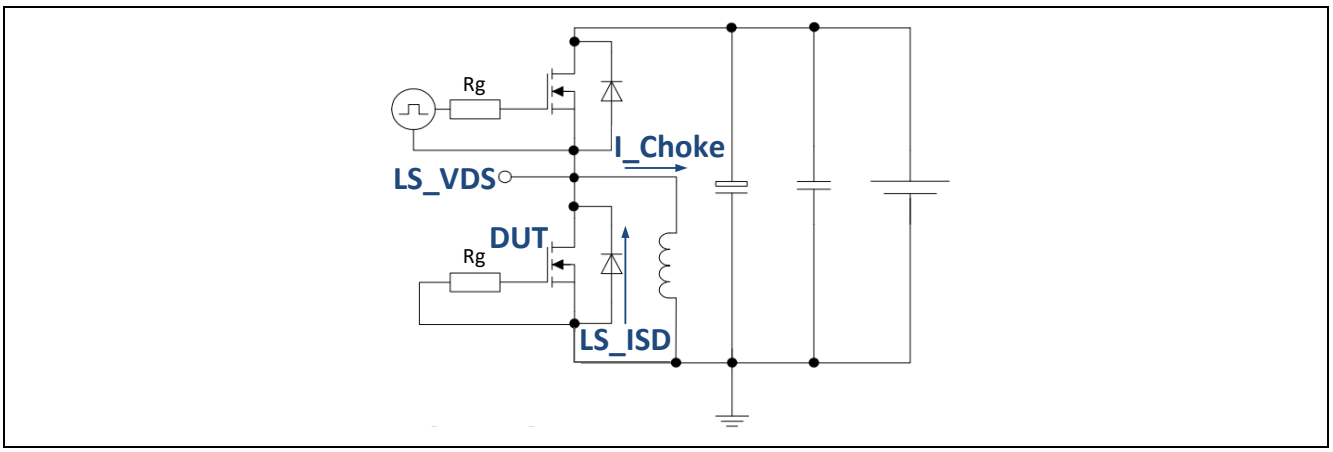


Figure 21 Double pulse circuit for testing the diode characteristics

Following sequence is approached:

DUT is the low side MOSFET body diode (Q2)

Phase 1: By applying the double pulse driving signal to the high side MOSFET (Q1), Q1 is turned-on and the inductor current increases linearly through Q1 to a final value determined by the pulse width and the inductor value.

Phase 2: After Q1 has been turned-off, the freewheeling phase starts when the energy stored in L discharges the output capacitance of Q2. When it is completely discharged, the body diode of Q2 starts conducting.

Phase 3: After a short freewheeling time, Q1 turns-on again and the body diode of Q2 starts hard commutating the current. V_{DS} (Q2) starts rising again and a negative reverse recovery current spike is seen in the diode current waveform (LS_ISD) and so we have hard commutation on the body diode.

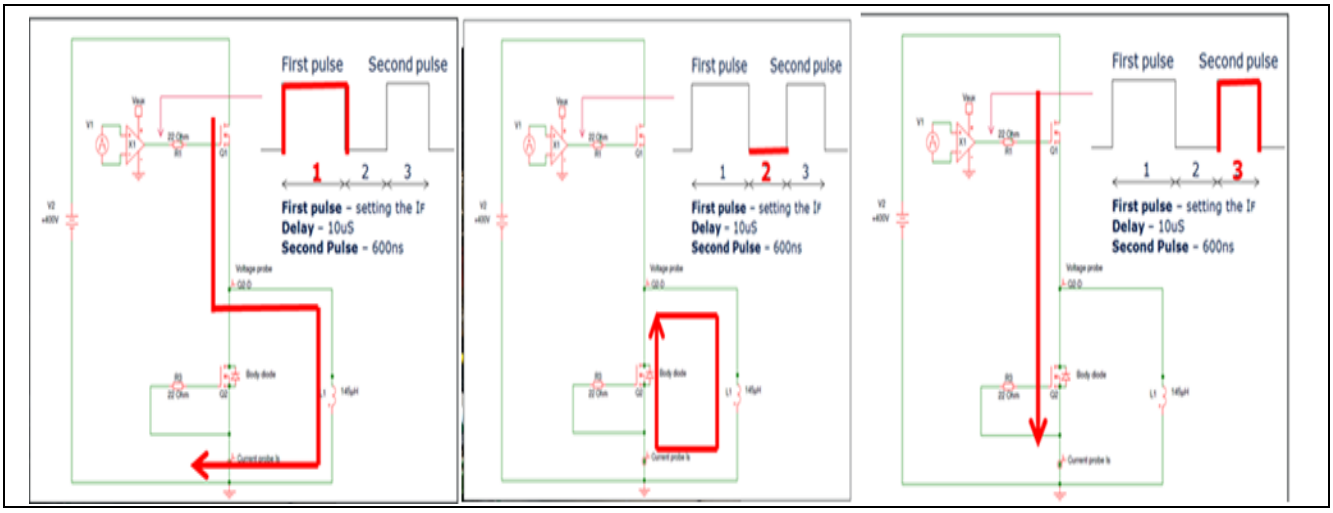


Figure 22 Double pulse test sequence

From this test we get the following waveforms, shown in Figure 23.

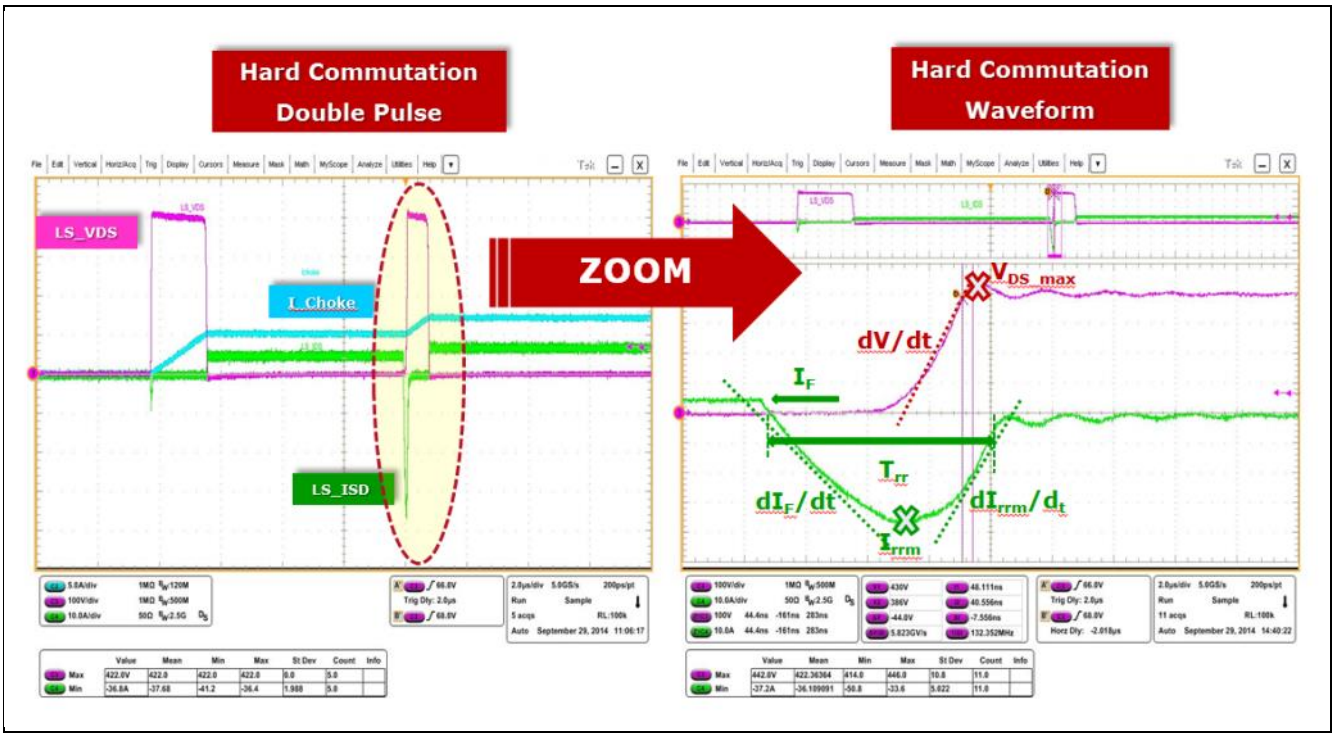


Figure 23 Diode hard diode commutation waveform in a double pulse test circuit

2.10.3 600 V CoolMOS™ P7 outstanding body diode ruggedness

According to the test procedure described in chapter 2.10.2, it is proven that P7 survives a maximum dv/dt rating of 50 V/ns and di/dt rating of 900 A/µs without any damage. With these values we are able to reach a commutation speed from the body diode at the same level as the widely used fast body diode device CoolMOS™ CFD2.

The key message of the table below: P7 offers new BIC dv/dt and di/dt values for a "non" fast body diode device. 3 times higher dv/dt and nearly 2 times higher di_f/dt compared to P6

Table 4 Comparison of the body diode ruggedness

Body diode	P7_600 V	P6_600 V	Competitor 1_600 V	CFD2_650 V fast body diode device
Reverse diode dv/dt [V/ns]	50	15	15	50
Maximum diode commutation speed di_f/dt[A/µs]	900	500	400	900

It is obvious that hard commutation events are most critical at very low forward currents through the body diode. At lower forward current this forces higher dIr/dt resulting in a higher V_{DS}_overshoot based on V_{DS} = L * dIr/dt.

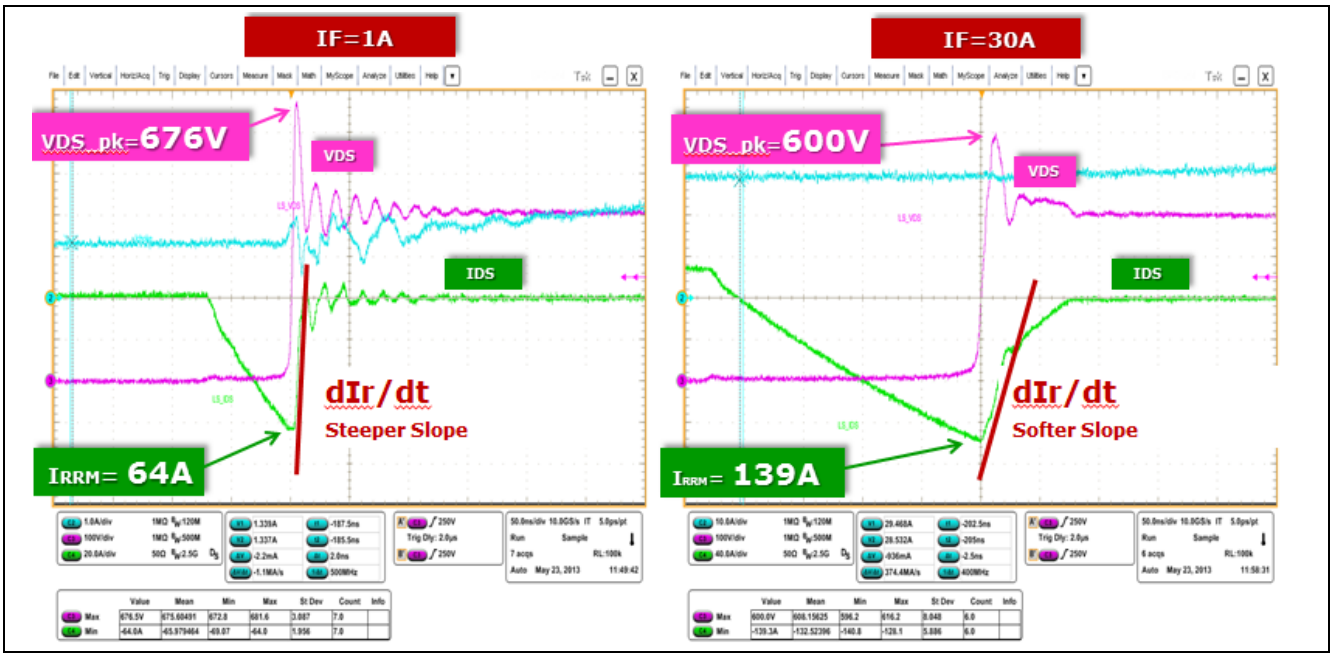


Figure 24 Commutation event of a competitior's SJ device at 1 A current and with 30 A flowing through the body diode at V_{gs}=13 V and $R_{g,ext}$= 5 Ω

Due to the outstanding body diode behavior, 600 V CoolMOS™ P7 remains within the 80 percent derating of the breakdown voltage and shows no damage from the smallest currents up to more than double the device rated current level even with very low values of external R_g.

The following graph shows the extremely smooth voltage overshoot V_{DSMAX} and the reverse recovery current peak from a 600 V CoolMOS™ P7 180 mΩ at extreme conditions where V_{GS}=13 V and $R_{g,ext}$=1.8 Ω.

The key message of the graph below: P7 offers a very smooth switching behavior, enables a very rugged body diode with a reduced voltage overshoot and is able to survive more than 2.5 times higher current than the nominal I_D

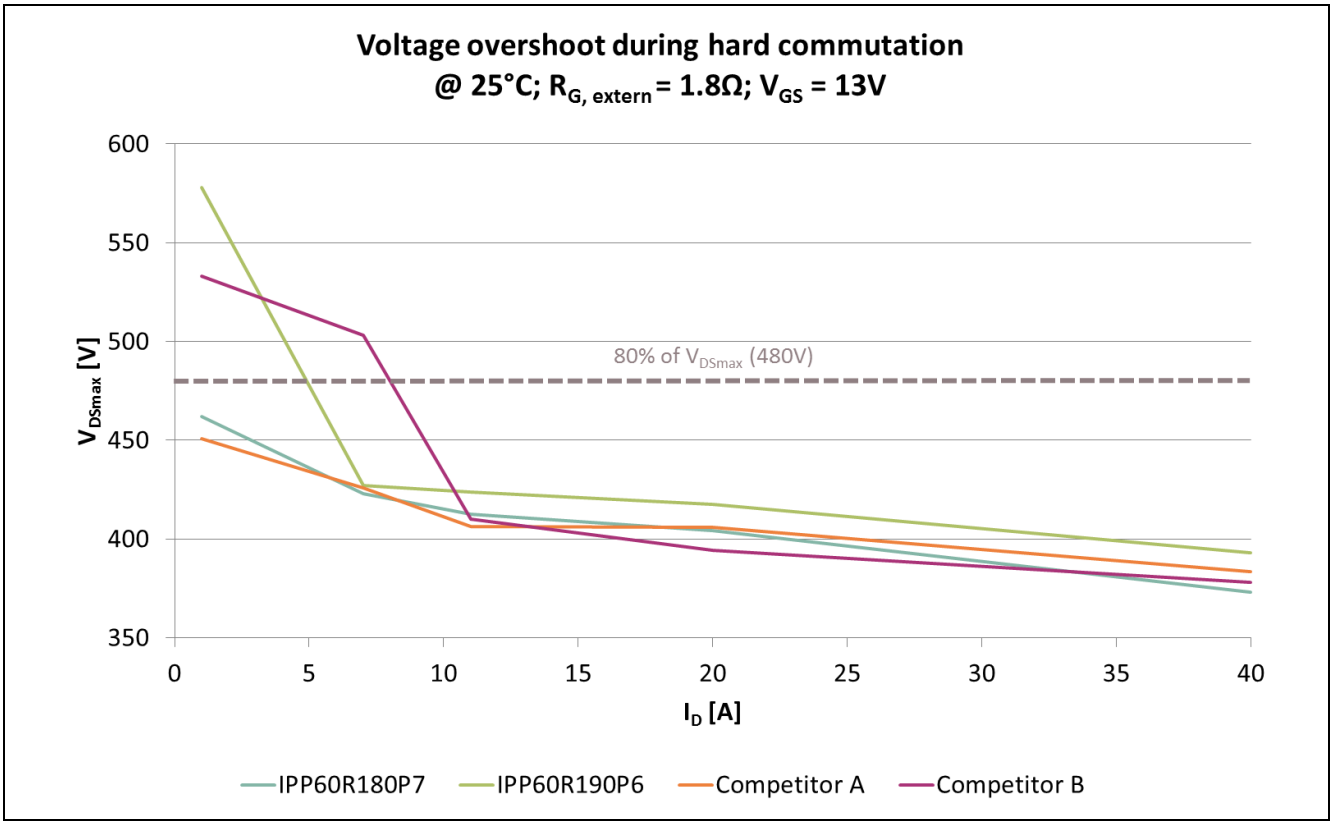


Figure 25 Voltage overshoot during hard commutation of CoolMOS™ P7, P6 and competitors

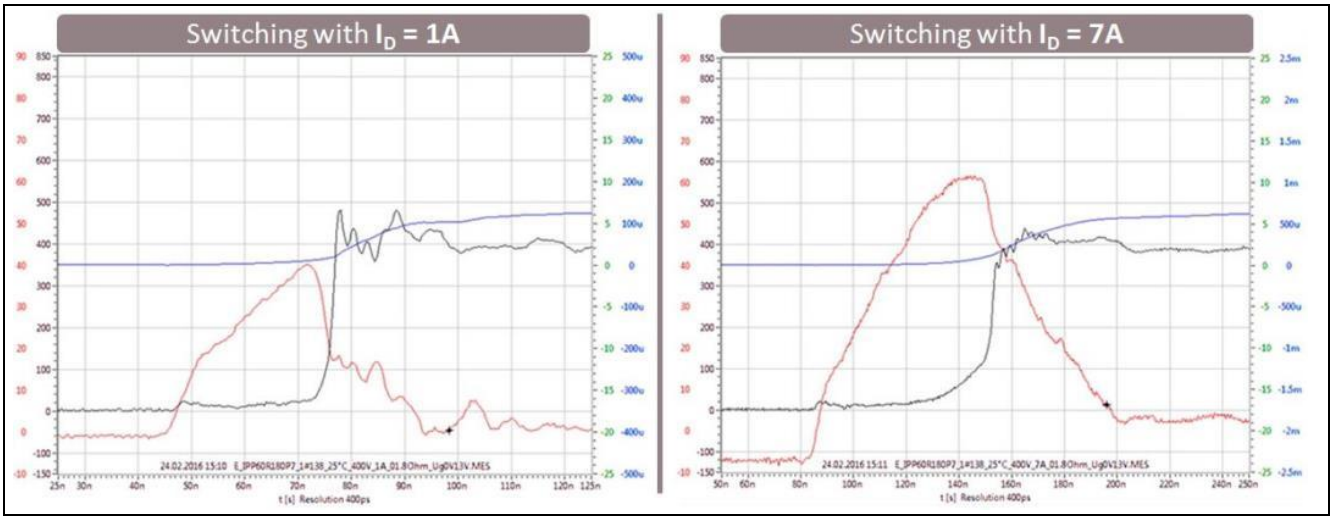


Figure 26 Hard commutation event of a 180 mΩ device at 1 A and 7 A for CoolMOS™ P7

In Figure 26, the hard commutation event of a 180 mΩ, 600 V rated SJ device with 1 A and 7 A current flowing through the body diode can be seen.The current is shown in red and the voltage waveform in dark grey.

It is worth mentioning that the results presented in this section are circuit and layout specific. They will vary for different designs, and are only intended for relative comparison and understanding.

2.11 Move to smaller packages by enabling lower $R_{DS(on)}$

Due to the technology breakthrough, the latest CoolMOS™ 7 family is able to offer the best performance in the CoolMOS™ family, providing a significant reduction of conduction and switching losses.

At the same time, the package limitation is further extended. For the same packages the CoolMOS™ P7 technology offers lower $R_{DS(on)}$. As shown in Figure 27, the lowest $R_{DS(on)}$ of the TO-220 package is 60 mΩ which is 32 percent lower than other technologies. Overall it enables high power density and efficiency for superior power conversion systems.

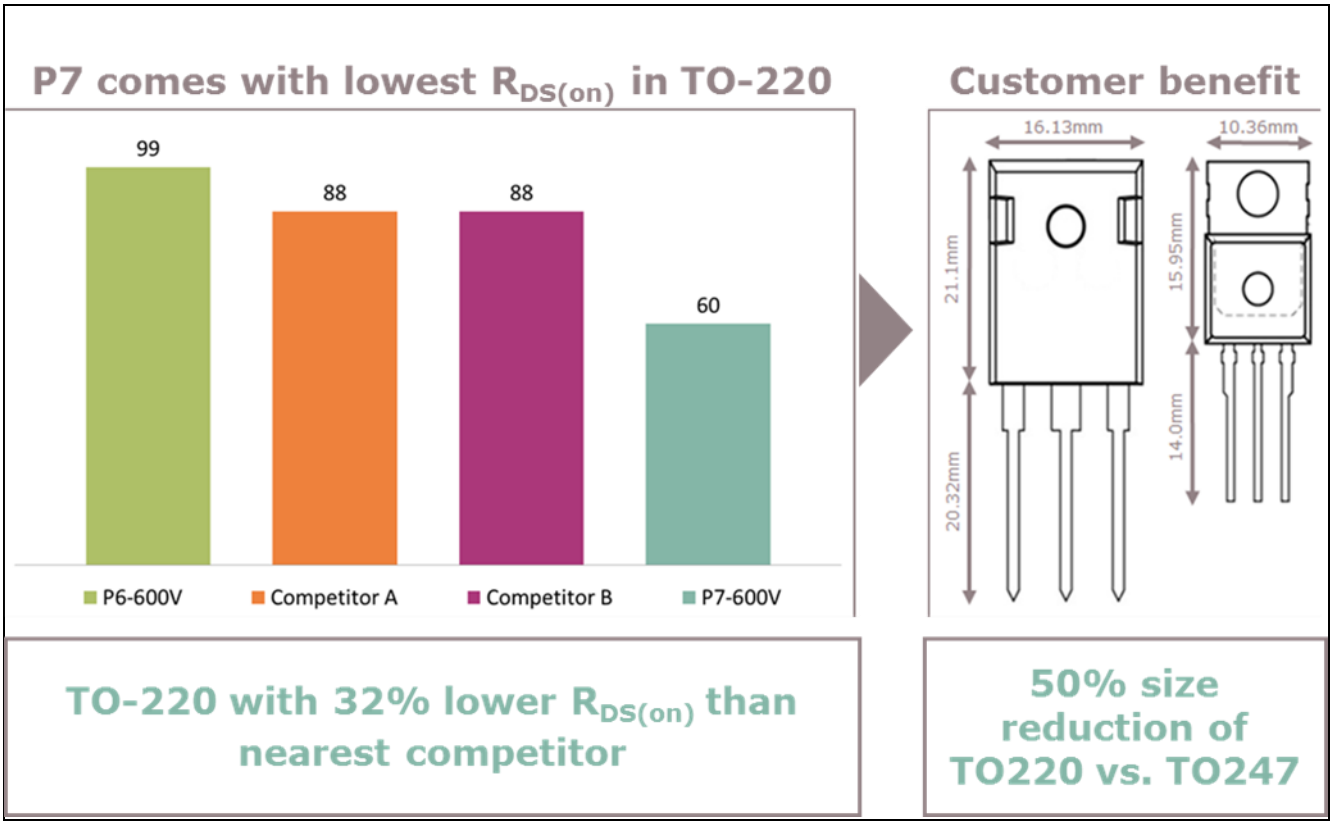


Figure 27 Lowest available $R_{DS(on)}$ comparison of CoolMOS™ P7, P6 and competitors

Normally, the choice of package is determined by its thermal dissipation, which in some cases prevents the adoption of smaller packages with a smaller thermal interface area. But, with the reduction of the total losses, such as in 600 V CoolMOS™ C7, the thermal and mechanical designs are able to use smaller packages and maintain similar temperature performance at the same time. Usually also the purchaising costs are lower for smaller packages.

3 Experimental results

3.1 Efficiency comparison in a 500 W CCM PFC

Referring to the characterization data, it is clear that the 600 V CoolMOS™ P7 has clear and substantial improvements for hard switching topologies including lower E_{oss}, lower switching losses, lower Q_g and lower $R_{DS(on),typ}$.

Figure 28 shows an efficiency difference chart for a 500 W hard switching CCM PFC at 65 kHz with 10 Ω external R_g. P7 offers the best performance over the whole load range with the benefit of at least 0.15 percent better efficiency.

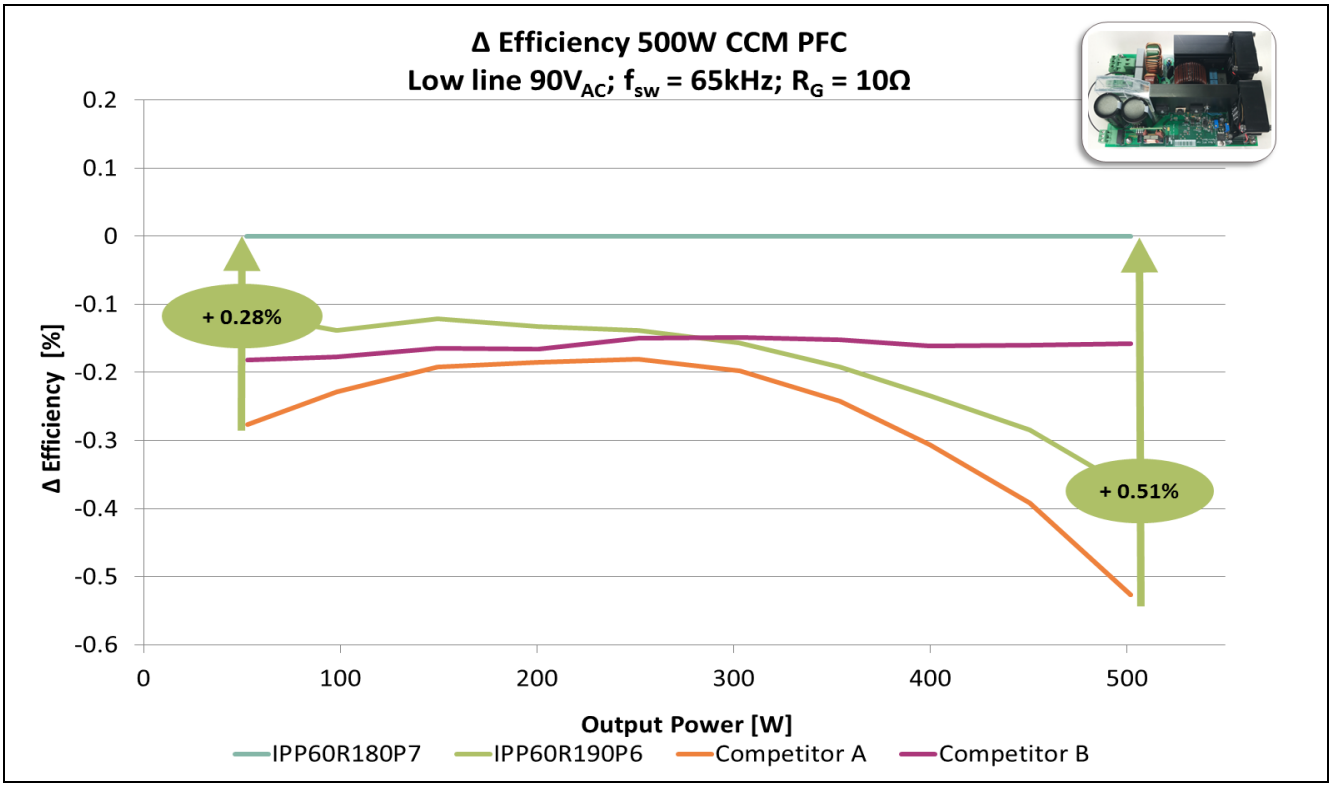


Figure 28 Efficiency comparison between CoolMOS™ P7, CoolMOS™ P6 and competitors

The 0.51 percent improved efficiency from P7 will result in 2.5 W lower losses in full load, only by changing the Mosfet.

It is worth mentioning that at higher switching frequencies the benefit of P7 will be even more pronounced.

3.2 Efficiency comparison in a resonant 600 W LLC half bridge

Figure 29 shows the efficiency comparison for a 600 W LLC circuit with V_{in}=380 V, and V_o=12 V, running at a resonant frequency of f_o=157 kHz. Due to lower turn-off losses and lower conduction losses the P7 offers approximately 0.1 percent efficiency improvement across the load range compared to best competition device.

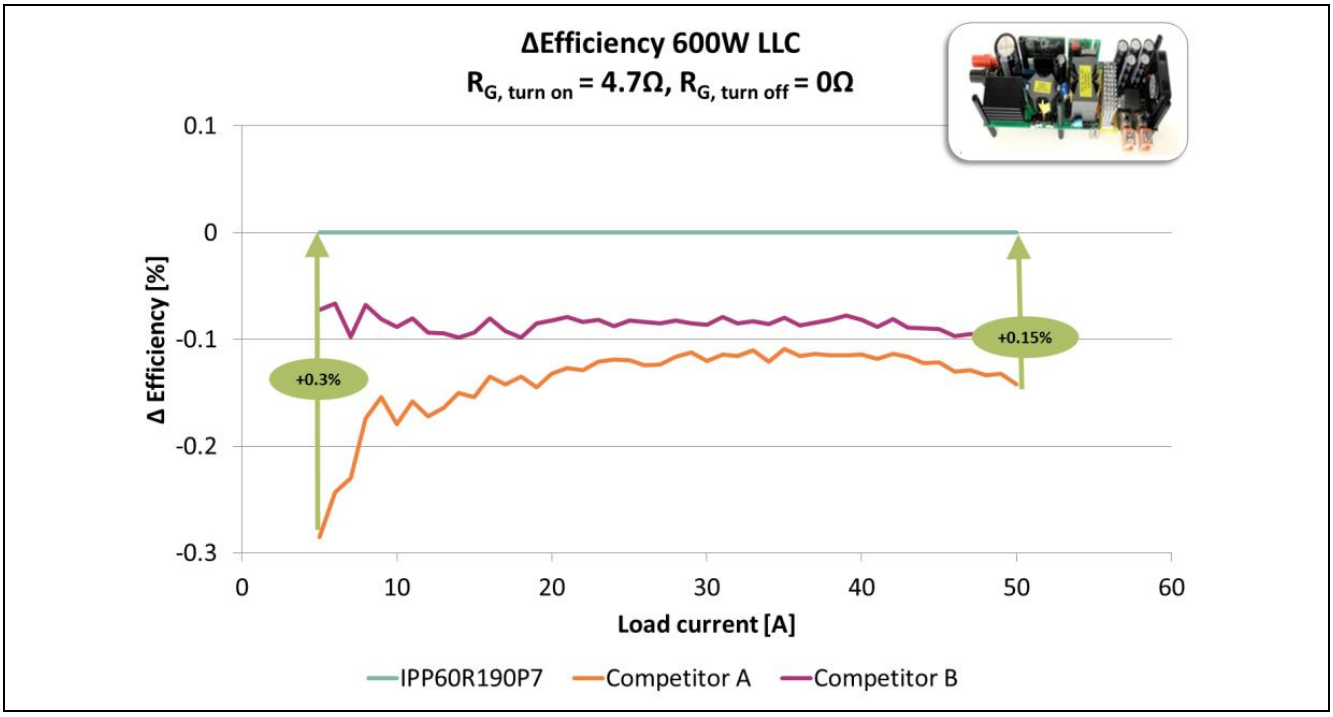


Figure 29 Efficiency comparison in a 600 W LLC half bridge application of CoolMOS™ P7 and competitors

The 0.15 percent improved efficiency from P7 will result in nearly 1 W lower losses in full load, only by changing the Mosfet.

3.3 Efficiency comparison in a real customer 240 W PC 'silver box'

Figure 30 shows the efficiency comparison in a real customer 240W PC Silverbox. In this plug and play measurement at V_{in}=90 V and with a switching frequency at around 65kHz P7 offers up to 0.3 percent efficiency improvement in light load thanks to the improved driving - and switching losses and in full load P7 offers around 0.2 percent higher efficiency thanks to lower conduction losses.

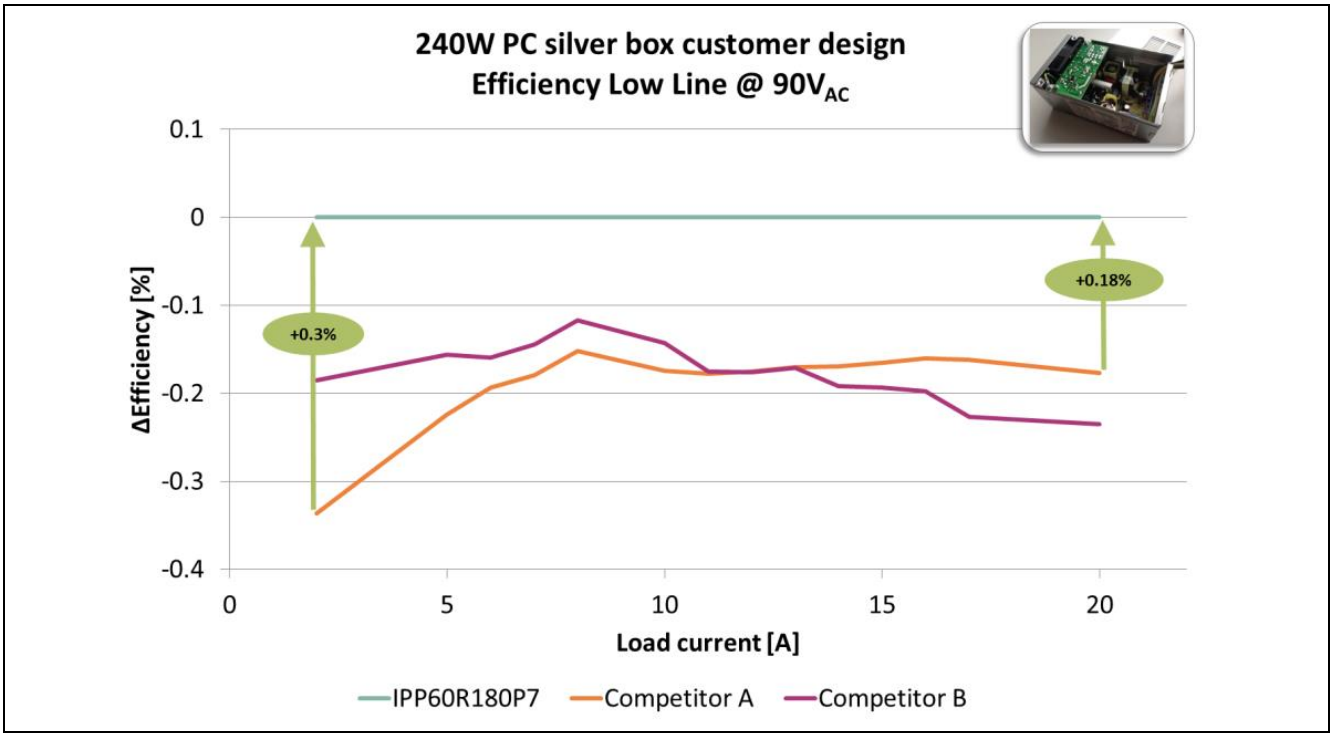


Figure 30 Efficiency comparison of CoolMOS™ P7 and competitors in a 240 W customer power supply

The 0.18 percent improved efficiency from P7 will result in nearly 0.5 W lower losses in full load, only by changing the Mosfet.

3.4 Brown out test in a real customer 240 W PC 'silver box'

In SMPS, the brown out test is very important. It is a test to shut down the power supply under a specified minimum input voltage and to check the possibility for damage. This condition is normally covered by the protection function of the controller, so that the MOSFET will be protected against input undervoltage (brown out) at low line. One of the challenges during operation in the brown out range is managing the temperature stability of the MOSFET while the power supply is delivering the output power. The combination of high conduction and switching losses due to the high operating current that creates high power dissipation in the MOSFET resulting in a high temperature rise in the device.

CoolMOS™ P7 offers reduced Q_g and a balanced and integrated low R_g that enable the fast switching that provides low turn-on and turn-off losses. Apart from the very efficient switching losses, P7 offers very low conduction losses, due to the lower $R_{DS(on)}$. In the 240 W CCM PFC application test shown inFigure 31 below, CoolMOS™ P7 case temperature is between 5 and 7°C lower than competitor A and competitor B at low line input voltage.

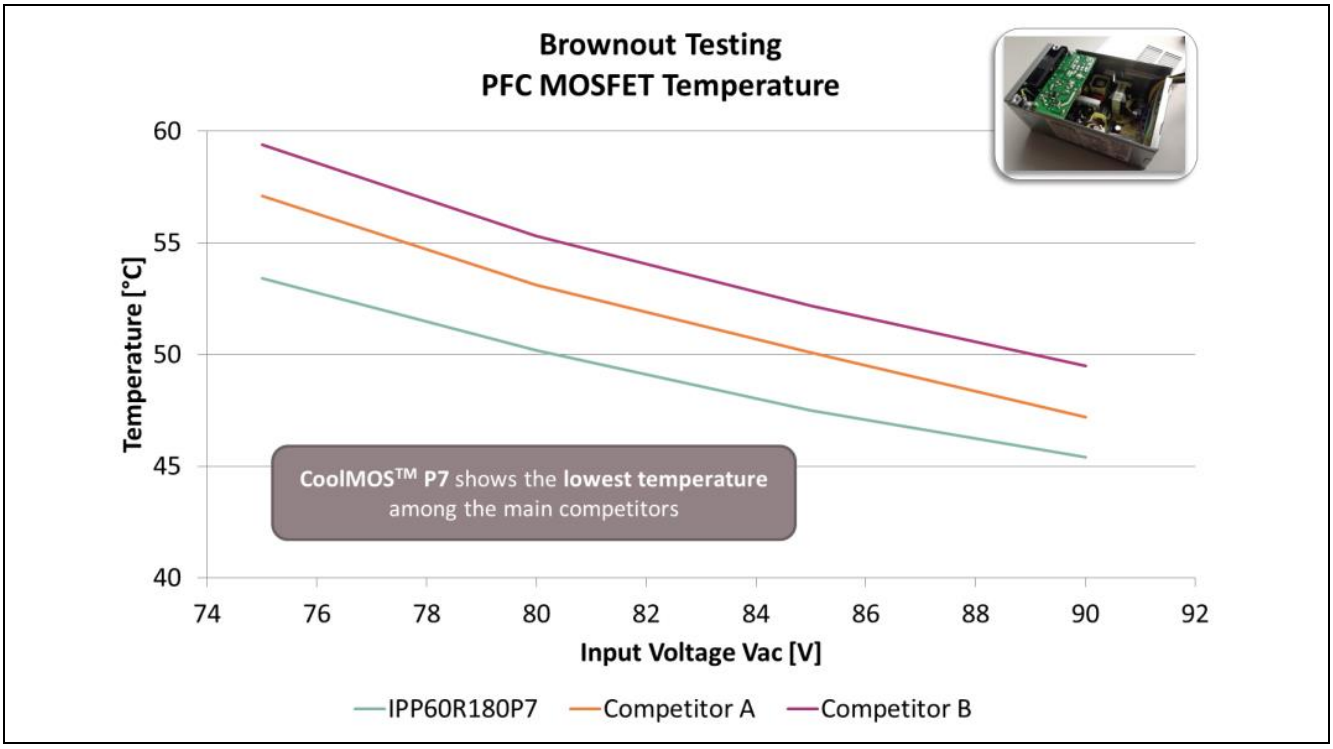


Figure 31 Temperature comparison of CoolMOS™ P7 and competitors in a 240 W customer power supply

3.5 Ringing

Figure 32 shows the peak volgage for the gate ringing oscillations of P7 in comparison with P6, competitor A and competitor B. V_{GS} peak is measured using a typical PFC stage with 7.2 pF capacitive coupling between the gate and drain emulating the parasitic capacitance of the PCB while continuous increasing the switched drain current. The layout parasitic capacitance can be a source of noise on the gate switching waveforms especially with increasing load current.

In the measurement, P7 shows a very good gate switching waveform even with reduced Q_g and provides plenty of margin before reaching the ±30 V gate ringing specification limit within normal operation current levels.

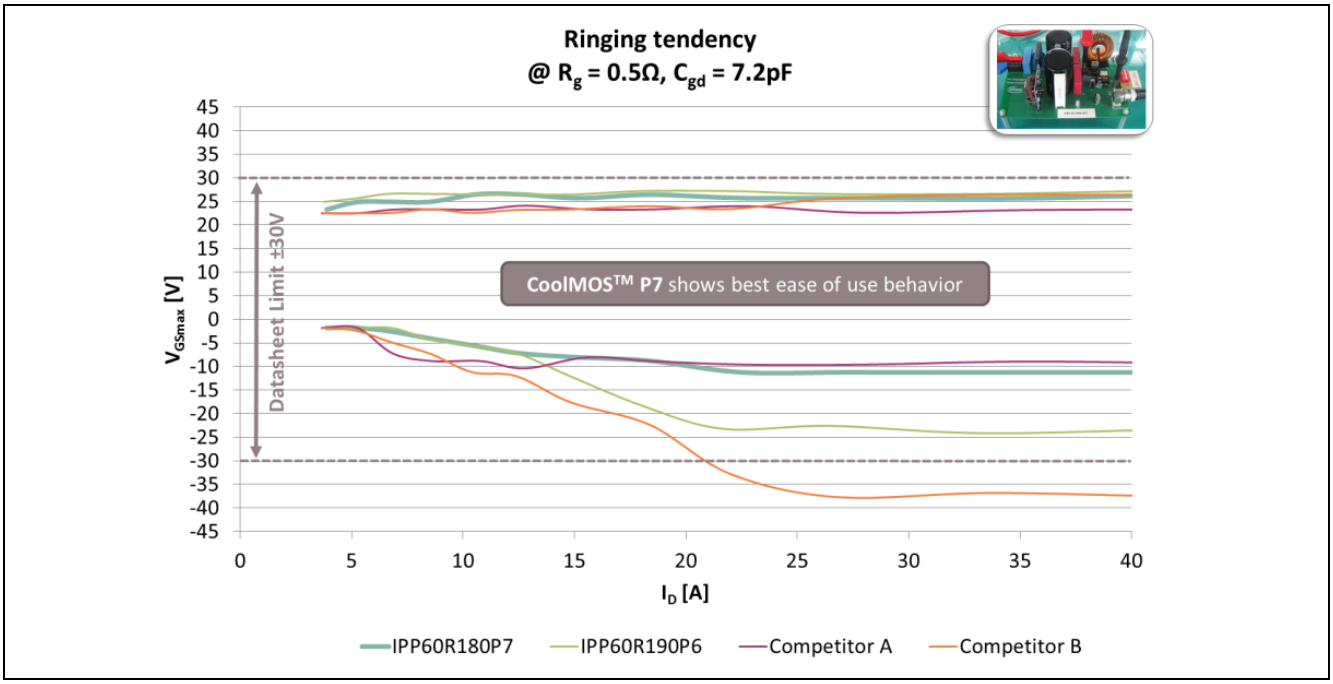


Figure 32 Ringing tendency comparison of CoolMOS™ P7, P6 and competitors

Figure 33 shows a typical switching waveform for IPP60R180P7 in a PFC circuit. This test circuit is configured with an additional external gate to drain capacitance with 7.2 pF for capacitive coupling between gate and drain emulating PCB parasitic capacitance. Designers should take care with the layout to minimize this parasitic capacitance to enable the highest performance of the MOSFET. In this measurement, an extremely low 0.5 Ω external R_g for a 180 mΩ device is used.

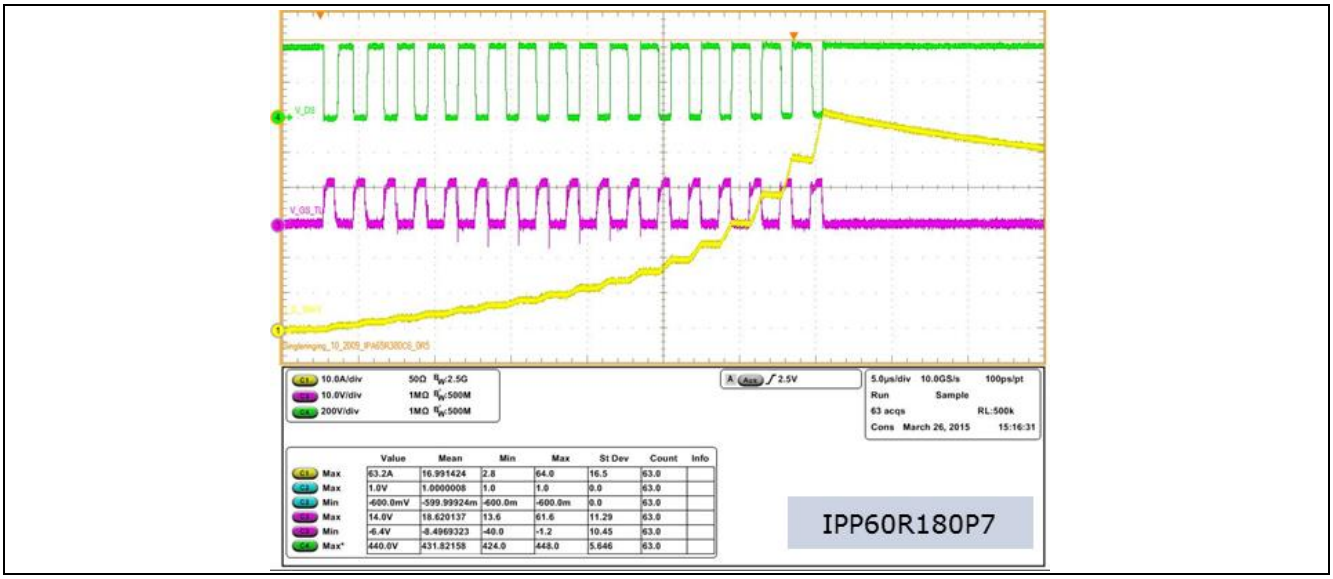


Figure 33 Ringing tendency of CoolMOS™ P7 in a PFC

Switching waveforms are measured with V_{DS}=400 V (shown in green) and V_{GS}=13 V (shown in crimson). The current waveform shown in yellow is increasing with every pulse up to saturation which is represented with an offset in V_{DS} at the peak current level of 64 A. P7 with optimized R_g shows a very nice switching waveform with plenty of margin to the +/-30 V V_{GS} limitation.

4 Design guideline

In the following sections we will give some guidelines on how to use the CoolMOS™ P7 in the best way to enable an optimized performance.

4.1 Minimum external gate resistor ($R_{g,ext}$)

In a well designed power supply we recommend to use an external resistor in the range of 5Ω for turn-on and zero Ω for turn-off. By implementing this R_g we have observed a very good efficiency level, very nice smooth swithing behaivior combined with very limited spikes on the gate. This efficiency driven R_g selection was possible due to the implementation of an $R_{g,int}$ and the very robust design of CoolMOS™ P7. However, the selection of external R_g is always a function of the PCB parasitic components that generate an unexpected voltage or current peak on the MOSFET due to the voltage signal from L_{stray} *di/dt and current signal from $C_{parasitics}$ *du/dt. To prevent such peaks, a reduction of the parasitic components or an increased $R_{g,ext}$ for the MOSFET is recommended.

4.2 Paralleling of 600 V CoolMOS™ P7

For paralleling 600 V CoolMOS™ P7 we generally recommend the use of ferrite beads on the gate or separated totem poles driving circuit. Thanks to the beads we damp the switching speed and make the paralleling less critical.

5 Portfolio

CoolMOS™ P7 series follows the same naming guidelines as already established with the P6 series e.g. IPP60R190P6, where "I" stands for Infineon Technologies, "P" for power MOSFETs, "P" for the package TO-220, "60" for the voltage class (divided by 10), "R190" for the on-state resistance in Ohms and P7 for the name of the series. Figure 34 shows the portfolio of CoolMOS™ P7.

The product innovations from a CoolMOS™ C7 are implemented in the 600 V CoolMOS™ P7. The major points are:

1. The popular TO-247 4pin package that offers huge performance advantages for the higher power range due to the fourth pin (Kelvin source). The increased creepage distance is also a clear benefit.

2. Much lower $R_{DS(on),max}$ compared to competitive devices in the TO-220 package. This package differentiation offers approximately 50 percent less source inductance and approximately 50 percent less space compared to the popular TO-247 packages.

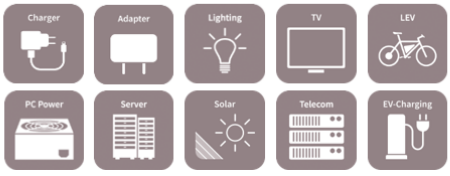
3. Much lower $R_{DS(on),max}$ products compared to the competition in the ThinPAK package. Reduced parasitic source inductance enables faster switching and increased efficiency.

4. The wide granularity of this portfolio enables SMPS designers to implement smart trade-offs for optimization.

5. A customized application relevant portfolio including industrial grade and standard grade.

6. The TO-220 FullPAK Wide Creepage allows boosting the production quality level due to the increased creepage distance.

	$R_{DS(ON)}$ [mΩ] Max.	DPAK	D²PAK	ThinPAK 8x8	TO220 FullPAK	TO220	TO220 FP NL	TO220 FP WC	TO247	TO247-4	SOT223
Industrial grade	600	IPD60R600P7			IPA60R600P7	IPP60R600P7					
	360/365	IPD60R360P7	IPB60R360P7	IPL60R365P7	IPA60R360P7	IPP60R360P7					
	280/285	IPD60R280P7	IPB60R280P7	IPL60R285P7	IPA60R280P7	IPP60R280P7					
	180/185	IPD60R180P7	IPB60R180P7	IPL60R185P7	IPA60R180P7	IPP60R180P7			IPW60R180P7	IPZA60R180P7	
	160				IPA60R160P7	IPP60R160P7					
	120/125		IPB60R120P7	IPL60R125P7	IPA60R120P7	IPP60R120P7			IPW60R120P7	IPZA60R120P7	
	99/105		IPB60R099P7	IPL60R105P7	IPA60R099P7	IPP60R099P7			IPW60R099P7	IPZA60R099P7	
	80		IPB60R080P7	IPL60R085P7	IPA60R080P7	IPP60R080P7			IPW60R080P7	IPZA60R080P7	
	60/65		IPB60R060P7	IPL60R065P7	IPA60R060P7	IPP60R060P7			IPW60R060P7	IPZA60R060P7	
	45		IPB60R045P7						IPW60R045P7	IPZA60R045P7	
	37								IPW60R037P7	IPZA60R037P7	
	24								IPW60R024P7	IPZA60R024P7	
Standard grade	600	IPD60R600P7S			IPA60R600P7S		IPAN60R600P7S	IPAW60R600P7S			IPN60R600P7S
	360	IPD60R360P7S			IPA60R360P7S		IPAN60R360P7S	IPAW60R360P7S			IPN60R360P7S
	280	IPD60R280P7S			IPA60R280P7S		IPAN60R280P7S	IPAW60R280P7S			
	180	IPD60R180P7S			IPA60R180P7S		IPAN60R180P7S	IPAW60R180P7S			



- Large $R_{DS(on)}$ and package variety
- Offering through hole and SMD packages
- Suitable for a wide variety of applications and power ranges

Figure 34 600 V CoolMOS™ P7 portfolio

6 Conclusion

This document has described Infineon's latest HV SJ 600 V CoolMOS™ P7 MOSFET technology with the following key features:

1. Best–fit performance for target markets

- Significant reduction of switching losses (-50 percent E_{oss}, -30 percent Q_g, -20 percent turn-off losses)
- Lower $R_{DS(on)}$ packages (60 mΩ in TO-220, 65 mΩ in ThinPAK,…)
- Enabling smaller form factors

2. New state-of-the-art in "ease-of-use"

- Very low ringing tendency
- Outstanding body diode ruggedness with new BIC dv/dt and di_f/dt values like CFD2
- Smooth switching waveforms
- Excellent ESD robustness greater than 2 kV (HBM)

3. Best-in-class commercial aspects

- Best-in-class price performance ratio
- 60 parts in 9 different packages
- $R_{DS(on)}$ granularity from 37 to 600 mΩ
- Available in industrial and standard grade packages
- Suitable for a wide variety of applications and power ranges

It has also been demonstrated in real application measurements that the CoolMOS™ P7 with a lower FOM enables improved efficiency in combination with a smooth "ease-of-use" in comparison to the most common competitor devices.

This feature enables the design engineers to easily design their power converters with high efficiency, high power density, high robustness and cool thermal behavior. Furthermore CoolMOS™ P7 is the best price/performance solution that enables a long term perspective.

7 Demoboards

For evaluating the P7 600 V performance we can offer following IFX Demo boards, which are available at ISAR:

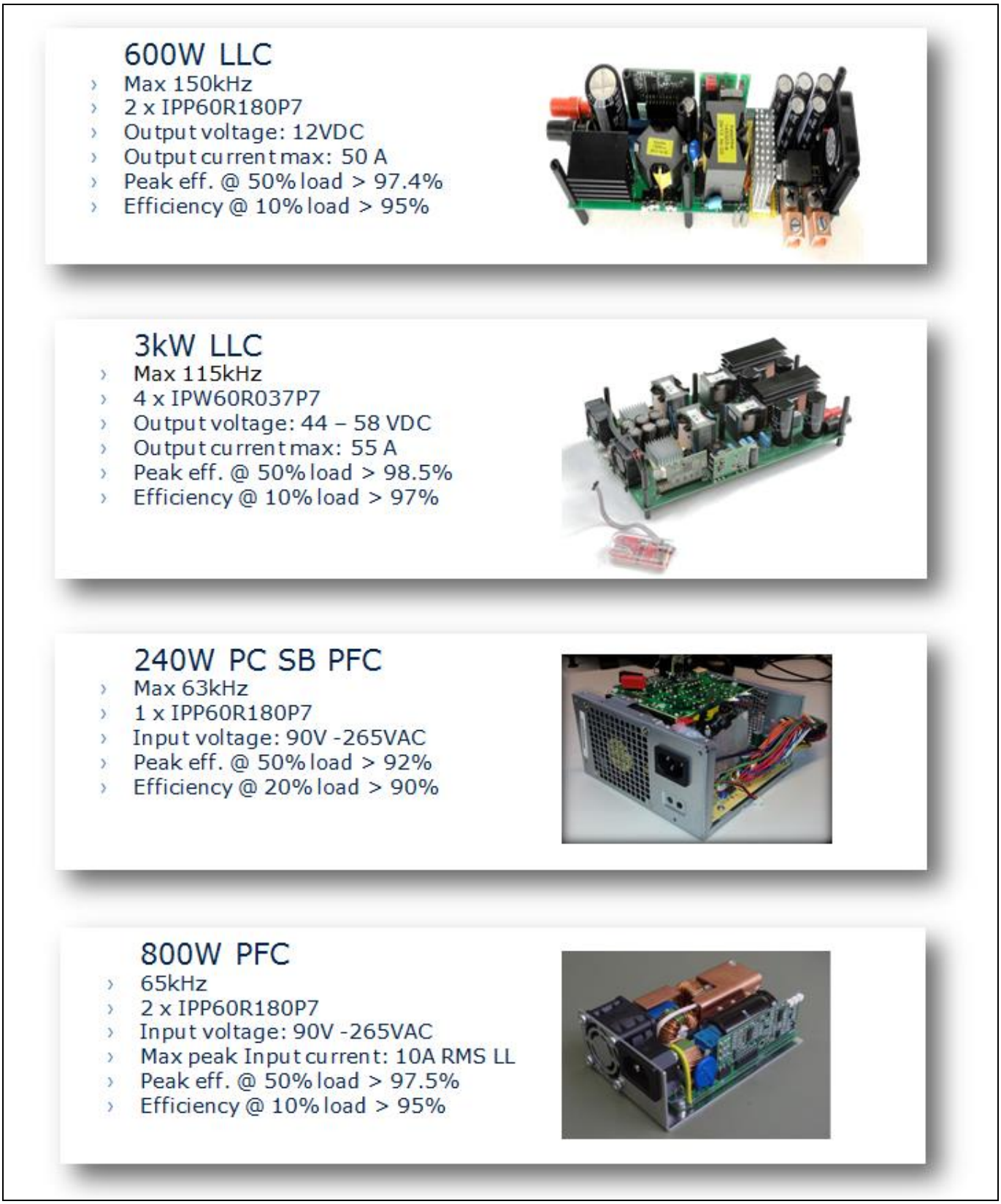


Figure 35 Demo boards overview for 600 V CoolMOS™ P7

8 List of abbreviations

C_{GD} ..... internal gate drain capacitance $C_{GD}=C_{rss}$
C_{iss} ..... input capacitance $C_{iss}=C_{GS}+C_{GD}$
$C_{o(er)}$ ..... effective output capacitance
di/dt ..... steepness of current comutation at turn off / turn on
DUT ..... device under test
dv/dt ..... steepness of voltage comutation at turn off / turn on
E_{off} ..... power loss during switch off
E_{on} ..... power loss during switch on
E_{oss} ..... stored energy in output capacitance (Coss) at typ. V_{DS}=400 V
FOM ..... figures of merit
I_D ..... drain current
MOSFET ..... metal oxide semiconductor field effect transistor
PFC ..... power factor correction
PNP ..... bipolar transistor type (pnp vs. npn)
Q_{OSS} ..... Charge stored in the C_{OSS}
$R_{DS(on)}$ ..... drain-source on-state resistance
SMPS ..... switched mode power supply
V_{DS} ..... drain to source voltage
ZVS ..... zero voltage switching
Q_G ..... gate charge
Q_{GS} ..... gate charge, gate to source
Q_{GD} ..... gate charge, gate to drain
R_G ..... gate resistor
CCM PFC ..... continous conduction mode power factor correction
L_S ..... source inductance
LLC ..... DC-DC stage with resonant tank in order to maintain zero voltage switching

9 Usefull material and links

- **600 V CoolMOS™ P7 webpage**
  www.infineon.com/600V-P7

- **600 V CoolMOS™ C7 webpage**
  www.infineon.com/C7

- **600 V CoolMOS™ P6 webpage**
  www.infineon.com/P6

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[13] A. Steiner, J.Cathly 600V CoolMOS™ P6 600V Superjunction MOSFET for Server, Telecom, PC Power and Consumer

11 Revision history

Major changes since the last revision

Page or Reference	Description of change
Page 24	Update link to figure
Page 3…34	Update format

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