# Linear Mode Operation and Safe Operating Diagram of Power-MOSFETs

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Application Note

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# 1 Introduction

The development of modern Power-MOSFETs has focused on ultra-fast switching and ultra-low ohmic devices leading to continuously decreasing area specific on-resistances. Consequently, compared to Power-MOSFETs from 10 years ago today's state of the art Power-MOSFETs utilize a much smaller silicon die area for any given $R_{DS(on)}$. Thus the power handling capabilities of devices for a specific $R_{DS(on)}$ generally have decreased. Especially in linear operation mode when MOSFETs handling high power dissipation due to the simultaneous occurrence of voltage at the pins and current in the MOSFET this is of importance. The Safe Operating Area diagram (SOA diagram) defines the allowed maximum current-voltage range. It must be considered during the design-in phase of the Power-MOSFETs especially in cases with linear mode operation.

Many applications exist with the Power-MOSFET being operated primarily in linear mode [2]. Linear mode operation refers to the current saturation region in the output characteristics. The drain current ($I_{DS}$) is nearly independent of the drain to source voltage ($V_{DS}$) for a given gate to source ($V_{GS}$) voltage. It depends then directly on the $V_{GS}$-voltage of the MOSFET. In Fig. 1 the area of linear mode operation is indicated as red shaded area.

Contrary to the region of linear mode operation is the so called ohmic region (indicated as blue shaded area in Fig. 1). The relationship between $V_{DS}$ and $I_{DS}$ follows Ohm's law.

As shown in Fig. 1 MOSFET operating at low $V_{GS}$ voltage (e.g. 2.9V) and high $V_{DS}$ (e.g. $V_{DS}$=4V) voltage is able to carry considerable currents (e.g. ~200A). Here, the MOSFET operates in linear mode. The power dissipation is very high (e.g. 800W) which bares the potential for MOSFET destruction as being discussed later. The SOA diagram is a tool to check for a given parameter set of $V_{DS}$, $I_{DS}$ and stress time whether or not the Power-MOSFET operates within specification. This is important as operation outside the specification can deteriorate the device and decreases its reliability. In severe cases of specification violation a catastrophic failure can occur. To verify that the MOSFET stays within the SOA it is necessary to understand the application and the time dependent voltage and current functions ($V_{DS}$=f(t), $I_{DS}$=f(t)).

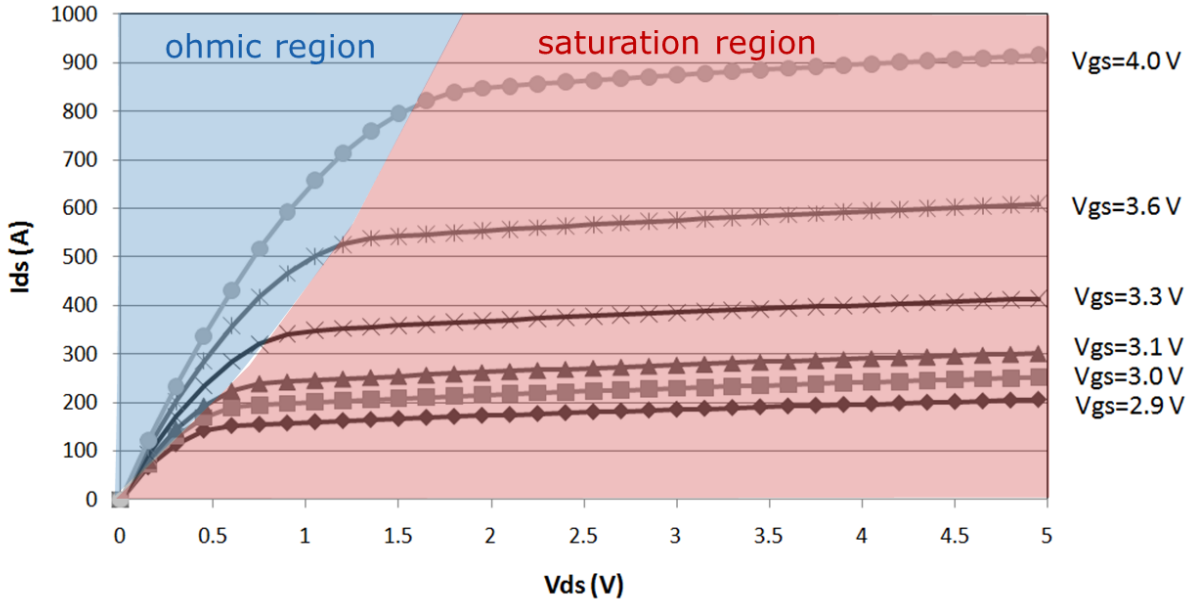


Fig. 1: Output characteristics of a Power-MOSFET (OptiMOS™ 25V, BSC010NE2LS [1]). The blue shaded area indicates the operation in the ohmic region, the red shaded region represents linear mode operation.

## 1.1 Applications driving MOSFETs in linear mode operation

Many applications exist where the MOSFET enters linear mode operation. It will be shown that even fast switching MOSFETs operate briefly and repetitively in linear mode. Consequently, when the switching speed of a MOSFET is

being slowed down by adding an external gate resistor $R_g$ the MOSFET will operate in linear mode for a longer time and could violate by SOA limitations.

### *Traditional linear mode operation – battery charger, fan controller*

A fan controller arrangement where the MOSFET is used as current source is shown in Fig. 2. The fan speed (or in case of a battery charger the charging current) is controlled by the current flow through the fan. The current is exclusively controlled by the MOSFET. This means that the MOSFET must be operated in linear mode. Changing the $V_{GS}$ voltage will change the current flowing through the motor and thus the fan speed. On the right hand side of Fig. 2 the output characteristics of the MOSFET is shown. The point where the MOSFET is being operated is shown as red dot. According to the diagram the voltage across the MOSFET will be the input voltage minus the voltage drop across the fan and might be as high as $V_{DS}$=7.5V, for example. The current flowing through the MOSFET could be ~15A depending on fan speed. Therefore the power dissipation in the MOSFET can be as big as 112.5W. The choice of a thermally good performing package (low $R_{thJC}$ and $R_{thJA}$ values) and an adequate thermal management (cooling with airflow and/or heatsink) are obviously necessary to ensure safe operation of the MOSFET. When the MOSFET is used as a fan speed controller the linear mode operation could last forever and the current (fan speed) is only controlled via the $V_{GS}$ voltage. As the MOSFET is operated exclusively in linear mode, the $R_{DS(on)}$ of the MOSFET is completely irrelevant when calculating the power dissipation. The power dissipation in the MOSFET depends only on the voltage drop across the MOSFET and the current flow: $P_{diss}=V_{DS} \cdot I_{DS}$.

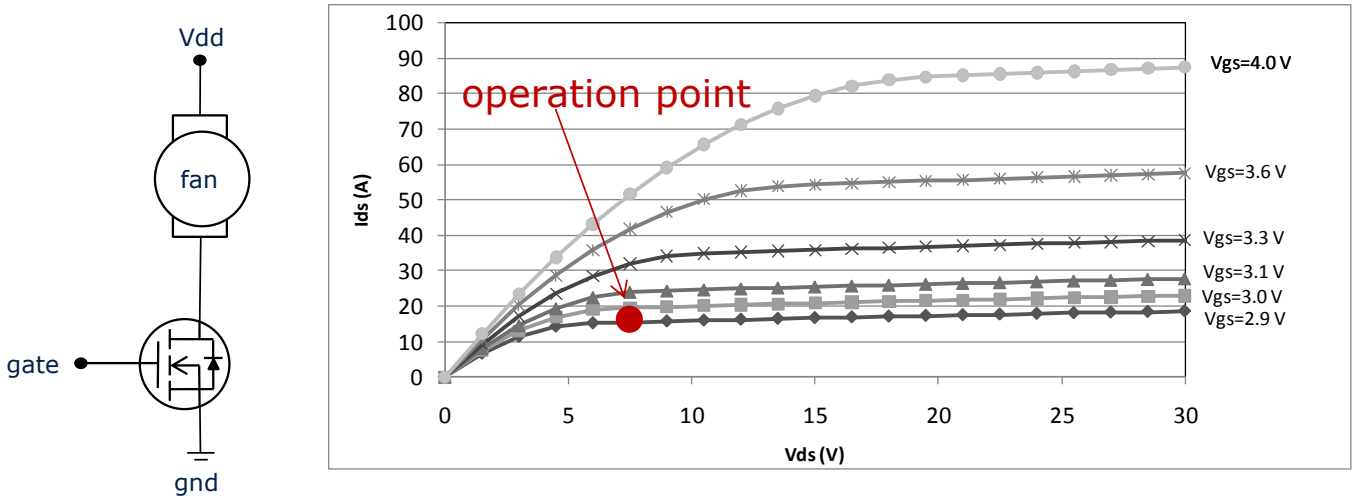


Fig. 2: MOSFET used as constant current source. The current flow through the fan is controlled exclusively by the $V_{GS}$ voltage at the MOSFET gate.The red point in the output characteristics diagram on the right hand side indicates a potential operation point of the MOSFET in the saturation region.

### *Partial linear mode operation – e-fuse, load-switch*

In e-fuse applications or load-switches the MOSFET can be used to maintain slow turn on avoiding high inrush currents. For e-fuse applications an e-fuse controller senses the current and controls the current flow by varying the MOSFET $V_{GS}$ voltage. In doing so the MOSFET briefly operates in linear mode. The $V_{GS}$ voltage is being increased only slowly until the full current flows and finally the MOSFET is being operated in the ohmic region. The diagram on the right part of Fig. 3 illustrates the three operation states of the MOSFET in the output characterstics diagram.

At first the MOSFET is off and the entire voltage drops across the MOSFET. Then the $V_{GS}$ voltage is being increased continiously and drain current starts to flow. At this point the MOSFET operates in linear mode which is shown as 2nd operational state in the diagram. Here the SOA becomes relevant. Finally the MOSFET is fully enhanced (turned on) and it is being operated in the ohmic region. The same three operational states occur when the MOSFET is used as a load switch. Critical for the MOSFET is the time in linear mode which depends on the load-switch controller (or the e-fuse controller) timing. Typical timings are in the range of µ-seconds and may even

reach milli-seconds. It is vital to understand this timing in detail so that time dependent voltage and current stress on the MOSFET can be derived to check for potential violation of the SOA.

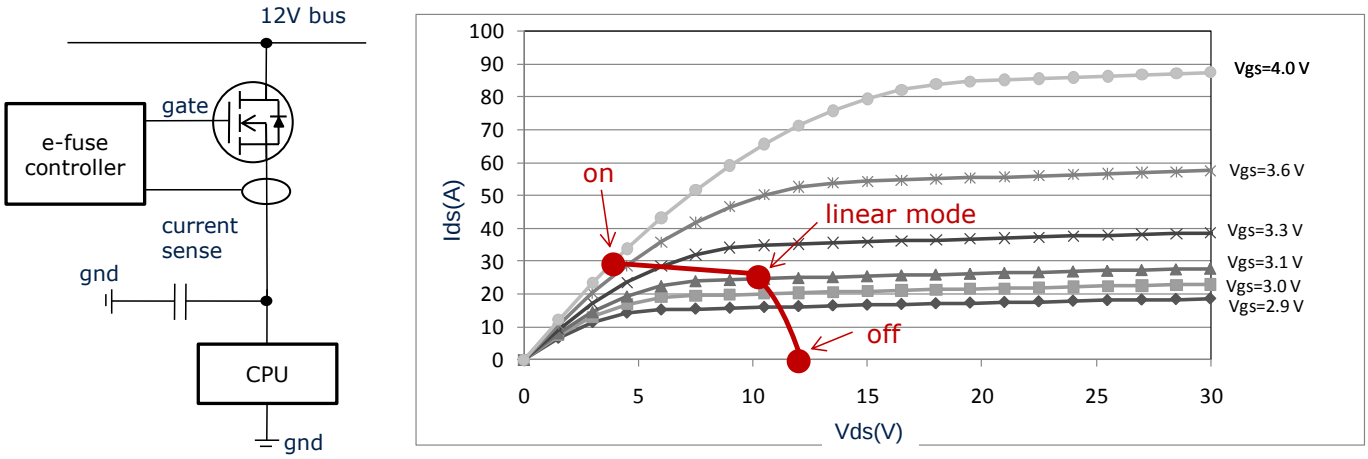


Fig. 3. MOSFET used in e-fuse application (left). In e-fuse application (during turn-on) the MOSFET passes the linear mode operation region for a significant period of time. The SOA must be checked to verify the MOSFET can withstand the thermal stress.

*Short linear mode operation – buck converter, general switching*

When the MOSFET is used as high-side switch in a buck converter for example it also enters linear mode operation for a very short period of time [2]. Linear mode operation starts exactly when the MOSFET's $V_{GS}$ voltage is at the threshold voltage ($V_{GS(th)}$) and ends with the drain-source voltage reaching zero. This corresponds to the end of the Miller plateau. In other words: during the switching event the MOSFET is in linear mode operation. Modern power MOSFETS, however, demonstrate dramatically short switching times. State of the art 25V-250V MOSFETs are capable of switching thourgh the saturation region within a few nano-seconds (<10ns), depending on the specific product. The period of linear mode operation is usually as short as a few ns for MOSFETs utilized as high-side switches in high-performance buck converters. The example also demonstrates that any reduction of switching speeds by introducing external gate resistance ($R_g$) or utilizing a slow driving concept (e.g. MOSFET gate is charged from a constant current source with low current rating) the SOA diagram could become relevant. Therefore, whenever soft-turn on or reduction of ringing by slowing down the switching speed is implemented the SOA diagram should be considered.

## 2.0 The Safe Operation Area diagram

In section 1 the SOA diagram has been introduced as crucial diagram for designs with MOSFETs in linear mode operation. Now the SOA will be explained in detail. The origin of the limit-lines in the SOA diagram will be discussed. Furthermore, it will be shown that one must pay attention to the conditions the SOA diagram is given in the datasheet versus the application conditions.

## 2.1 SOA limit-lines

In Fig. 4 the SOA diagram of an Infineon power MOSFET (BSC010NE2LS) is shown. The five limit-lines defining the SOA diagram are the $R_{DS(on)}$ limit-line (blue line), the current limit-line (red line), the maximum power limit-line (dark green line), the thermal instability limit-line (light green line) and the breakdown voltage limit-line (yellow line). Within these limit-lines the green shaded area gives the area where the MOSFET can be safely operated. In this example the SOA diagram is calculated for a constant case temperature of $T_c$=25°C and a single pulse with duration 100µs. The datasheet provides additional limit-lines for various pulse lengths up to continuous operation (DC operation). To calculate limit-lines for other case temperatures and/or continuous pulsed operation the origins of the limit-lines must be understood. The following paragraphs give insight to the derivation of the SOA diagram limit-lines.

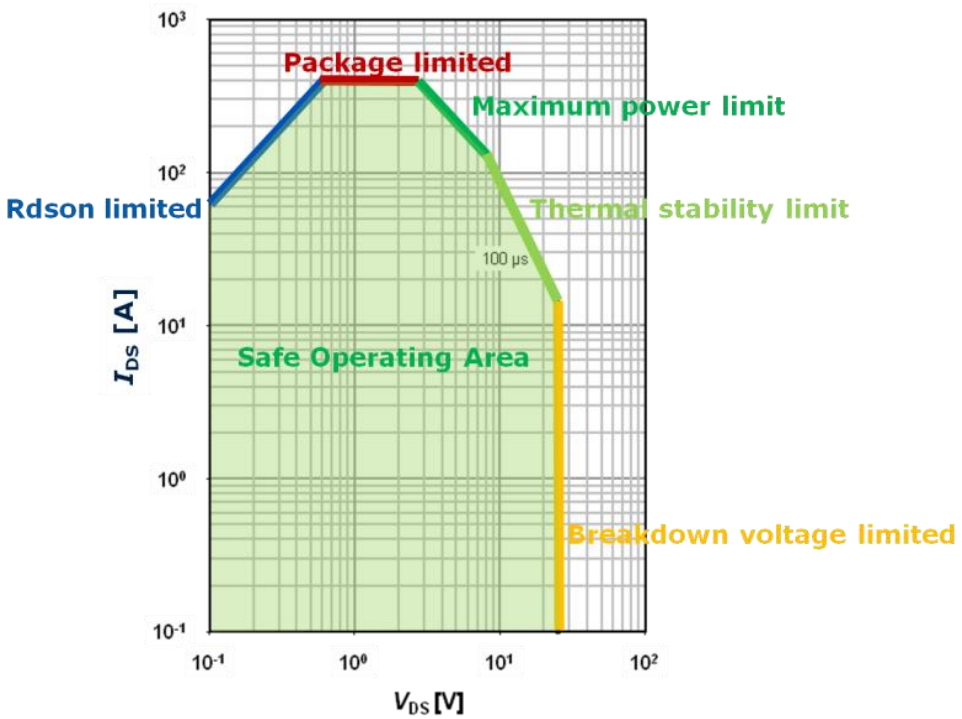


Fig. 4 Safe operating area diagram of a 25V Power MOSFET (BSC010NE2LS). The SOA is shown for 100µs pulse time and the limiting lines are indicated.

$R_{DS(on)}$-*limit-line (blue line)*

As seen in Fig. 4 the $R_{DS(on)}$ limit-line gives a linear dependency between $V_{DS}$ and $I_{DS}$. The slope of the line is simply the maximum $R_{DS(on)}$ of the MOSFET at $T_j$=150°C and $V_{GS}$=10V. Therefore the $R_{DS(on)}$-limit-line is given as

$$I_{DS} = \frac{V_{DS}}{R_{DS(on)}(@V_{GS}=10V, T_j=150°C)} \quad \text{eq.1}$$

This means

- For lower $V_{GS}$ voltages the $R_{DS(on)}$-limit-line will be lower since the $R_{DS(on)}$ value increases with lower $V_{GS}$ voltages. The dependency of $R_{DS(on)}$ vs $V_{GS}$ voltage can be found in the MOSFET datasheet.
- In case $T_j$ is known to be lower than 150°C the $R_{DS(on)}$-limit-line will move up again since the $R_{DS(on)}$ value decreases with lowering $T_j$.

Therefore the $R_{DS(on)}$ limit-line can easily be recalculated using equation 1 and datasheet parameters for $R_{DS(on)}$ and the relevant $T_j$.

*Package-limit-line (red line)*

When following the $R_{DS(on)}$ limit-line towards higher currents and voltages the current-limit-line is found. This limit-line is typically defined by the maximum current the package can handle. Therefore the amount of this current will be strongly package dependent. Packages with bond wires (DPAK) will show different maximum current handling capabilities compared to packages with clip bonding technology (SuperSO8). Also the die size will impact the current handling capability of the package since it determines the bonding scheme (number of bond wires, bond wire diameter, clip dimension). The package limit-line will not change in case application conditions such as ambient temperature vary.

*Maximum-power-limit-line*

After the package limit-line the maximum power limit-line follows. It is calculated from the maximum power the system is allowed to generate to reach a stable junction temperature $T_j$ of 150°C in thermal equilibrium and $T_c$=25°C. It is obvious that the cooling concept of the system and therefore thermal variables like case temperature ($T_c$) and thermal impedance ($Z_{thJC}$) will strongly impact this limit-line. The limit-line can be calculated by assuming thermal equilibrium:

$$P_{dissipated} = P_{generated}$$

The equation for $T_j$ in a simple thermal model:

$$T_j = T_c + Z_{thJC} \cdot P_{dissipated}$$

the $I_{DS}$ as function of $V_{DS}$ is given by

$$I_{DS} = \frac{\Delta T_{max}}{Z_{thJC}(t_{pulse}) \cdot V_{DS}} \quad \text{eq. 2}$$

This equation illustrates some important dependencies:

- The $I_{DS}$ depends on the maximum allowable temperature rise for $T_j$. The maximum allowable temperature rise $\Delta T_{max}$ will depend on $T_c$ and the maximum $T_j$ the device is permitted to sustain.
- The $I_{DS}$ value is influenced by the value of the thermal impedance $Z_{thJC}$. For short pulses the value of $Z_{thJC}$ depends on the pulse length and its duty cycle. $Z_{thJC}$ can be taken from the corresponding diagram in the datasheet. The SOA diagram visualizes that an increase of pulse length shifts the maximum thermal limit-line downwards. It reflects the higher thermal impedance at longer pulse times and/or higher duty cycle.
- Due to the increased power dissipation with increasing $V_{DS}$ the $I_{DS}$ also depends with indirect proportionality on the applied $V_{DS}$ voltage.

The SOA diagram shown in Fig. 4 has been calculated for the BSC010NE2LS MOSFET:

- $t_{pulse}$=100µs → $Z_{thJC}$=0.102 K/W from datasheet
- $T_c$=25°C and $T_{jmax}$=150°C → $\Delta T_{max}$=125°C

$$I_{DS} = \frac{125}{0.102 \cdot V_{DS}} \quad \text{eq.3}$$

For an application where $T_c$ is greater than 25°C and/or the maximum allowed $T_j$ is less than 150°C the maximum power limit-line will naturally be lower and can be calculated with the help of equation 3. The SOA diagram in the datasheet is given at dutycycle D=0 for various pulse lengths. Exposing the MOSFET to repetitive pulses results in D≠0. In that case the thermal impedance diagram $Z_{thJC}=f(t_p, D)$ has to be used to get the correct $Z_{thJC}$ value. Then, the maximum power limit-line can be calculated by equation 2 according to the needs of the engineer.

*Thermal (in-)stability limit-line*

Following the maximum-power limit-line reveals a point at which the slope of the limit-line changes. This point indicates the on-set of the thermal-instability limit-line. To understand the origin of this limitation it is necessary to consider the criterium for thermal instability. A MOSFET (or generally a system) is considered to be thermally un-stable in case the power generation ($P_{generated}$) rises faster than the power dissipation ($P_{dissipated}$) over temperature. That means

$$\frac{\partial P_{generated}}{\partial T} > \frac{\partial P_{dissipated}}{\partial T}$$

In such a condition the temperature of the system is not stable and the system is *not in thermal equilibrium* unlike for the maximum-power limit-line. With the help of

$$P_{generated} = V_{DS} \cdot I_{DS}$$

and

$$P_{dissipated} = \frac{T_j - T_{amb}}{Z_{thJC}}$$

the inequality can be rearranged to

$$V_{DS} \cdot \frac{\partial I_{DS}}{\partial T} > \frac{1}{Z_{thJC}(t_{pulse})}$$

For further elaboration here it will be assumed that $V_{DS}$ is being constant over temperature.

The equation above defines the range where the MOSFET may encounter thermal instability. The term $\frac{\partial I_{DS}}{\partial T}$ is called *Temperature Coefficient*. Since $V_{DS}$>0 and $\frac{1}{Z_{thJC}(tpulse)}$>0 thermal instability can occur only if the temperature coefficient of the drain to source current is positive. The question under what conditions such a positive temperature coefficient can be found is answered by the transfer-funtion graph in the MOSFET datasheet showing $I_{DS}$ over $V_{GS}$ for various temperatures. An example for such a graph is given in Fig. 5. Comparing the currents at $V_{GS}$=2V for $T_j$=25°C and $T_j$=150°C indicate that in case of $V_{GS}$=2V the current will rise over temperature. This means the temperature coefficient for $V_{GS}$=2V is positive. At $V_{GS}$=3.5V the current will decrease over temperature and the corresponding temperature coefficient is negative. In between is a crossover for the transconductance curves of

$T_j$=25°C and $T_j$=150°C. This crossover point is being referred to as Zero Temperature Coefficient (ZTC) point. Clearly, thermal instability can occur only for $V_{GS}$ below the $V_{GS}$ of the ZTC point.

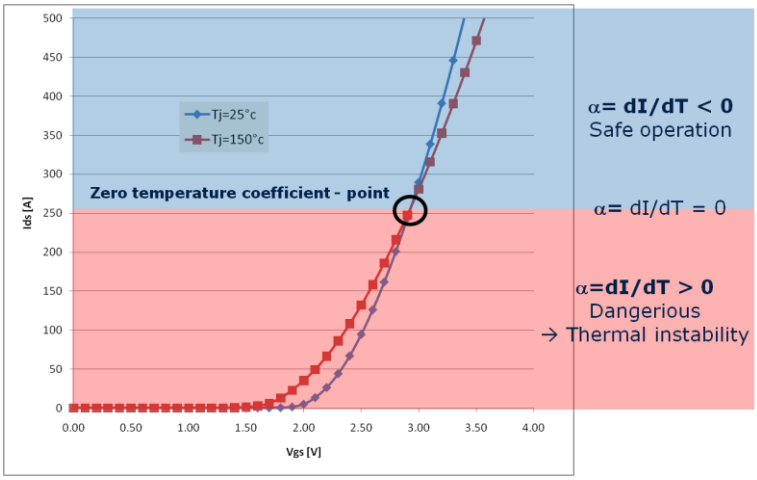


Fig. 5 Transfer characteristic of a Power-MOSFET for $T_j$=25°C (blue line) and $T_j$=150°C (red line).

The change of temperature coefficient from positive to negative over $V_{GS}$ is caused by two competing effects. On one hand the resistance of a MOSFET increases over temperature due to lower electron mobility in the crystal lattice. On the other hand the threshold voltage of the MOSFET decreases over temperature since more electrons have been excited into the conduction band of the MOSFET. At low temperatures the effect of decreasing threshold voltage over increasing temperature dominates and currents increase over temperature. At higher temperatures the increase of $R_{DS(on)}$ over temperature dominates and currents decrease over temperature.

As shown above thermal instability will occur for $V_{GS}$ being below the ZTC point. Thus, MOSFETs with a ZTC at high currents and high $V_{GS}$ voltages will be more prone to thermal instability. The ZTC point is in direct relationship to the MOSFET transconductance. With increasing transconductance the ZTC point will move towards higher $V_{GS}$. Modern power MOSFETs exhibit ever increasing transconductances and therefore also ZTC-points at higher $V_{GS}$ .

When comparing comparing the transconductance curves in datasheets for 25V and 150V MOSFETs (eg 30V OptiMOS™ vs 150V OptiMOS™ 3) one will realize that for the 150V technology the ZTC point is located at lower currents and $V_{GS}$ voltages. This is because for higher voltage class MOSFETs (e.g. 150V) the increase of $R_{DS(on)}$ over temperature will dominate the transconductance behavior over temperature as they have thicker EPI layers, lower cell pitch and generally a lower doping level compared to lower voltage class MOSFETs (25V).

Having discussed the origins of thermal instability the destruction mechanism in case of thermal instability can be explained as follows: Generally, it is assumed that the temperature distribution over the MOSFET is uniform so that $T_j$ is the same over the entire chip. In reality this is not the case. Small inhomoginities of, for example, solder thickness between die and package exist. They will lead to minimal higher local temperatures. This local temperature differences will develop in dependence on the operation point of the MOSFET with respect to the ZTC point:

- For operation above ZTC the temperature coefficient is negative. Hotter spots will draw less current and the spot cools down. The chip stabilizes itself and initial temperature variations become irrelevant.
- For operation below ZTC the temperature coefficient is positive. In this case the local hot spots will draw more current as they heat up. This will lead to increased local power dissipation and further heating. Ultimately this results in thermal runaway and local destruction of the chip.

Finally, the question of how to adjust the thermal instability line for application conditions different from the datasheet must be answered. The on-set of the thermal instability line is given by

$$V_{DS} \cdot Z_{thJC}(t_{pulse}) \cdot \frac{\partial I_{DS}}{\partial T} = 1$$

This means that the temperature coefficient must be known. The latter cannot be easily calculated. The most straight forward approach to de-rate the thermal-instabiliy limit line is to displace the line vertically according to the following procedure:

First, the $R_{DS(on)}$ limit-line, package limit-line and maximum power consumption limit-line can be calculated and plotted in a SOA diagram for any given Tc, maximum $T_j$ and pulse lengths as explained above. The formula for the thermal-instability limit line in the form:

$$log(I_{DS}) = \alpha \cdot \log(V_{DS}) + \beta$$

can be derived by utilizing two points (point A, point B) on the limit line as indicated in Fig.6. In Fig. 6: point A is at: $I_{DS}$=105A and $V_{DS}$=8V; point B: $I_{DS}$=12A and $V_{DS}$=25V. The two equations

$$\log(105) = \alpha \cdot \log(8) + \beta$$

$$\log(12) = \alpha \cdot \log(25) + \beta$$

give the parameters α and β of the thermal-instability-limit-line (here: $\alpha = -1.904, \beta = 3.740$).

Now the formula for the de-rated limit line can be found by simply determining a new β as the slope α does not change upon de-rating. This is done by using point C on the derated power limit-line at the $V_{DS}$ of the connection point of power limit-line and thermal instability limit-line as given in the datasheet. In Fig. 6: point C: $I_{DS}$=65A and $V_{DS}$=8V.

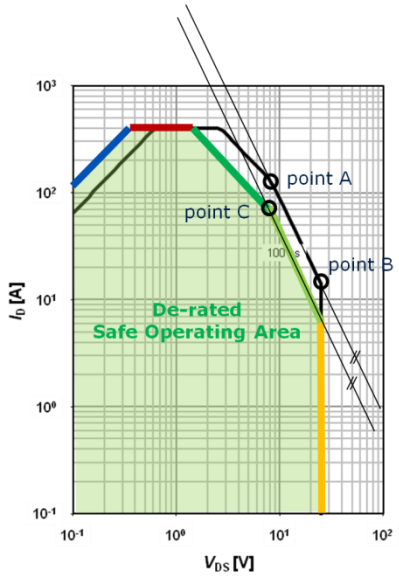


Fig. 6 Method for derating of the thermal instability limit-line.

Therefore

$$\beta_{\text{derated}} = \log(65) + 0.585 \cdot \log(8) = 3.532$$

This finally provides the de-rated thermal-instability limit line for Fig. 6:

$$\log(\text{I}) = \alpha \cdot \log(\text{Vds}) + \beta_{\text{derated}} = -1.904 + \log(Vds) + 3.532$$

*Breakdown voltage limit-line*

On the right hand-side the limit of the SOA is given by the MOSFETs maximum applicable $V_{DS}$ voltage. This is generally the breakdown voltage $V_{br(DSS)}$ of the device and will depend on the $T_j$. The relationship between $V_{br(DSS)}$

and $T_j$ is given in a separate graph in the MOSFET datasheet. It can be seen that the BVDSS voltage might be significantly reduced at low temperatures. Therefore care must be taken in case the application is located in an environment of low ambient temperatures. For example, this could be the case for Telecom Base station equipment.

Violating the maximum applicable $V_{DS}$ voltage will lead to MOSFET junction breakdown and without any current or power limiting scheme the MOSFET will face thermal destruction.

So far the various limit-lines in the SOA diagram have been discussed. The datasheet typically provides the SOA diagram for $T_c$=25°C, $T_{jmax}$=150°C and various single pulse lengths. Now recalculation of the SOA diagram is possible to adapt to application conditions different from datasheet conditions.

# 3.0 Choosing the right MOSFET for linear mode operation

As discussed in section 1 linear mode operation will operate the MOSFET at high $V_{DS}$ and $I_{DS}$ simultaneously. Consequently, power dissipation will be high. The SOA diagram is a tool to evaluate the suitability of the MOSFET operation in linear mode. In section 2 the various limit-lines of the SOA have been discussed and formulas have been presented that allow for recalculation of the SOA diagram for various application conditions. These equations also enable the deduction of some general rules for selecting the best suited MOSFET for linear mode operation. At first it is important to understand whether the MOSFET will be operated continuously in linear mode (e.g. current source) or the MOSFET passes the linear mode operation region for a period of time before it is fully turned on.

- *Continuous operation in linear mode*
  In case of continuous operation in linear mode the MOSFET's $R_{DS(on)}$ and dynamic parameters are irrelevant to judge power dissipation but the SOA is the key design criterium to the power engineer. Thermal design is most important and therefore MOSFETS with low $Z_{thJC}$ are most suitable. To remove the generated heat an appropriate package and cooling concept must be applied. Thermal instability can be avoided by utilizing MOSFETs with low ZTC point. This means that MOSFETs of previous technology generations and/or higher voltage classes will be more suitable for this kind of application.

- *Limited operation time in linear mode*
  The MOSFET will pass the linear mode operation region for a given period of time. The applied $V_{DS}$ voltage, the $I_{DS}$ current and the pulse length must be known to understand if the MOSFET can handle the generated power. It has to be verified that the MOSFET is being operated within the SOA. If the application conditions differ from the SOA datasheet conditions ($T_c$ temperature, $V_{GS}$ voltage, duty cycle …) the SOA diagram needs to be recalculated according to the formulas given in section 2. Generally, a MOSFET with low $Z_{thJC}$ and very low $R_{DS(on)}$ will be a suitable product in cases where linear mode operation ruggedness is needed.

# 4.0 Summary

The application note has shown that the safe operation area (SOA) of MOSFETs is an important design criterion. Especially, when the MOSFET is in linear mode operation the SOA diagram has to be considered. This can be either in applications where the MOSFET is being operated continuously in linear mode (e.g. MOSFET as current source) or in applications where the MOSFET passes through linear mode operation for a certain time (e.g. e-fuse). The SOA diagram in datasheets is only valid for the given conditions. For different application conditions a derating to the SOA has to be performed as discussed here.

## References

[1] BSC010NE2LS OptiMOS™ PowerMOSFET data sheet; www.infineon.com

[2] Infineon Technologies AG: Application of OptiMOS™ Linear FET as protection switch in batterypowered motor drive applications, Application Note (V 1.0); 2022-08; www.infineon.com

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