TRENCHSTOP™ 5 for SMPS

Fast IGBT optimized for switch mode power supplies

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Application Note

About this document

Scope and purpose

Historically, fast IGBTs were proposed as a replacement for conventional or Superjunction MOSFETs due to higher power levels. Because of technological limitations, IGBTs are best suited in applications featuring switching frequencies below 40 kHz.

The new TRENCHSTOP™ 5 IGBT overcomes many of the technical limitations, providing an interesting solution for highspeed applications, particularly PFC and LLC/ZVS stages typically found in SMPS.

After providing a brief introduction of the new product and technology platform, the document is structured into two core parts. One is dedicated to PFC topology and the second to LLC and ZVS stages, providing measurements and evaluation of basics and principle figures of merit.

Intended audience

This application note intends to provide information on the capabilities of the new IGBT to designers familiar with MOSFETs and advices on how to integrate the new TRENCHSTOP™ 5 IGBT into high speed applications.

Table of contents

1 Product family and MOS-like electrical features

The TRENCHSTOP™ 5 technology derives from an optimization of the Infineon Trench Field Stop or TRENCHSTOP™ concept combining Trench Gate and Field Stop structure. The new technology platform is called TRENCHSTOP™ 5. Different optimizations of the technology have been carried out in order to meet different application requirements.

This application note focuses on the description and operation mode of products, deriving from the above mentioned technology platforms, explicitly designed to address fast switching SMPS circuit topologies. Within the development of the new technology, two different device versions have been released called HighSpeed 5 (H5) and the HighSpeed 5 FAST (F5).

The H5 version is characterized by an optimized Field Stop design, providing smooth and soft switching performance. This allows the plug-and-play replacement of planar or Superjunction MOSFETs present nowadays in SMPS without any special need for board redesign or adaptation. It provides a moderate voltage rise during hard commutation at turn-off even with low gate resistor values and very high current change rates.

The F5 version is a solution with even higher performance. An optimized gate resistor value selection is required to limit voltage overshoots. Nevertheless, the F5 version provides a significant gain in efficiency over the entire load range especially if the board design has low stray inductance.

To understand the difference between the H5 and F5 versions, turn-off switching waveforms are illustrated in Figure 1for a 40 A device. Both versions show a similar voltage rise in the initial part of the turn-off before the current starts to decrease.

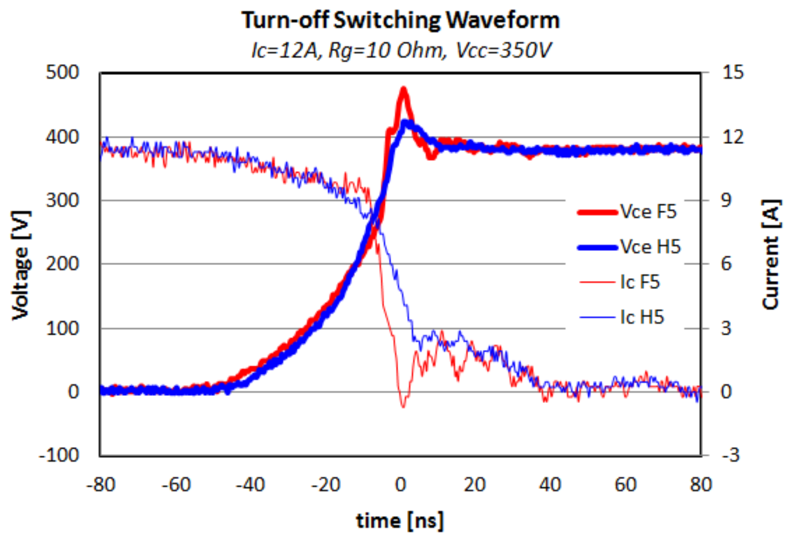

Figure 1 Current and voltage waveforms in hard switching turn-off for the H5 and F5 versions of the 40 A device. The waveforms are captured at 2 kW output power of a H4 hard switching converter developed within Infineon

The F5 version shows higher dI/dt compared to the H5 version. This results in a higher voltage overshoot defined by $L_S \cdot dI/dt$ across the parasitic stray inductance L_S of the commutation loop. Up to 10 A collector current, the voltage spike is well below 80% of the rated breakdown voltage.

TRENCHSTOP™ 5 is available in a variety of current classes in TO-220, TO-220 FullPAK and TO-247 3pin and TO-247 4pin packages, where the current rating is specified at 100°C case temperature. It is offered as a single IGBT or duopacked with a fast recovery freewheeling Diode. Details of the portfolio can be found on www.infineon.com/trenchstop5.

1.1 TRENCHSTOP™ 5 MOS-like electrical features

This section will guide the reader through a comparison between the TRENCHSTOP™ 5 H5 and F5 versions and Infineon's CoolMOS™ C6 and CFD2. Both, static and dynamic characterization data is analyzed.

1.2 Datasheet comparison with CoolMOS™

Table 1 provides a datasheet comparison between the 40 A H5 and F5 versions of the IGBT and the CoolMOS™ C6 and CFD2 Superjunction MOSFETs.

Based on the $R_{CE(on)}$ definition, computed as voltage over current at half the nominal current, both IKW40N65H5 and IKW40N65F5 can be compared to a 70 mΩ CoolMOS™ device.

Table 1 Table 1: Key performance parameter comparison between TRENCHSTOP™ 5 and Infineon's C6 and CFD2 CoolMOS™ technology

Parameter[1]	IPW65R070C6	IPW65R080CFD	IKW40N65H5	IKW40N65F5	Unit
$R_{DS(on)}/R_{CE(on)max}$[2] @T_C=25°C	70	72	66	66	mΩ
$I_{c(max)}$ @ T_C=100°C	33.8	27.4	46.0	46.0	A
$I_{D,pulse}$ @ 25°C	150	137	120	120	A
$Q_{g(typ)}$	170	170	95	95	nC
C_{iss}/C_{ies}	3900	5030	2500	2500	pF
C_{oss}/C_{oes}	215	215	50	50	pF
Q_{rr}	19	1	0.4	0.4	µC
t_{rr}	730	180	120	122	ns
I_{rrm}	50	10	3.0	2.8	A

1) Values to be considered under datasheet's measurement conditions.

2) Based on application tests results.

Particular focus should be placed for improved figures such as $Q_{g(typ)}$, C_{ies}, C_{oes} and the large improvement of Diode parameters. Due to an optimized gate structure, the Q_g of the TRENCHSTOP™ 5 IGBT is very low compared to C6 and CFD2. This reduces driving losses resulting in improved efficiency especially at partial load. Moreover, it is possible to use low cost Gate Drivers. For the anti-parallel Diode, a low Q_{rr} compared to CFD2 gives higher ruggedness and improved reliability especially in resonant applications such as LLC and phase shift ZVS. This is achieved through the use of an anti-parallel fast Diode in duopack configuration.

1.3 Robust duopack Diode

In order to provide a visible advantage of the duopack Diode robustness, diode switching tests were carried out in a standard double pulse commutation platform. Results are visible in Figure 2. A non-integrated duopack Diode provides the lowest t_{rr} compared to an optimized and integrated Superjunction MOSFET's body Diode, like in the case of Infineon's CFD2 family, or to a standard Superjunction MOSFET, for example C6. Also to be noticed is the higher softness that results in withstanding higher dI/dt transients for a duopack Diode.

Thus, this feature for TRENCHSTOP™ 5 reduces the risk of Diode hard commutation providing a higher level of reliability even if compared to optimized body Diode Superjunction MOSFETs.

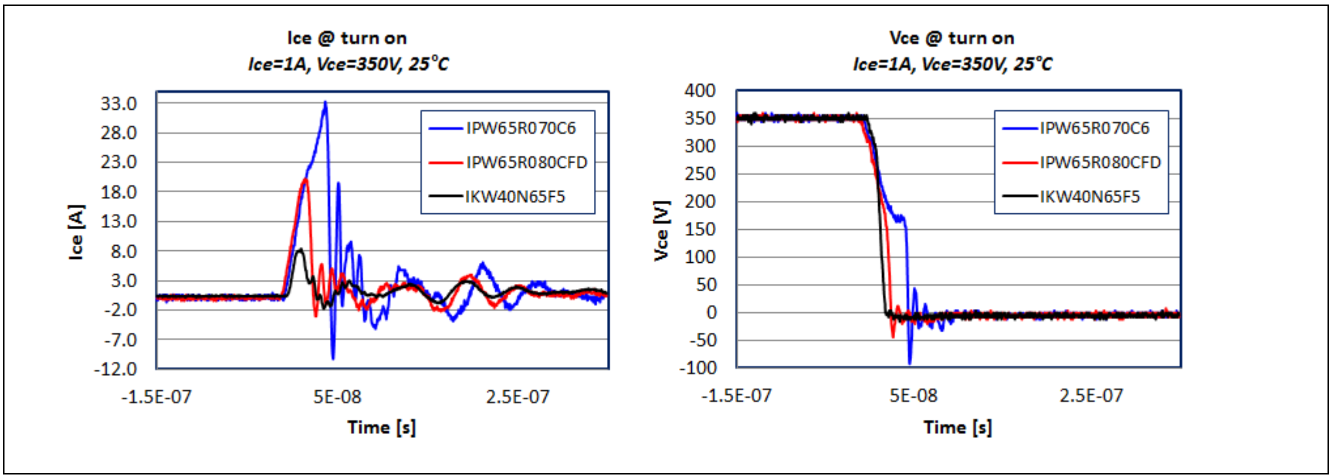

Figure 2 Current, left side, and voltage, right side, switching waveforms for the TRENCHSTOP™ 5 anti-parallel duopack Diode and Superjunction MOSFET body Diode

1.4 IGBT breakdown voltage over junction temperature

The IGBT has a high breakdown voltage, visible in the left side of Figure 3, over a wide temperature range, where 650 V as a related value is specified at 25°C junction temperature.

The right hand side of Figure 3 depicts the IGBT transfer characteristic curve characterized by a very high transconductance. Despite the gate-emitter threshold voltage $V_{GE(th)}$ set at 4 V against typical ~3 V for MOSFETs, at V_{GE}= 8 V the IGBT already conducts twice the nominal current, hence it can be safely driven even at 8-10 V gate voltage without entering linear mode operation.

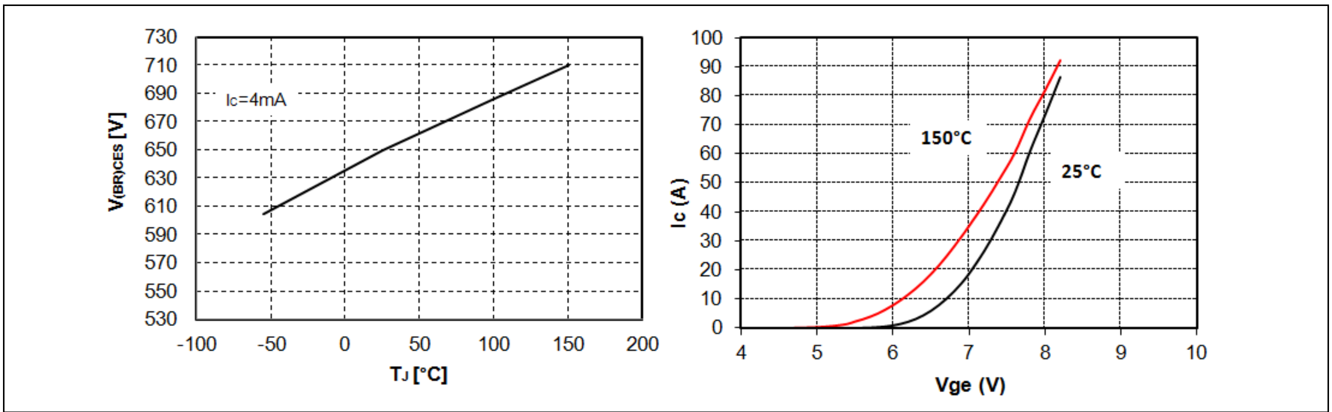

Figure 3 Left side TRENCHSTOP™ 5 blocking characteristic as a function of temperature, right side 40 A TRENCHSTOP™ 5 transfer characteristics

2 Switch mode power supply application test

The purpose of this section is to illustrate to the SMPS designer how to integrate the TRENCHSTOP™ 5 IGBT into the application. It is highlighting pros and cons of the proposed solution compared to standard and Superjunction MOSFETs. The value proposition of the new IGBT is explored through extensive application tests in both hard and resonant-switching topologies typically used for input PFC and high voltage DC to DC stages found in commercial SMPS.

2.1 PFC in DCM and CCM operation

To verify the behavior of the new TRENCHSTOP™ 5 at partial load, a 40 A TRENCHSTOP™ 5 IGBT IKW40N65F5 is compared to the CoolMOS™ C6 with comparable $R_{DS(on)}$ – rating of approximately 70 mΩ and the previous IGBT generation HighSpeed 3. A 500 W PFC test board is used. Results are summarized in Figure 4.

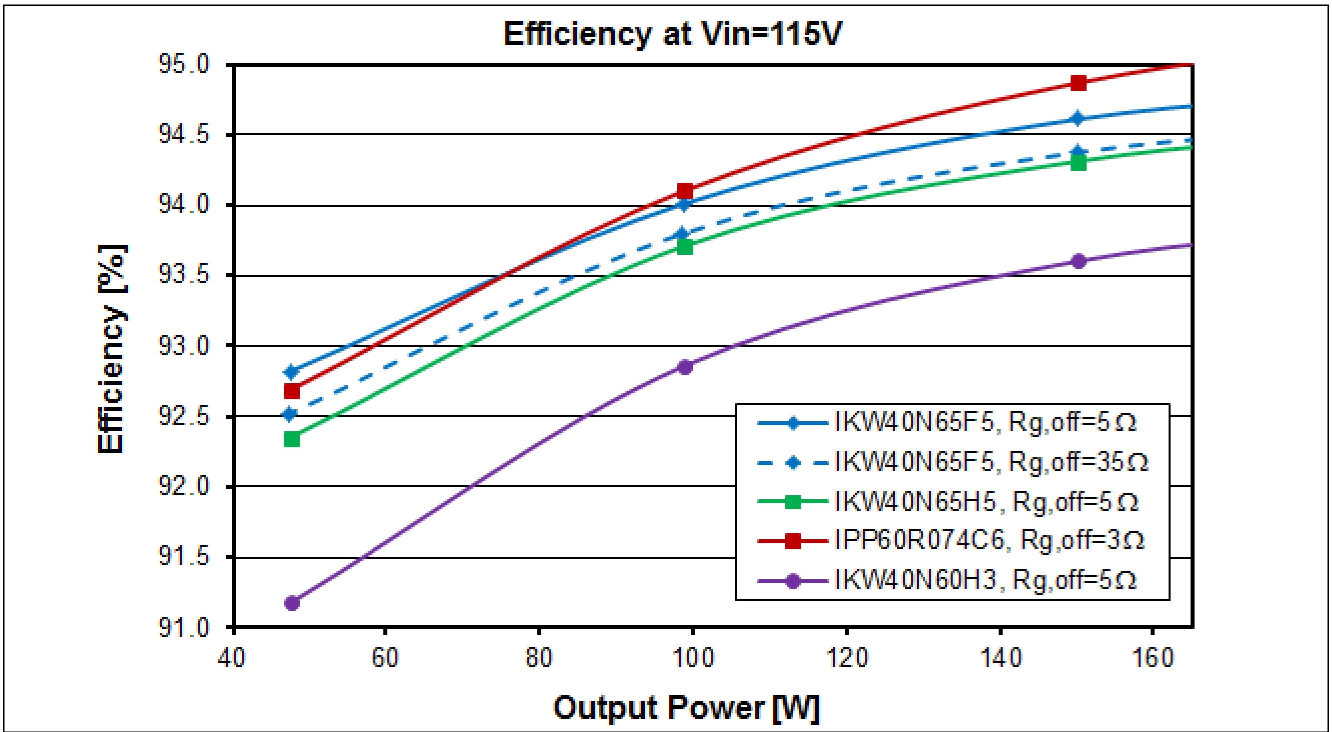

Figure 4 System efficiency versus partial load of a 500 W PFC, comparing TRENCHSTOP™ 5 IGBT and CoolMOS™ C6 used as a boost switch. All devices were measured with $R_{G(on)}$= 1.5 Ω

To minimize turn-on losses, $R_{G(on)}$ is set to 1.5 Ω for all devices tested, while $R_{G(off)}$ – values are individually selected in order to keep the transient voltage below 80% of $V_{BR(CES)}$ in all operating conditions. Gate resistor selection is discussed in the next section.

Thanks to the conduction-loss and switching-loss reduction, the TRENCHSTOP™ 5 IGBT provides a 1.3% efficiency improvement compared to HighSpeed 3 IGBT of Infineon. Additionally, due to very low C_{oss} and E_{oss} values, the device has comparable efficiency value as a CoolMOS™ C6 at 5 to 10% load range, 50~100 W, where the PFC mainly works in Discontinuous Current Mode (DCM).

2.1.1 Gate resistor selection

The functionality of the IGBT in normal and abnormal operating conditions was verified by several tests performed on commercial units as well as internal test boards. Tests conducted included events like brown-out, dynamic load-jump, in-rush current and short circuit. The main outcome is that the TRENCHSTOP™ 5 IGBT survives these tests without failing or triggering failures within the SMPS.

Figure 5depicts the results of the Line Cycle Drop Out (LCDO) test performed on the PFC test board and provides an example of $R_{G(off)}$ optimization. In this test, the input line is interrupted for 20 ms causing a decrease of 100 V on the DC-link capacitor, discharging from 400 V to 300 V. The peak current reaches 50 A in this case, generating the highest overvoltage peak. The peak current is reduced, once the DC capacitor is charged back to 400 V after a few cycles.

On the right side of the maximum transient voltage across the device as a function of $R_{G(off)}$ for different combinations of boost switch and Diode are given. Either 8 A ultrafast Rapid 2 Si Diodes or SiC Schottky Diodes from Infineon were used in the test circuit as boost Diode. The F5 version combined with the Rapid 2 ultrafast silicon Diode gave the highest overvoltage amplitude during turn-off; however by using the H5 version instead, the overshoot was drastically reduced. When a SiC Schottky boost Diode is used, the voltage peak is dampened significantly for both F5 and H5 versions.

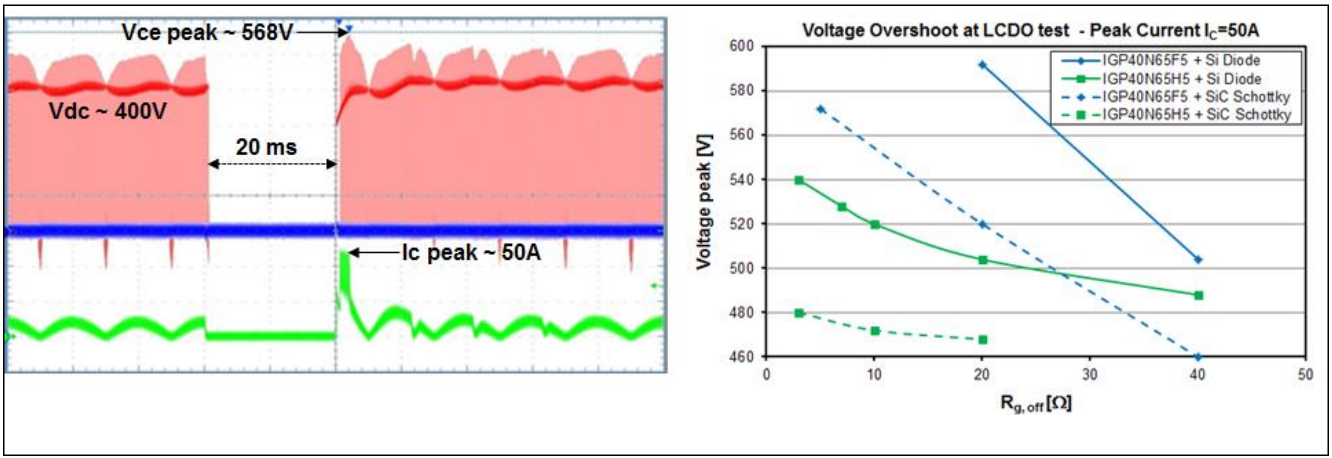

Figure 5 Line cycle drop out test in PFC. Current and voltage waveforms to the left, voltage overshoot at turn-off for different configurations to the right.

It can be concluded from the PFC measurements, that the H5 is best used in combination with a Si Diode, offering an excellent cost performance ratio. For higher performance, the F5 can be used in combination with a SiC boost Diode.

The voltage overshoot can be further reduced by increasing the equivalent capacitance at the collector node by introducing an anti-parallel Diode and eventually a decoupling capacitor in the commutation loop.

The H5 version is designed as a plug-and-play, ease of use device with softer switching behavior and the gate resistor selection is less critical. As a result, it is possible to take a single turn-on/-off gate resistor of 5 Ω, and meet the voltage overshoot specification.

Due to the very high dV/dt of the F5 version, the driver stage should be equipped with split $R_{G(on)}$ / $R_{G(off)}$ to maximize efficiency and to control the voltage overshoot at turn-off in correspondence to high load currents. With an optimized layout in terms of stray inductance, it is possible to use a lower $R_{G(off)}$.

2.1.2 Anti-parallel duopack Diode and its effect on partial load efficiency

Figure 6provides current and voltage measured during PFC-operation in a system equipped with IKW40N65H5, duopack, and IGW40N65H5, single IGBT. As it can be seen, when the PFC enters into DCM operation and the current goes to zero, the anti-parallel Diode conducts a reverse current across the device having a reverse V_{CE}. Without the anti-parallel Diode, a reverse voltage with a maximum measured value of 192 V is present across the IGBT. This operation is not recommended as it would generate additional losses, thus a worsening in efficiency especially at partial load. The anti-parallel Diode guarantees safe operation and increased robustness.

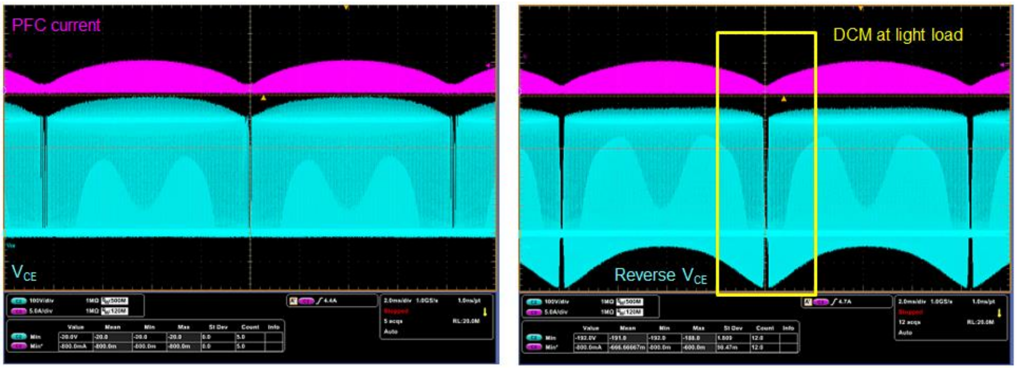

Figure 6 Current and voltage waveforms equipped with anti-parallel Diode and right side without anti-parallel Diode, $V_{CE, min}$=-192 V, voltage and current waveforms during PFC operation. P_{out}=170 W.

2.1.3 Device selection to meet efficiency target

Figure 7shows a PFC efficiency comparison for different combinations of IGBT and boost Diodes, with $R_{G(off)}$ values selected to not exceed 520 V, 80% safety margin from 650 V at the LCDO.

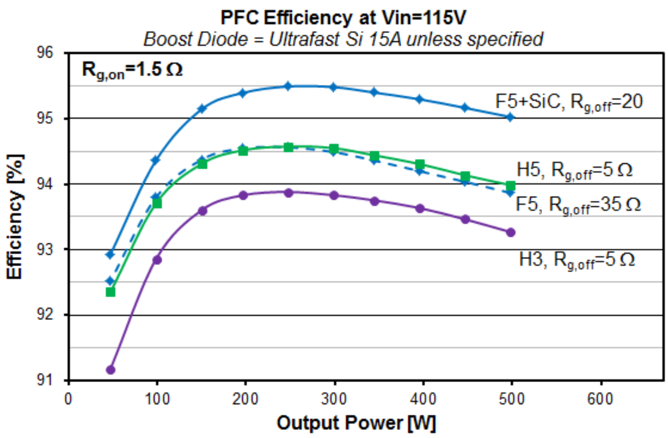

Figure 7 Effect of $R_{G(off)}$ and boost Diode on PFC efficiency, PFC switching frequency = 70 kHz.

The results indicate that for a plug-and-play approach, the H5 series with low $R_{G(on)}$=$R_{G(off)}$ paired with an ultrafast silicon boost Diode is the best fit. For higher efficiency targets, the F5 series with split $R_{G(on)}$ / $R_{G(off)}$ in combination with a SiC Schottky boost Diode provides the optimum combination. In this case, the SiC Diode allows the use of a lower $R_{G(off)}$ value of 20 Ω compared to 35 Ω if a silicon ultrafast Diode is used, hence achieving the highest efficiency. For the same reason, this combination is also the best fit for designs with low stray inductance in the commutation loop and / or low inductance packages, as in this case lower voltage overshoots at turn-off would be achieved even with low $R_{G(off)}$.

2.2 DC-DC in ZVS and LLC operation

The purpose of this chapter is to give the designer an overview of the pro and cons that TRENCHSTOP™ 5 provide when used in resonant converters compared to optimized body Diode Superjunction MOSFETs like Infineon's CoolMOS™ CFD2 technology.

Tests and evaluations were carried out on Infineon's in-house ZVS phase-shift full bridge evaluation boards. It is possible to find a detailed description of the application circuit topology and operation in the Infineon application note "ZVS PHASE SHIFT FULL BRIDGE, CFD2 OPTIMIZED DESIGN" [1].

The application test outcome is that there are three main parameters, which make the TRENCHSTOP™ 5 attractive for ZVS topologies: the low Q_G, the minimal Q_{oss} and the available duopack configuration with anti-parallel fast Diode - a separate section is fully dedicated to this last topic (section 2.2.1).

A low Q_{oss} value allows for ZVS in correspondence of low load currents causing partial load efficiency improvement and providing turn-on and turn-off losses optimization over the entire power range.

Figure 8 shows partial load efficiency for both IKW40N65F5 and CoolMOS™ CFD2, IPW65R080CFD.

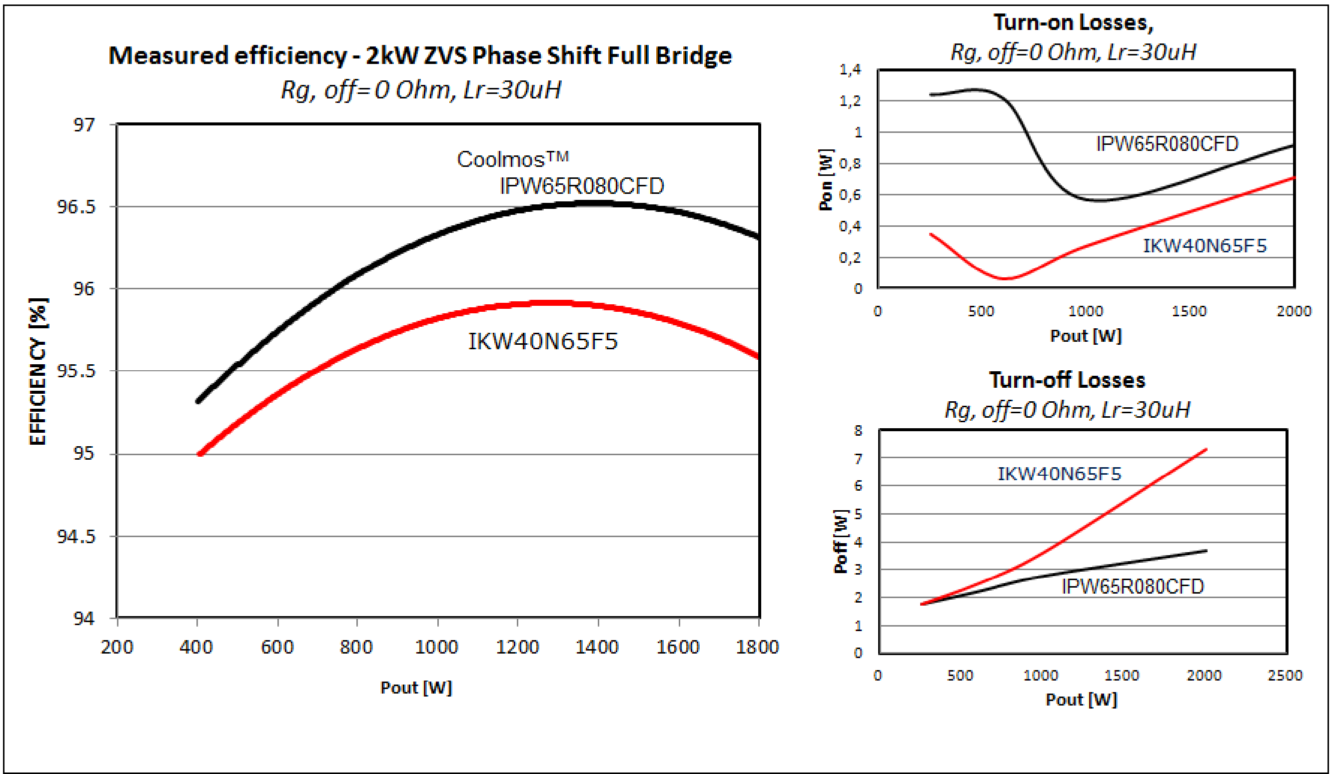

Figure 8 Efficiency and switching losses in ZVS as a function of the output power measured on Infineon's in-house ZVS phase-shift full-bridge evaluation boards

The gap in efficiency of about 0.5% maximum can be explained by the turn-on and turn-off losses shown on the right hand side. Turn-on losses are actually improved compared to Superjunction MOSFET due to lower Q_G; however the IGBT limitation is in the turn-off losses, basically due to the tail current. It is nevertheless important to underline that the contribution of these two factors provides significant efficiency improvement at partial load compared to previous IGBT generations.

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Similar results were observed by comparing the TRENCHSTOP™ 5 and the Superjunction MOSFETs in the DC-DC stage of a 300 W Platinum Silver Box internally developed as an evaluation design. Figure 9shows the efficiency curves for the overall SMPS system. For this measurement, a Superjunction MOSFET was used in the PFC stage and three different solutions were adopted for the LLC stage in order to provide a comparison of the device performances.

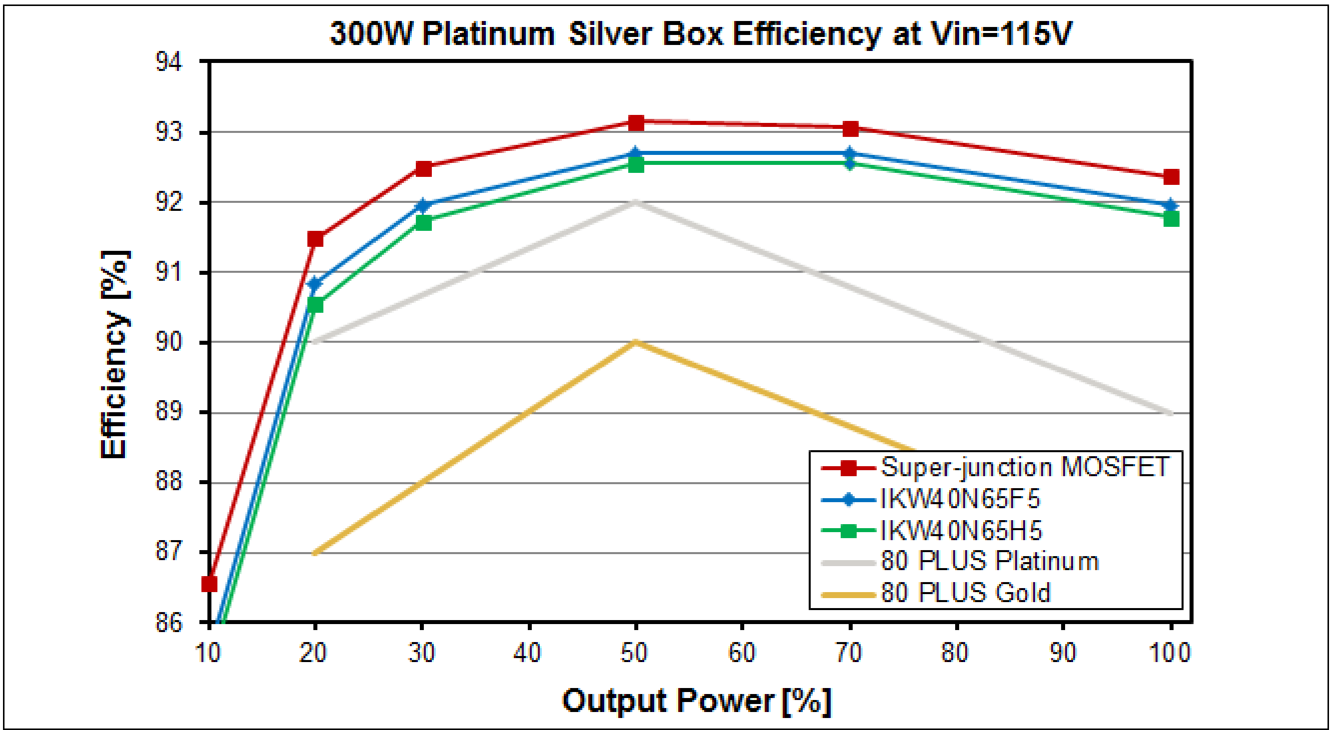

Figure 9 SMPS System efficiency. The device in the PFC stage is a standard Superjunction MOSFET and R_G = 5 Ω for all three solutions, it provides LLC efficiency evaluation for the three different devices selected

Using the TRENCHSTOP™ 5 results in lower efficiency compared to a Superjunction MOSFET solution in LLC topologies. There are two main reasons for this decrease in efficiency.

The first reason is found in the conduction losses at low currents. IGBTs in general are characterized by the knee voltage, due to the IGBT being a bipolar device, which causes higher conduction losses compared to MOSFETs at low currents. Thus, its effect is visible at partial load condition, where the TRENCHSTOP™ 5 provides 0.75% to 1% lower efficiency than the SJ-MOSFET.

The second reason is added losses coming from the anti-parallel Diode. The Rapid Diode duopack in the IKW40N65F5/H5 is characterized by higher V_F during conduction compared to the Superjunction MOSFET's body Diode.

However, it must by noted, that the IGBT performs extremely well in the LLC stage and can match the platinum efficiency standard, while at the same time it offers a highly robust anti-parallel Diode.

2.2.1 Impact of the reverse conducting Diode robustness

In ZVS and LLC applications, the reverse conducting Diode plays a role in terms of efficiency, performance and device failure due to its robustness.

During zero voltage switching turn-on, the devices placed on the full or half-bridge face a short time frame of reverse conduction, so current is flowing from the source to the drain and at the same time through the body Diode of the MOSFET, dictated by the circuit and topology characteristics. In the case of an IGBT solution, this current is flowing only on the duopack Diode. This causes losses that are highly dependent on forward voltage and frequency. This effect is visible on the overall efficiency plot, resulting in a gap on performance compared to Superjunction MOSFETs.

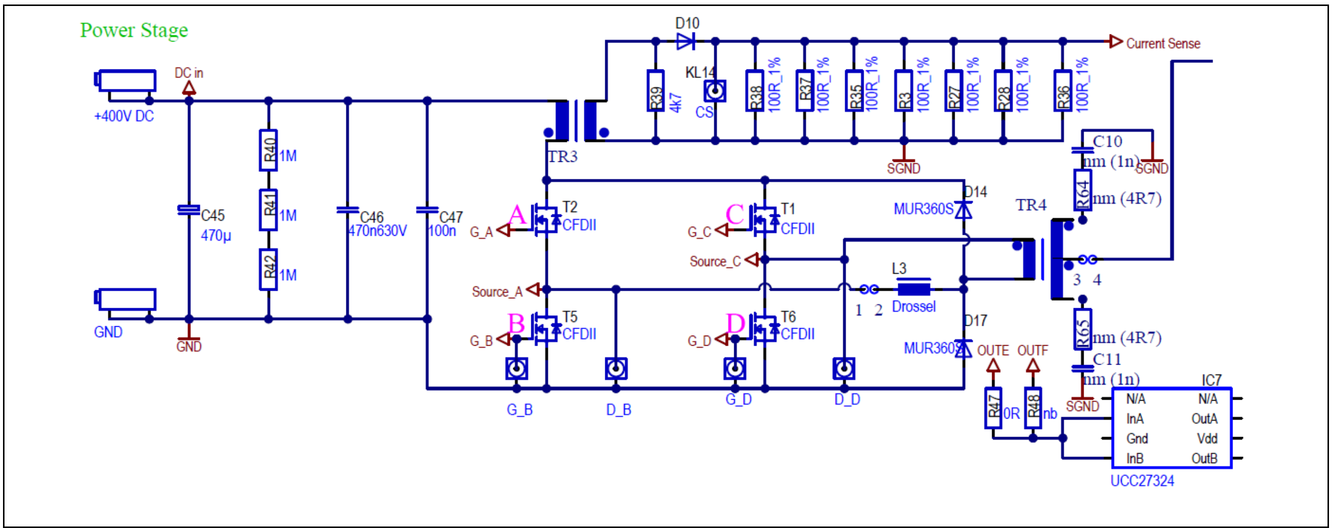

Figure 10 ZVS phase shift full-bridge circuit topology

On the other hand, as historically proven, there is the need for a fast body Diode, with reduced Q_{rr} and t_{rr} in order to have less minority carriers during body Diode reverse recovery. During the device's turn-on, the anti-parallel or body Diode is flooded with minority carriers which need to be removed. If there still is a significant amount of minority carriers at device turn-off, there is a high risk of current shoot-through in the half-bridge and increased Diode stress with high dV/dt and dI/dt. Moreover, in this condition the device is not able to fully block the voltage causing possible dynamic avalanche within the transistor. These operating conditions exist in start-up, burst mode, current limiting and output short circuit [2].

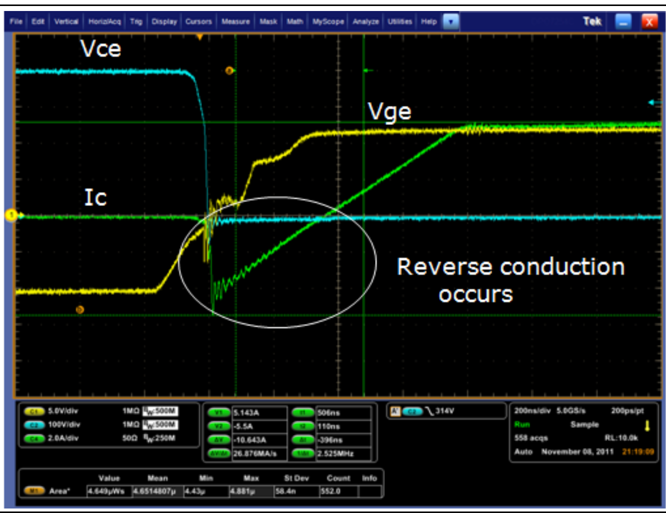

Figure 11 IKW40N65F5 turn-on leg b in ZVS phase shift full bridge at P_{out}=1 kW and L_{LOAD}=30 uH; $R_{G(on)}$=2.7 Ω

3 Portfolio

TRENCHSTOP™ 5 IGBT product naming includes the device type where G is used for single IGBT and K for duopack, package type, the IGBTs nominal current at 100°C case temperature in ampere, the voltage class in volt, divided by 10 and IGBT optimization where H5 represents HighSpeed 5 and F5 the HighSpeed 5 FAST. Figure 12 presents the portfolio of the 650 V TRENCHSTOP™ 5 IGBT.

Continuous Collector Current @ T_c=100°C		TO-220	TO-220 FullPAK	TO-247
Single IGBT	20A	IGP20N65F5		
Single IGBT	20A	IGP20N65H5		
Single IGBT	30A	IGP30N65F5		
Single IGBT	30A	IGP30N65H5		
Single IGBT	40A	IGP40N65F5		IGW40N65F5
Single IGBT	40A	IGP40N65H5		IGW40N65H5
Single IGBT	50A			IGW50N65F5
Single IGBT	50A			IGW50N65H5
Single IGBT	75A			IGW75N65H5
DuoPack	8A	IKP08N65F5	IKA08N65F5	
DuoPack	8A	IKP08N65H5	IKA08N65H5	
DuoPack	15A	IKP15N65F5	IKA15N65F5	
DuoPack	15A	IKP15N65H5	IKA15N65H5	
DuoPack	20A	IKP20N65F5		
DuoPack	20A	IKP20N65H5		
DuoPack	30A	IKP30N65F5		
DuoPack	30A	IKP30N65H5		IKW30N65H5
DuoPack	40A	IKP40N65F5		IKW40N65F5
DuoPack	40A	IKP40N65H5		IKW40N65H5
DuoPack	50A			IKW50N65F5
DuoPack	50A			IKW50N65H5

Figure 12 Portfolio of 650 V TRENCHSTOP™ 5 IGBT

4 Summary

The TRENCHSTOP™ 5 technology provides a high performance solution for SMPS application, thanks to many electrical feature improvements, such as lower switching and capacitive losses, low Q_G and fast anti-parallel Diode. Due to the IGBTs higher power density, thanks to the bipolar structure, the IGBT offers a cost optimized alternative to MOSFETs. This advantage is more pronounced in high power application utilizing typically low $R_{DS(on)}$ FETs. In this category, the IGBT provides especially high efficiency at high input voltages. In lower power range applications, the IGBT is a good fit when the design has higher margin to target efficiency specifications.

This application note guided the reader in designing-in the IGBT into typical SMPS topologies, such as PFC and LLC/ZVS in order to achieve higher efficiency and better performances out of the circuit design evaluation and optimization.

The commutation behavior of the TRENCHSTOP™ 5 in both soft and hard switching conditions is verified by several application tests in normal and abnormal circuit operation. Particular focus was set to comparing the new IGBT to best in class and optimized Superjunction MOSFETs nowadays commonly used in these applications.

5 References

[1] F. Di Domenico, R. Mente: “ZVS phase shift full-bridge, CFD2 optimized design”, Infineon Technologies 2011.

[2] H. Aigner, K. Dierberg, D. Grafham: “Improving the full-bridge phase shift ZVT converter for failure-free operation under extreme condition in welding and similar applications”, IAS 98 St. Louis 1998.

Revision History

Major changes since the last revision

Page or Reference	Description of change
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