EiceDRIVER™ 1EDNx550 high-side and low-side non-isolated gate driver IC

Application examples and layout guidelines

About this document

Scope and purpose

This document describes applications and design guidelines for the EiceDRIVER™ 1EDNx550 family of non-isolated gate drivers with Truly Differential Inputs (TDI). The TDI input stage provides excellent Common-Mode Robustness (CMR) and eliminates the risk of false triggering. As a result, the EiceDRIVER™ 1EDNx550 is suitable for:

- Four-pin Kelvin-source MOSFETs in boost PFCs
- Low-side driving in scenarios with high PCB parasitic inductances (e.g., control system and power system placed on different PCBs)
- High-side and low-side driving in half-bridges with no isolation requirements
- Driving superjunction and SiC MOSFETs, GaN HEMTs

Chapter 1 introduces EiceDRIVER™ 1EDNx550 and the guidelines to select the proper input resistor value, tolerance and form factors to configure the CMR. Chapter 2 describes the target applications of the EiceDRIVER™ 1EDNx550 and shows some practical examples of its use. Chapter 3 describes PCB layout effects on the CMR and provides reference layouts to achieve optimal performance.

Intended audience

This document is targeted at design engineers, application engineers and component verification engineers who wish to evaluate SMPS performance using EiceDRIVER™ 1EDNx550. The aim of this application note is to provide layout guidelines and application examples.
## Table of contents

**About this document** .................................................................................................................. 1  
**Table of contents** ....................................................................................................................... 2  
1  **Introduction** ............................................................................................................................... 3  
1.1  Input resistor dimensioning ........................................................................................................ 5  
2  **Typical applications** ................................................................................................................. 6  
2.1  Driving four-pin Kelvin-source MOSFETs in boost PFCs ......................................................... 6  
2.2  Driving MOSFETs with high PCB parasitic inductance ............................................................. 8  
2.3  Driving half-bridges or high-side switches ............................................................................... 9  
3  **PCB layout considerations and guidelines** ............................................................................. 11  
3.1  Effect of PCB parasitics on TDI input stage ............................................................................. 11  
3.1.1  Typical configuration of EiceDRIVER™ 1EDNx550 .............................................................. 11  
3.1.2  Full TDI input stage circuit model including PCB parasitics ............................................. 11  
3.1.3  Effect of input PCB parasitic capacitances $C_{P+}$ and $C_{P-}$ ................................................ 13  
3.2  Common layout issues with EiceDRIVER™ 1EDNx550 .......................................................... 16  
3.3  Layout guidelines ..................................................................................................................... 17  
4  **List of abbreviations** ................................................................................................................. 19  
5  **References** .................................................................................................................................. 20  
**Revision history** ........................................................................................................................... 21
1 Introduction

The output state of a gate driver IC is determined by the PWM input voltage $V_{IN}$, with respect to its input logic thresholds. For instance, for a conventional gate driver IC with TTL inputs, the input logic thresholds are:

- $V_{IN_{LH}} = 2 \text{ V} \rightarrow$ TTL on-state for $V_{IN} \geq V_{IN_{LH}}$
- $V_{IN_{HL}} = 0.8 \text{ V} \rightarrow$ TTL off-state for $V_{IN} \leq V_{IN_{HL}}$

where the control PWM signal $V_{IN}$ is single-ended and referenced to system ground, as shown in Figure 1.

If high $di/dt$ transients and relatively high parasitic series inductance (e.g., long PCB traces) are present in the ground loop, having a single-ended PWM input signal can affect the correct operation of the driver. Indeed, even if the driver and the controller ground potentials are theoretically the same (i.e., the same net on the PCB), $di/dt$ transients on the ground parasitic inductance can generate voltage shifts between the ground pins of the driver and the controller. This affects the ground reference potential, and consequently the input thresholds and the interpretation of the $V_{IN}$ input signal, leading to unpredictable behavior of the output and impacting the overall system reliability.

The EiceDRIVER™ 1EDNx550 gate driver IC is designed to handle this problem (see Figure 1) as the Truly Differential Input (TDI) stage is driven by the differential PWM signal $\Delta V_{IN}$ between the input pins $IN+ \text{ and } IN-$ independent of the ground potential. The input state detection is then independent of the driver ground, and consequently the output state is immune to any voltage shift between the driver and the controller ground pins. Ground shifts up to $\pm 200 \text{ V DC}$ and $\pm 400 \text{ V AC}$ can be achieved with EiceDRIVER™ 1EDNx550.

Figure 1 Conventional non-isolated gate driver IC vs. EiceDRIVER™ 1EDNx550 with TDI input stage

Figure 2 shows a typical connection, where the $IN-$ pin is connected to the controller GND (net $IN_\text{n}$) via the input resistor $R_{IN-}$, and the $IN+$ pin is connected to controller PWM output (net $IN_\text{p}$) via the input resistor $R_{IN+}$. The two input resistors $R_{IN-}$ and $R_{IN+}$ are mandatory for proper operation of the EiceDRIVER™ 1EDNx550, as they enable rejection of the common-mode voltage and scale the PWM voltage as shown in Figure 3.

Figure 2 Schematic example of EiceDRIVER™ 1EDNx550
Introduction

The choice of the input resistors $R_{IN+}$ and $R_{IN-}$ can be made according to Section 1.1.

![Diagram of EiceDRIVER™ 1EDNx550 gate driver IC](image)

**Figure 3** TDI input stage of the EiceDRIVER™ 1EDNx550 gate driver IC

EiceDRIVER™ 1EDNx550 offers a hysteresis window of 0.2 V for the input voltage $\Delta V_{Rin}$ between the nets $IN_+$ and $IN_-$, and the operating input thresholds for the TDI driver are:

- $\Delta V_{Rin,\text{LH}} = 1.7 \text{ V} \rightarrow$ TDI on-state for $\Delta V_{Rin} \geq \Delta V_{Rin,\text{LH}}$
- $\Delta V_{Rin,\text{HL}} = 1.5 \text{ V} \rightarrow$ TDI off-state for $\Delta V_{Rin} \leq \Delta V_{Rin,\text{HL}}$

The capability of the EiceDRIVER™ 1EDNx550 to withstand AC ground shifts is shown in **Figure 4**. An Infineon evaluation board generating AC ground shifts up to 108 V has been used to test the driver.

![Waveforms showing the AC ground shift robustness of the EiceDRIVER™ 1EDNx550](image)

**Figure 4** Waveforms showing the AC ground shift robustness of the EiceDRIVER™ 1EDNx550;
Red: AC voltage shift between the driver ground and the controller ground
Green: PWM input signal $\Delta V_{Rin}$
Blue: Gate driver output signal
Introduction

1.1 Input resistor dimensioning

The Common-Mode Robustness (CMR) shall be configured using Table 1. Depending on the controller PWM voltage $V_{\text{Rin}}$ and the required ground shift robustness, the following three parameters have to be chosen for $R_{\text{IN}+}$ and $R_{\text{IN}-}$:

- Resistance value
- Tolerance
- Form factor

First identify the PWM voltage in high state (usually equal to the controller supply voltage $V_{\text{DD}}$ or the I/O bank reference voltage), then estimate the highest static and dynamic common-mode shifts expected in the application, and eventually the three parameters above can be chosen for $R_{\text{IN}+}$ and $R_{\text{IN}-}$.

**Table 1**: Input resistor configuration look-up table

<table>
<thead>
<tr>
<th>Controller PWM output voltage</th>
<th>$R_{\text{IN}+}$ and $R_{\text{IN}-}$ configuration</th>
<th>Ground shift robustness</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Value</td>
<td>Tolerance</td>
</tr>
<tr>
<td>2.5 V</td>
<td>24 kΩ</td>
<td>1%</td>
</tr>
<tr>
<td></td>
<td>0.1%</td>
<td>≥0603</td>
</tr>
<tr>
<td>3.3 V</td>
<td>33 kΩ</td>
<td>1%</td>
</tr>
<tr>
<td></td>
<td>0.1%</td>
<td>≥0603</td>
</tr>
<tr>
<td>5 V</td>
<td>51 kΩ</td>
<td>1%</td>
</tr>
<tr>
<td></td>
<td>0.1%</td>
<td>≥0805</td>
</tr>
<tr>
<td>12 V</td>
<td>127 kΩ</td>
<td>1%</td>
</tr>
<tr>
<td></td>
<td>1%</td>
<td>≥1206</td>
</tr>
<tr>
<td></td>
<td>0.1%</td>
<td>≥1206</td>
</tr>
<tr>
<td>15 V</td>
<td>160 kΩ</td>
<td>1%</td>
</tr>
<tr>
<td></td>
<td>1%</td>
<td>≥1206</td>
</tr>
<tr>
<td></td>
<td>0.1%</td>
<td>≥1206</td>
</tr>
</tbody>
</table>

* Driver ground to system ground
** Please check PWM signal duty cycle and resistor power rating
2 Typical applications

2.1 Driving four-pin Kelvin-source MOSFETs in boost PFCs

In a typical TO-220/247 package the parasitic source inductance is in the range of \(\approx 10\) nH. This parasitic inductance is in series with the gate loop and negatively influences the performances as it increases the turn-on switching losses and causes ringing on the MOSFET source terminal. For this reason, in power supplies targeting the best-in-class efficiencies, four-pin CoolMOS™ devices are employed to minimize the parasitic source inductance on the gate driving loop. Four-pin CoolMOS™ devices have an additional Kelvin-source terminal, which is characterized by low parasitic series inductance and is used as reference source for the driving circuit.

Driving four-pin CoolMOS™ devices requires a circuit capable of handling the offset between the Kelvin-source potential and the ground voltage of the controller. The voltage shift occurs during the switching phase, when the source parasitic inductance in Figure 5 experiences an abrupt change of the drain current. The system ground voltage then resonates, creating an AC shift on the driver ground, which can affect the input PWM signal.

To overcome this ground shifting problem and drive four-pin CoolMOS™ devices, isolated gate driver ICs are commonly used. In Figure 5 this configuration is shown: GND1 is the PWM reference voltage (and the controller GND), GND2 is connected to the Kelvin-source potential. The input signal is processed by the driver primary side and proper operation of the driver is ensured by connecting the primary ground GND1 to the controller ground.

![Figure 5: Isolated gate driver IC driving a four-pin CoolMOS™](image)

However, isolated gate driver ICs are an over-specified solution to drive four-pin CoolMOS™ devices because their integrated galvanic isolation is capable of handling hundreds or even thousands of volts. EiceDRIVER™ 1EDNx550 is a smaller and cheaper alternative to galvanically isolated gate driver ICs, as it offers good enough common-mode robustness to drive four-pin CoolMOS™ devices.

A typical configuration to drive four-pin MOSFETs with EiceDRIVER™ 1EDNx550 is shown in Figure 6. The ground pin of EiceDRIVER™ 1EDNx550 is connected to the Kelvin-source terminal of the four-pin MOSFET, and the controller PWM signal and ground are connected respectively to the \(\text{IN}^+\) and \(\text{IN}^−\) pins of the driver through the input resistors \(R_{\text{IN}^+}\) and \(R_{\text{IN}^−}\). This allows the differential input stage to handle the AC ground shift generated by the switching of four-pin CoolMOS™ devices. This is also valid for any other four-pin device such as CoolSiC™ MOSFETs.
EiceDRIVER™ 1EDNx550 high-side and low-side gate driver
Application examples and layout guidelines

Typical applications

Figure 6  EiceDRIVER™ 1EDNx550 driving a four-pin CoolMOS™

In a PFC-boost application with four-pin MOSFETs, the EiceDRIVER™ 1EDNx550 is a low-cost driving solution compared to the isolated driver: it is realized with a single die, and available in smaller SOT23-6 package (2.8x2.9mm body size) compared to the SOIC8 package available for isolated drivers (5x6 mm body size).

EiceDRIVER™ 1EDNx550 driving a four-pin CoolMOS™ has been tested using the 2.5 kW PFC-boost evaluation board from Infineon EVAL_2.5KW_CCM_4PIN [3] (Figure 7).

Figure 7  EiceDRIVER™ 1EDN7550B driving a four-pin CoolMOS™ in the 2.5 kW PFC evaluation board [3]; four-pin CoolMOS™ highlighted in yellow, EiceDRIVER™ 1EDN7550B in red
2.2 Driving MOSFETs with high PCB parasitic inductance

Series parasitic inductance in the ground loop can be due to the MOSFET’s package (e.g., pin leads), the PCB (e.g., trace stray inductances, power stage and controller on different boards, etc.), or both. In these cases, a sudden change in the drain current of the MOSFET or in the ground return current can result in voltage spikes or ringings due to the ground parasitic inductance (see Figure 8). Consequently, an AC voltage difference appears between the controller ground and the gate driver ground, which can affect the PWM input signal and cause retriggering of the driver.

Figure 8 Conventional non-isolated gate driver IC in a boost stage

EiceDRIVER™ 1EDNx550 provides a robust solution in applications with high stray inductances in the ground loop. Figure 9 shows how to connect this gate driver to handle the ground shift and properly drive the MOSFET.

Figure 9 EiceDRIVER™ 1EDNx550 driving in a boost stage with high stray inductance on the PCB

The use of the EiceDRIVER™ 1EDNx550 is therefore recommended in circuits with high stray inductances on the PCB, as for example in:

1. Long PWM signal traces from the controller to the driver IC
2. Control IC and driver on different PCBs
3. Single-layer PCBs
4. Un-optimized or complex PCB layouts
5. TO-220 and TO-247 power switches with long leads
2.3 Driving half-bridges or high-side switches

The DC ground shifting capability of the EiceDRIVER™ 1EDNx550 can be also used to drive high-side switches. Considering a generic high-side driving circuit, if the voltage difference between the high-side driver ground and the respective PWM input voltage does not exceed the CMR limits configured with Table 1, the EiceDRIVER™ 1EDNx550 can drive the high-side switch.

A half-bridge use case example is shown in Figure 10. In this case, a DC offset equal to $V_{BULK}$ occurs between the ground of the high-side driver (i.e., the switching node) and the controller PWM and ground signals. As long as the $V_{BULK}$ voltage is below the configured CMR static value, driving the high-side switch is possible with the EiceDRIVER™ 1EDNx550.

According to Table 1, floating driver ground up to 84 V can be achieved with a 3.3 V PWM input signal. In case of different PWM input voltage levels, DC or AC noise ground shift robustness, the input resistors $R_{IN+}$ and $R_{IN-}$ shall be selected according to Section 1.1 and Table 1 (e.g., 126 V maximum bus voltage is possible with 5 V PWM signal; 200 V maximum bus voltage with 12 V or 15 V PWM signal).

![Figure 10](image)

**Figure 10** EiceDRIVER™ 1EDNx550-based driving of the high-side MOSFET in a half-bridge converter

Other application examples where high-side driving with EiceDRIVER™ 1EDNx550 is possible are synchronous buck converters, full-bridge converters and high-side switches in switched capacitor topologies.

In any case the maximum ground shift shall not exceed the CMR static value reported in Table 1.

The functionality of the EiceDRIVER™ 1EDNx550 as a high-side driver has been tested on the half-bridge buck converter evaluation board EVAL_HB_BC_1EDN8550B [4] with 48 V input, as shown in Figure 11. This evaluation board enables testing of the EiceDRIVER™ 1EDNx550 common-mode robustness against DC ground shifts, and different AC ground shift scenarios.
Application examples and layout guidelines

Typical applications

Figure 11  Top view of the EVAL_HB_BC_1EDN8550B buck converter evaluation board [4]; EiceDRIVER™ 1EDN8550B used to drive the half-bridge highlighted in yellow, low-side and high-side MOSFETs highlighted in red

The high-side driver capability of the EiceDRIVER™ 1EDNx550 is demonstrated by the half-bridge waveforms in Figure 12.

Figure 12  DC ground shift robustness of the EiceDRIVER™ 1EDN8550 driver in the EVAL_HB_BC_1EDN8550B evaluation board [4].
Green: low-side PWM signal; Yellow: low-side Vgs voltage
Magenta: half-bridge switching node voltage; Cyan: inductor current
3 PCB layout considerations and guidelines

The layout of a fast-switching power system has a strong influence on the overall performance and its design is critical. EiceDRIVER™ 1EDNx550 with TDI is the best solution to overcome the effects of parasitics in the ground loop; however, it requires special care while routing the input signals.

This chapter provides a comprehensive overview of the effects of PCB nonidealities on the input stage of EiceDRIVER™ 1EDNx550, together with guidelines to achieve an optimized and noise-immune layout.

3.1 Effect of PCB parasitics on TDI input stage

3.1.1 Typical configuration of EiceDRIVER™ 1EDNx550

Figure 13 shows a typical use case example where the EiceDRIVER™ 1EDNx550 drives a low-side MOSFET. The controller nodes INP and INN are assumed to be routed as a differential pair from the controller to the gate driver IC. If the routing of the PWM differential couple INP/INN is optimal, any noise source applied to the differential couple will result in a common-mode noise. This allows the PWM differential signal to be theoretically immune against any coupled noise source or ground voltage bouncing.

Figure 13 EiceDRIVER™ 1EDNx550 typical configuration with long PWM wires to drive a MOSFET

However, if the input signals INP and INN of the EiceDriver™ 1EDNx550 are not routed properly, this could lead to lower CMR performances or false triggering problems. To overcome these common issues, two key points should be kept in mind when designing with the EiceDRIVER™ 1EDNx550:

1) Input resistors $R_{INP}$ and $R_{INN}$ are mandatory for the proper operation of the TDI gate driver IC;

2) Asymmetric or improper layout of the input resistors $R_{INP}$ and $R_{INN}$ could lead to uncontrolled PCB parasitic capacitances, which couple the input pins to noise sources and can reduce the overall SNR of the input signal.

Paying attention to points 1) and 2) by following Table 1 and the layout guidelines provided in the datasheet, already allows to reach optimal performance. The theoretical analysis presented in this chapter complements the layout guidance with a full input circuit model to better understand the impact of layout on overall performance.

3.1.2 Full TDI input stage circuit model including PCB parasitics

The two key points presented in Section 3.1.1 can be quantitatively analyzed by means of the full equivalent circuit presented in Figure 14, which introduces PCB parasitic capacitances $C_{P+}$ and $C_{P-}$ to the model already shown in Figure 3.
In Figure 14 a single-ended PWM signal with amplitude $V_{DD}$ is generated from the controller and is routed as a differential pair IN$_+$ and IN$_-$ (i.e., traces close together) from the controller to the input resistors $R_{IN+}$ and $R_{IN-}$. The two input resistors shall be placed as close as possible to the gate driver IC.

At this point, $R_{IN-}$ and $R_{IN+}$ and the TDI stage internal resistances $R_{C1}$ and $R_{C2}$ act as a resistor divider and scale down the $\Delta V_{IN}$ voltage by a factor $k$, to meet the IC input specs at pins IN$_+$ and IN$_-$. 

$$\Delta V_{IN,IC} = \frac{\Delta V_{IN}}{k} = \frac{\Delta V_{Rin}}{k} = \frac{2R_{C2}}{2R_{C1} + 2R_{C2} + R_{IN+} + R_{IN-}}$$ \[1\]

After one further scaling, the resulting signal $\Delta V_{trg}$ downstream in the analog chain is applied to a Schmitt trigger.\(^1\)

Table 2 describes each component represented in the model.

<table>
<thead>
<tr>
<th>Components</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{IC1}$, $R_{IC2}$ and $C_{IC}$</td>
<td>On-chip trimmed passive components inside the gate driver IC</td>
</tr>
<tr>
<td>$R_{IN+}$ and $R_{IN-}$</td>
<td>Mandatory SMD input resistors. They shall be placed as close as possible to the gate driver IC</td>
</tr>
<tr>
<td>$C_{S+}$ and $C_{S-}$ (50 fF to 100 fF range)</td>
<td>Parasitic capacitances of SMD resistors $R_{IN+}$ and $R_{IN-}$ respectively</td>
</tr>
<tr>
<td>$C_{P+}$ (100 fF to 10 pF range)</td>
<td>Parasitic capacitance that models PCB couplings between the input net connected to IN+ and a generic adjacent net #NetA. Coupling is modeled through the equivalent noise voltage source $V_{n+}$</td>
</tr>
<tr>
<td>$C_{P-}$ (100 fF to 10 pF range)</td>
<td>Parasitic capacitance that models PCB couplings between the input net connected to IN- and a generic adjacent net #NetB. Coupling is modeled through the equivalent noise voltage source $V_{n-}$</td>
</tr>
</tbody>
</table>

Figure 15 and Figure 16 show the reasons behind the parasitic capacitances $C_{P+}$ and $C_{P-}$ in the layout.\(^2\)

\(^1\) According to Equation [1] and Figure 14, the peak-to-peak voltage of $\Delta V_{IN,IC}$ between pins IN+ and IN- is $V_{DD}/k$.

It is important to notice that, since $k$ is greater than 1 (e.g., $k = 12$ for $R_{IN+} = R_{IN-} = 33 \text{ k}\Omega$), signal $\Delta V_{IN,IC}$ is the most sensitive to noise. This already suggests placing $R_{IN}$ and $R_{IN+}$ as close as possible to the gate driver IC.

\(^2\) $C_{P+}$ and $C_{P-}$ must be calculated considering the contributions coming from all the PCB layers. In this specific case: $C_{P+} = C_{P1} + C_{P2}$ and $C_{P-} = C_{P1} + C_{P2}$. 

1. According to Equation [1] and Figure 14, the peak-to-peak voltage of $\Delta V_{IN,IC}$ between pins IN+ and IN- is $V_{DD}/k$.

   It is important to notice that, since $k$ is greater than 1 (e.g., $k = 12$ for $R_{IN+} = R_{IN-} = 33 \text{ k}\Omega$), signal $\Delta V_{IN,IC}$ is the most sensitive to noise. This already suggests placing $R_{IN}$ and $R_{IN+}$ as close as possible to the gate driver IC.

2. $C_{P+}$ and $C_{P-}$ must be calculated considering the contributions coming from all the PCB layers. In this specific case: $C_{P+} = C_{P1} + C_{P2}$ and $C_{P-} = C_{P1} + C_{P2}$.
Figure 15  Example of non-optimal layout with unwanted couplings on PCB (only Layer 1 contributions are shown); IN+ is coupled to a generic adjacent #NetA, IN- is coupled to a generic adjacent #NetB

Figure 16  Example of non-optimal layout with unwanted couplings on the PCB (only Layer 1 to Layer 2 contributions are shown); IN+ and IN- on Layer 1 are coupled to a generic adjacent net on Layer 2

According to the model in Figure 14, the $\Delta V_{IN,IC}$ voltage and the associated IN+ and IN- nets are the most critical from the noise perspective. This confirms that layout symmetry and PCB parasitics $C_P+$ and $C_P-$ must be kept under control during routing: keeping IN+ and IN- input traces symmetrical and avoiding capacitive coupling to any switching or noisy net is fundamental to achieve optimal performances and CMR levels listed in Table 1.

3.1.3  Effect of input PCB parasitic capacitances $C_{P+}$ and $C_{P-}$

Due to the voltage scaling $\Delta V_{IN,IC} = \Delta V_{Rin}/k$ (see Section 3.1.2), the two nets IN+ and IN- highlighted in green in Figure 17 are the most noise-sensitive as they have lower signal amplitude compared to the original PWM.
EiceDRIVER™ 1EDNx550 high-side and low-side gate driver
Application examples and layout guidelines

PCB layout considerations and guidelines

signal. For example, in case of $R_{IN} = R_{IN'} = 33$ kΩ the PWM signal amplitude $V_{DD}$ is reduced by a factor $k = 12$. Furthermore, any asymmetry in the layout related to IN+ and IN- leads to $C_P/C_P' \neq 1$ and eventually common-mode noise or disturbances can be translated into differential-mode ones that affect the driver input $\Delta V_{IN,IC}$.

![Layout example for description purposes. Reference layouts are shown in Section 3.3](image)

**Figure 17** Layer 1 layout example; IN+ and IN- noise-sensitive nets are highlighted in green

Consequently, it is important from a layout perspective to ensure for the nets IN+ and IN:-

1) Symmetrical layout (i.e., $C_P/C_P' = 1$, see Figure 18 and Figure 19 for layout symmetry criteria)

2) Keep switching or noisy nets away from IN+ and IN- as they couple either to IN- or IN+, directly affecting the differential PWM signal

3) Minimize $C_P$ and $C_P'$ by placing resistors $R_{IN}$ and $R_{IN'}$ as close as possible to the gate driver IC. The lower $C_P$ and $C_P'$, the lower the effect of $V_{IN}$ and $V_{IN'}$ (see Figure 14) on the input signal

Common layout issues and design guidelines to optimize the performances of EiceDRIVER™ 1EDNx550 are addressed in Section 3.2.
EiceDRIVER™ 1EDNx550 high-side and low-side gate driver

Application examples and layout guidelines

PCB layout considerations and guidelines

Layout example for description purposes.

Reference layouts are shown in Section 3.3

Figure 18  Example of symmetric IN+, IN- and reference plane on outer layer (e.g., Layer 1); component outlines are referred to the same layer

Figure 19  Example of symmetric IN+, IN- and reference plane on first inner layer (e.g., Layer 2); component outlines are referred to the external layer (e.g., Layer 1)
3.2 Common layout issues with EiceDRIVER™ 1EDNx550

As explained in Section 3.1, the following conditions should be ensured to avoid improper operation of the EiceDRIVER™ 1EDNx550:

1) Symmetrical layout (i.e., $C_{P+}/C_{P-} = 1$, see example in Figure 18 and Figure 19).
2) Keep switching or noisy nets away from IN+ and IN- as they couple either IN- or IN+, directly affecting the differential PWM signal.
3) Minimize $C_{P+}$ and $C_{P-}$ by placing resistors $R_{IN+}$ and $R_{IN-}$ as close as possible to the gate driver IC. The lower $C_{P+}$ and $C_{P-}$, the lower the effect of $V_{n+}$ and $V_{n-}$ (see Figure 14) on the input signal.

Table 3 addresses the common layout issues when designing with EiceDRIVER™ 1EDNx550, and links them to the respective potential solution.

<table>
<thead>
<tr>
<th>Problem/Effect</th>
<th>Possible layout reason</th>
<th>Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Sub-optimal CMR performances</strong></td>
<td>Wrong or misplaced resistors</td>
<td>Check if resistors’ value, tolerance and form factor are chosen according to Table 1. Ensure that resistors are both placed close to the gate driver IC according to design guidelines provided in Section 3.3.</td>
</tr>
<tr>
<td></td>
<td>Asymmetric layout</td>
<td>Check layout and routing of IN+, IN- and surrounding nets. Shield IN+ and IN- nets with planes connected to driver ground. Always ensure symmetry of IN+, IN- and shielding plane(s). An example of symmetrical layout is shown in Figure 18 and Figure 19, with IN+ and IN- also shielded by the driver ground of EiceDRIVER™ 1EDNx550.</td>
</tr>
<tr>
<td><strong>Unwanted retriggering of the output</strong></td>
<td>Wrong or misplaced resistors</td>
<td>Check if resistors’ value, tolerance and form factor are chosen according to Table 1. Ensure that resistors are both placed close to the gate driver IC according to design guidelines provided in Section 3.3.</td>
</tr>
<tr>
<td></td>
<td>Cross-coupling at input pins</td>
<td>Check layout and routing of IN+, IN- and surrounding nets. Shield IN+ and IN- nets with planes connected to driver ground. Always ensure symmetry of IN+, IN- and shielding plane(s). An example of symmetrical layout is shown in Figure 18 and Figure 19, with IN+ and IN- also shielded by the driver ground of EiceDRIVER™ 1EDNx550.</td>
</tr>
</tbody>
</table>
3.3 Layout guidelines

Layout guidelines can be restricted to the following:

- Place input resistors \( R_{\text{IN}+} \) and \( R_{\text{IN}-} \) as close as possible to the driver, ideally in front of the input pins \( \text{IN}+ \) and \( \text{IN}- \) to minimize PCB parasitic capacitances.
- Make a symmetrical routing of the input traces \( \text{IN}+ \) and \( \text{IN}- \) with respect to the IC body (see Section 3.1.3).
- Shield the input traces \( \text{IN}+ \) and \( \text{IN}- \) with the driver ground on the outer layer and first inner layer (if applicable – see Section 3.1.3).
- Use a low-ESR decoupling capacitance for the \( V_{\text{DD}} \) supply and place it as close as possible to the driver.
- Minimize power loop inductance, as the most critical limitation of switching speed due to the resulting unavoidable voltage overshoots.

Layout recommendations for the input path of the SOT23-6 package version is given in Figure 20. Layout recommendations for the TSNP-6 package with 0603 and 0402 form factor resistors are given in Figure 21 and Figure 22 respectively.

![Figure 20](image-url)

**Figure 20** Layout recommendation for SOT23-6 package (component layer); shielding with driver ground net is recommended on inner layer below \( \text{IN}+ \) and \( \text{IN}- \), whenever possible.
EiceDRIVER™ 1EDNx550 high-side and low-side gate driver
Application examples and layout guidelines

PCB layout considerations and guidelines

Figure 21  Layout recommendation for TSNP-6 package with SMD resistor 0603

Figure 22  Layout recommendation for TSNP-6 package with SMD resistor 0402
## List of abbreviations

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMR</td>
<td>Common-Mode Robustness</td>
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<tr>
<td>CMRR</td>
<td>Common-Mode Rejection Ratio</td>
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<tr>
<td>ESD</td>
<td>Electrostatic Discharge</td>
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<tr>
<td>ESR</td>
<td>Equivalent Series Capacitance</td>
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<tr>
<td>GND</td>
<td>Ground</td>
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<tr>
<td>GaN</td>
<td>Gallium Nitride</td>
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<tr>
<td>LPF</td>
<td>Low-Pass Filter</td>
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<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
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<tr>
<td>SiC</td>
<td>Silicon Carbide</td>
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<td>SOT</td>
<td>Small Outline Transistor package</td>
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<tr>
<td>SMD</td>
<td>Surface Mount Device</td>
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<td>TO</td>
<td>Transistor Outline package</td>
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<tr>
<td>TSNP</td>
<td>Thin Small Discrete Package</td>
</tr>
<tr>
<td>UVLO</td>
<td>Undervoltage Lockout</td>
</tr>
</tbody>
</table>
References

5 References

[1] Infineon Technologies AG – EiceDRIVER™ 1EDN-TDI Product Page
Single-channel non-isolated gate driver IC family with truly differential inputs

[2] Infineon Technologies AG – EiceDRIVER™ 1EDNx550 Device Datasheet
Single-channel high-side and low-side gate driver with high-CMR TDI inputs

[3] Infineon Technologies AG – Application Note: AN_201408_PL11_027 – EVAL_2.5KW_CCM_4PIN
2.5 kW PFC evaluation board with CCM PFC controller ICE3PCS01G

[4] Infineon Technologies AG – Application Note: AN_1805_PL52_1805_091441 – EVAL_HB_BC_1EDN8550B
Half-bridge buck converter evaluation board using the EiceDRIVER™ 1EDN TDI (Truly Differential Inputs)

Non-isolated bi-directional synchronous buck converter EVAL_BIDI_HB_1EDN7550B

Single-Channel Non-Isolated Gate Driver with Truly Differential Inputs
PCIM Europe 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion,

Data Center Application
PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent
EiceDRIVER™ 1EDNx550 high-side and low-side gate driver
Application examples and layout guidelines

Revision history

<table>
<thead>
<tr>
<th>Document version</th>
<th>Date of release</th>
<th>Description of changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>V 1.0</td>
<td>2018-04-25</td>
<td>First release</td>
</tr>
<tr>
<td>V 1.1</td>
<td>2019-08-07</td>
<td>Updated the look-up table with different controller output voltage</td>
</tr>
</tbody>
</table>
| V 2.0            | 2022-04-06      | • Added PCB layout considerations and guidelines chapter  
|                  |                 | • Editorial enhancement of layout and descriptions  
|                  |                 | • Updated maximum CMR range to ±200 V static, ±400 V dynamic  
|                  |                 | • Added references  
|                  |                 | • Added list of abbreviations |
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