# 800 W Platinum® server power supply

## Using 600 V CoolMOS™ P7 and digital control with XMC™

## About this document

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### Scope and purpose

This document introduces a complete Infineon system solution for an 800 W server power supply that achieves the 80Plus® Platinum® standard. The power supply is composed of a Continuous Conduction Mode (CCM) Power Factor Correction (PFC) converter and a half-bridge LLC DC-DC converter. This document focuses on the necessary microcontroller configuration and the controls implemented for adequate system performance, which is demonstrated by the test results.

The Infineon components used in the 800 W server power supply are:

- 600 V CoolMOS™ P7 SJ MOSFET in TO-247 and TO-220 packages
- CoolSiC™ Schottky diode 650 V G5
- 40 V and 25 V OptiMOS™ 5 MOSFETs
- EiceDRIVER™ 1EDI isolated and 2EDN non-isolated gate drivers
- ISOFACE™ 4DIR1400H quad-channel reinforced digital isolator
- XMC1402 and XMC4200 microcontrollers
- ICE2QR2280G CoolSET™ QR Flyback controller

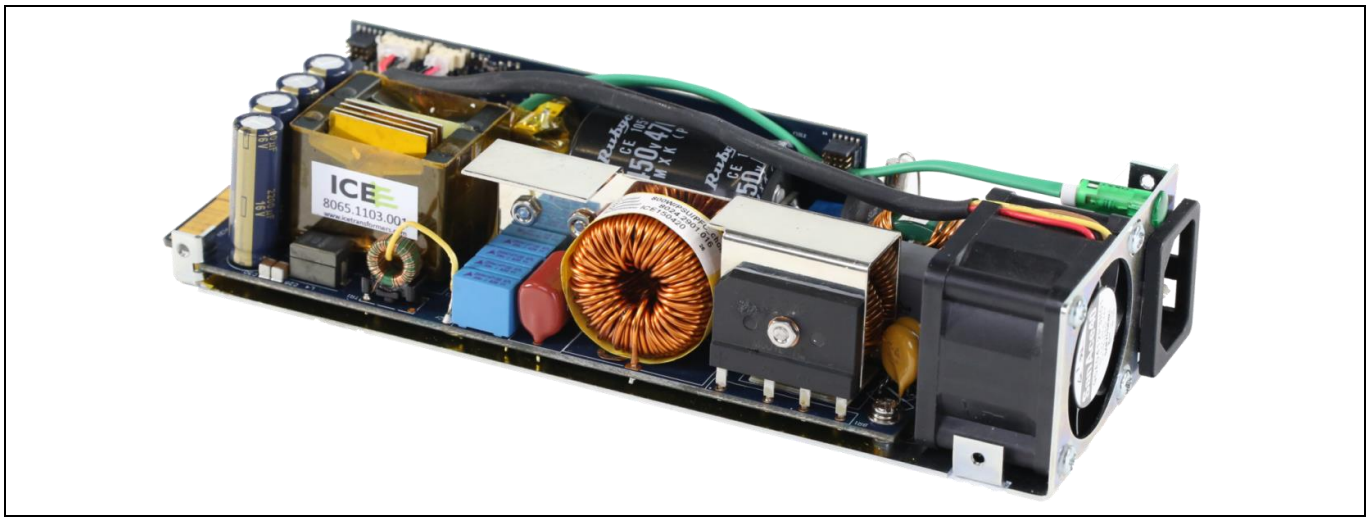

**Figure 1 800 W Platinum® server power supply**

### Intended audience

This document is intended for design engineers who want to verify the performance of:

- The 600 V CoolMOS™ P7 MOSFET technology in the TO-247 package in hard-switching topologies like the CCM PFC boost converter working at 65 kHz along with the CoolSiC™ Schottky diode 650 V G5

- The 600 V CoolMOS™ P7 MOSFET technology in soft-switching topologies like the LLC, working at a resonant frequency around 150 kHz
- Isolated and non-isolated gate drivers in the EiceDRIVER™ ICs family
- The flexibility and powerful performance of the XMC™ microcontrollers for server power supplies

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# 1 Summary of the 800 W Platinum® server power supply board

This AN provides a very detailed description of the design considerations, and operation under both steady-state and abnormal operating conditions, as well as the results of a total Platinum® efficiency complaint server power supply by using several different Infineon Technologies semiconductors, ranging from power MOSFETs to microcontrollers.

Below is a summary of the key features that this demo board offers when used as a design reference for power supplies in server applications:

- Attractive compact design in 30 W/in$^3$ form factor
- Efficiency that outperforms the Platinum® efficiency standard throughout the entire load demand at both 115 V AC and 230 V AC, as shown in Figure 50 in Section 6.1
- Low Total Harmonic Distortion (THD) and high Power Factor (PF) response, as shown in Figure 51 and Figure 52 respectively, from 20 percent of the load
- Fully digital control implementation in both the PFC boost converter using XMC1400, as described in the Power Factor Correction (PFC) stage section, and the LLC resonant converter using the XMC4200, as described in the LLC resonant DC-DC converter section
- High performance achived by using Infineon Technologies best price-performance ratio devices:
  - Single TO-247 600 V CoolMOS™ P7 SJ MOSFET in the PFC boost converter, along with a single TO-220 CoolSiC™ Schottky diode 650 V G5
  - TO-220 600 V CoolMOS™ P7 SJ MOSFET on the primary side of the LLC resonant converter, and OptiMOS™ 5 40 V and 25 V as Synchronous Rectification (SR) and O-ring MOSFETs, respectively
  - EiceDRIVER™ 1EDI isolated and EiceDRIVER™ 2EDN non-isolated gate driver ICs
  - QR Flyback controller ICE2QR2280G CoolSET™
- Robust and reliable operation under different abnormal conditions:
  - Smooth inrush current during start-up, as shown in Figure 55
  - Power Line Disturbance (PLD) events, like AC-Line Drop-Out (ACLDO), as described in Table 9, as well as voltage sags, as described in Table 10
  - Brown-out reaction, as shown in Figure 67
  - Load-step response at different abrupt load changes, as depicted in Figure 68 and Figure 69
  - Over Current (OC) condition reaction, as described in the Overcurrent Protection (OCP) section, as well as the response of the PSU in a short-circuit event, as depicted in Figure 74
- Fully compliant with both peak and average Class B conducted EMI EN 55022 standard limits, as shown in Figure 75 and Figure 76

# 2 System description

This document presents an Infineon system solution for an 800 W server power supply in 30 W/in$^3$. The evaluation board consists of a classic CCM PFC boost converter with average current control as the AC-DC stage. The PFC converter provides regulated bulk voltage from universal AC input, while it demands high-quality current from the grid. The DC-DC stage is an LLC resonant converter, which provides a 12 V regulated output. Both converters have a dedicated Infineon microcontroller to manage the converter control as well as the system behavior.

Figure 2 shows a block diagram of the implemented power supply with the previously described blocks. In addition, an O-ring switch is implemented in order to consider the efficiency of a full system solution, even though no advance O-ring functionality is implemented. Furthermore, an I$^2$C channel is reserved in the secondary controller, which enables PMBus communication implementation.

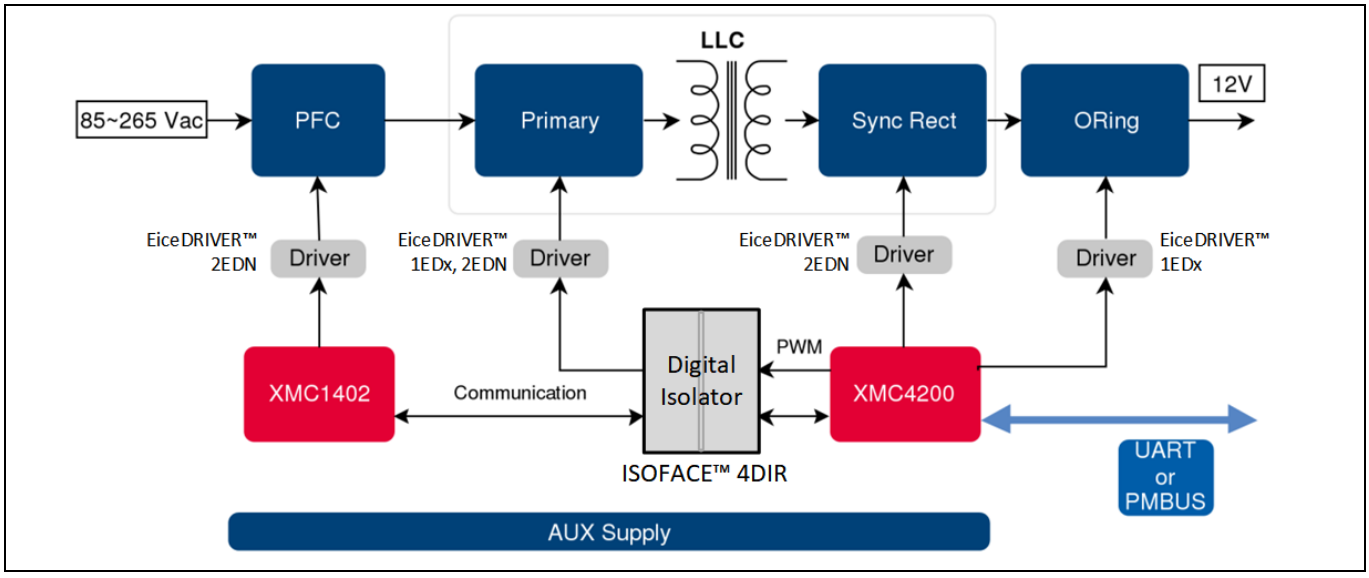


**Figure 2 800 W server power supply block diagram**

The target efficiency level of the 800 W server power supply is Platinum® efficiency according to the 80Plus® standard. As shown in Figure 3, this efficiency level is reached with a wide margin, which makes the obtained efficiency close to the Titanium level for light and full load.

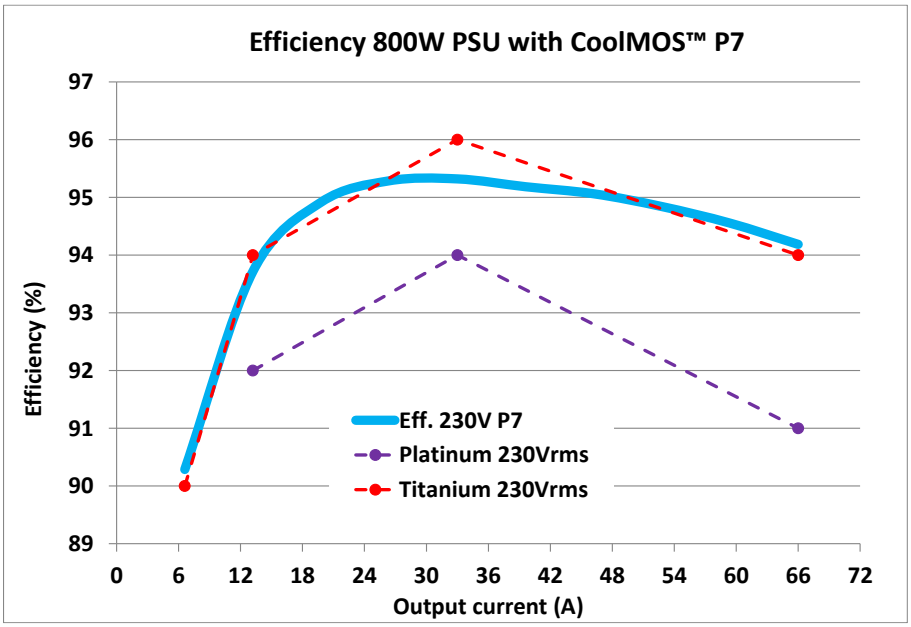


**Figure 3** **Measured efficiency of the 800 W server power supply with 600 V CoolMOS™ P7, compared to the Platinum® and Titanium standards**

## 2.1 Specifications

This section presents the main electrical specification of the Infineon server power supply evaluation board for both input and output.

The requirements for the universal AC input are introduced in Table 1, which also includes the required hold-up time to provide regulated output when the AC input is not present.

**Table 1** **Input requirements**

| Parameter | Value |
|---|---|
| Input voltage range, $V_{in\_range}$ | 90 V AC–265 V AC |
| Nominal input voltage, $V_{in}$ | 230 V AC |
| AC-line frequency range, $F_{AC}$ | 47 Hz–63 Hz |
| Max peak input current, $I_{in\_max}$ | 10 $A_{RMS}$ at $V_{in}$ = 90 V AC, $P_{out\_max}$ = 800 W |
| Turn-on input voltage, $V_{in\_on}$ | 80 V AC–87 V AC, ramping up |
| Turn-off input voltage, $V_{in\_off}$ | 75 V AC–85 V AC, ramping down |
| PFC | Shall be greater than 0.9 from 20 percent rated load and above |
| Hold-up time | 10 ms after last AC zero point at $P_{out\_max}$<br>20 ms after last AC zero point at 0,5 × $P_{out\_max}$ |
| THD | < 10 percent from 20 percent load at high-line, for class A equipment |

In the case of the regulated 12 V output, the requirements are shown in Table 2. It must be mentioned that the output voltage dynamic range considered must be kept not only in dynamic load conditions, but also in case of PLD of the AC input.

**Table 2 Output requirements**

| Parameter | Value |
|---|---|
| Nominal output voltage | 12.2 V ± 2 percent in static conditions at nominal $V_{in}$ |
| Nominal output current | 67 A |
| Output voltage ripple | Max. 120 $mV_{pk-pk}$ at $I_{out}$ = 67 A |
| Output OV set-point | Min. 13.5 V, max. 14 V |
| Output OC threshold | 30 s up to 74 A<br>10 s up to 83 A<br>Max. 1 ms over 83 A |
| Dynamic output voltage variation | ±240 mV<br>*Note: Load-step 3 A–33 A and 33 A–66 A with 0.5 A/µs current slope*<br>*Note: Input voltage variation and PLD* |

**Table 3 Overall efficiency target**

| Load condition | Efficiency at low-line | Efficiency at high-line |
|---|---|---|
| 20% | 90% | 90% |
| 50% | 92% | 94% |
| 100% | 90% | 91% |

## 2.2 Infineon Technologies semiconductors

### 2.2.1 600 V CoolMOS™ P7

The CoolMOS™ seventh-generation platform is a revolutionary technology for HV power MOSFETs, designed according to the SJ principle and pioneered by Infineon Technologies. The 600 V CoolMOS™ P7 series is the successor to the CoolMOS™ P6 series. It combines the benefits of a fast-switching SJ MOSFET with excellent ease of use, e.g. very low ringing tendency, outstanding robustness of the body diode against hard commutation, and excellent ESD capability. Furthermore, extremely low switching and conduction losses make switching applications even more efficient, more compact and much cooler.

### 2.2.2 CoolSiC™ Schottky diode 650 V

Selection of the boost diode is a major design decision in a CCM boost converter because the diode is hard commutated at a high current and the reverse recovery can cause significant power loss, as well as noise and current spikes. Reverse recovery can be a bottleneck for high switching frequency and high power density power supplies. Additionally, at low-line, the available diode conduction duty cycle is quite low, and the forward current quite high in proportion to the average current. For that reason, the first criteria for selecting a diode in a CCM boost circuit are fast recovery with low reverse recovery charge, followed by $V_f$ operating capability at high forward current.

Since CoolSiC™ Schottky diodes have a capacitive charge, $Q_c$, rather than reverse recovery charge, $Q_{rr}$, their switching loss and recovery time are much lower than a silicon ultrafast diode, leading to enhanced

performance. Moreover, SiC diodes allow higher switching frequency designs. Hence, higher power density converters are achieved. The capacitive charge for SiC diodes is not only low, but also independent of di/dt, current level and temperature, which is different from silicon diodes that have strong dependency on these conditions.

The recommended diode for CCM boost applications is the 650 V CoolSiC™ Schottky diode generation 5 and generation 6, which both include Infineon's leading-edge technologies, such as a proprietary soldering process and wafer thinning technology. These are families of products that show improved efficiency over all load conditions, resulting from the improved thermal characteristics. The new generation 6 of the 650 V CoolSiC™ Schottky diode further boosts efficiency, while keeping the strong technical characteristics of the generation 5 CoolSiC Schottky diodes.

The proper current rating of the PFC diode must be calculated by considering 1.3 to 1.5 times the RMS current of the diode, which is expressed as:

$$I_{D\_RMS} = \frac{P_{OUT\_MAX}}{V_{IN\_RMS} \cdot \eta} \times \sqrt{\frac{8 \cdot \sqrt{2} \cdot V_{IN\_RMS}}{3 \cdot \pi \cdot V_{OUT}}} = \frac{800}{90 \cdot 0{,}885} \times \sqrt{\frac{8 \cdot \sqrt{2} \cdot 90}{3 \cdot \pi \cdot 405}} = 4{,}1\ A$$

In this demo board, a 6 A IDH06G65C5 diode is used.

## 2.2.3 EiceDRIVER™ 2EDN non-isolated gate driver for MOSFETs

### 2.2.3.1 Introduction

The 2EDN7x24 is a non-inverting fast dual-channel driver for low-side switches. Two true rail-to-rail output stages with very low output impedance and high current capability are chosen to ensure the highest flexibility and cover a wide variety of applications.

All inputs are compatible with LV TTL signal levels. The threshold voltages (with a typical hysteresis of 1 V) are kept constant over the supply voltage range.

Since the 2EDN7x24 is particularly aimed at fast-switching applications, signal delays and rise/fall times have been minimized. Special effort has been made to minimize delay differences between the two channels to very low values (typically 1 ns).

The 2EDN7x24 driver used in this demo board comes in a standard PG-DSO-8 package.

### 2.2.3.2 Driver outputs

The two rail-to-rail output stages realized with complementary MOS transistors are able to provide a typical 5 A of sourcing and sinking current. The on-resistance is very low, with a typical value below 0.7 Ω for the sourcing p-MOS and 0.5 Ω for the sinking n-MOS transistor. The use of a p-channel sourcing transistor is crucial for achieving real rail-to-rail behavior and not suffering from the source follower's voltage drop.

Gate drive outputs are held low for floating inputs (ENx, Inx) or during start-up or power-down, once undervoltage lockout (UVLO) threshold is not exceeded.

#### 2.2.3.3 Undervoltage lockout (UVLO)

The UVLO function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO threshold voltage. Therefore, it can be guaranteed that the switch transistor is not operated if the driving voltage is too low to completely switch it on, thereby avoiding excessive power dissipation.

The default UVLO level is set to a typical value of 4.2 V or 8 V (with some hysteresis). For higher levels, such as HV SJ MOSFETs, a minimum active voltage of 8 V is used (2EDN7424), while the 4.2 V is used for the logic level-driven LV MOSFETs (2EDN7524).

### 2.2.4 EiceDRIVER™ 1EDI galvanically isolated single-channel driver

The 1EDI driver family is based on Infineon's coreless transformer technology, enabling a benchmark-setting minimum Common Mode Transient Immunity (CMTI) of 100 kV/µs.
The 1EDI20N12AF driver provides output currents of up to 2 A on separate output pins for applications up to 1200 V. They are ideal for use in charge stations for electric vehicles as well as power supplies for servers, and industrial and telecommunications systems.
Due to lower inductive losses, these drivers enable an additional gain in efficiency of 0.5 percent with the latest generation of CoolMOS™ P7.

### 2.2.5 OptiMOS™ 5 40 V

OptiMOS™ 5 40 V, Infineon's latest generation of power MOSFETs, is optimized for SR in SMPS such as those found in servers and desktops. The OptiMOS™ 5 40 V product family features not only the industry's lowest $R_{DS(on)}$ but also the perfect switching behavior for fast-switching applications. 15 percent lower $R_{DS(on)}$ and 31 percent lower Figure of Merit (FOM) ($R_{DS(on)} \times Q_g$) compared to alternative devices has been realized by advanced thin wafer technology.

### 2.2.6 XMC™ for digital control

#### 2.2.6.1 XMC1400 for PFC control implementation

The XMC1400 is part of the XMC™ microcontroller family from Infineon Technologies. This family of microcontrollers based on ARM® Cortex®–M0 cores is designed for real-time critical applications. The control of power supplies is a strong focus for XMC™ microcontrollers, where users can benefit from features such as analog comparators, PWM timers, co-processors or high-precision ADCs.

Some of the XMC1400 features are listed here:

- 12-bit ADC, 1 MSample/s; flexible sequencing of conversions including synchronization
- Clock frequency is 48 MHz, nevertheless, key peripherals can run at double the CPU frequency, like PWM timers or math co-processors, to accelerate calculations or improve PWM resolution
- Fast analog comparators for protections such as OCP
- Co-processor that can run in parallel to the main core (Cortex®-M0); in this particular case it will help with executing faster divisions (17 clock cycles)
- Flexible timing scheme due to CCU timers; these timers allow synchronization of PWM patterns and accurate generation of ADC triggers
- Interconnection matrix to route different internal signals from one peripheral to another. As an example, the timers can connect to an ADC to signify the exact point in time when a signal must be sampled, or a comparator output can be connected to a PWM timer. This can be used to make sure that whenever the comparator trips, the PWM stops.

Serial communication protocols are supported, including UART, I²C and SPI. These can be used for GUI or possible communication with the secondary stage of a full power supply.

### 2.2.6.2 XMC4200 for LLC control implementation

All XMC4000 devices are powered by ARM® Cortex®-M4 with a built-in DSP instruction set. The Single Precision Floating Point Unit (SPFPU), Direct Memory Access (DMA) feature and Memory Protection Unit (MPU) are state-of-the-art for all devices – even the smallest XMC4000 runs with up to 80 MHz in core and peripherals. It comes with a comprehensive set of common, fast and precise analog/mixed-signal, timer/PWM and communication peripherals.

Some of the XMC4200 features are listed here:

- Up to 256 kB embedded Flash with 22 ns access time and error correction unit
- Up to 40 kB embedded RAM
- 8-channel DMA
- 4-channel high-resolution PWM (150 ps)
- Two ADCs with up to 8 channels each; each channel has 12-bit resolution, selectable reference and total conversion time of less than 500 ns
- Two Digital to Analog Converters (DACs) of 12-bit resolution
- Four multi-functional serial interface channels configurable to SPI, I²C, I²S or UART
- 2 CAN nodes and USB 2.0 module
- Extended temperature range up to 125°C ambient temperature

## 2.2.7 QR controller (CoolSET™)

Integrated power management IC with 800 V avalanche rugged CoolMOS™, start-up cell and QR current mode Flyback PWM controller in a DSO-16/12 package. Capable for 25.5 W SMPS design. The QR CoolSET™ series continues to deliver design agility and miniaturization. This new series offers the possibility of higher efficiency and better EMI performance. The digital frequency reduction feature ensures very stable operation with decreasing load change, and the fold-back correction keep the maximum power limits within tolerances desired by SMPS designers. The Active Burst Mode (ABM) operation during low power consumption provides best-in-class power consumption during standby.

# 2.3 Board description

Figure 4 shows a top view of the 800 W server power supply. The distribution on the PCB of the different stages that compose the PSU is highlighted: AC input and EMI filter, PFC stage, LLC (DC-DC) stage and DC output, bias (auxiliary) power supply and control board.

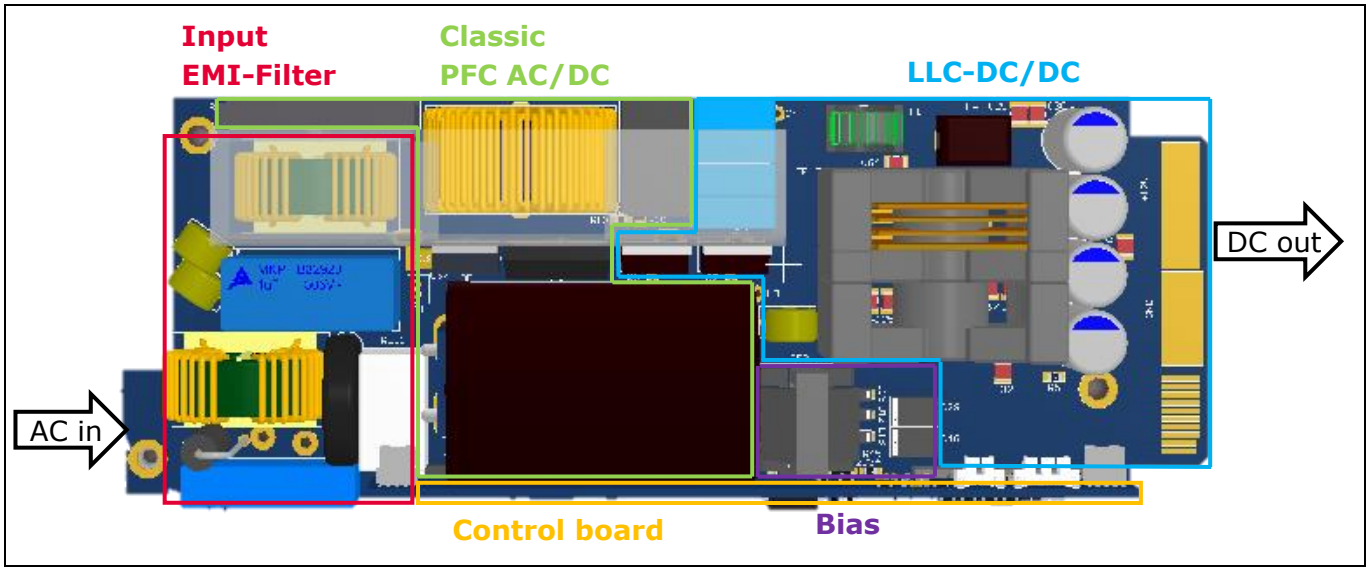


**Figure 4 Distribution (top view) of the different stages of the 800 W server power supply**

A bottom view of the same PCB is shown in Figure 5, which shows the distribution of the drivers for both the AC-DC and DC-DC stages, as well as the SR and O-ring switches.

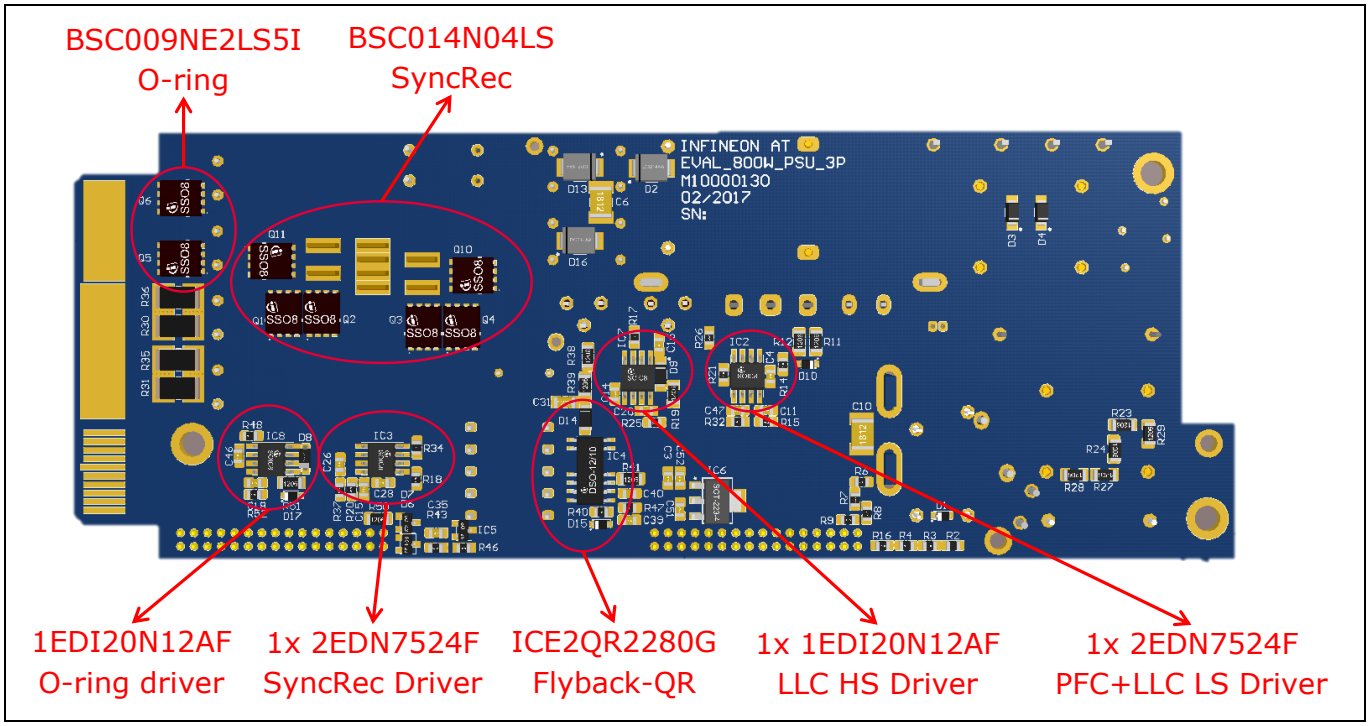


**Figure 5 Bottom view of the 800 W server power supply main board**

A view of the control card present on the side of the PSU is shown in Figure 6, where the XMC™ microcontrollers selected for primary- and secondary-side control are depicted, together with the digital isolator. The control card is designed to support PFC monitoring and PMBus communication. However, these functionalities have not been implemented in the current power supply.

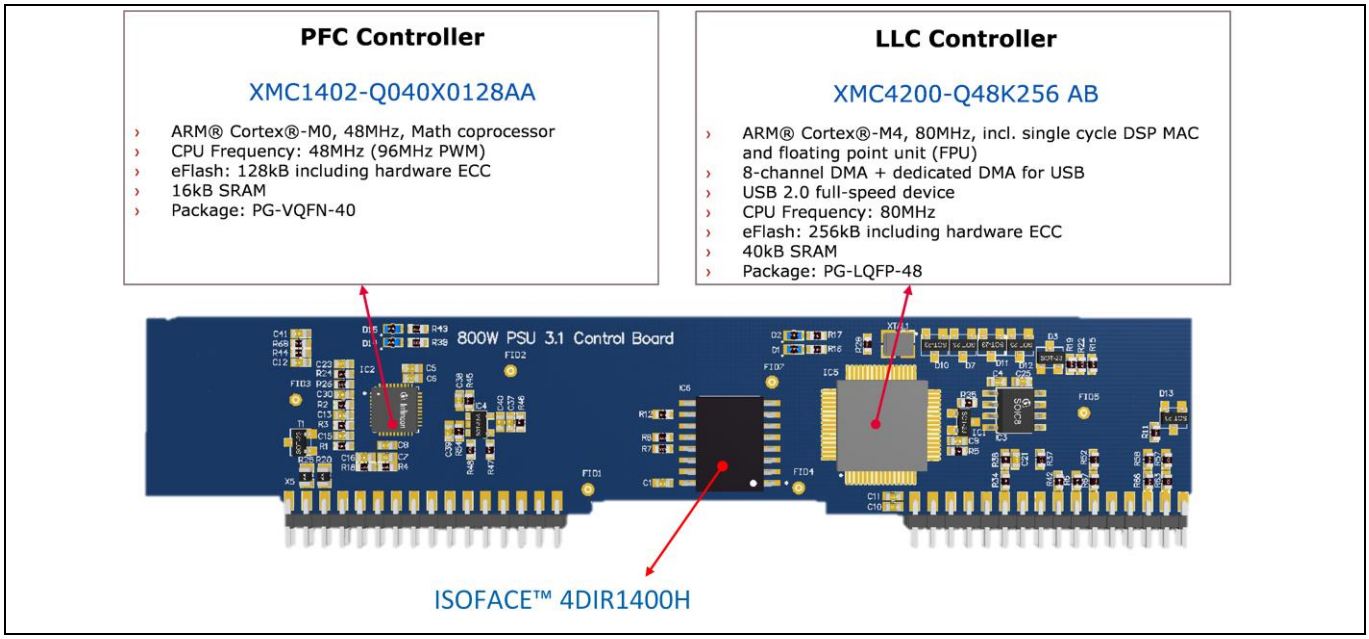


**Figure 6 Control board of the 800 W server PSU with the XMC™ microcontrollers and their main characteristics**

In order to demonstrate the highly efficient performance and good regulation control under dynamic conditions (load jumps) of the board as in a real application, an external connector PCB has been included. This gives access to the power connections and different external signals as well as containing a 2200 µF capacitor, which simulates the load behavior of the different PoL voltage regulators in a server mother board. Figure 7 shows the connector PCB described with the main connections:

- 12 V and GND are the connections of the 12 V DC output.
- 12 V sense and GND sense can be used for output sensing in external equipment, and this is the voltage used for 12 V DC regulation.
- The switch included enables the PSU to be turned on and off.

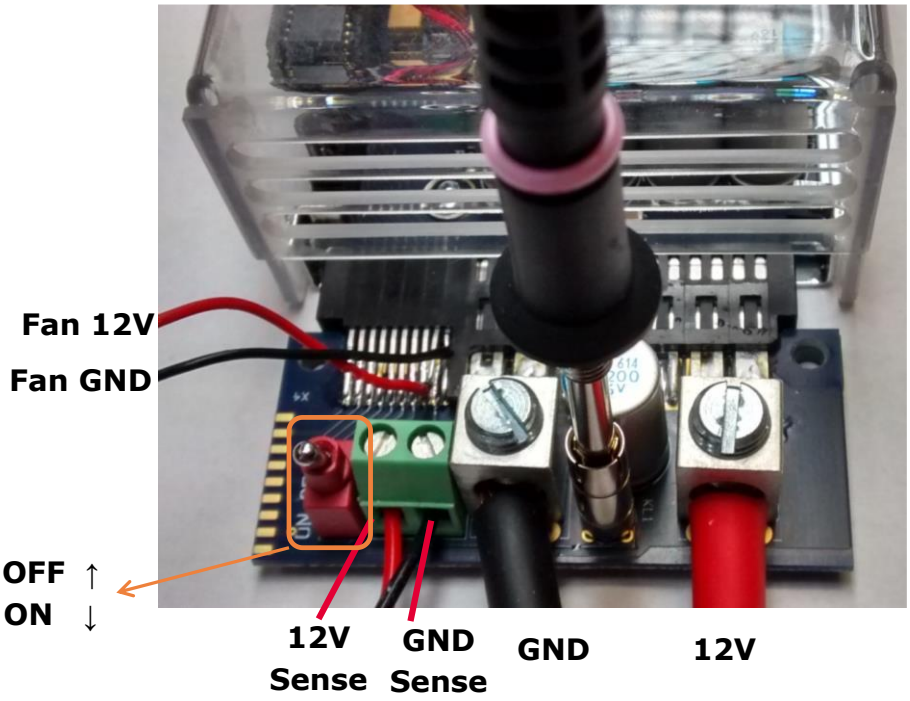


**Figure 7 Output connector PCB with the main available connections**

The fan included in the 800 W server PSU is supplied from the 12 V DC output of the power supply. The external connector PCB enables the connection of the output voltage terminals to the fan supply. However, the external fan supply is made possible by directly accessing the connector pin. In that case, the second pin of the signal connector (fan 12 V in Figure 8) must be lifted to provide the proper fan supply voltage.

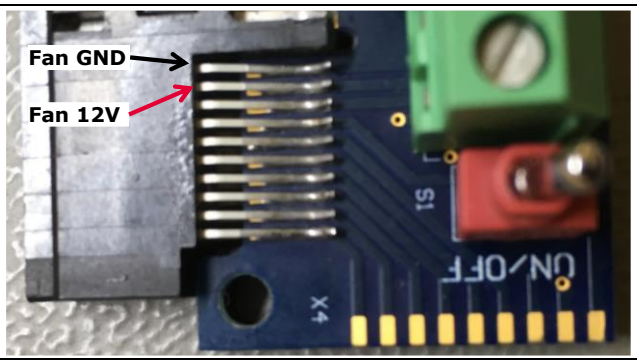


**Figure 8 Fan supply connections in the output connector board**

# 3 Power Factor Correction (PFC) stage

The AC-DC stage of the 800 W server power supply is a classic PFC boost converter. Figure 9 shows the implemented topology, which uses a single 600 V CoolMOS™ P7 MOSFET, a CoolSiC™ Schottky diode 650 V G5 and a 2EDN EiceDRIVER™. The Infineon microcontroller XMC1402 is used for the PFC control implementation.

The boost converter is operated at 65 kHz and provides, from universal AC input voltage range, a regulated bulk voltage to the DC-DC converter stage of around 395 V–405 V. The active PFC functionality is implemented in this AC-DC stage in order to demand a high-quality current waveform from the grid, according to the input requirements specified in the previous section.

This section presents the main design parameters of the implemented PFC as well as the digital control used for such functionality, with a special focus on the influence of the power stage design in the control-loop design and realization.

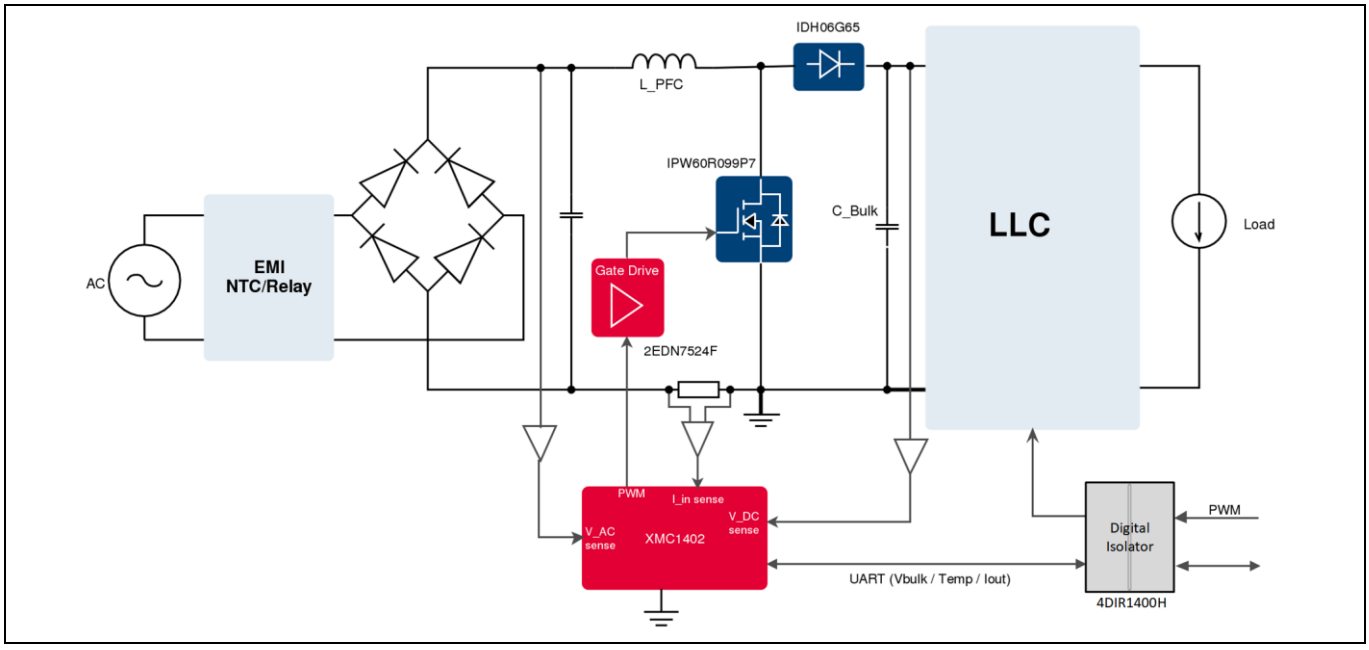


**Figure 9 800 W PSU PFC topology with required sensing and Infineon devices**

## 3.1 EMI filter and rectifier bridge

The EMI filter is implemented as a two-stage filter, as shown in Figure 10, which provides sufficient attenuation for both Differential Mode (DM) and Common Mode (CM) noise.

The two high-current CM chokes L_cm are based on high-permeability toroid ferrite cores. Both CM chokes implement two windings with 29 turns each, resulting in a minimum inductance of 4 mH on each side. The relatively high number of turns, together with the winding strategy, causes a considerable amount of stray inductance. This stray inductance ensures sufficient DM attenuation.

According to the average and RMS currents through the rectifier bridge [1], the rectifier LVB2560 with very low forward voltage drop was selected. This 800 V device also has sufficient voltage reserve, with $V_{in}$ = 265 V.

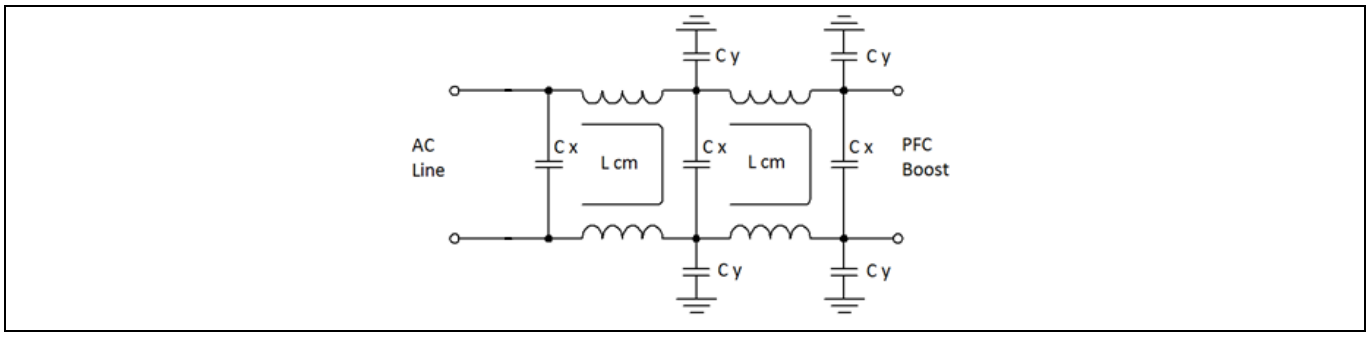


**Figure 10 Two-stage filter structure**

## 3.2 PFC choke and bulk capacitor

The PFC choke design is based on a toroidal high-performance powder core. Toroidal chokes have a large surface area and allow a good balance, minimizing core and winding losses, and achieving a homogeneous heat distribution without hot spots. For this reason they are suitable for systems that are targeting the highest power density with forced-air cooling.

The core material chosen was Chang Sung Corporation's (CSC) HS, which has a good balance between DC bias, core losses and temperature stability, while its cost is lower than that of HighFlux. The part number is HS270060, with an outer diameter of 27 mm and 60 µ permeability.

The built inductor has 90 turns with a small-signal bias inductance of 617 µH. The effective inductance respect to the current bias is determined by the permeability variation of the core with the DC magnetizing force (H), and is illustrated in Figure 11.

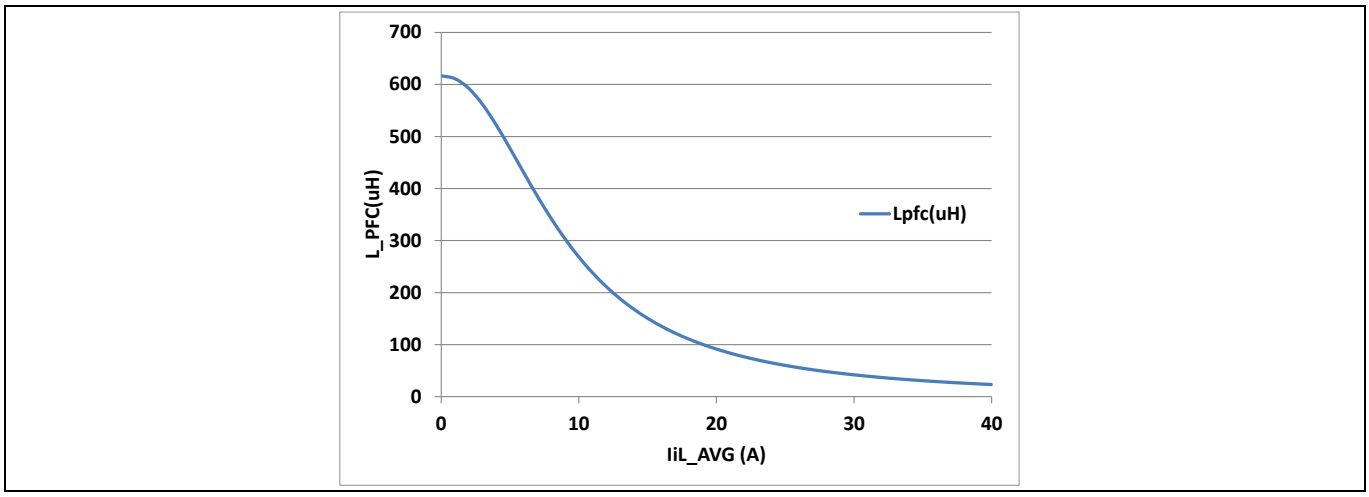


**Figure 11 Inductance variation with the inductor current; linear approximation**

The bulk capacitor (C_Bulk in Figure 9) is typically designed according to the minimum bulk voltage allowed for a given hold-up time, i.e. the time that the power supply must provide stable output voltage while the grid voltage is zero [1]. A 470 µF 450 V electrolytic capacitor is mounted in the 800 W server power supply, which provides a minimum voltage of 330 V for a hold-up time of 10 ms at full load.

## 3.3 Functional description and control implementation

The AC-DC stage of this 800 W power supply performs PFC by digital implementation of an average current control, in a classic CCM boost converter. Figure 12 shows the control block diagram, which corresponds to a

typical two-loop approach, with line feed-forward, used in average current control [2]. The blocks shown are implemented in software (SW).

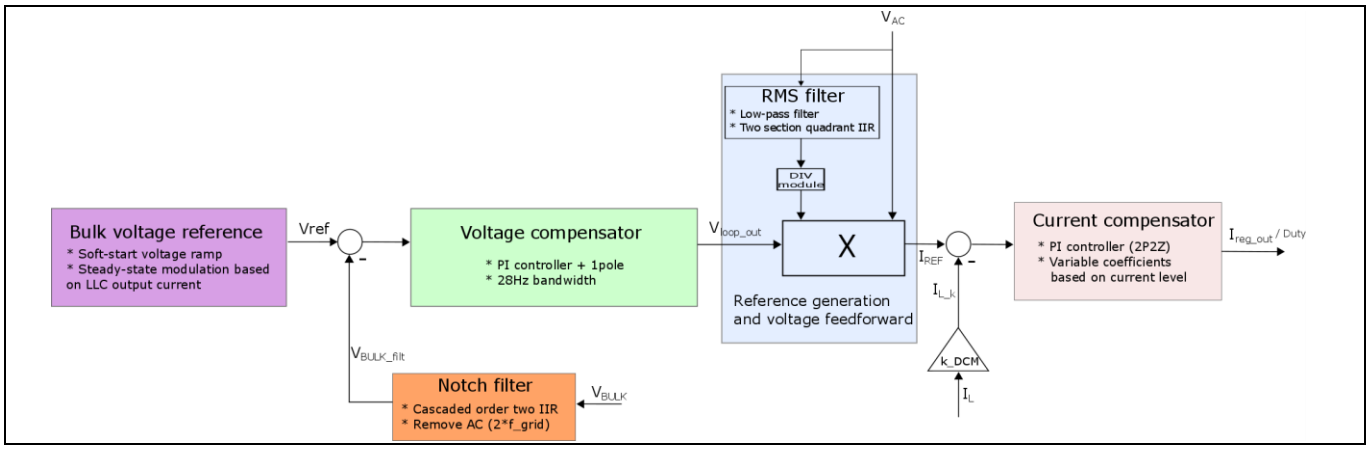


**Figure 12 800 W PSU PFC control scheme**

These SW blocks are shown in blue in Figure 13, together with the required HW peripherals (red) for proper operation of the PFC stage. The peripherals can be summarized as follows:

- Three CCU8 slices: two slices configured in compare mode to generate the PWM for the PFC switch and ADC trigger; one slice used in capture mode for conduction time acquisition in Discontinuous Conduction Mode (DCM)
- Three CCU4 units used as fixed-frequency interrupt trigger and reference generation for the analog comparators
- Two analog comparators: one for Peak Current Limitation (PCL) using the CCU8 trap functionality, and one for zero current detection during DCM operation
- Division unit of the math co-processor: the use of this peripheral allows a reduction in the division computation up to four times with respect to the standard SW implementation
- Four ADC channels with two different triggers for synchronized voltages and Current Sensing (CS)

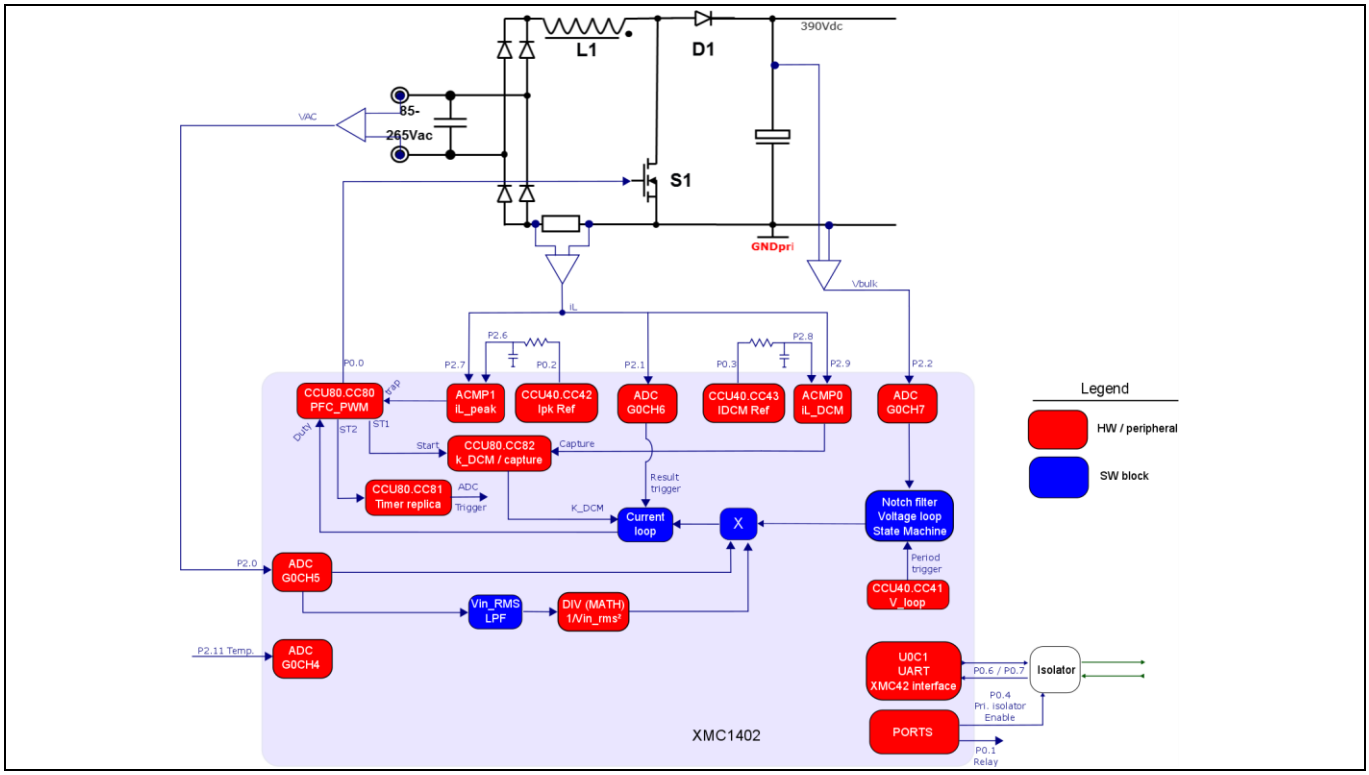


**Figure 13 Peripherals and SW blocks used in the PFC of the 800 W server power supply**

The CCU8 unit available in the XMC1402 microcontroller is a two-channel capture-compare unit. The possibility of using these two channels independently, together with the versatility of the ADC and the programmable signal conditioning between the timer and ADC modules, allows a synchronized and noise-free sensing of the necessary voltages and currents for PFC operation.

Figure 14 shows the time diagram of the ADC sensing and Interrupt Service Routine (ISR) trigger of the implemented current loop, which is executed every switching cycle ($f_{sw}$ = 65 kHz). Compare channel 1 (CR1) of the main timer (PFC PWM) carries the duty-cycle information. However, compare channel 2 (CR2) is set to half of the CR1 value to trigger the ADC queue [3]. Therefore, the inductor current is sensed in half of the on-time, which corresponds to the inductor current average value in CCM operation. The resulting event of the ADC is used to trigger the current control ISR, which ensures using the last acquired current value.

At the same time, a second timer (timer-replica) is synchronized with the main timer. The use of the replica allows synchronizing as well the bulk voltage measurement. In this case, a second ADC group, e.g., the scan ADC [3], is triggered in the middle of the off-time, thus reducing the sensing noise.

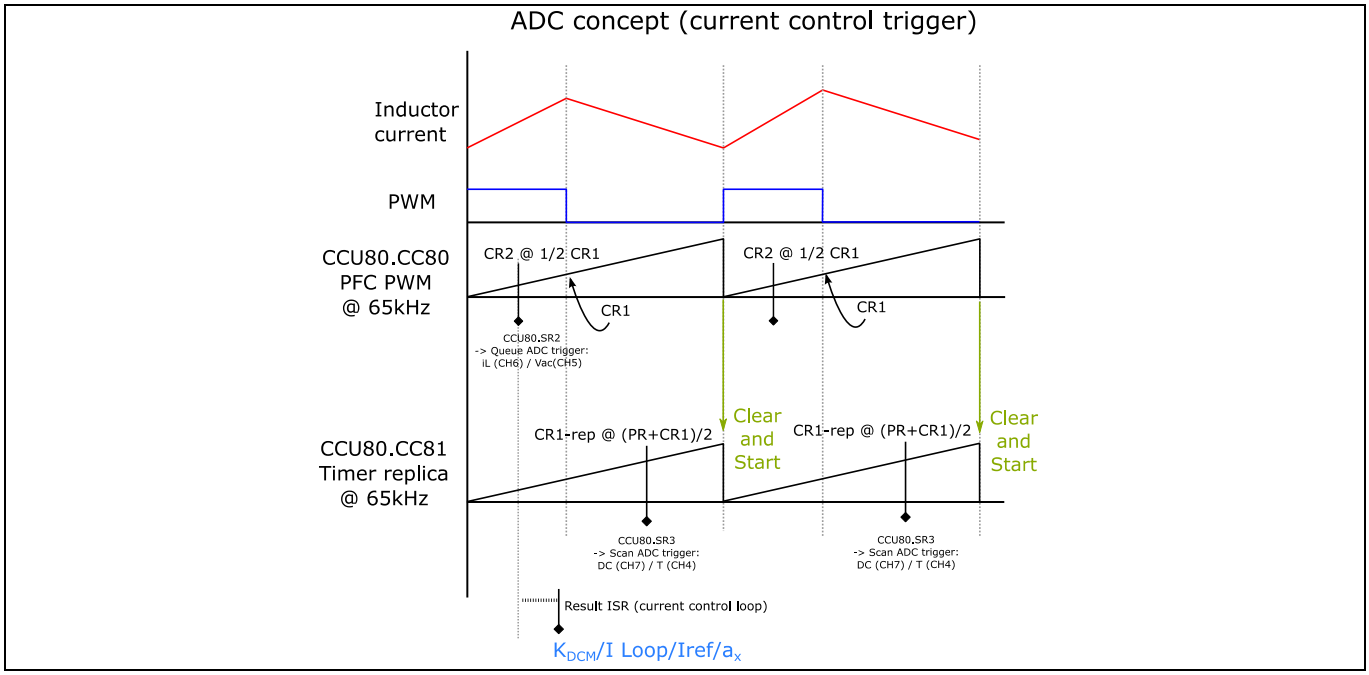


**Figure 14 Timers and ADC synchronization in the implemented PFC control scheme**

The voltage loop, PFC state machine, Low Pass Filter (LPF) of the input voltage and the bulk voltage notch filter are implemented in a second ISR triggered at a fixed frequency of 6.5 kHz using a CCU4 slice. The scheduling of these functionalities is shown in Figure 15.

Both the AC filter (LPF of the AC voltage) and the notch filter of the bulk voltage are two cascaded sections of second-order IIR filters.

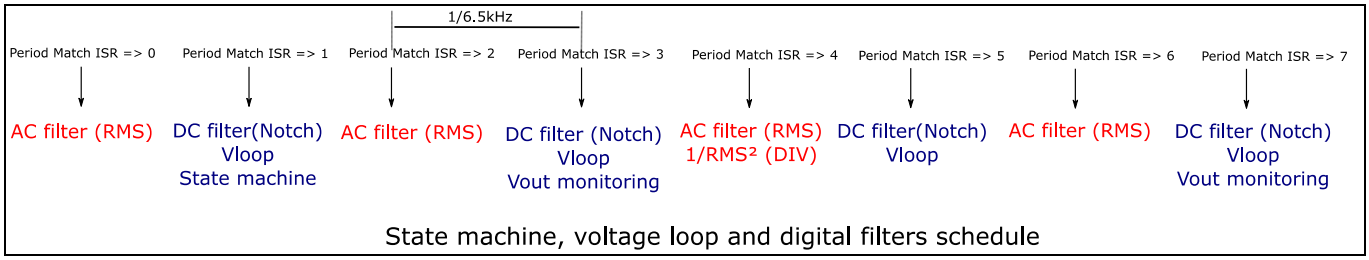


**Figure 15 Time schedule of the voltage-loop interrupt at 6.5 kHz**

The state machine (Figure 16) ensures the correct behavior of the PFC systems by controlling the start-up phase and monitoring the output and input voltage during operation. During start-up the relay is closed before the boost converter starts switching, in order to bypass the NTC resistance, which limits the inrush current. The relay is then open only in case the bulk voltage goes under a defined level, under which the PFC is restarted.

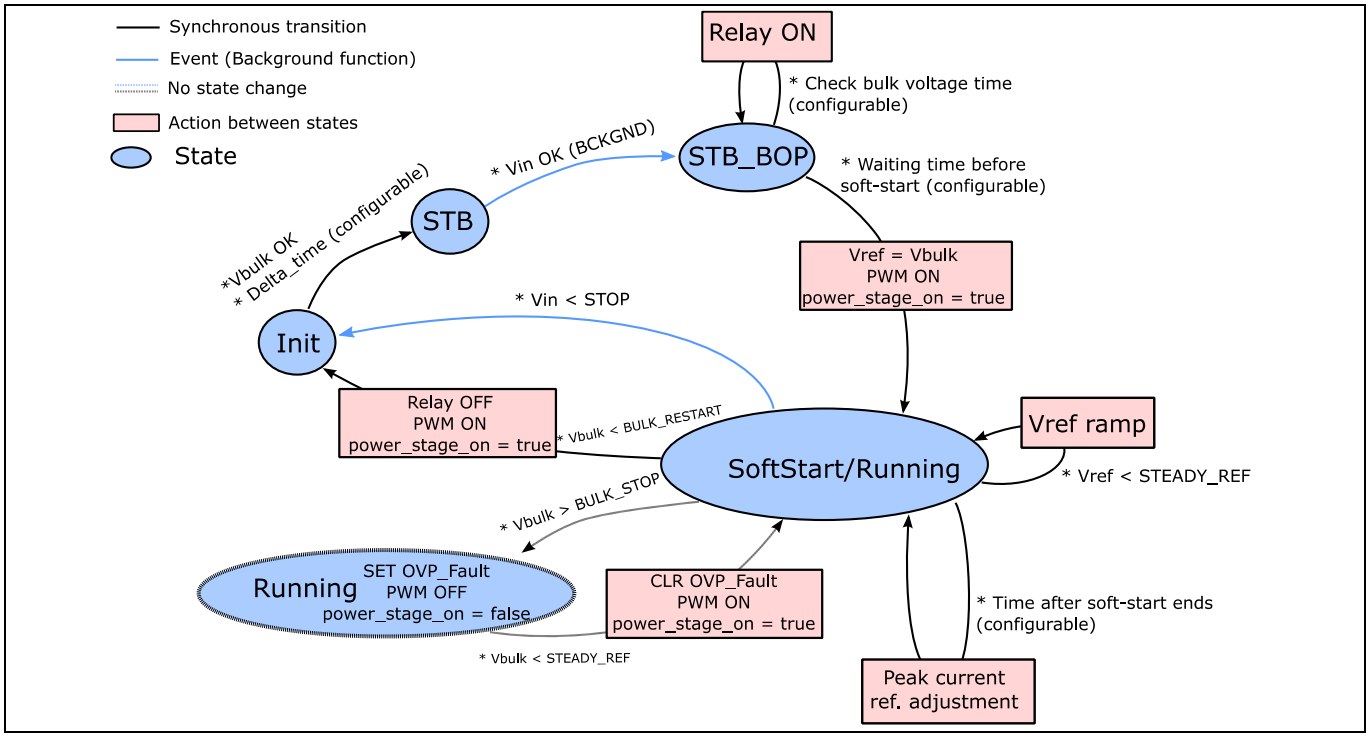


**Figure 16 PFC state machine**

### 3.3.1 Current controller

The design of the current controller in a PFC boost converter in CCM operation is well known for both analog and digital implementation, using PI or PID controllers and with or without duty cycle feed-forward [1, 2]. Nevertheless, different issues such as inductance variation of the saturable inductor, DCM operation and filter interactions arise during PFC operation.

- Saturable core inductance variation in the PFC current loop

According to the references shown, the gain of the duty cycle to inductor current transfer function, Gid(s), is inversely proportional to the inductance value. In the PFC choke design shown, a saturable core is used in this way, and the inductance changes as shown in Figure 11. This inductance variation implies a gain change according to the average current, i.e., a change in Gid(s) during the AC half-cycle. Therefore, if a single controller is used for all the operating conditions, bandwidth (BW) variations will occur with the risk of instability, as shown in Figure 17.

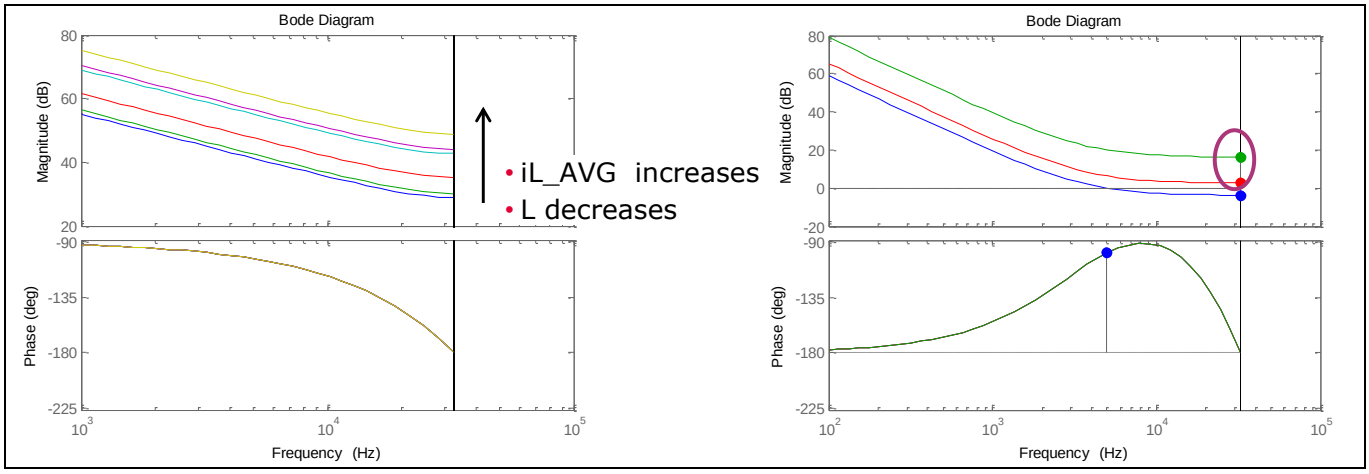


**Figure 17** **Control to inductor current transfer function gain variation with the inductor average current (left), and instability caused by inductance change with a single controller**

In the digital implementation introduced above, the controller gain is modified according to the inductance variation to maintain adequate stability margins during the half-line cycle. A linear approximation is used for the inductance variation, which is known by design. As shown in Figure 18, two different linearizations are used depending on the sensed current level (under or over 15 A). This variation is coded in the SW and is used to modify the controller coefficients in the current-loop ISR, according to the sensed current. As a result, the BW variation is limited, avoiding instabilities and enhancing the loop performance (Figure 18).

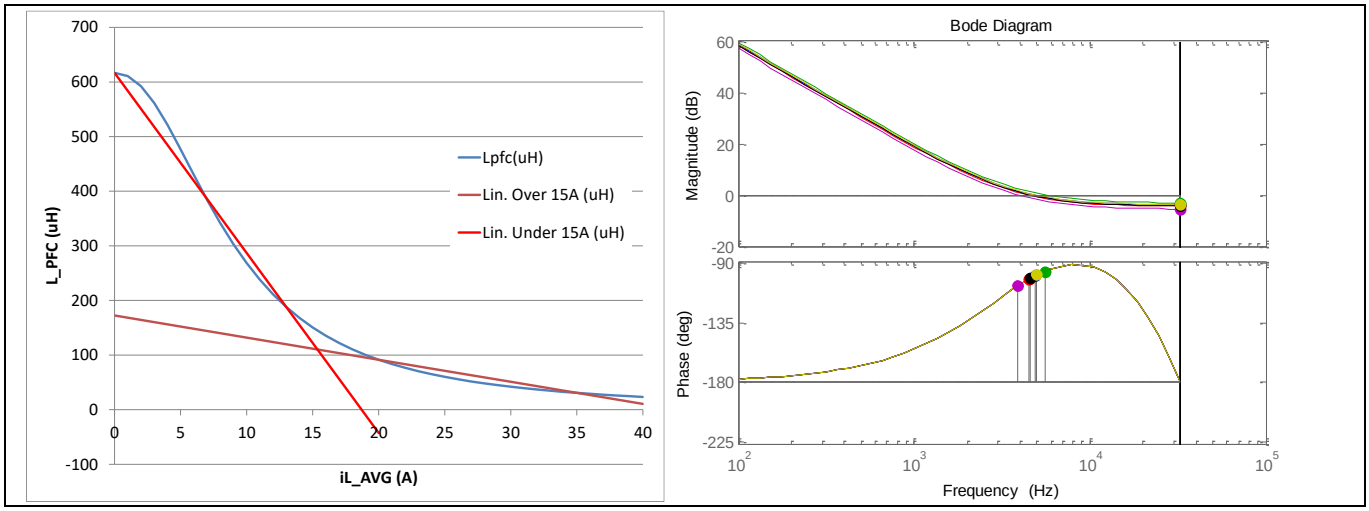


**Figure 18** **Inductance linear approximation (left) enables stable operation with limited BW variation during a half-line cycle (right)**

- DCM operation at light load

The second issue in PFC is the change from CCM to DCM operation at light load, especially in high-line conditions. In [1] the coexistence of both operation modes during a half-line cycle is analyzed as well as the Gid(s) change between the two conduction modes. This coexistence leads to an increase of the input current distortion due to two main factors: the BW degradation of the current loop if a CCM controller is used in DCM operation, and the mis-match of the sensed current and the actual average inductor current.

The dynamics change in the boost converter operating in CCM and DCM is presented in [4]. As a consequence, if a current controller designed for CCM operation is used in DCM operation a drastic degradation of the current

loop BW occurs. Figure 19 shows this performance degradation for the 800 W PSU PFC stage. In this case a current loop with a 2 kHz BW is designed for CCM operation. If the same controller is applied in DCM operation the BW is reduced to 64 Hz, leading to significant current tracking error and, therefore, an increased distortion.

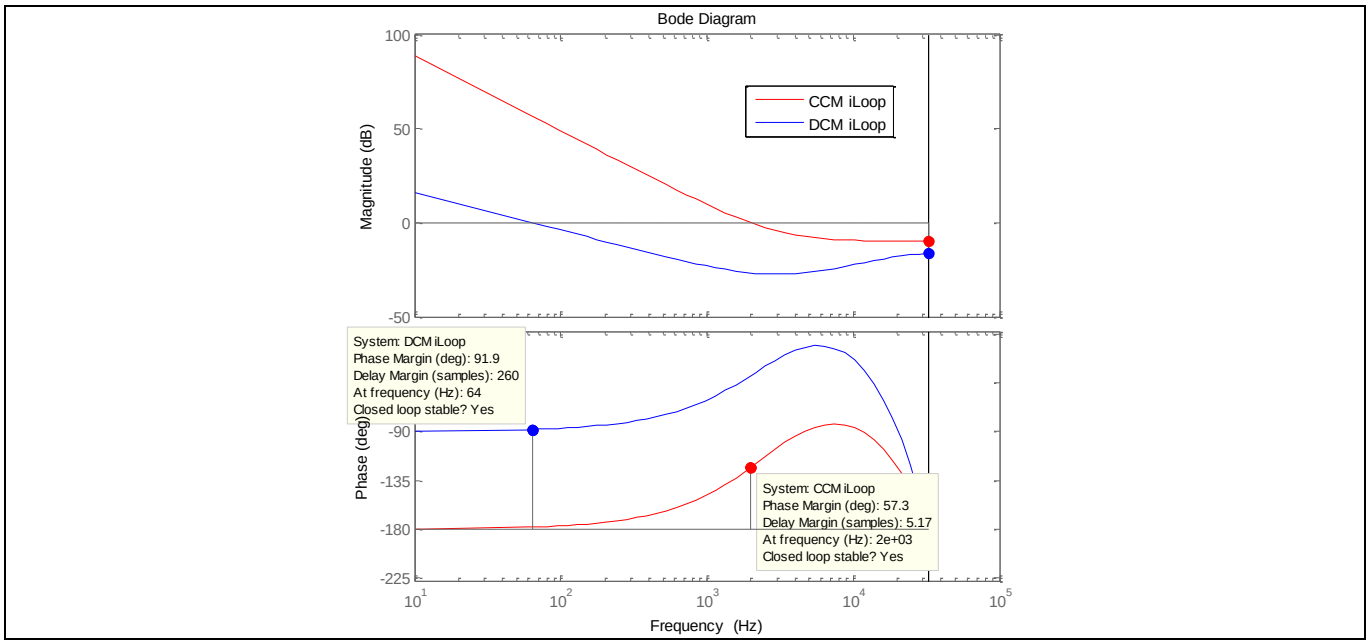


**Figure 19 Inductance linear approximation (left) enables stable operation with limited BW variation during a half-line cycle (right)**

In order to keep a similar BW when the converter operates in different conduction modes, the controller gain must be increased by a factor greater than 10 in DCM operation in respect to CCM. This implies a risk of instability in the change from DCM to CCM if the wrong controller is applied, which increases the complexity and necessary accuracy in the conduction mode detection.

In the solution shown, a controller that provides a 9 kHz BW in CCM operation is applied. This BW increase enables a BW in DCM operation over 270 Hz, while no accurate DCM/CCM detection is required.

The delay in the current tracking caused by the diminished loop BW is aggravated by the fact that the sensed current does not match the actual average inductor current. As stated above, the CS is triggered in half of the on-time, which corresponds to the average inductor current in CCM operation. However, in DCM the sensing point provides a current that is higher than the actual average current (Figure 20). This increases the already high error rate due to the reduced BW.

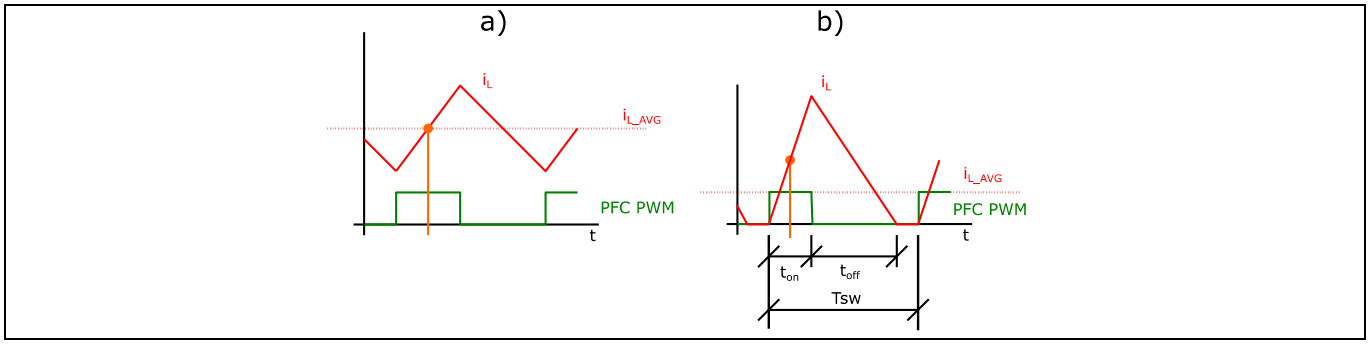


**Figure 20 Average inductor current and ADC sensed value for CCM (a) and DCM (b) operation**

According to the presented waveform in Figure 20 the average current ($i_{L\_AVG}$) is proportional to the sensed current with a factor $K_{DCM}$, as expressed in equation (1) [4].

$$i_{L\_AVG} = k_{DCM} \cdot i_{L\_ADC}; \qquad k_{DCM} = \frac{t_{on} + t_{off}}{T_{sw}} \tag{1}$$

The timers present in XMC1402 can be used in compare mode, allowing the generation of PWM signals or ADC triggers, as shown. In addition, the same timers can be configured in capture mode. In this case, the timer can be configured to capture the timer value when a certain event occurs.

This functionality is used to acquire the inductor conduction time ($t_{on}$+$t_{off}$ in Figure 20), enabling calculation of the correction factor for the inductor current in DCM operation. The timer is initialized with the rising edge of the main timer. On the other side, the timer acquisition is done with the falling edge of the comparison output of the inductor current with a fixed reference value close to zero. DACs are not available in the XMC1000 series, and a PWM with an external RC filter is used instead to generate such a reference. The required HW configuration is depicted in Figure 21.

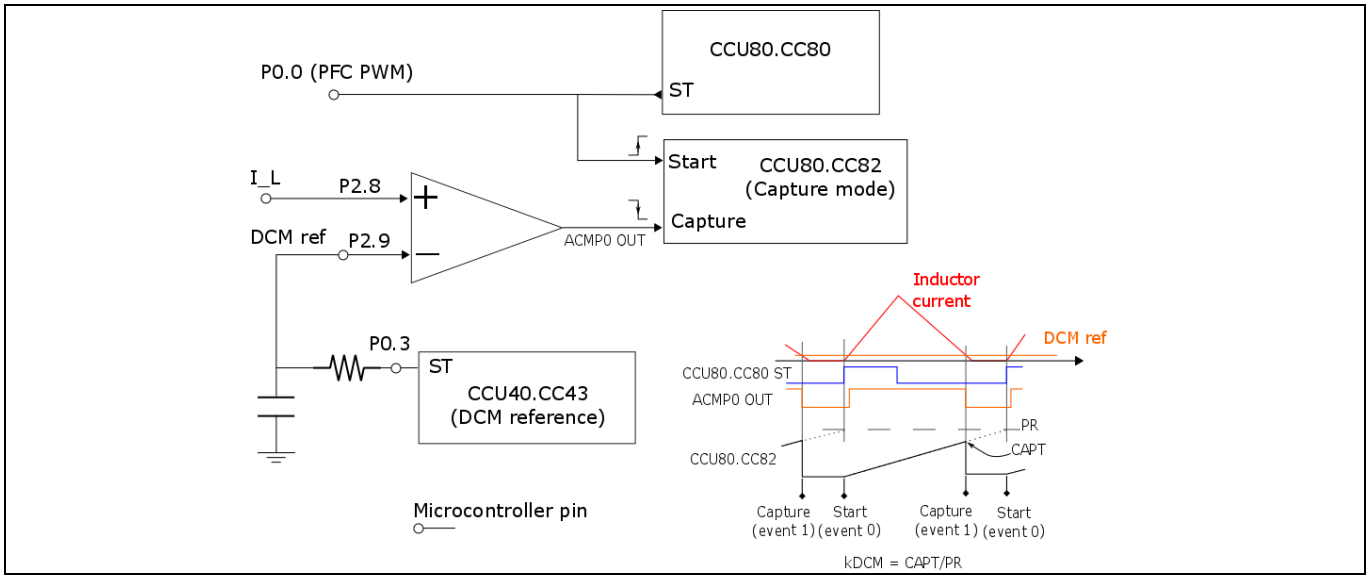


**Figure 21 Inductor current conduction time acquisition using the XMC™ timer capture functionality**

- Filter interactions

A third issue to consider when designing the PFC current loop is the possible interaction between the EMI filter and the boost converter. This is caused by the interaction between the output impedance of the filter and the converter input impedance, as shown in [5].

In low-line operation the current demanded by the PFC increases, and therefore the input impedance of the boost converter decreases. Figure 22 shows the output impedance of the EMI filter together with the input impedance of the PFC converter at low-line and full load. According to the frequency response shown, if a 9 kHz BW is applied in these operating conditions, the intersection of the impedances provokes oscillation in the input current.

Reducing the current loop BW avoids the impedance intersection, as the green curve in Figure 22 shows. Therefore, in high-current operating conditions, the controller BW is reduced to 5 kHz to minimize the filter interactions.

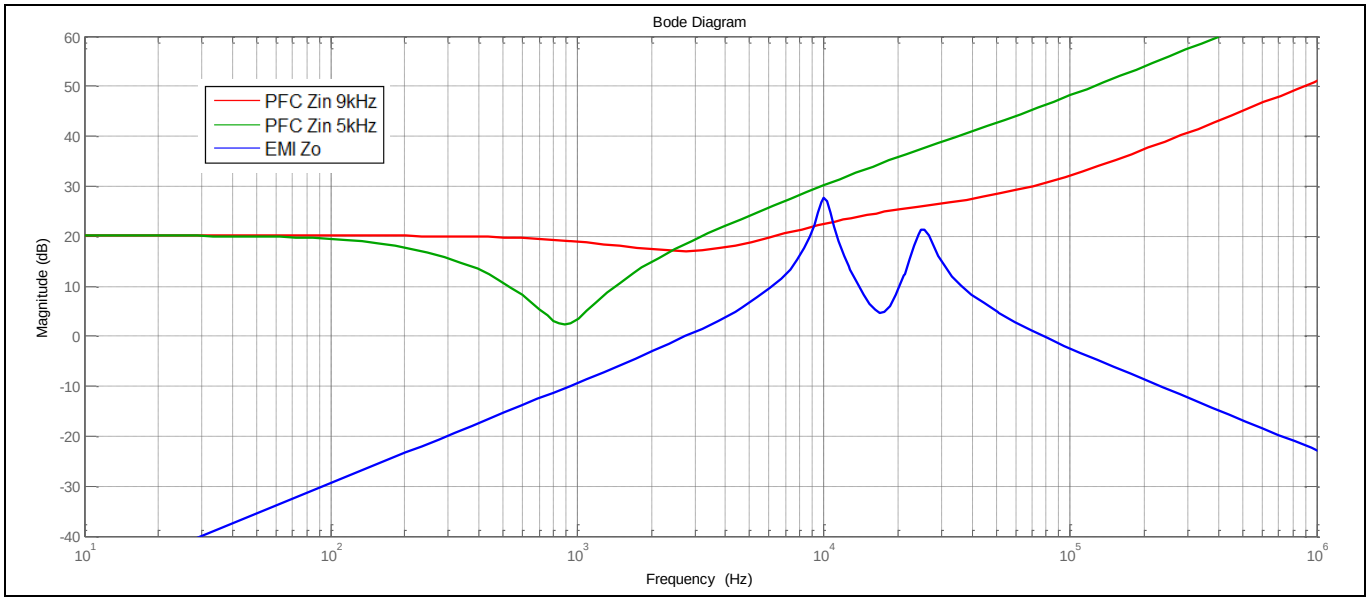


**Figure 22 PFC input impedance with 9 kHz (red) and 5 kHz (green) current loop BW, and EMI filter output impedance (blue) for full-power operation at 90 Vrms**

Figure 23 shows the BW change implementation according to the sensed average current. A high BW is kept under 6 A operation when there is no risk of filter interactions, to maintain a good performance in terms of PF and THD. However, when the current increases the BW is reduced to minimize the current oscillations due to filter interactions. A hysteresis is applied to avoid stability problems due to continuous BW modification.

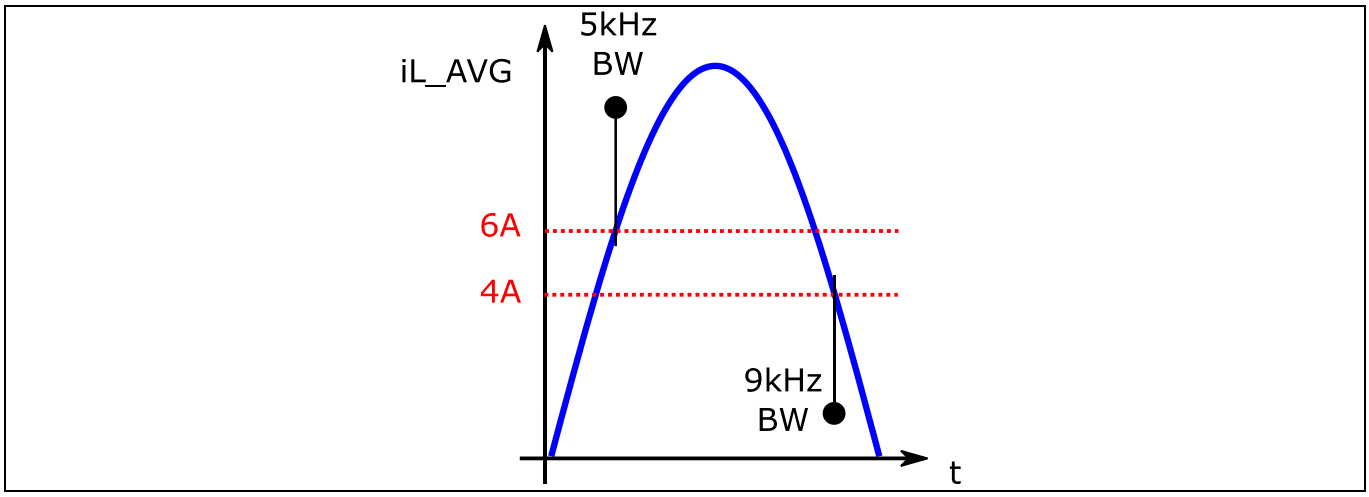


**Figure 23 BW change according to current level**

## 3.3.2 Voltage loop

In the selected control scheme, the required current reference is generated by the multiplication of the sensed input voltage, the RMS information of this same voltage and the information provided by the voltage loop. Therefore, the voltage-loop design has a direct impact not only on the adequate voltage regulation but also on the current distortion.

In order to obtain a non-distorted input current reference, the voltage loop must filter the twice-line frequency ripple present in the bulk voltage. A simple way is to use the controller itself as a filter, by reducing the loop BW (under 10 Hz). However, this option seriously jeopardizes the voltage-loop regulation.

Instead, the approach used in this PFC (Figure 12) is the introduction of a highly selective filter that eliminates the twice-line frequency ripple from the sensed bulk voltage. The filtered information is then fed into the voltage loop, which enables the loop BW to be increased to close to 30 Hz (Figure 24).

In the selected implementation two-notch digital IIR filters tuned to 100 Hz and 120 Hz are placed in cascade. As a result, these two frequencies are removed from the sensed bulk voltage, as shown in the loop gain presented in Figure 24. This implementation, although computationally costly, does not require frequency detection and is robust against grid frequency changes during the converter operation.

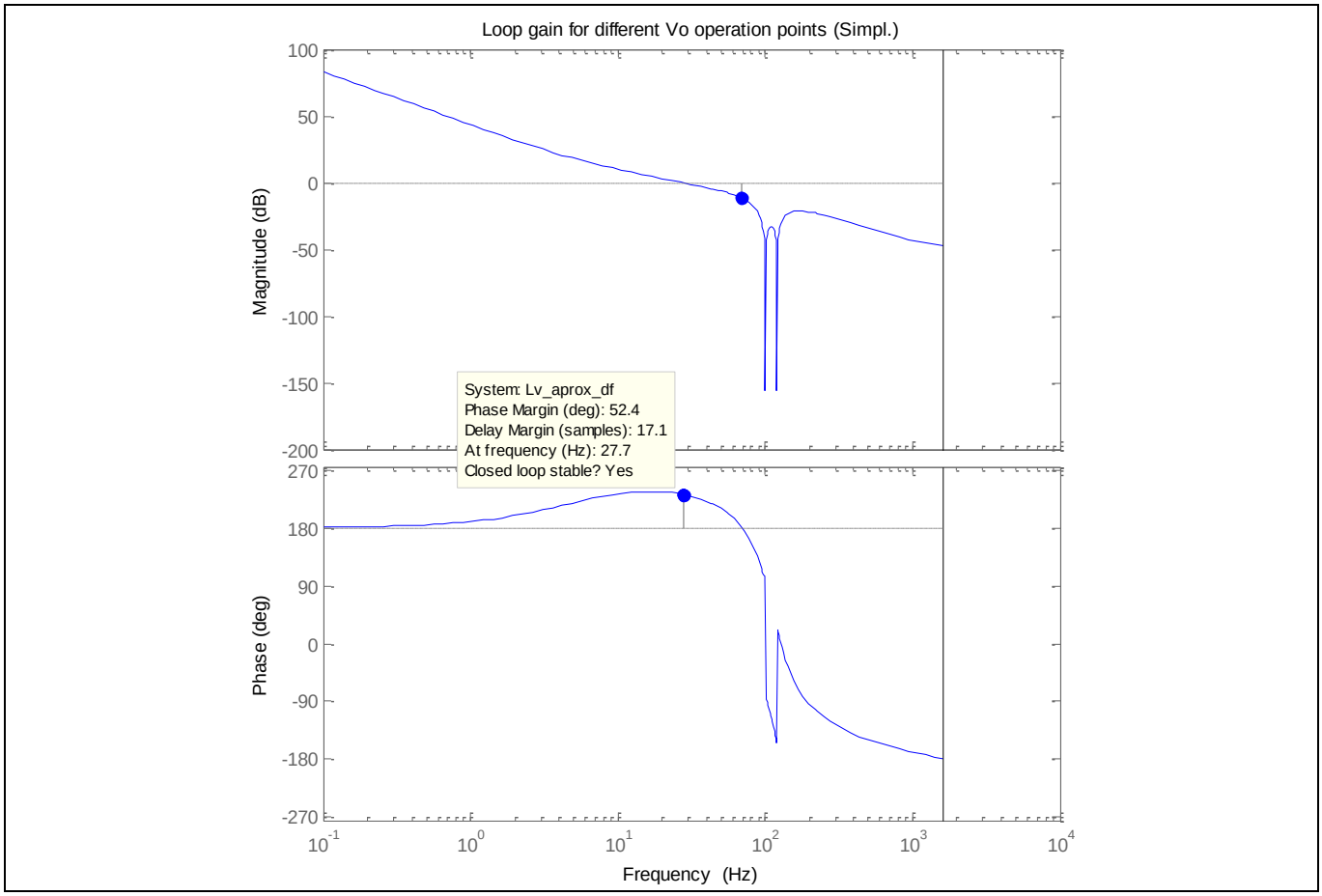


**Figure 24 Loop gain of the voltage control loop**

Despite the achieved BW in the proposed implementation, under certain situations such as load jumps or PLD the bulk voltage can over- or under-shoot, leading to different issues such as instability or maximum voltage violation. Furthermore, the bulk voltage level directly affects the DC-DC converter operation. For these reasons the bulk voltage is monitored as part of the state machine presented in Figure 16. Three main actions are implemented in this monitoring:

- In case of over-shoot (programmable level), the PWM is off until the sensed voltage returns to the target value.
- If the sensed voltage is under a certain defined level, the current reference is increased by a factor of 4 until the sensed voltage reaches a higher limit.
- In case the sensed voltage is under 333 V, the PFC is turned off and its operation is resumed with soft-start after a defined time. This causes the DC-DC converter to be turned off as well.

The digital implementation also enables a modification of the PFC output voltage target according to the delivered output current/power. This voltage directly influences the DC-DC converter switching frequency, since it is a frequency-controlled resonant converter.

Figure 25 shows the implemented voltage target variation used in the 800 W server power supply. The output current information is sent from the secondary to the primary controller via UART through a digital isolator. As a side-effect of this implementation, a higher voltage at full power gives extra voltage in case of ACLDO.

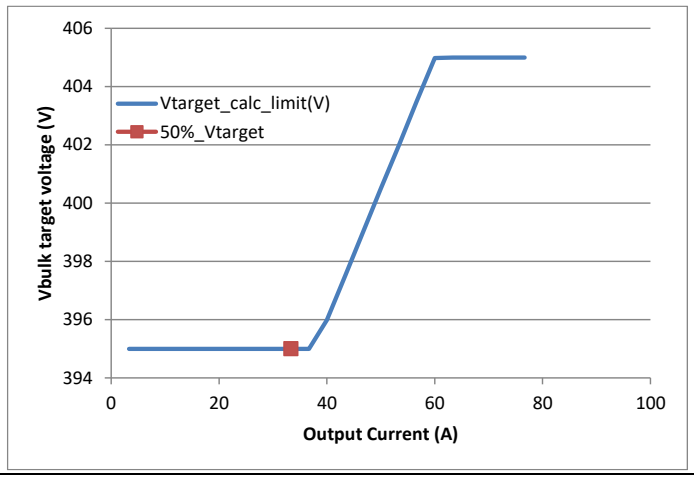


**Figure 25 Bulk voltage variation for efficiency optimization**

# 4 LLC resonant DC-DC converter

The DC-DC stage of the 800 W server power supply is a half-bridge LLC resonant converter with split capacitors and center-tap transformer configuration. The implemented topology is depicted in Figure 26, which includes 600 V CoolMOS™ P7, 40 V OptiMOS™, EiceDRIVER™ 1EDI20N12F and 2EDN7524F, ISOFACE™ 4DIR1400H and XMC4200 as a controller. Since the selected microcontroller is located on the secondary side, a digital isolator is used for communication with the PFC controller. In addition, the inclusion of this digital isolator allows the PWM signals to be sent to the half-bridge drivers without using pulse transformers. The DC-DC stage also includes the O-ring switch.

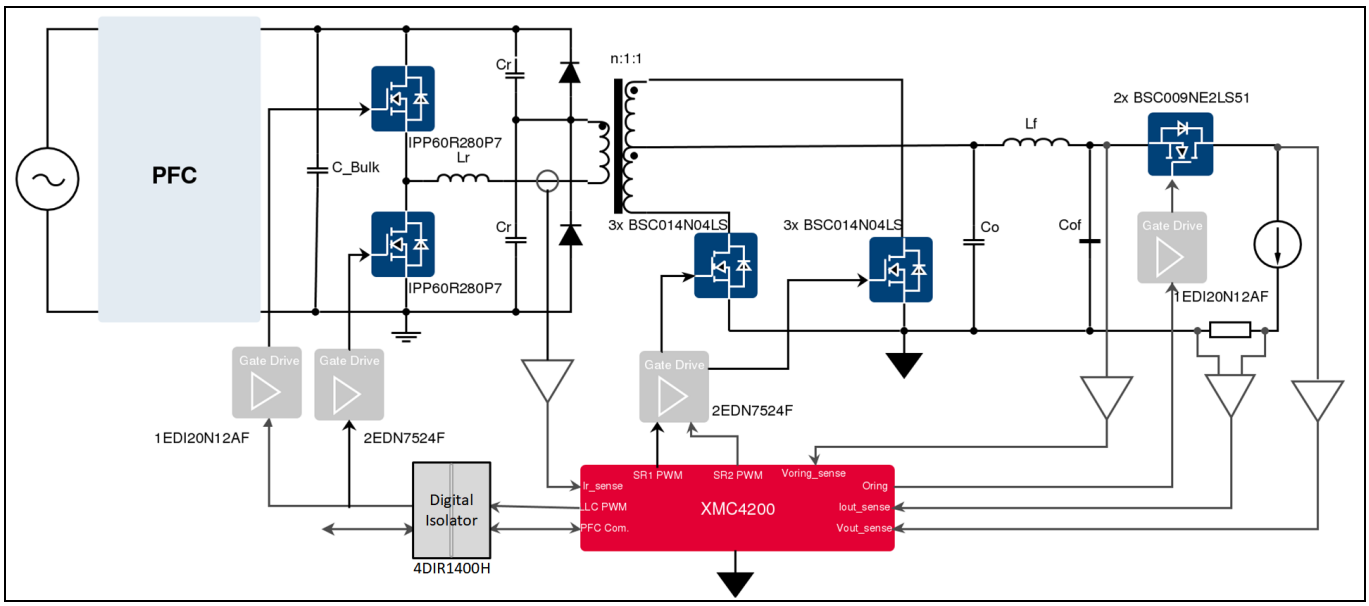


**Figure 26 800 W PSU LLC topology with sensing and Infineon devices**

## 4.1 Resonant tank design

The design of the LLC converter involves several steps in a well-defined design flow, as introduced in [6]. In the case of the server power supply shown in this document, the input voltage variation is influenced by the selected bulk capacitor in case of loss of the AC input voltage. In these conditions the maximum gain of the LLC operation is required, since the lowest input voltage must be boosted to the specified regulated output voltage. With this consideration and a resonant frequency target close to 150 kHz, the resultant tank parameters are:

- Resonant inductance: Lr = 9 µH, with 1 µH coming from the transformer stray inductance
- Resonant capacitance: Cr = 132 nF, in split capacitor configuration
- Magnetizing inductance: Lm = 169 µH

Considering the parameters shown, the gain curve at full load is shown in Figure 27, together with the maximum required gain.

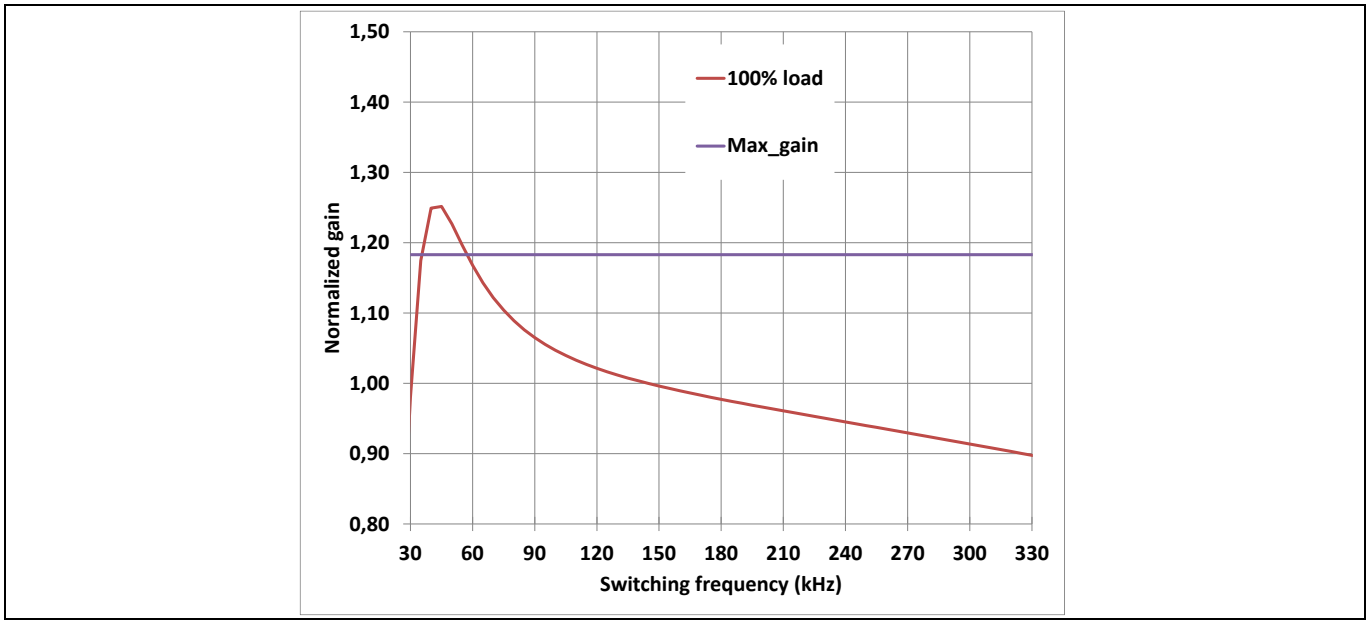


**Figure 27 Normalized gain curve at full load and maximum required gain for the LLC converter of the 800 W server power supply**

### 4.1.1 Transformer and resonant inductor

Two main value drivers for the server power supply shown are high performance and power density. The main transformer and the required resonant inductance have been integrated with these parameters in mind. The resulting magnetics integration, which takes advantage of the flux cancellation, is shown in Figure 28.

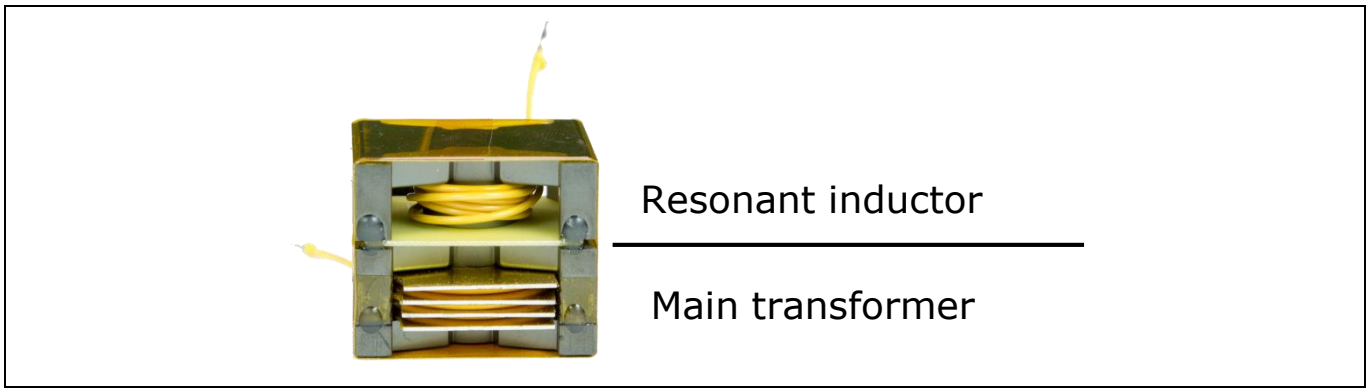


**Figure 28 Main transformer and resonant inductor integration**

The transformer and resonant inductor are both built using PQI35/23 cores. The secondary windings are implemented using 0.6 mm thickness copper foils. The primary-side turns are wound between the copper foils, thus improving the transformer coupling, using 7 × 0.3 mm litz wire. The same wire is used for the resonant inductor turns, which are in series with the transformer primary windings.

## 4.2 Driving scheme

The driving scheme of the server power supply can be cost-optimized by using the galvanically isolated driver (1EDI) and the non-isolated dual-channel driver (2EDN) provided by Infineon Technologies. Figure 29 shows the implemented driving scheme in the 800 W server power supply with 600 V CoolMOS™ P7.

As can be seen, one non-isolated dual-channel driver is used for the SR driver. The same part is used on the primary side to drive the grounded transistors: one channel for the PFC MOSFET, and another channel for the low-side switch of the LLC converter. For those transistors that are not grounded, i.e., the high-side switch in the LLC half-bridge and the O-ring switch, an isolated driver is used.

The different time behavior of the two different drivers used in the LLC half-bridge implies asymmetries in the applied PWM if the PWM timing is not properly adjusted. The implemented SW in the secondary controller (XMC4200) considers the timing difference of the different drivers in the systems to ensure safe operation of the LLC converter, both in the primary half-bridge and the secondary SR.

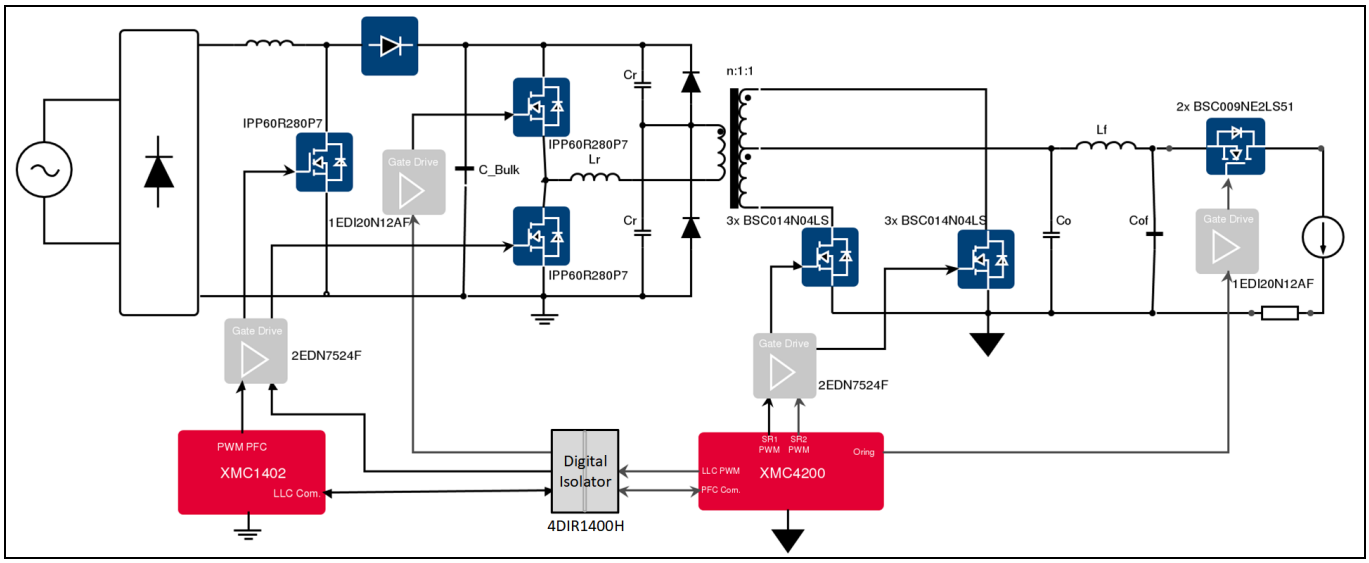


**Figure 29 Driving scheme of the 800 W PSU with 600 V CoolMOS™ P7**

## 4.3 Isolation partitioning on the control board

The recently released ISOFACE™ 4DIR1400H digital isolator has been used in EVAL_800W_PSU_3P_P7 to implement the isolation partitioning on the control board. The isolator device is based on coreless transformer technology, enabling robust data transmission and safe behavior.

Each side of the digital isolator can be independently supplied with a voltage between 2.7 V and 6.5 V. In this case, the primary and secondary sides are supplied with 3.3 V, as shown in the schematic (see Figure 30).

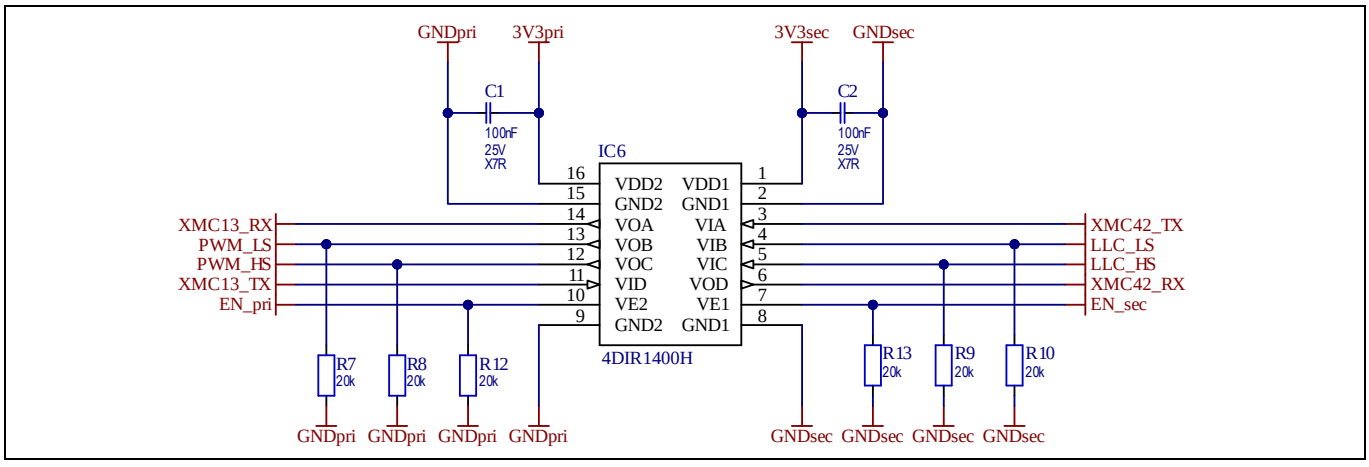


**Figure 30 Schematic implementation of ISOFACE™ 4DIR1400H**

Compared to similar devices, ISOFACE™ 4DIR1400H offers higher reliability (VISO = 5700 Vrms according to UL 1577) and high CMTI > 100 V/ns. Input pull-down resistors allow for default and defined startup state of the signals, which is highly required when transferring PWM signals with low and precise propagation delay. An internal deglitch filter also detects and bypasses any glitch on the input side with a pulse duration <10 ns, preventing the transfer of unwanted noise from the primary to the secondary side and vice versa.

Eventually, the improved delay performance of the ISOFACE™ compared to similar competitor parts allows for an increased timing budget to improve the safety margin or reduce dead times.

Table 4 compares the timing performance between the ISOFACE™ 4DIRx40xH product family and the equivalent competitor part.

Further information about designing with Infineon ISOFACE™ digital isolators can be found in [8].

**Table 4 Timing specification of ISOFACE™ 4DIRx40xH vs competitor parts**

| | | | ISOFACE™ 4DIRx40xH | | | Equivalent competitor part | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Unit** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** |
| $t_{PD,on}$ $t_{PD,off}$ | Input-to-output propagation delay | ns | 22.0 | 26.0 | 33.0 | 50.0 | 75.0 | 100.0 |
| $\Delta t_{PD,p-p}$ | Part-to-part propagation delay mismatches | ns | - | - | 3.0 | - | - | - |
| $\Delta t_{PD,ch-ch}$ | Codirectional channel-to-channel propagation delay mismatch | ns | - | - | 3.0 | - | - | 50.0 |
| PWD | Pulse width distortion | ns | - | - | 3.5 | - | - | 40.0 |
| $t_{PW,min}$ | Minimum pulse width [ns] | ns | 8.0 | 12.5 | 15.0 | 1000.0 | - | - |

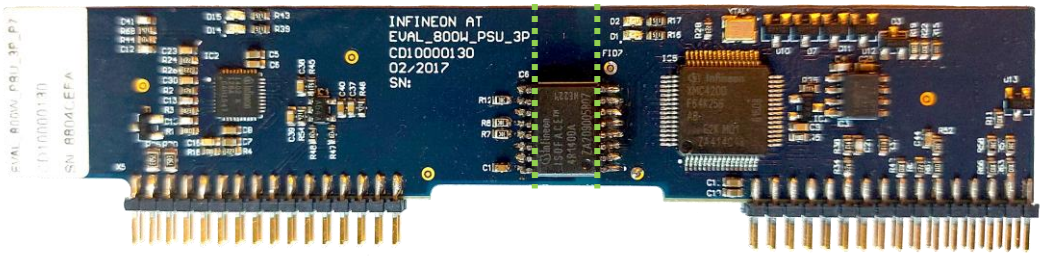


**Figure 31 Overview of the isolation partitioning (green) on the control board – top side**

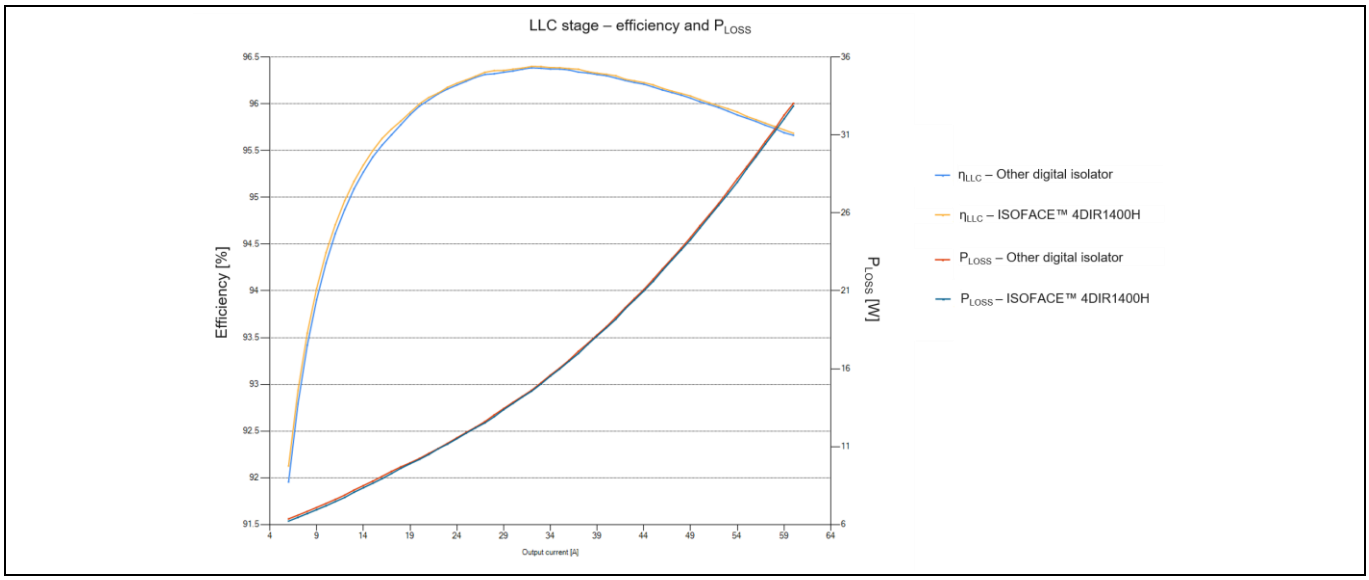


**Figure 32 Efficiency η and losses of the LLC stage with 4DIR isolator and equivalent competitor part**

Robustness of ISOFACE™ 4DIR1400H against common-mode voltages has been tested in abnormal conditions on the EVAL_800W_PSU_3P_P7. Power line disturbances have been applied to the PSU with ISOFACE™ 4DIR1400H as described in Section 6.3 and reported in Figure 33, Figure 34, Figure 35, and Figure 36.

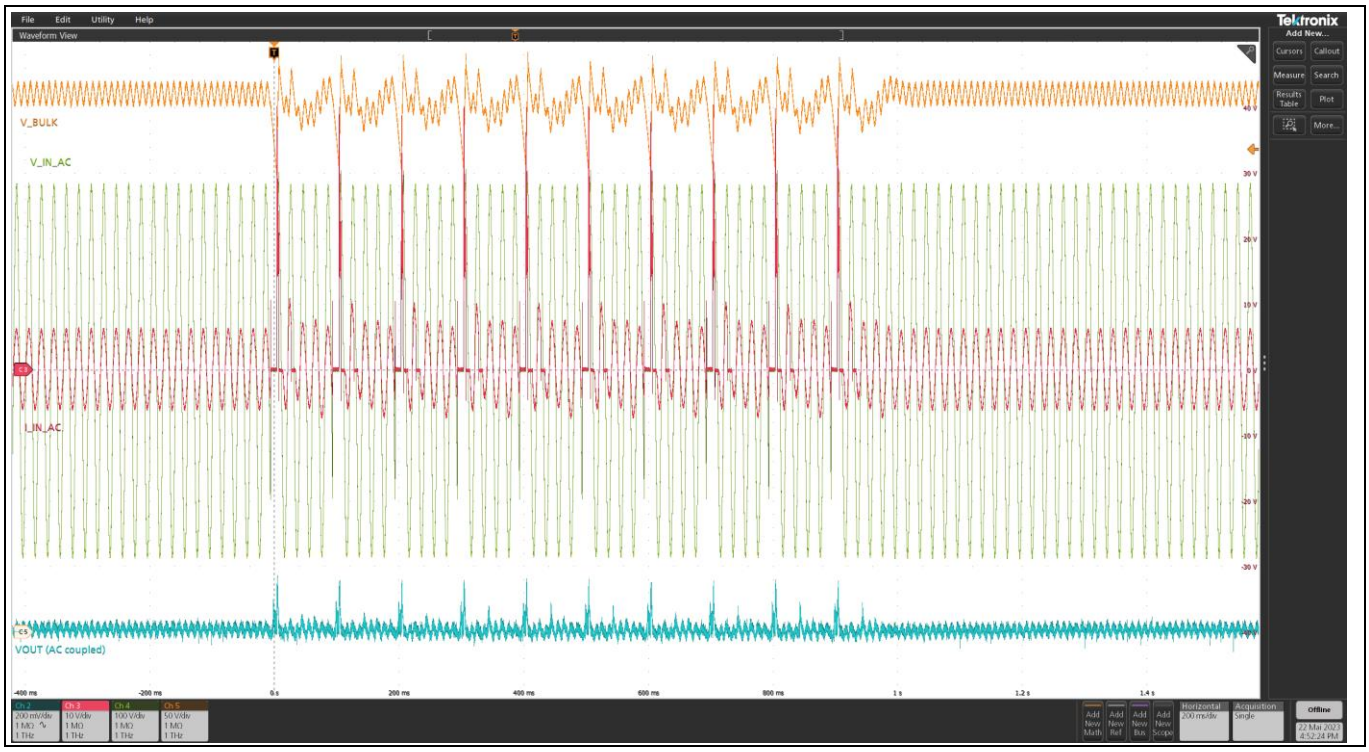


**Figure 33 AC line cycle drop out behavior with ISOFACE™ 4DIR1400H (10x, $V_{AC.RMS}$ = 200 V, 45°)**

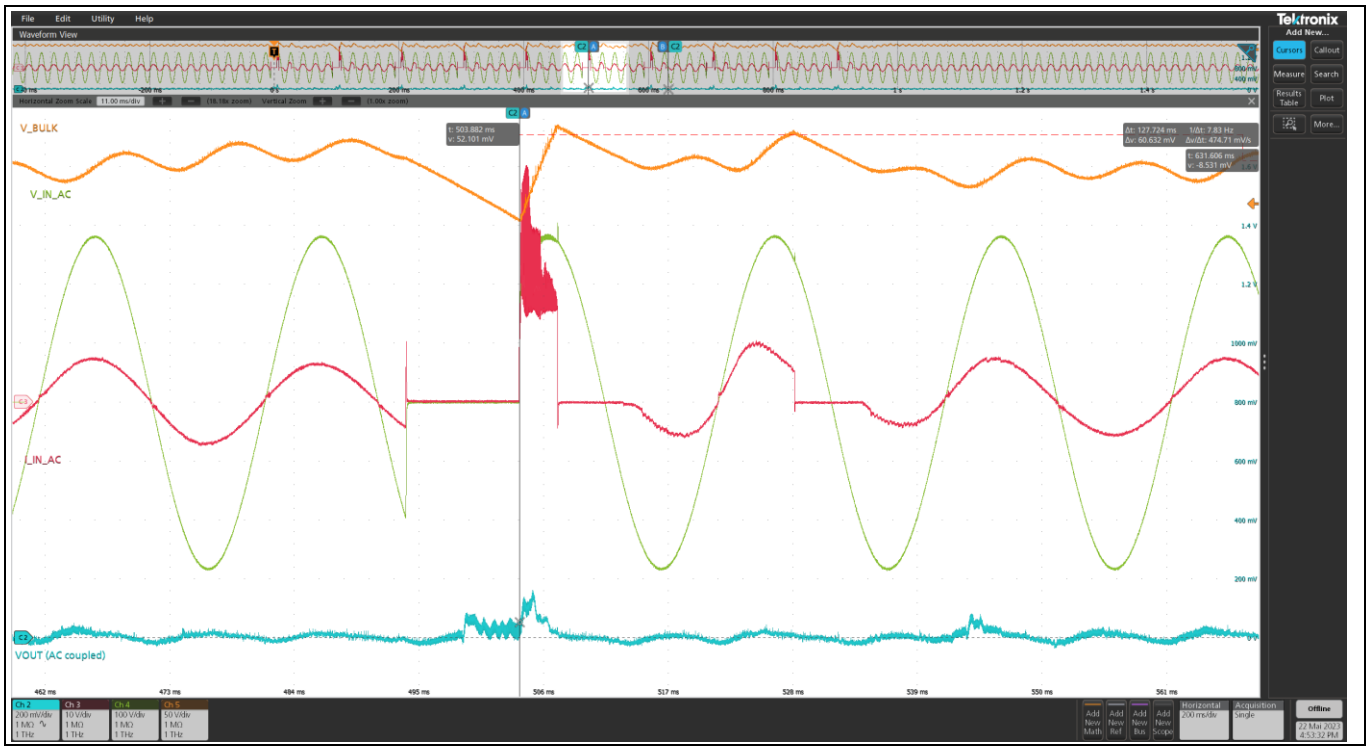


**Figure 34 AC line cycle drop out - zoom Figure 33**

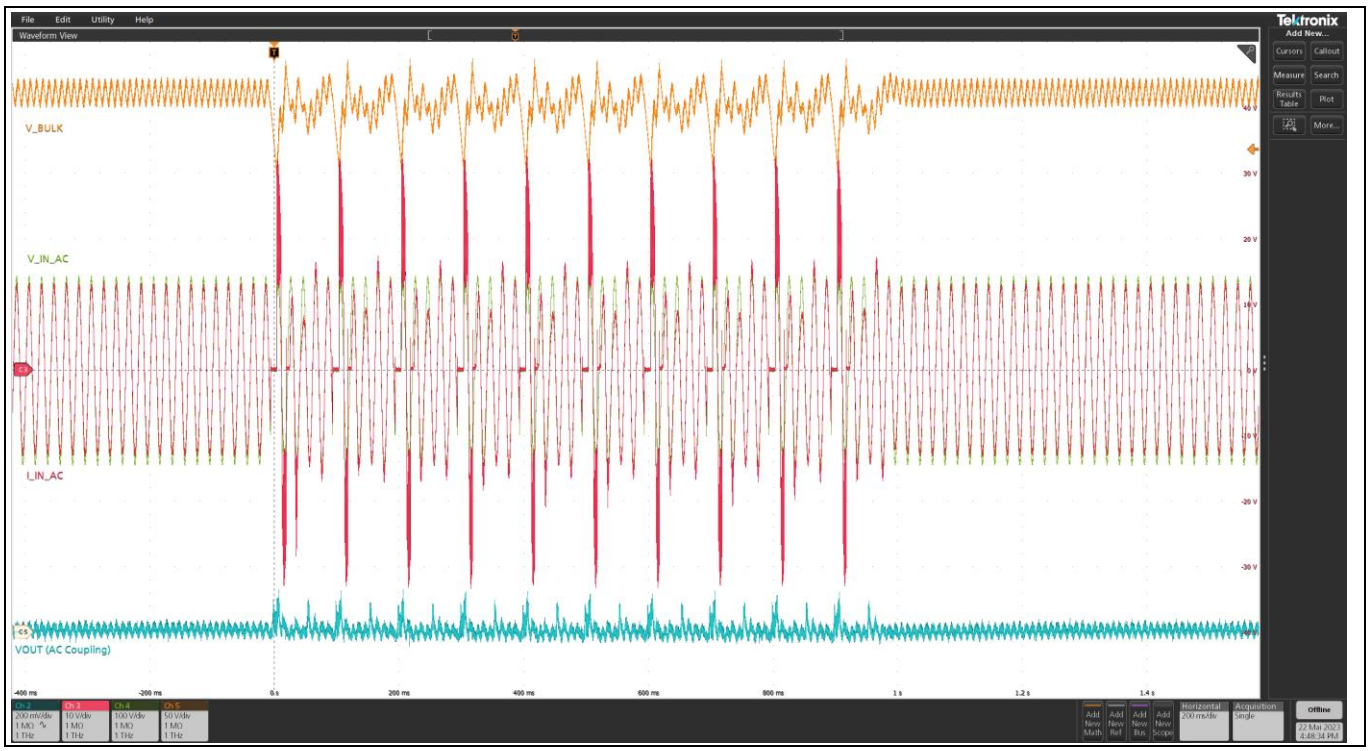


**Figure 35 AC line cycle drop out behavior with ISOFACE™ 4DIR1400H (10x, $V_{AC.RMS}$ = 100 V, 45°)**

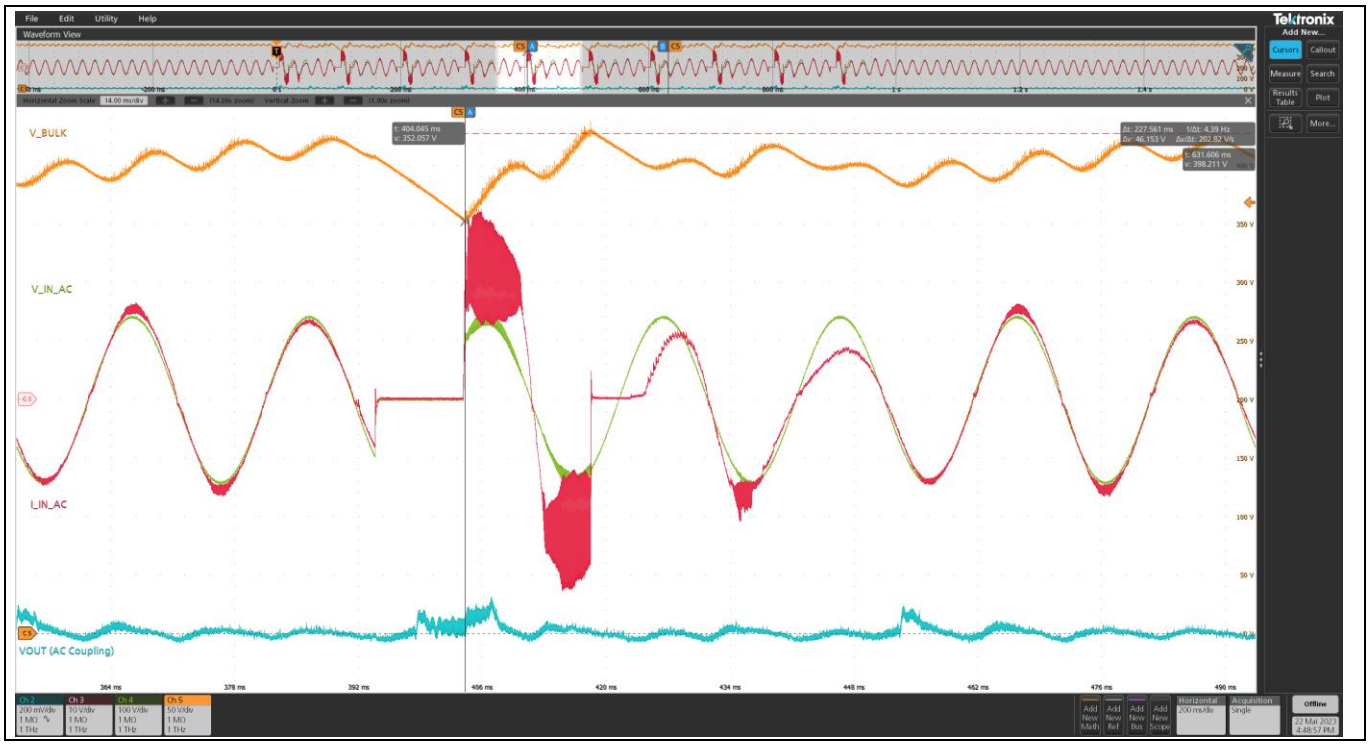


**Figure 36 AC line cycle drop out - zoom Figure 35**

## 4.4 XMC™ configuration and functional description

As shown in Section 2.2.6.2, the control of the DC-DC stage in the 800 W server power supply is implemented in a XMC4200. Figure 37 shows a block diagram of the HW (red) and SW (blue) resources used for the control implementation.

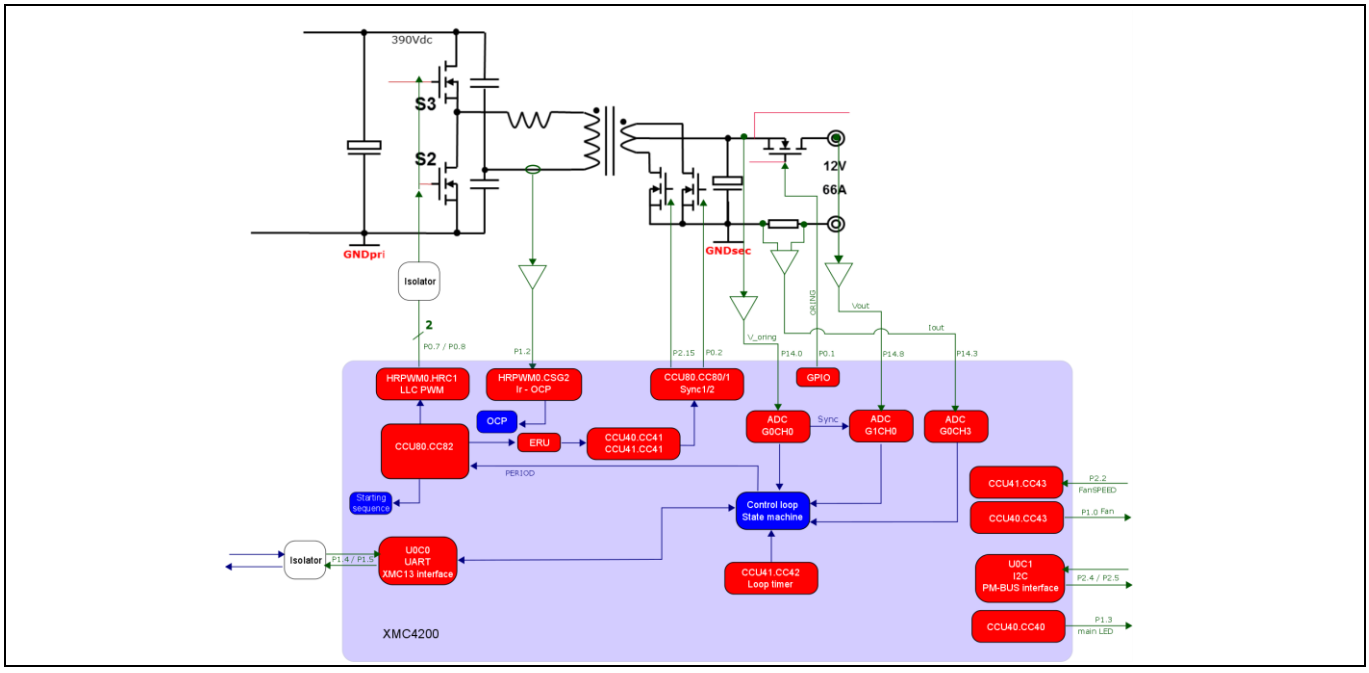


**Figure 37 XMC4200 configuration for the LLC converter of the 800 W server power supply. Red – HW blocks (peripherals); blue – SW blocks.**

As a resonant converter, the LLC requires frequency modification (60 –300 kHz) to regulate voltage. Therefore, if the control loop is synchronized with the switching frequency, the necessary operations for control-loop calculation must be executed within a maximum time corresponding to the minimum switching period. In addition, more functions than the control loop are typically implemented in the controller, complicating the control synchronization and switching frequency. This is why a fixed-frequency interrupt (100 kHz) should be included to implement the following functions, which will be covered in this section:

- Overvoltage Protection (OVP)
- Overcurrent Protection (OCP)
- Receive information from the primary-side controller
- State machine
- Voltage controller
- Burst mode detection
- Send information to the primary-side controller

### 4.4.1 Sensing

Proper operation of the LLC converter requires sensing of the output voltage, both before and after the O-ring switch, since it is the variable to be controlled. In addition, the output and resonant current are necessary for OCP, and the input voltage is used for brown-out protection.

- Resonant current and short-circuit protection

The resonant current is sensed using a current transformer, and the signal is rectified afterward. The obtained voltage is connected to the internal analog comparator of the high-resolution PWM module [7], which includes an internal DAC. The DAC is programmed to a constant value, which is reached only in case of short-circuit. If this comparison happens, the converter operation is frozen and a microcontroller reset is necessary to resume operation.

- Input voltage

The microcontroller is located in the secondary-side ground, which is a problem when sensing the bulk voltage (LLC input voltage). Nevertheless, this information is available in the primary-side controller for the PFC control. The XMC4200 receives the input voltage information via UART through the digital isolator. The communication rate is fast enough for the proper operation of the brown-out protection of the LLC, but slow enough to minimize noise problems.

- Output current and voltages

The rest of the variables mentioned, output voltages and current, are sensed using the ADC of the secondary-side controller. The XMC400 series ADC enables an external reference to be used via channel 0 of the ADC [7]. In this case a high-accuracy 2.5 V reference is used, to minimize the production tolerances.

Furthermore, the output voltages before and after the O-ring switch are acquired at the same time by using the channel synchronization of the versatile ADC of the XMC™ microcontroller [7]. After these voltages are sensed, the output current is also acquired. The output current information is sent to the primary-side controller via UART (full-duplex) communication. This information is used to modulate the bulk voltage, as explained in the PFC section.

As in the case of the PFC, the ADC is triggered with the second available compare register of the CCU8 unit, which is generating the half-bridge driving signal (Figure 38). With this configuration, the different variables are sensed every switching cycle in a noise-free environment.

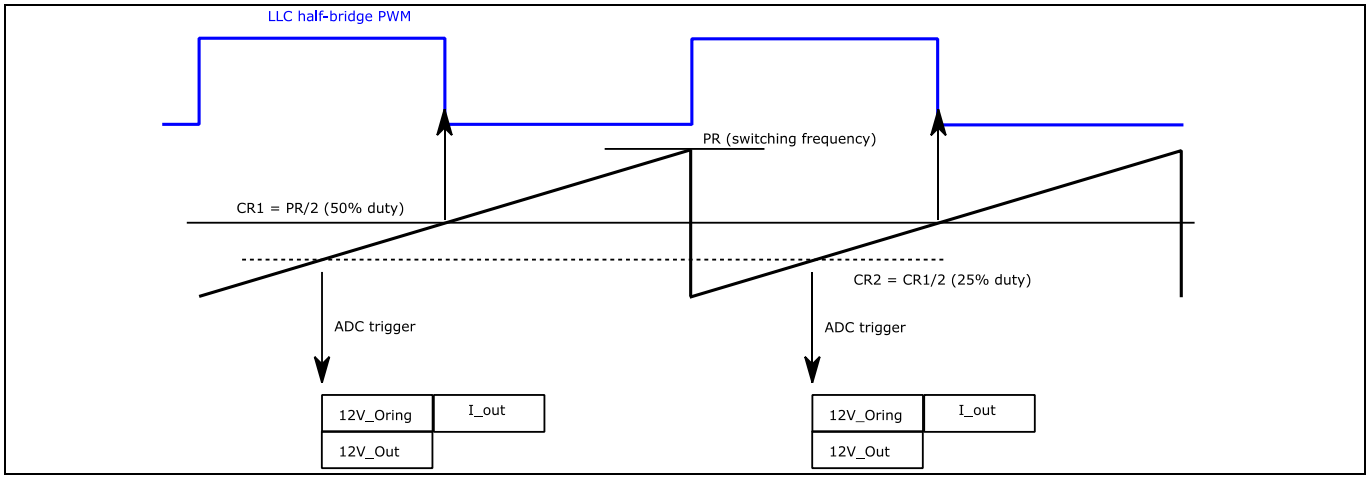


**Figure 38 ADC time schedule**

## 4.4.2 XMC™ configuration for CoolMOS™ and OptiMOS™ safe operation

The required timing for the SR switches with regard to the half-bridge operation is different if the LLC converter operates in under- or above-resonance conditions [6]. Despite the SW considering this timing, abrupt switching frequency changes can happen in case of dynamic situations, i.e., load jumps, which might lead to timing mis-match and device stress.

Different HW configurations have been implemented, taking advantage of the XMC4200 peripherals' flexibility and connectivity, in order to avoid SR cross-conduction or timing mis-match between primary and secondary driving signals in these conditions. The connection of the required timers is shown in Figure 40.

The main timer sets the switching frequency according to the voltage controller. This information is used in the High Resolution PWM module (HRPWM in Figure 40), which enables the modification of the dead-time safely and synchronously with the frequency change. The dead-time of the half-bridge LLC is modified, as shown in Figure 39, according to the switching frequency, to guarantee ZVS operation under any operating condition.

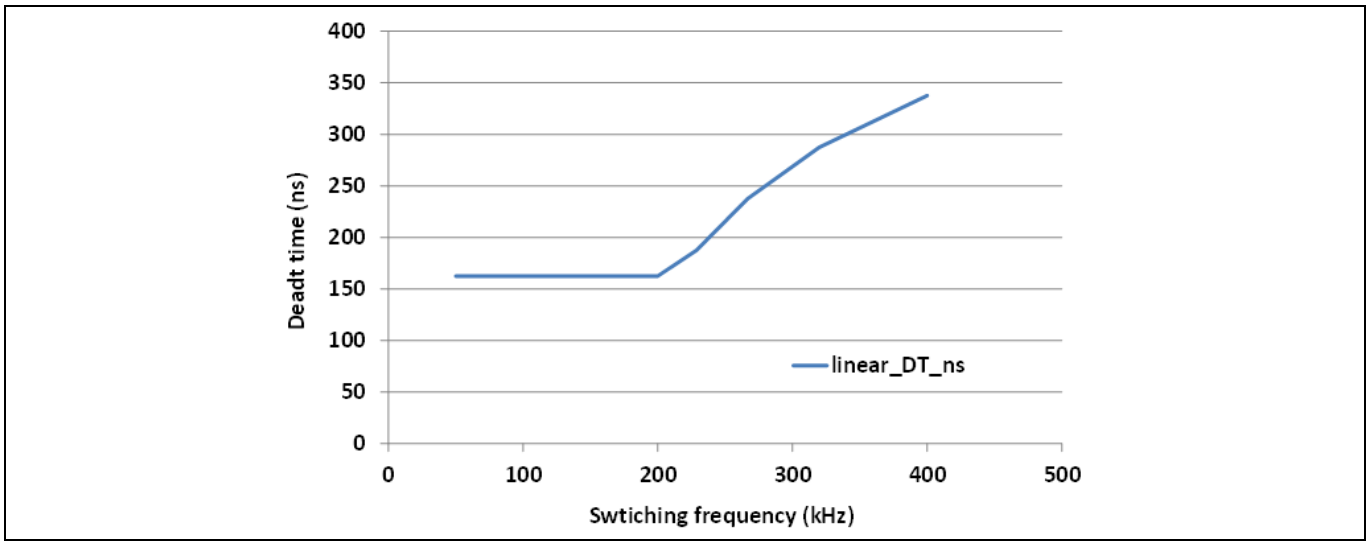


**Figure 39 Dead-time modification according to switching frequency of the half-bridge LLC**

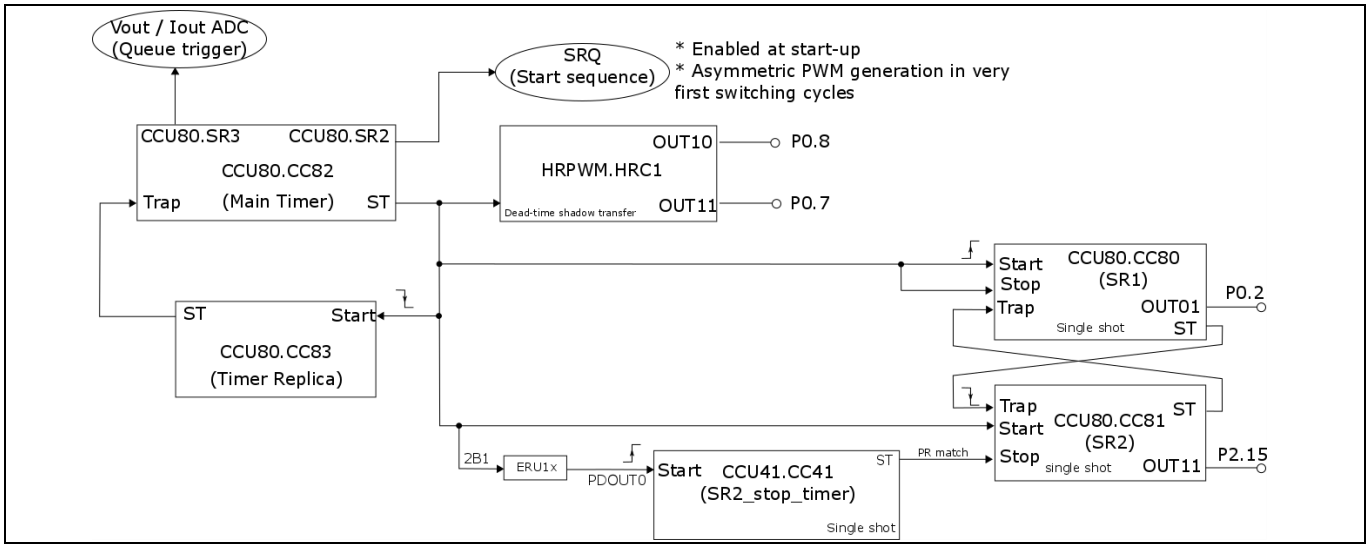


**Figure 40 Timer configuration for the LLC of the 800 W power supply with 600 V CoolMOS™ P7**

The same main timer information is sent to the SR timers, which are configured in single-shot mode, i.e., the timer counts once to the period every time a start-signal arrives. With this information the SR timers are started synchronously to the main timer and the turn-on delay is adjusted by SW. The turn-off time is controlled by the SW, but a HW limitation linked to the main timer is introduced. In this case, an intermediate timer (SR2_stop_timer in Figure 40) is included, considering the possible delay between primary and secondary signals in the driving scheme, as well as the driving scheme asymmetry introduced in Section 4.2. This connection is possible due to the Event Request Unit (ERU) available in the XMC4000 series, which enhances the peripheral connectivity. In addition, the SR timers are configured to trap each other, thus minimizing possible cross-conduction due to asynchronous timing changes motivated by the single-shot behavior. Figure 41 shows a no-load to full-load jump with no drain-source voltage spikes in the 40 V secondary side OptiMOS™ during the transition, according to the peripheral/SW configuration shown.

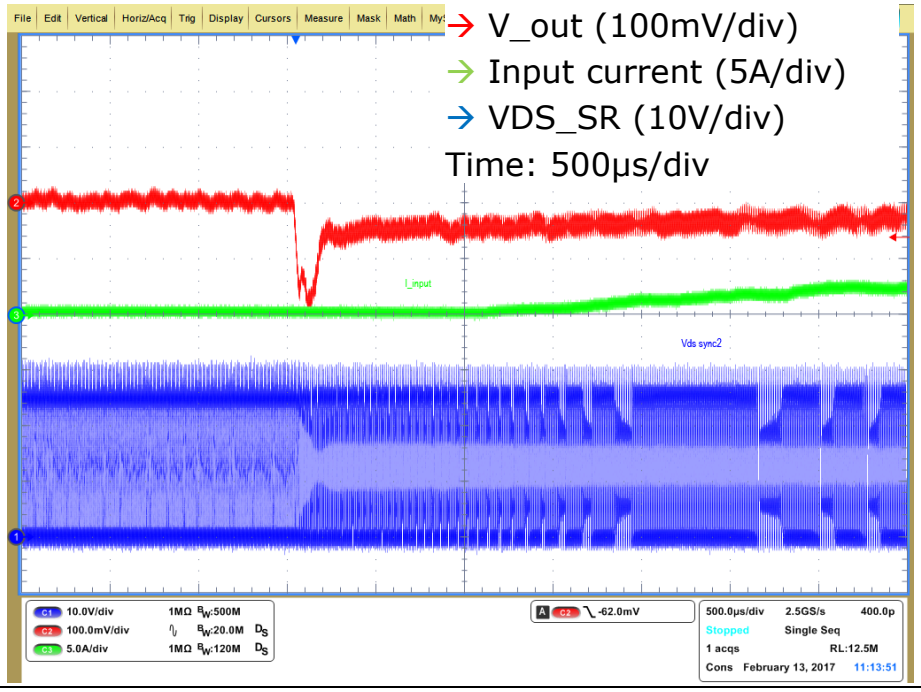


**Figure 41 No voltage spikes during the no-load to full-load transition**

Under certain operating conditions the LLC half-bridge must be turned off, and this transition must happen without voltage or current stress in the converter. In these conditions, it is possible to find burst mode operation or input voltage brown-out, as well as remote on/off command.

Again, using the main timer as a base, a timer-replica is generated, and the output signal of this timer is used to trap the main timer (Figure 40). Since the status of the timer-replica is synchronous with the main timer, the primary PWM signal can be turned off synchronously at the end of a switching cycle, and the same happens when the converter operation is resumed, i.e., during burst mode operation. Figure 42 shows the moment when the LLC converter is turning off based on an external off signal. As can be seen, no voltage stress is suffered by the SR switch.

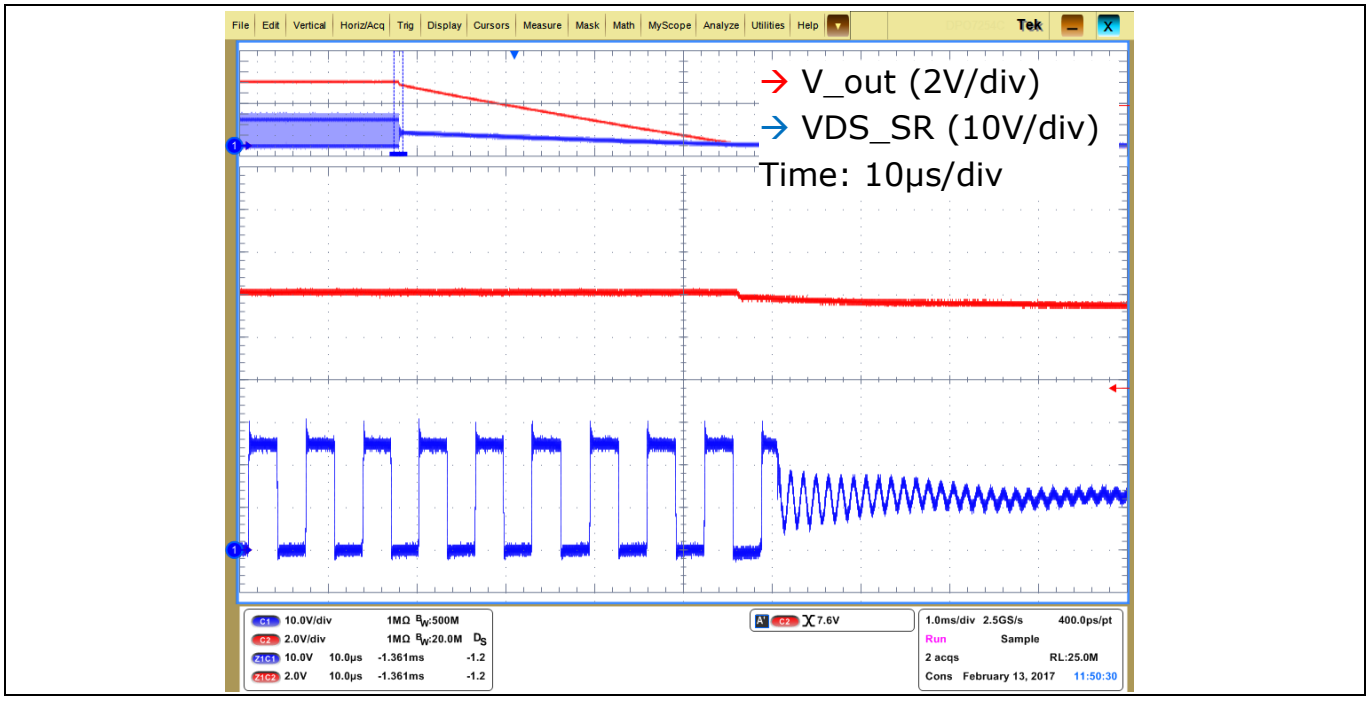


**Figure 42 LLC converter turn-off happens synchronously at the end of the switching cycle without voltage stress**

## 4.4.3 Voltage controller and state machine

The control implementation of the LLC converter in the XMC4200 is based on a PID controller, which modifies the switching frequency of the converter in order to regulate the output voltage. The controller must be designed to fulfill the output specifications considering the load variation and the wide input voltage range. This is probably the main concern when designing the controller, since the bulk voltage can change from 330 V to 430 V, at any load condition.

Figure 43 shows the voltage controller block diagram, which includes a soft-start path. During soft-start an open-loop linear variation of the switching frequency is applied, i.e., the frequency is linearly decreased toward the minimum allowed frequency. In parallel, the voltage loop (PID controller) is executed with a constant reference, which corresponds to the desired output voltage. The transition from open-loop to closed-loop operation is done either when the output voltage error is under a defined range, or when the closed-loop frequency is higher than the open-loop one.

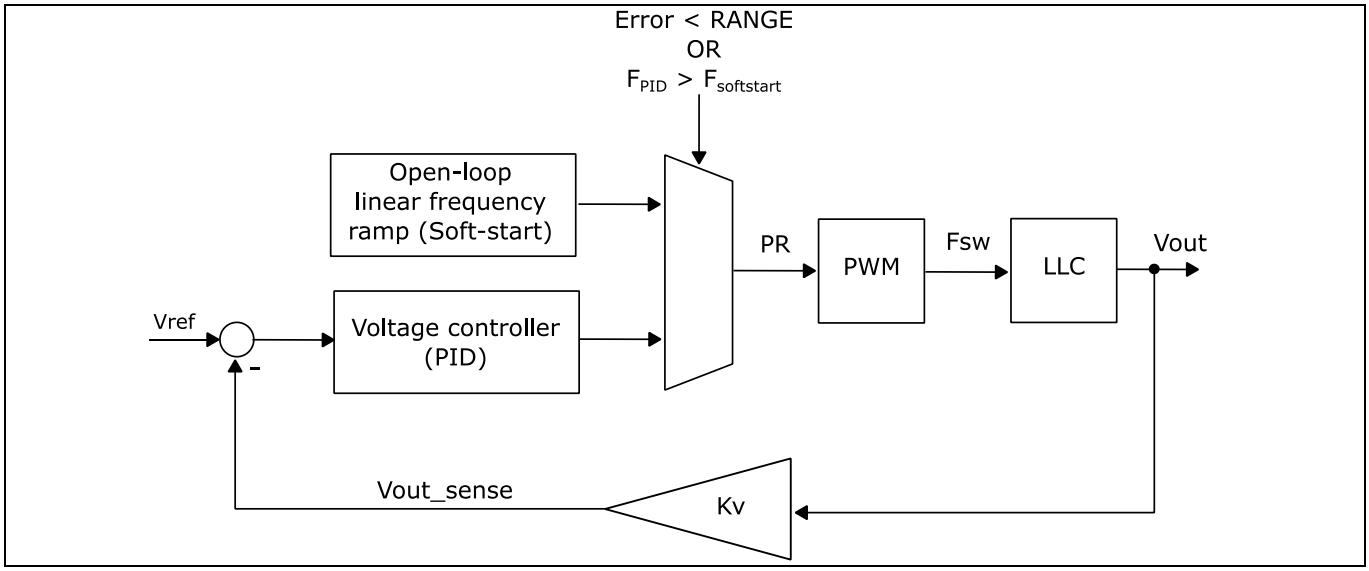


**Figure 43 LLC voltage-loop diagram block, including soft-start path**

The presented soft-start is integrated in a state machine (Figure 44) that controls the different operating conditions of the DC-DC stage in the 800 W server power supply. Apart from the start-up sequence and soft-start, the SR management, the O-ring switch control, burst mode detection and converter restart in case of input and output protections are considered in the state machine. In addition, a remote on–off functionality is integrated, according to an external signal that can be managed by a switch incorporated into the load connector board (Figure 7).

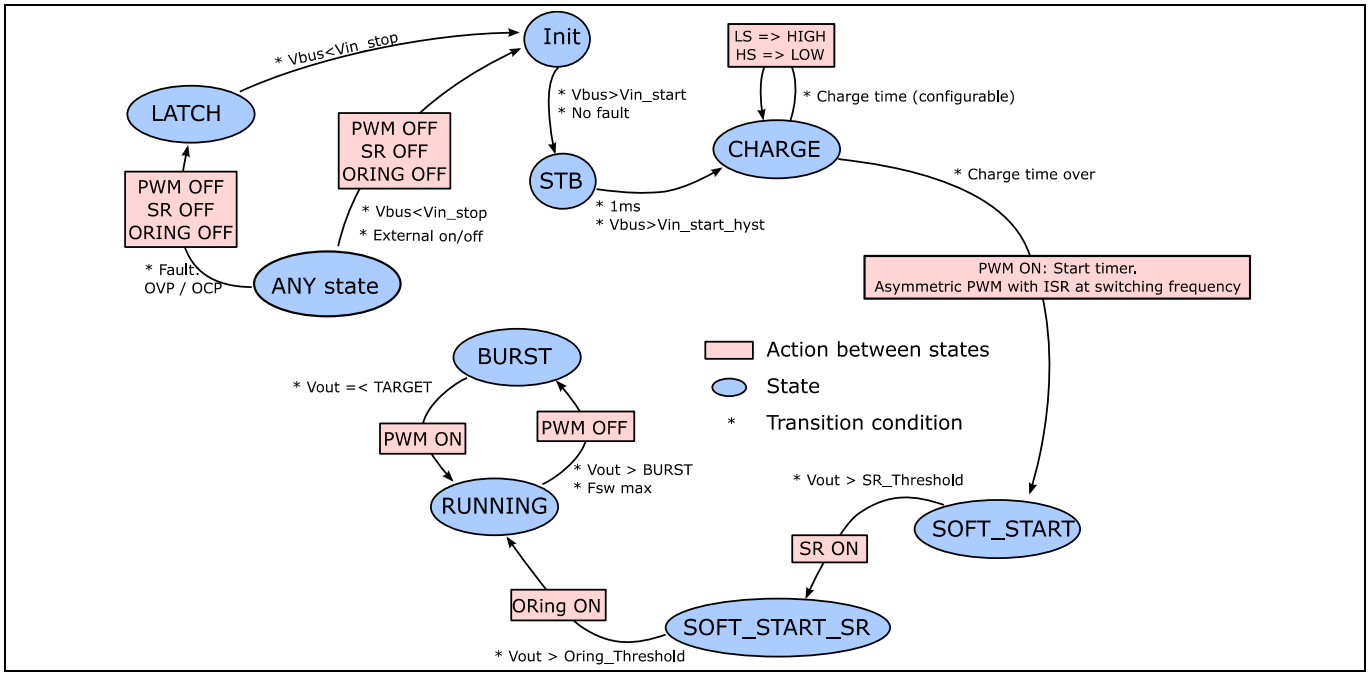


**Figure 44 LLC state machine**

Figure 45 depicts the output voltage variation during start-up, when the state machine shown in Figure 44 is applied, which includes the soft-start architecture shown above. During this process, the output voltage is monitored in order to decide when the SR switches are turned on (in the beginning they behave as diodes) as

well as the point where the O-ring switch is closed. Both decisions are taken when the output voltage reaches 10 V and 11.5 V respectively, as marked in Figure 45.

*Note: No special function is applied to the O-ring switch, since the implemented SW is not intended for hot-plug or parallel operation.*

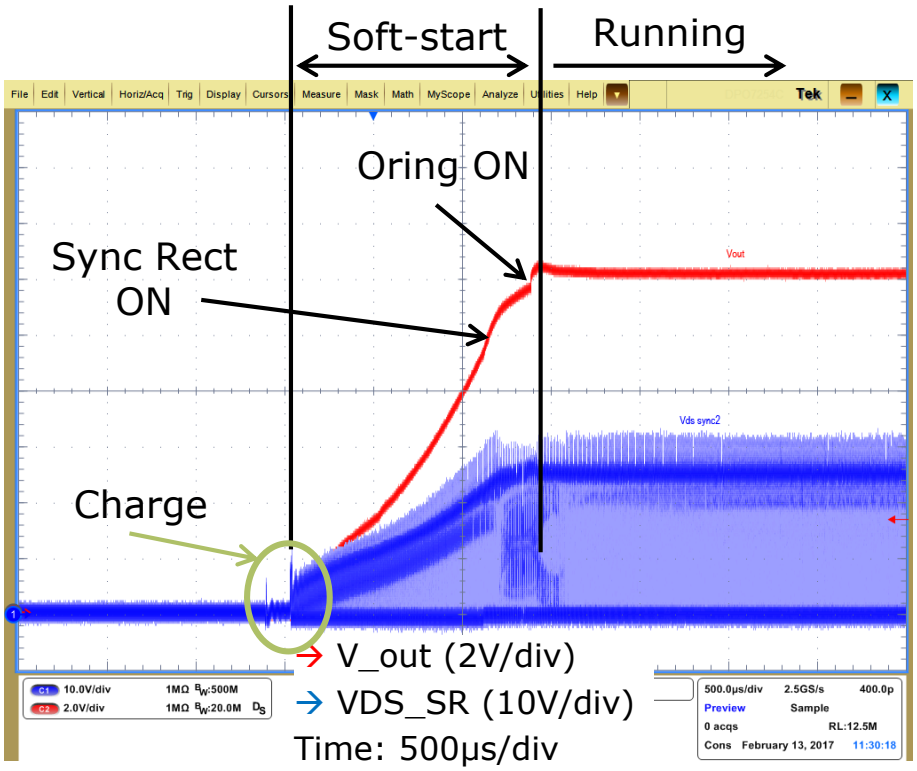


**Figure 45 Output voltage during start-up of the LLC of the 800 W server power supply**

The implemented driving scheme in the LLC converter of the 800 W power supply is based on a level shifter with bootstrap capacitor. This capacitor must be charged before the PWM starts in order to achieve proper operation of the converter.

Therefore, before the previously shown soft-start sequence begins, a long pulse is applied to the low-side switch of the LLC half-bridge. This pulse can be seen in the blue waveform of Figure 46, which shows the PWM and O-ring signals during start-up. In the detail view of the same figure, it can be appreciated how the PWM operation starts after this long pulse. A short period is introduced between the long pulse and PWM operation in which both half-bridge signals are at the low level to avoid half-bridge shoot-through.

In steady-state operation, LLC converter is controlled by modifying the switching frequency of a 50 percent PWM. However, the applied starting pulse to charge the bootstrap capacitor provokes a voltage imbalance in the resonant capacitors. This imbalance can originate hard-commutation situations if the resonant current is not allowed to change polarity before the active half-bridge switch is changed. To avoid this situation, a PWM with a duty cycle other than 50 percent is applied until the resonant capacitors are properly balanced, as shown in the detailed view of Figure 46. At that point, the soft-start process described above begins.

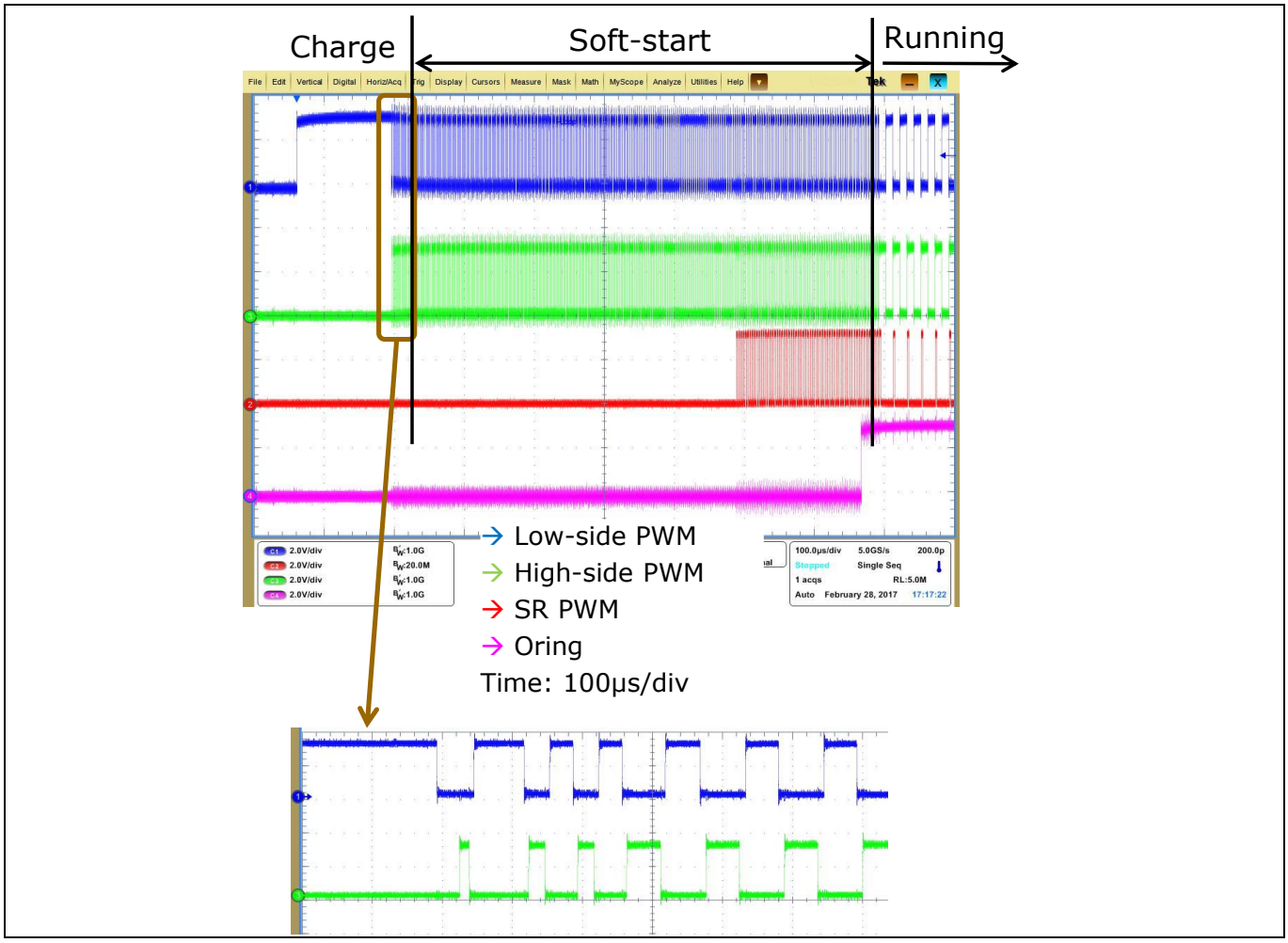


**Figure 46 Half-bridge (low-side and high-side) and SR PWM signals and O-ring signal during start-up. The bottom shows a detailed view of the first half-bridge PWM pulses.**

Burst mode operation is enabled when the applied switching frequency is at maximum, and the output voltage is over a specified offset (150 mV).

### 4.4.4 Protections and fan management

The LLC implements input and output protections as well as temperature protection and fan management.

As already shown, the input voltage (bulk voltage) is sensed by the primary-side controller and received by the LLC controller via UART. The received value is used for the brown-out protection: the converter is started when the bulk voltage reaches 390 V and turned off if the received voltage is under 330 V.

Regarding the output, both current and voltage protections have been included. In respect to the Over Voltage Protection (OVP), the LLC converter turns off if the output voltage reaches 14 V. The bulk voltage must go under 330 V (brown-out) for the LLC converter to restart.

OCP is divided into three different levels, with different times allowed for a given OC, as shown in Figure 47. The OCP is enabled after the soft-start phase in the state machine. As in the case of OVP, a brown-out is necessary for the LLC to restart after an OCP trigger.

An extra current protection is implemented based on the resonant current measurement, as explained in Section 4.4.1. This is meant to be a fast, HW-implemented protection in case of short-circuit operation.

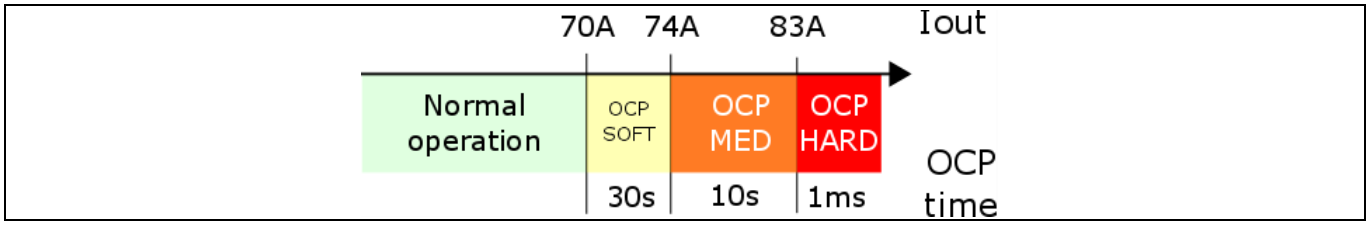


**Figure 47 OCP levels, with the time limit established for each**

Similar to the input voltage information, the temperature information is sent by the primary-side controller (XMC1402) via UART and the digital isolator. The heatsink temperature is acquired in the primary controller by means of a voltage partition, which includes a Negative Temperature Coefficient (NTC) thermistor. The received information is used to modify the duty cycle of the PWM applied to the fan, i.e., the speed of the fan, according to the graph shown in Figure 48.

The temperature information is also used for over-temperature protection. In this case, if the received temperature is over 120°C the LLC converter is turned off. The PFC converter maintains no-load operation with regulated bulk voltage. The DC-DC stage is restarted if the heatsink temperature drops under 100°C.

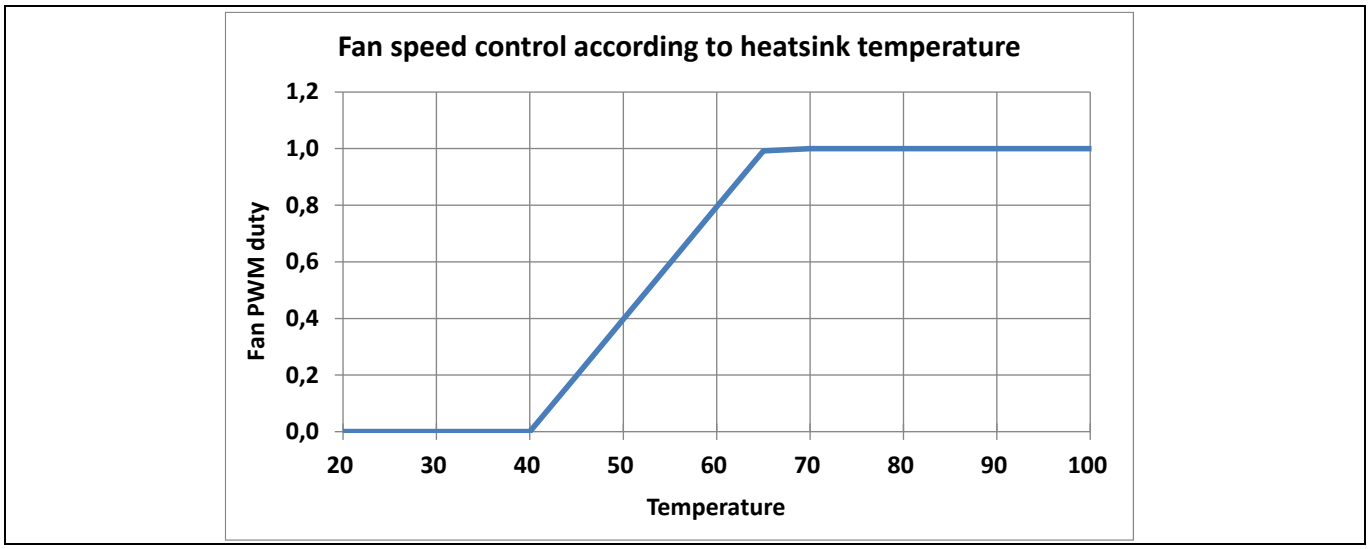


**Figure 48 Fan speed variation with respect to the heatsink temperature**

# 5 Auxiliary converter

The auxiliary power supply provides the required bias supplies for the control and driving circuitry of both primary and secondary converters. The auxiliary converter has been specifically designed for the 800 W server power supply using the QR Flyback controller ICE2QR2280G CoolSET™. In this case a Surface Mount Device (SMD) is utilized to fit in the power supply form factor, since the bias converter is implemented directly in the main board.

Note that no output of the auxiliary supply is available in the output connector, but all the generated supplies are used internally in the server power supply. The fan is supplied directly from the LLC output voltage, rather than using an extra winding in the auxiliary power supply. Efficiency is the reason for this configuration, since the necessary 3.3 W to drive the fan at maximum speed would be processed with around 80 percent efficiency in the auxiliary power supply, against the achievable 96 percent for the same power in the LLC converter.

The auxiliary converter concept is shown in Figure 49. The XMC4200 voltage supply (3.3 V_sec) is directly regulated and the rest of the supplies are generated by using the proper turn ratio. The primary-side controller supply voltage (3.3 V_pri) is generated from a 13 V winding using the linear voltage regulator IFX1117MEV33.

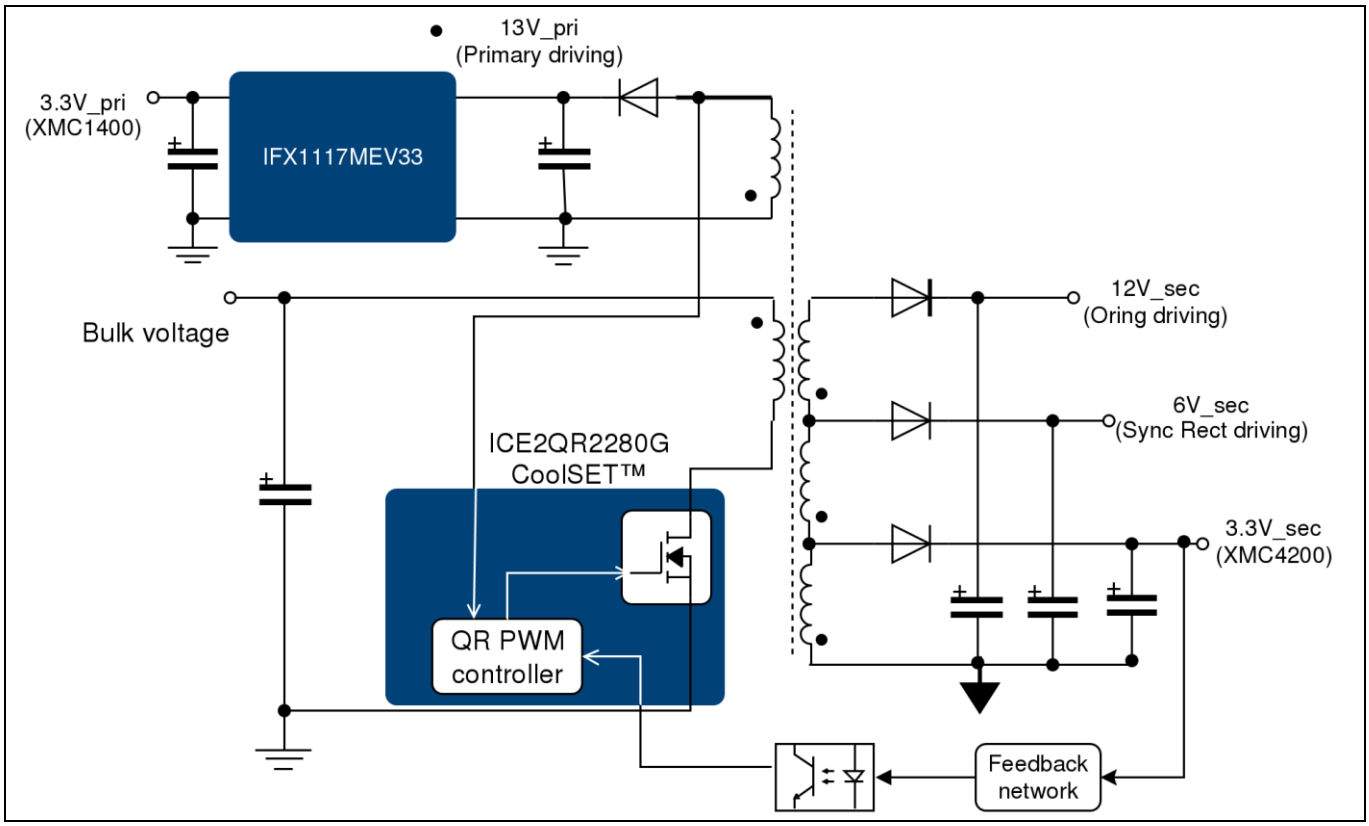


**Figure 49 Block diagram with the required supplies for the 800 W server PSU**

# 6 Test results

This chapter introduces the performance and behavior of the 800 W server power supply with 600 V CoolMOS™ P7, in both steady-state operation and under dynamic input and output conditions.

**Table 5 Summary of the tests in this section with the applied conditions and the main results**

| Test | | Conditions | Result | |
|---|---|---|---|---|
| Efficiency test | | 230 Vrms 50 Hz, 10% to 100% load | $\eta_{pk}$ = 95.32% at 400 W;<br>> 1% over 80Plus® Platinum® efficiency | |
| | | 115 Vrms 60 Hz, 10% to 100% load | $\eta_{pk}$ = 93.95% at 322 W | |
| | | 90 Vrms 60 Hz, 10% to 100% load | $\eta_{pk}$ = 92.99% at 322 W | |
| Current THD | | 230 Vrms 50 Hz, 10% to 100% load | THDi < 10% from 20% load | THDi ≈ 2% at 100% load |
| | | 115 Vrms 60 Hz, 10% to 100% load | THDi < 6.5% from 10% load | |
| | | 90 Vrms 60 Hz, 10% to 100% load | THDi < 4% from 10% load | |
| PF | | 230 Vrms 50 Hz, 10% to 100% load | PF > 0.9 from 20% load | |
| | | 115 Vrms/90 Vrms 60 Hz, 10% to 100% load | PF > 0.96 from 10% load | |
| Steady-state $V_{out}$ ripple | | 230 Vrms/115 Vrms/90 Vrms 50/60 Hz, 10% to 100% load | $\lvert\Delta V_{out}\rvert$ < 120 $mV_{pk\text{-}pk}$ | |
| Inrush current | | 230 Vrms, 50 Hz | $I_{in\_peak}$ < 10 A | |
| PLD | AC lost | 200 Vrms 50 Hz/100 Vrms 60 Hz<br>AC lost: 10 ms at 100% load, 20 ms at 50% load | $\lvert\Delta V_{out}\rvert$ < 240 $mV_{pk}$ | No damage:<br>* PSU soft-start if bulk voltage under 320 V<br>* PSU soft-start if V AC out of range for a certain time |
| | Voltage sag | 200 Vrms 50 Hz/100 Vrms 60 Hz<br>Different sag conditions; 100% load | | |
| Brown-out | | 100 V → 60 V, 60 Hz, 40 s–40 steps | 82 V OFF | |
| | | 60 V → 100 V, 60 Hz, 40 s–40 steps | 86 V ON | |
| Load transient | | 3 A ↔ 33 A, 0.5 A/µs | $\lvert\Delta V_{out}\rvert$ < 240 $mV_{pk}$ | |
| | | 33 A ↔ 66 A, 0.5 A/µs | | |
| | | 33 A → 0 A | $\Delta V_{out}$ < 200 mV (burst mode operation) | |
| OCP | | 30 s at 72 A | LLC OFF.<br>Resuming of operation requires bulk voltage to drop under 320 V | |
| | | 10 s at 78 A | | |
| | | 100 A | | |
| | | Output terminals in short-circuit | Detection within 100 µs. LLC OFF.<br>Resuming of operation requires controller reset | |
| EMI | | 230 Vrms 50 Hz, full load, resistive load, lab set-up | Complies with Class B limits | |

## 6.1 Performance and steady-state operation

This section presents the steady-state waveforms of the server PSU under different operating conditions. In addition, the PSU efficiency, THD and PF are shown.

Table 6 shows the efficiency measurements obtained from the 800 W server power supply for different input voltages and from 10 percent of the load to full-load operation. The same data is plotted in Figure 50. It can be concluded that the server power supply shown is far above the Platinum® standard efficiency limit. As an example, the efficiency at half-load and high-line (230 Vrms) is 1.3 percent over the mentioned limit. The efficiency measurements shown do not include the fan supply, which was externally powered.

**Table 6 Measured efficiency of the 800 W server power supply with 600 V CoolMOS™ P7**

| Output current (A) | Eff. (%) at 230 Vrms | Eff. (%) at 115 Vrms | Eff. (%) at 90 Vrms |
|---|---|---|---|
| 6.6 | 90.29 | 89.79 | 88.84 |
| 13.2 | 93.72 | 92.59 | 92.2 |
| 19.8 | 94.92 | 93.66 | 92.95 |
| 26.4 | 95.29 | 93.89 | 93.05 |
| 33 | 95.32 | 93.82 | 92.7 |
| 39.6 | 95.18 | 93.53 | 92.09 |
| 46.2 | 95.06 | 93.1 | 91.46 |
| 52.8 | 94.84 | 92.66 | 90.67 |
| 59.4 | 94.55 | 92.07 | 89.72 |
| 66 | 94.19 | 91.35 | 88.38 |

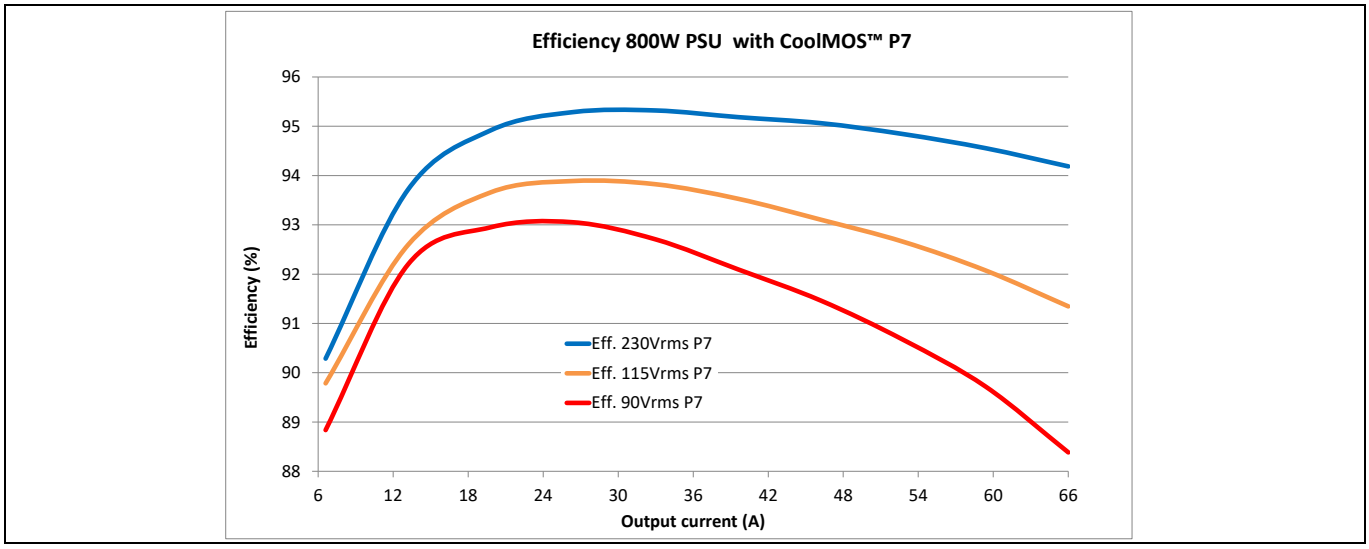


**Figure 50 Measured efficiency of the 800 W server power supply with 600 V CoolMOS™ P7**

The input current quality in terms of THD and PF is shown in Table 7 and Table 8 respectively. This information is also graphically presented in Figure 51 and Figure 52. For low-line operation (90 Vrms and 115 Vrms at 60 Hz) the THD is under 7 percent for the whole tested range, with a PF over 0.95. On the other side, for high-line (230 Vrms at 50 Hz) the THD is under 10 percent from 20 percent of the load onward, with a PFC over 0.9 from the same load conditions up to full load, as specified in Section 2.1.

**Table 7 Measured input current THD of the 800 W server power supply with 600 V CoolMOS™ P7**

| Output current (A) | THD (%) at 230 Vrms | THD (%) at 115 Vrms | THD (%) at 90 Vrms |
|---|---|---|---|
| 6.6 | 14.39 | 6.03 | 5.22 |
| 13.2 | 9.28 | 3.18 | 2.88 |
| 19.8 | 7.93 | 2.16 | 2.18 |
| 26.4 | 6.38 | 2.11 | 2.25 |
| 33 | 4.19 | 2.07 | 1.99 |
| 39.6 | 2.51 | 2.02 | 2.03 |
| 46.2 | 1.86 | 2 | 1.87 |
| 52.8 | 1.52 | 1.95 | 1.97 |
| 59.4 | 1.36 | 2.04 | 2.18 |
| 66 | 1.35 | 2.04 | 2.09 |

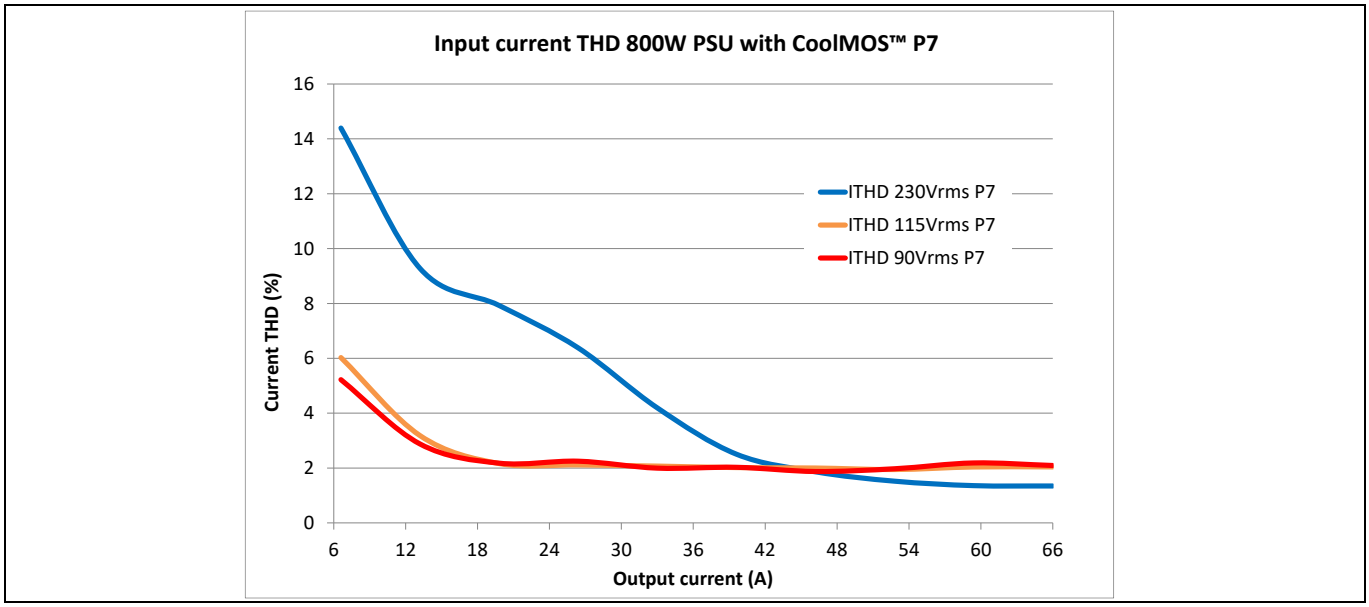


**Figure 51 Measured efficiency of the 800 W server power supply with 600 V CoolMOS™ P7**

**Table 8 Measured PF of the 800 W server power supply with 600 V CoolMOS™ P7**

| Output current (A) | PF at 230 Vrms | PF at 115 Vrms | PF at 90 Vrms |
|---|---|---|---|
| 6.6 | 0.774 | 0.966 | 0.984 |
| 13.2 | 0.902 | 0.989 | 0.997 |
| 19.8 | 0.945 | 0.997 | 0.999 |
| 26.4 | 0.964 | 0.998 | 0.999 |
| 33 | 0.972 | 0.999 | 0.999 |
| 39.6 | 0.981 | 0.999 | 0.999 |
| 46.2 | 0.987 | 0.999 | 0.999 |
| 52.8 | 0.991 | 0.999 | 0.998 |
| 59.4 | 0.994 | 0.999 | 0.998 |
| 66 | 0.995 | 0.999 | 0.998 |

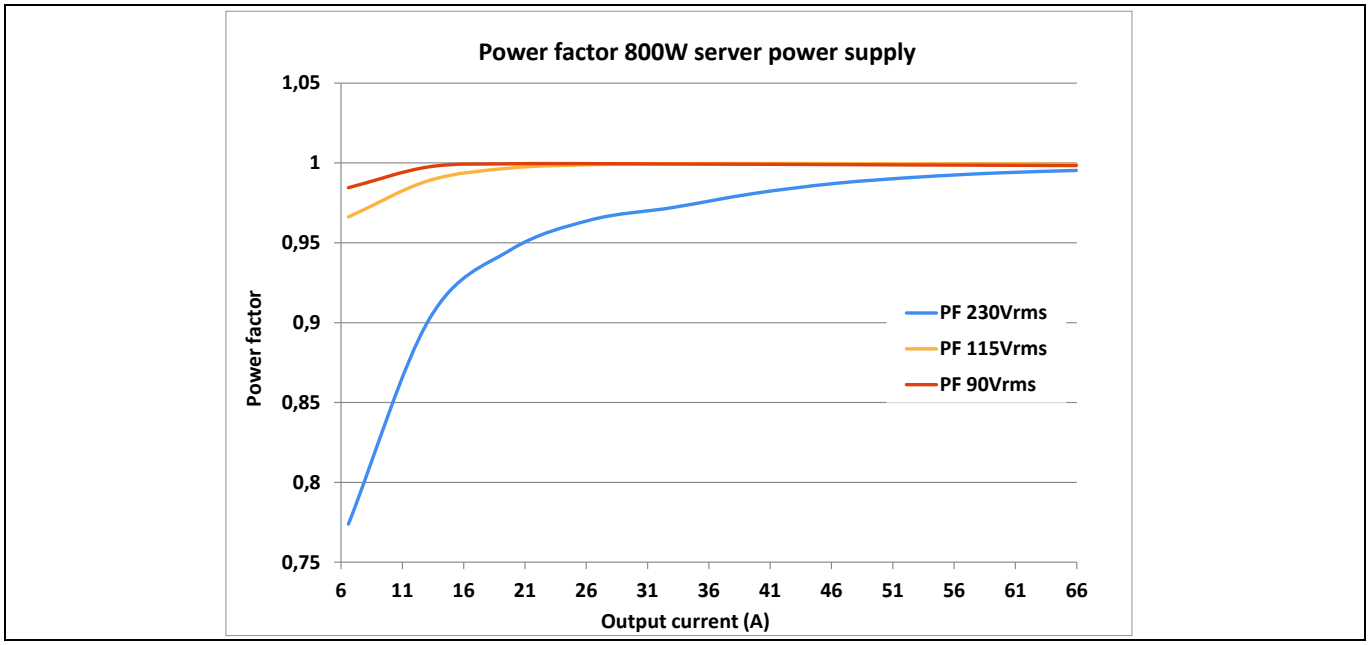


**Figure 52 Measured efficiency of the 800 W server power supply with 600 V CoolMOS™ P7**

The steady-state waveforms of the PSU for both high-line and low-line are presented in Figure 53 and Figure 54 respectively, for 20 percent and full-load operation. It can be seen how the input current degrades under light load at high-line because of the DCM operation already mentioned. Regarding the output voltage, the peak-to-peak ripple is inside the specified ±120 mV. The bulk voltage modulation can be also seen in the waveforms shown. In the case of 20 percent load a 395 V bulk voltage is measured, while this value increases to 405 V in the case of full-load operation.

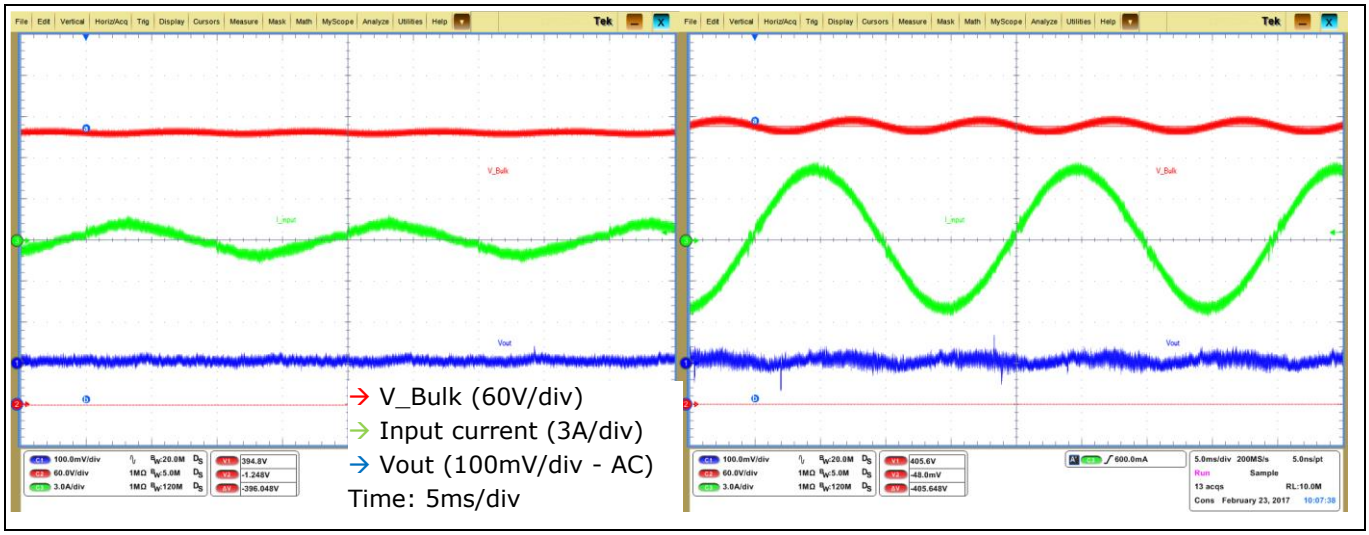


**Figure 53 Input current, bulk voltage and output voltage for the 800 W PSU at 20 percent (left) and 100 percent (right) load, 230 Vrms, 50 Hz operation**

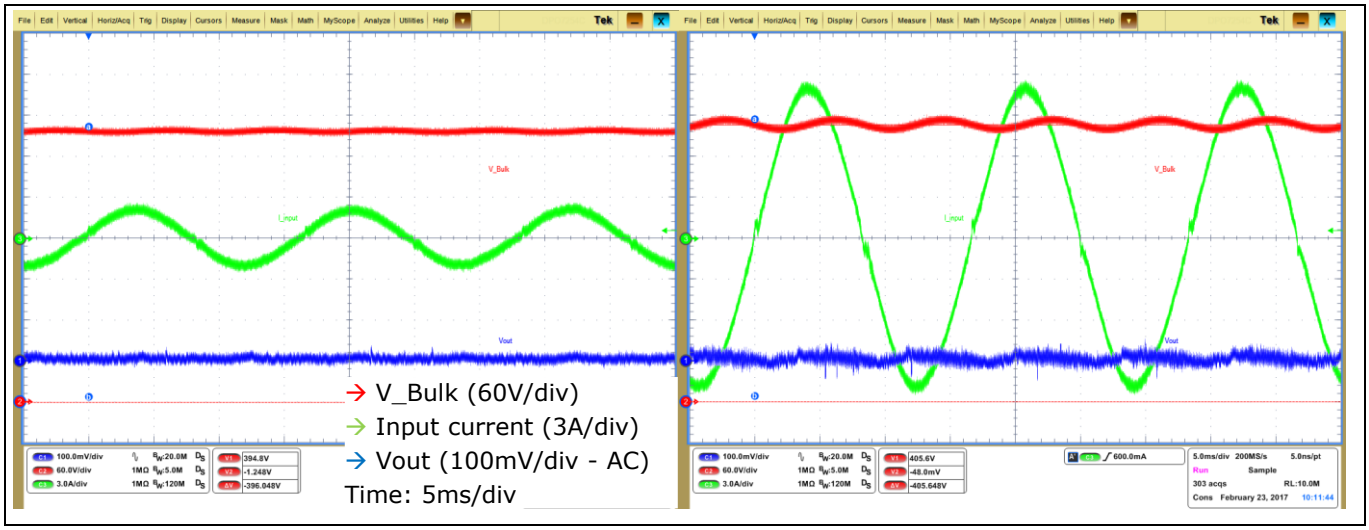


**Figure 54** **Input current, bulk voltage and output voltage for the 800 W PSU at 20 percent and 100 percent load, 115 Vrms, 60 Hz operation**

## 6.2 Inrush current (waveforms)

The power supply start-up at high-line and full load is shown in Figure 55. Due to the implemented state machine in both PFC and LLC, a time is required for the start-up of both converters after the input and bulk voltages are detected within the proper values. The inrush current in these conditions is shown in detail in Figure 56. As it can be seen, the inclusion of an NTC resistor in the PFC input limits the inrush current under 10 A in the tested conditions.

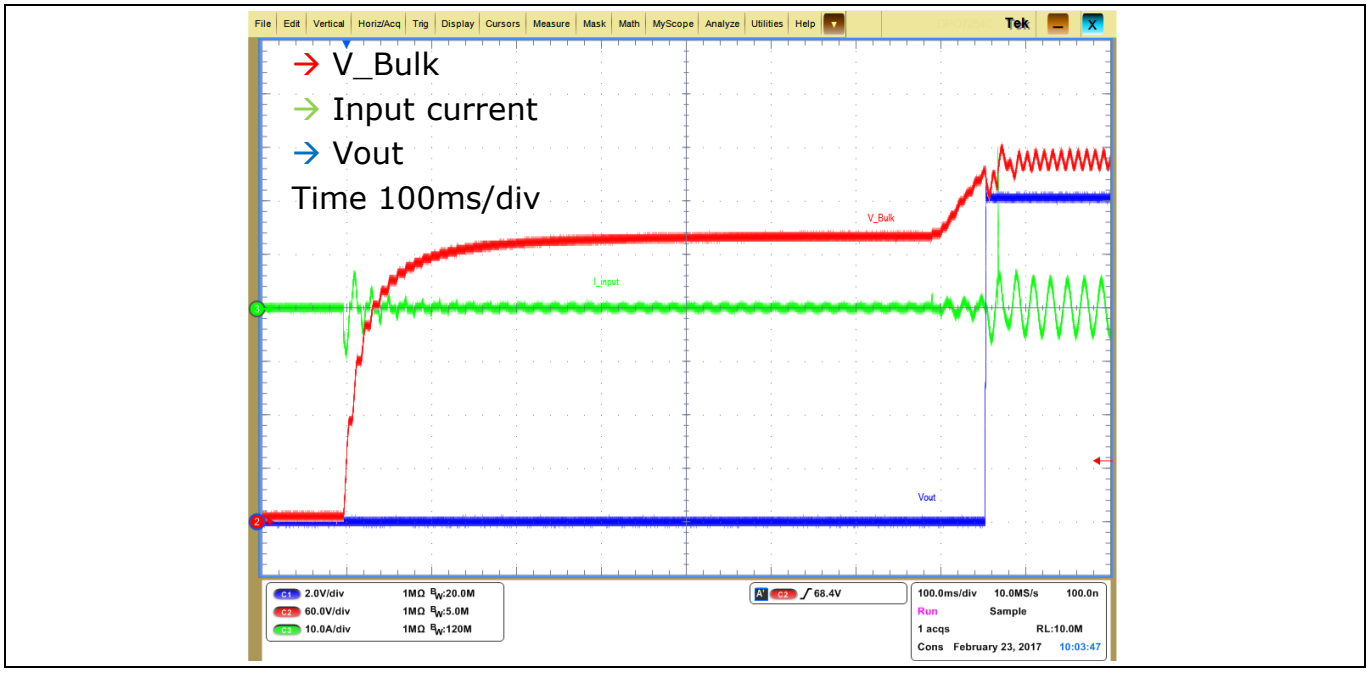


**Figure 55** **PSU start-up at 230 Vrms and full load**

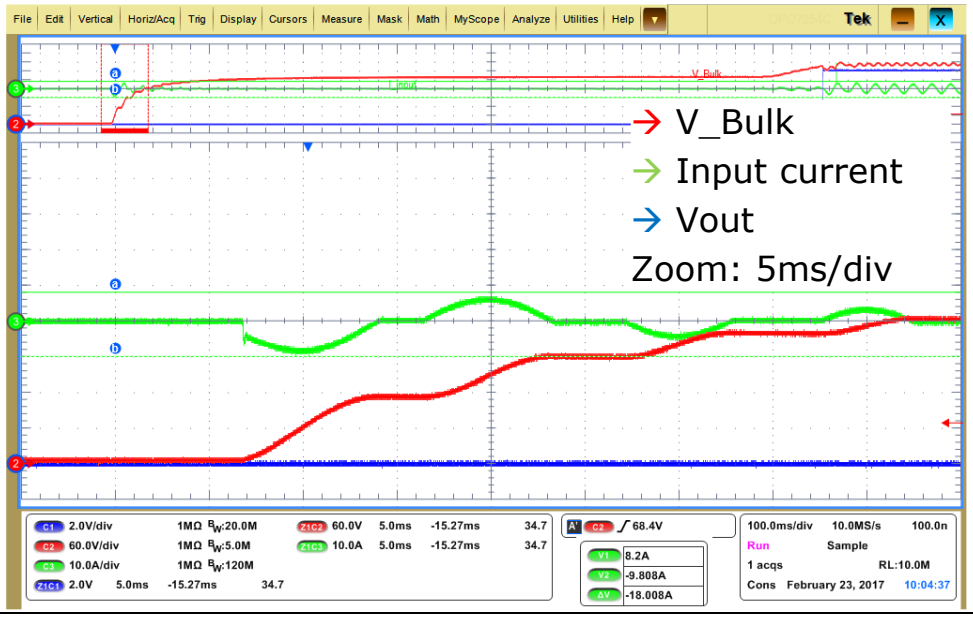


**Figure 56 Detail of the PSU inrush current during start-up at 230 Vrms and full load**

## 6.3 Power line disturbance (waveforms)

Different PLDs can appear when connected to the grid. These conditions have been tested using a programmable AC source. In this section, the PLD conditions are separated in AC lost during half-cycle, or ACLDO, and voltage sags. The results shown were obtained for full-load operation.

The applied conditions for ACLDO testing are summarized in Table 9. The AC is removed during 10 ms in a 100 ms period, and this is repeated 10 consecutive times, for both low- and high-line. The unit must operate error free, i.e. output voltage must remain in regulation inside the defined dynamic limits, in case of ACLDO. In the tests shown, an angle of 45 degrees is used for the ACLDO synchronization, since it shows the worst point from the bulk voltage point of view.

**Table 9 Applied voltages and cycle for ACLDO test**

| | | 1st to 10th time | |
|---|---|---|---|
| Duty cycle | Initial 5 s–10 s | 10% (10 ms) | 90% (90 ms) |
| AC input | 100 V AC | 0 V AC | 100 V AC |
| | 200 V AC | 0 V AC | 200 V AC |

The result of the applied test is shown in Figure 57 and Figure 58 for 100 Vrms input and in Figure 59 and Figure 60 when 200 Vrms are applied as AC voltage. In both cases, the bulk voltage decreases to 340 V during the AC lost and a fast response of the bulk voltage is observed, since maximum current is applied until the bulk voltage reaches 385 V. This extra injected current takes the bulk voltage to overshoot, despite the enhanced BW of the implemented voltage loop. In that case the PFC is turned off until the bulk decreases to the regulation level. This bulk voltage variation implies certain ripple in the output voltage. In any case the dynamic range of the output voltage is under the specified 2 percent.

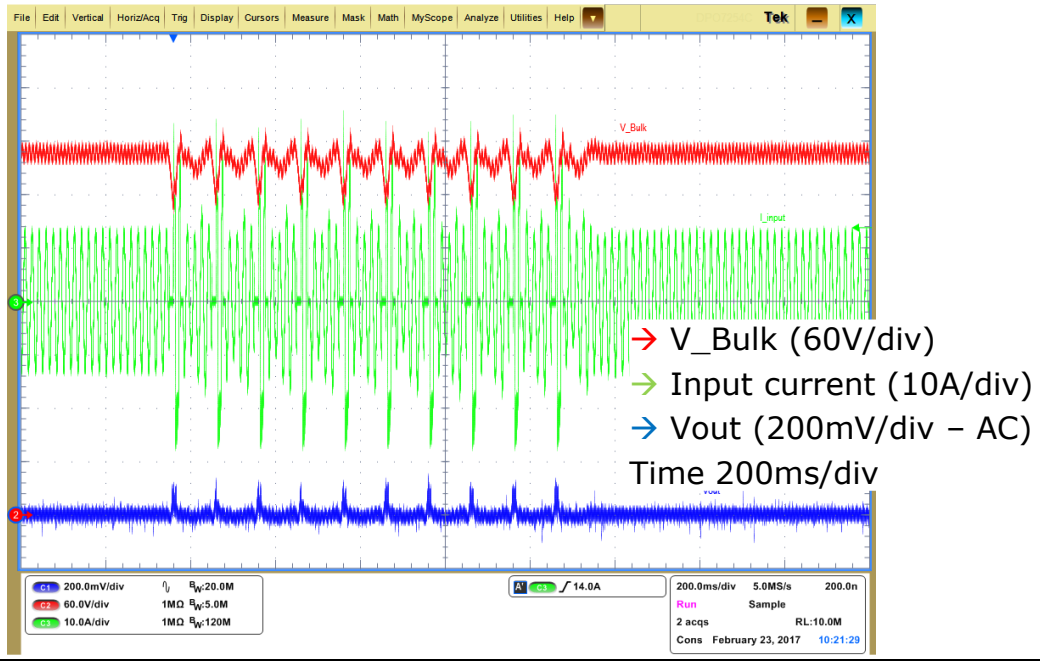


**Figure 57** **800 W PSU response to 10 times ACLDO at 100 V and 45 degrees, as defined in Table 9**

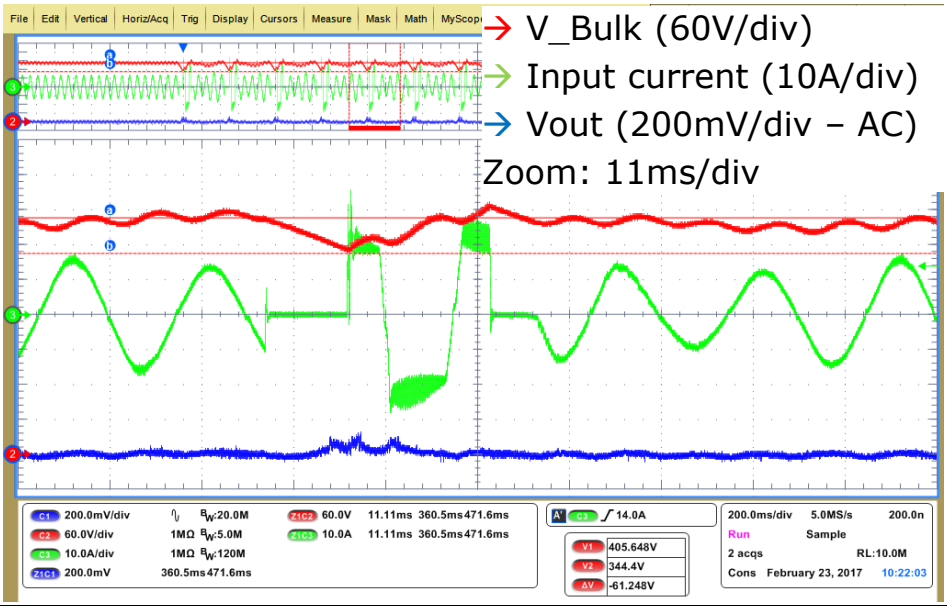


**Figure 58** **Detail of the response to 10 times ACLDO at 100 V and 45 degrees, as defined in Table 9**

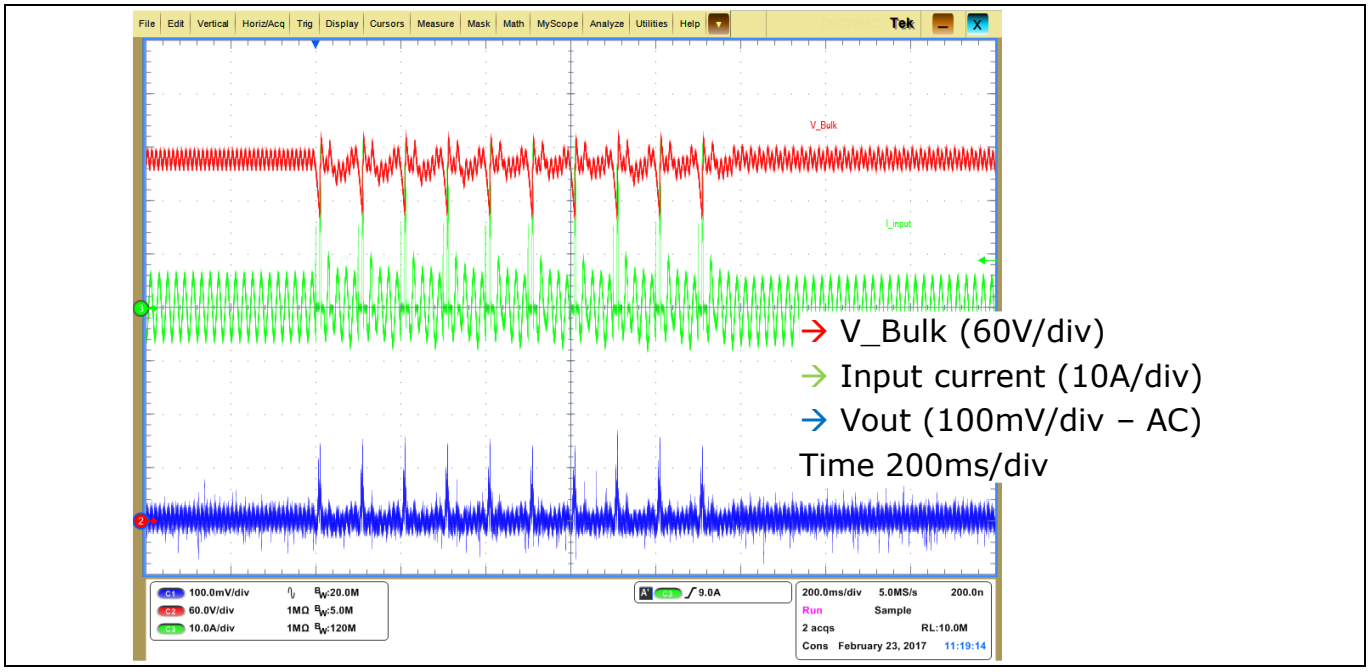


**Figure 59** **800 W PSU response to 10 times ACLDO at 200 V and 45 degrees, as defined in Table 9**

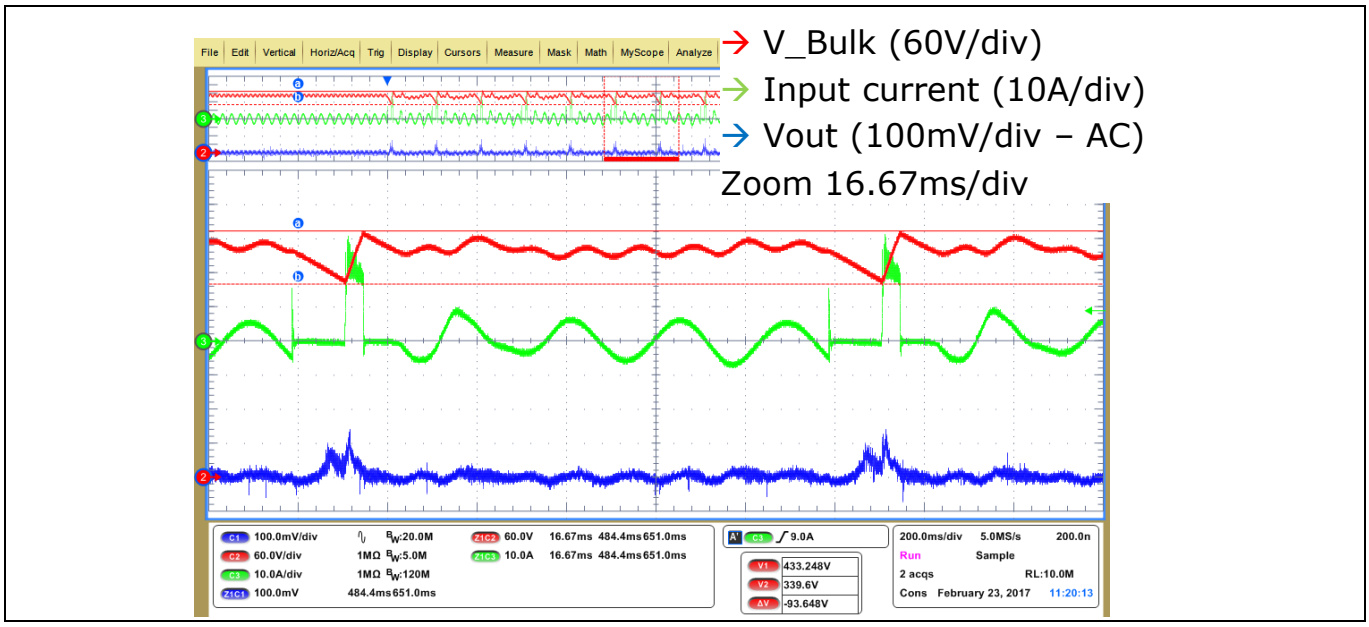


**Figure 60** **Detail of the 800 W PSU response to 10 times ACLDO at 200 V and 45 degrees, as defined in Table 9**

If the loss of the AC voltage is prolonged for more than 10 ms and the bulk voltage decreases to below 333 V, both the PFC and LLC stages are turned off and a soft-start of the system is initiated. Figure 61 shows the system behavior when the AC is removed for 15 ms for full-load operation. The bulk voltage decreases to 332 V, and therefore the PSU turns off. After a defined time of 100 ms, the start-up process begins with the PFC and LLC soft-start.

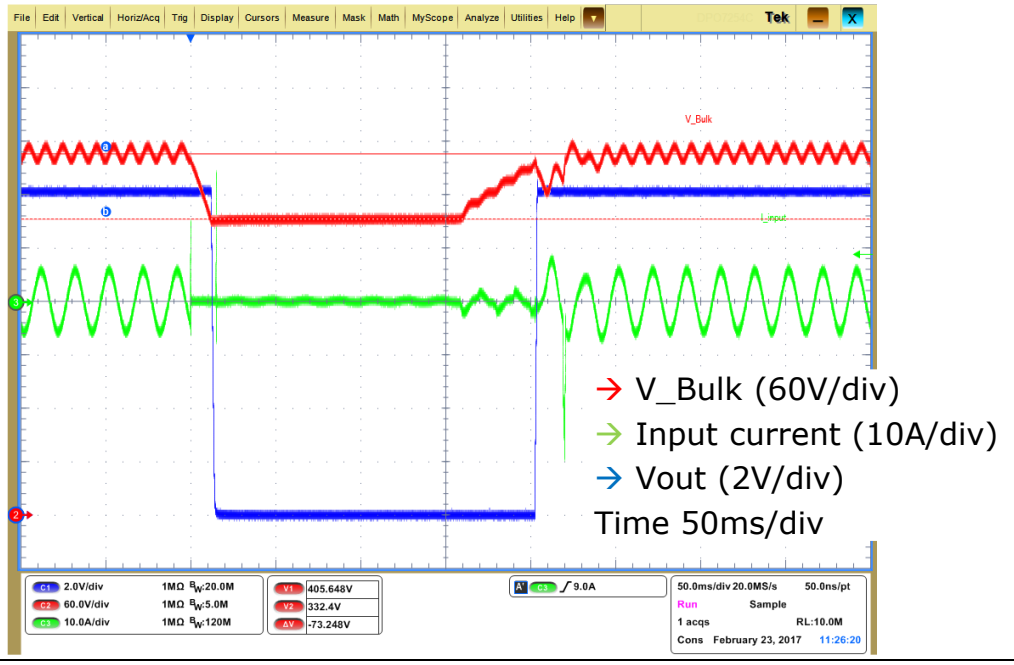


**Figure 61 800 W PSU response to 15 ms ACLDO at 200 V and 45 degrees for full-load conditions**

A second PLD condition is voltage sag, which is a temporary decrease in the line voltage. Table 10 shows the two different voltage sags tested in the 800 W PSU, including the applied timing. In this section the results for low-line (100 V) are shown, since the voltage reduction from 200 V to either 130 V or 150 V is inside the steady-state specifications.

**Table 10 Applied voltages and cycles for voltage sag test**

| | | 1st to 10th time | |
|---|---|---|---|
| Duty cycle | Initial 5 s–10 s | 10% (0.5 s) | 90% (4.5 s) |
| AC input | 100 V AC | 68 V AC | 100 V AC |
| | 200 V AC | 130 V AC | 200 V AC |

| | | 1st to 10th time | |
|---|---|---|---|
| Duty cycle | Initial 5 s–10 s | 10% (2 s) | 90% (18 s) |
| AC input | 100 V AC | 75 V AC | 100 V AC |
| | 200 V AC | 150 V AC | 200 V AC |

The result of the 68 V voltage sag applied during 500 ms with a period of 5 s is presented in Figure 62 for two consecutive variations. Figure 63 gives an insight into the waveforms at the beginning of the voltage sag. The system response when 75 V are applied during 2 s with a steady-state voltage of 100 V is depicted in Figure 64. A detailed view of the 100 V to 75 V step is shown in Figure 65. All the presented scope captures are taken at full-load conditions.

In both cases the input voltage step makes the PFC enter PCL, which is set to 20 A, leading to bulk voltage modulation. After this modulation ends, the bulk voltage returns to the expected regulation value (405 V at full load). The output voltage is not affected by the bulk voltage modulation since the voltage change is slower than in the case of ACLDO.

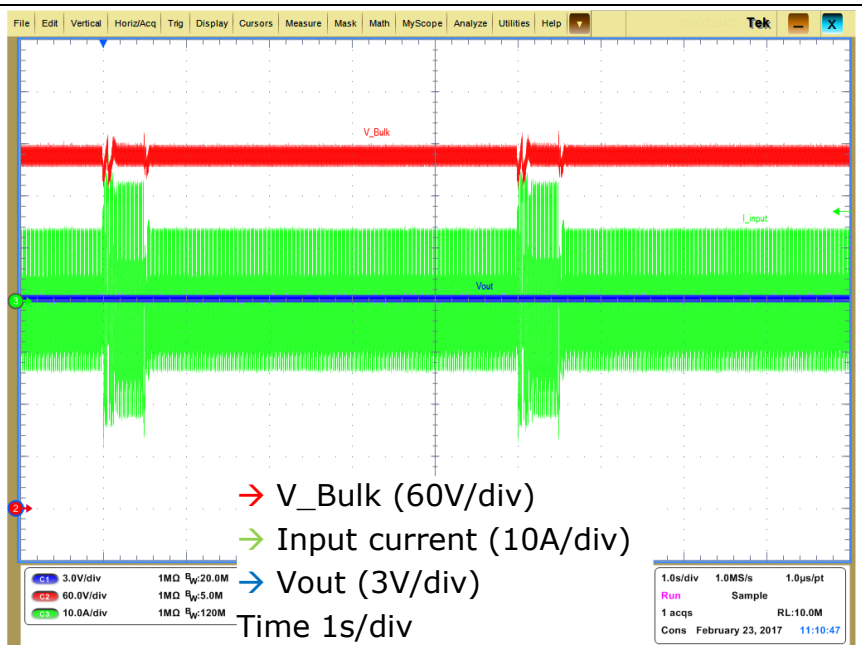


**Figure 62 Two-times 68 V voltage sag, as defined in Table 10**

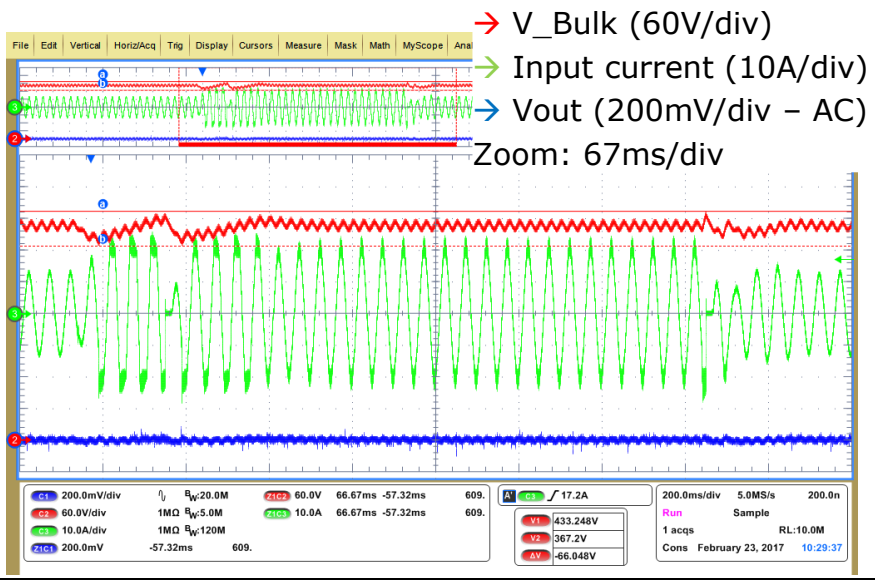


**Figure 63 Bulk voltage variation during 68 V sag over 500 ms**

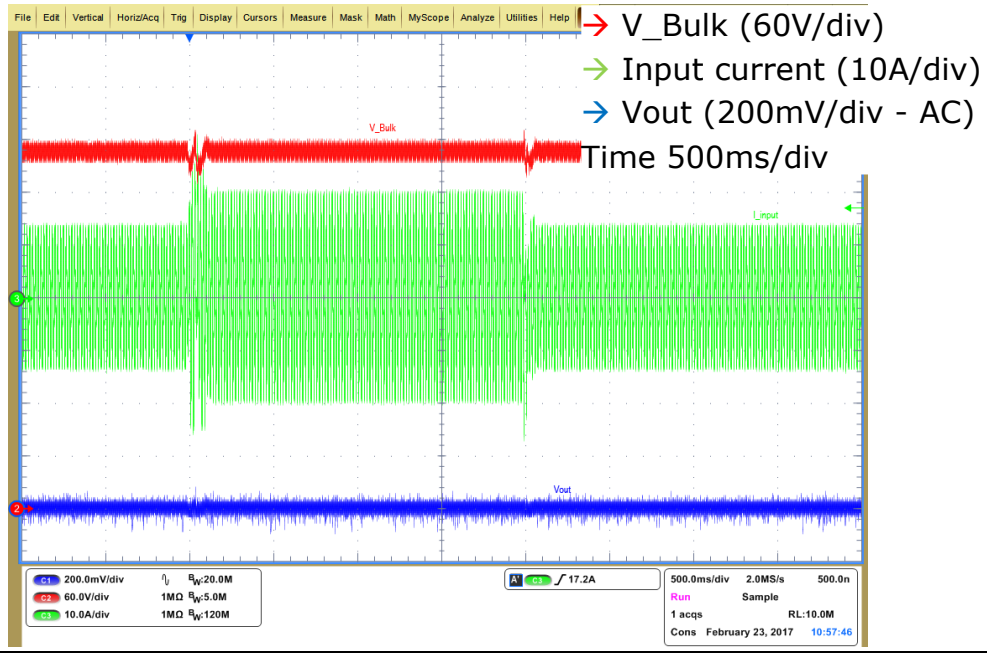


**Figure 64 Bulk voltage variation during 75 V sag over 2 s, as defined in Table 10**

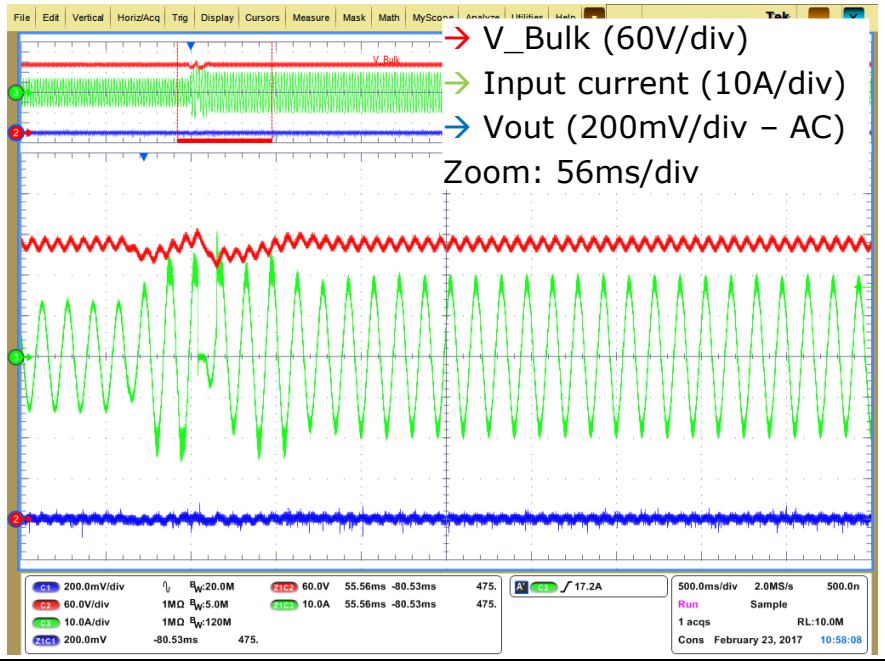


**Figure 65 Detail of the 75 V sag during 2 s, input voltage change from 100 Vrms to 75 Vrms**

Since the presented voltage sag can be under the brown-out levels for steady-state operation, a time filter is implemented in the PFC SW. In case the input voltage is under 82 V for longer than 2 s or under 75 V for more than 500 ms, the PFC (and therefore the LLC) is turned off. This situation is shown in Figure 66, where 68 V have been applied for 800 ms. The system is turned off and a start-up sequence including soft-start is implemented after the defined 100 ms waiting time.

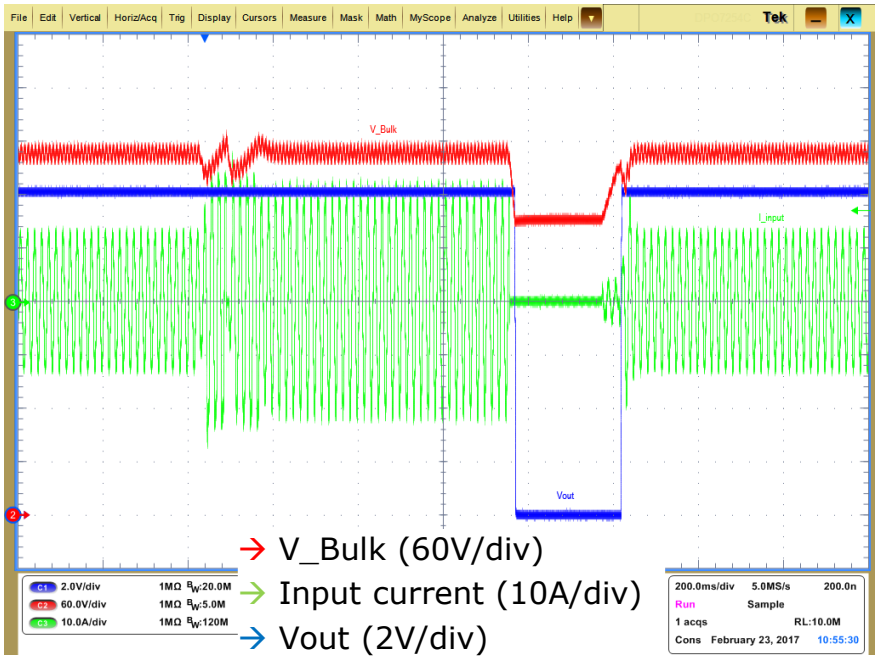


**Figure 66** **68 V voltage sag applied for more than 500 ms (800 ms), PFC and LLC turn-off and resume operation with soft-start**

## 6.4 Brown-out (graph)

The 800 W server power supply will shut down when the input voltage is under 82 V. The PFC unit implements the time filters introduced in the previous section, which enable the line voltage sag to be managed. The unit restarts when the input voltage is higher than 86 V.

Figure 67 shows the brown-out behavior of the power supply when the input voltage is linearly decreased from 100 V to 60 V, at 60 Hz, for a period of 40 s in 40 steps. Afterwards, the input voltage is increased from 60 V to 100 V, at 60 Hz, linearly with the same slew rate. The unit shuts down with 80 V input and restarts operation at 86 V.

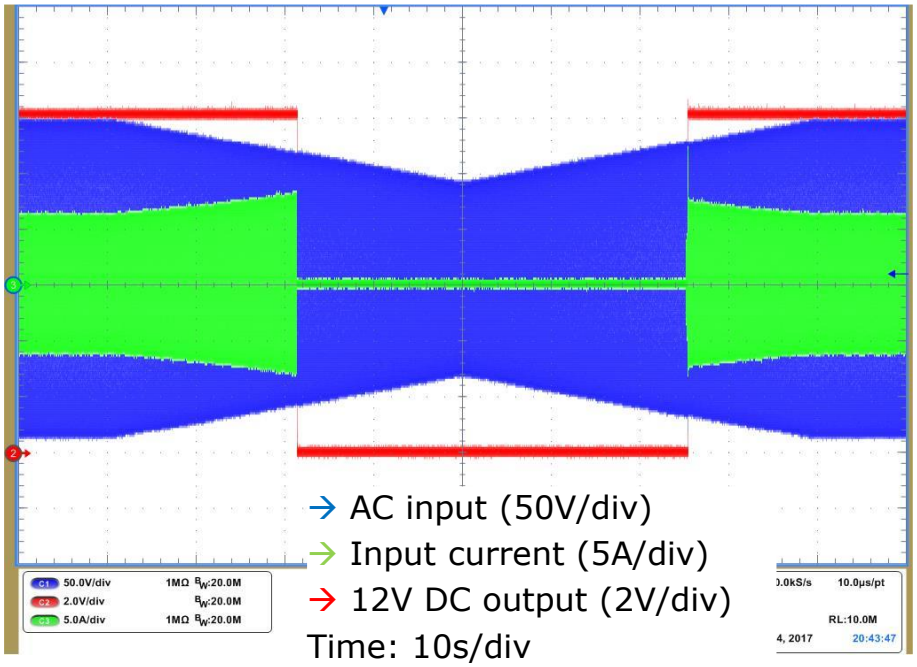


**Figure 67 Brown-out test with variation from 100 V to 60 V AC over 40 s in 40 steps**

## 6.5 Load transient response (waveforms)

The specification shown in Section 2.1 establishes a ±2 percent variation, i.e., ±240 mV, of the output voltage in case of dynamic load jumps. The specified slope is 0.5 A/µs, when the load changes from 3 A (5 percent load) to 33 A (50 percent load) and from 33 A to 66 A (100 percent load), and vice-versa. Figure 68 and Figure 69 show the result of the introduced dynamic test. As can be seen, the 800 W PSU stays within the margins when such load jumps are applied, with a maximum undershoot of -182 mV and an overshoot of approximately 150 mV.

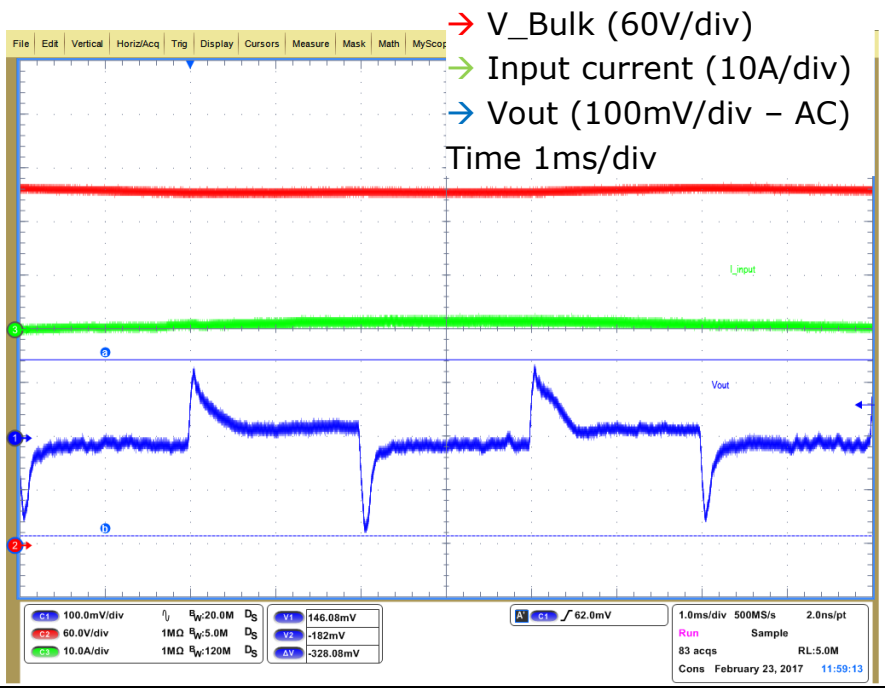


**Figure 68 Load-step response 3 A–33 A at 0.5 A/µs**

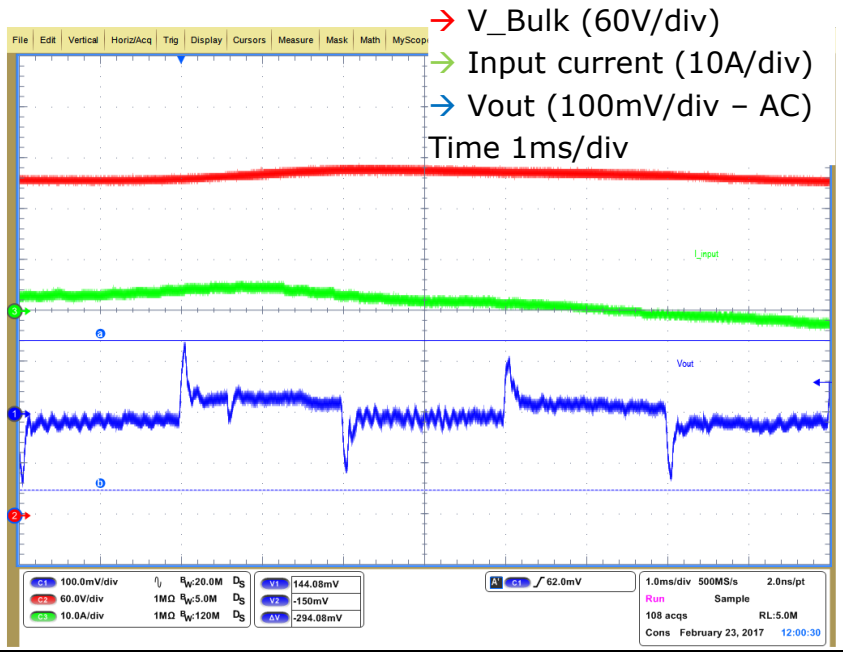


**Figure 69 Load-step response 33 A–66 A at 0.5 A/µs**

## 6.6 Burst mode operation

Under certain operating conditions, especially in light- or no-load operation, the bulk voltage can overshoot and the necessary LLC gain to maintain regulation cannot be reached due to maximum frequency limitation. In this situation, burst mode operation of the LSLC is triggered if the output voltage is over 150 mV while operating at maximum frequency (300 kHz).

Figure 70 shows a load dump from half- to no-load in which the burst mode operation is triggered. The reduction of the bulk voltage leads to frequency reduction in the LLC converter and therefore the burst mode operation is skipped.

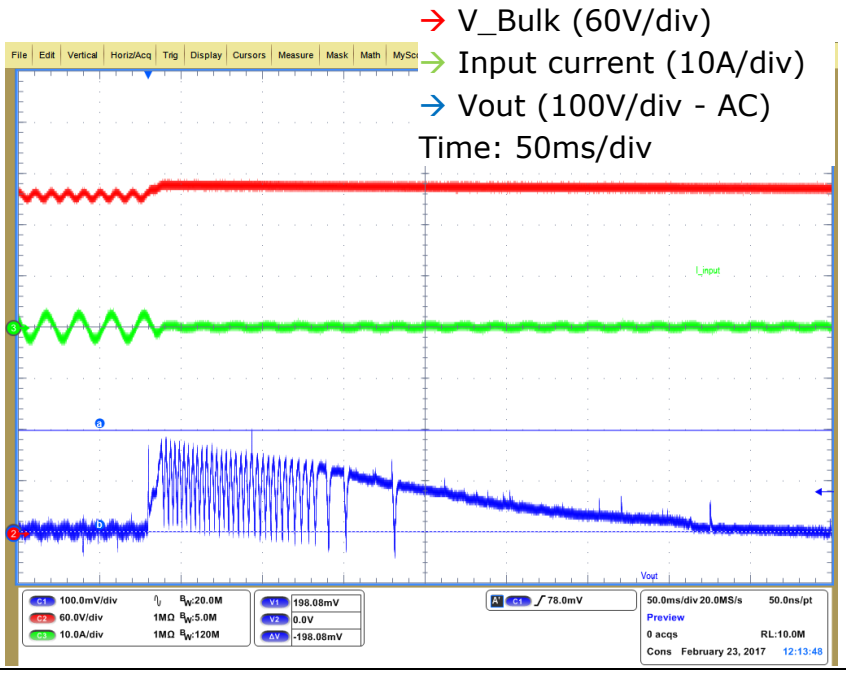


**Figure 70 Burst mode operation during a half-load to no-load dump**

## 6.7 Overcurrent Protection (OCP)

As shown in Figure 47, three different current levels with certain time allowances are programmed as OCP, considering the output CS. Figure 71 depicts the system behavior when a load of 72 A is applied for more than 30 s, when the PSU was operating at half-load. In that case, the LLC stage is turned off, but not the PFC converter. A bulk voltage modulation can be seen, due to the no-load operation of the boost converter. A similar situation is shown in Figure 72, where a 78 A load is applied for longer than 10 s. A third level of protection is set to 83 A. If this load is applied, the LLC converter turns off immediately, as shown in Figure 73.

For any of the three defined levels, the bulk voltage must decrease under 330 V in order to clear the fault and restart the PSU with a soft-start sequence for both the PFC and the LLC stages.

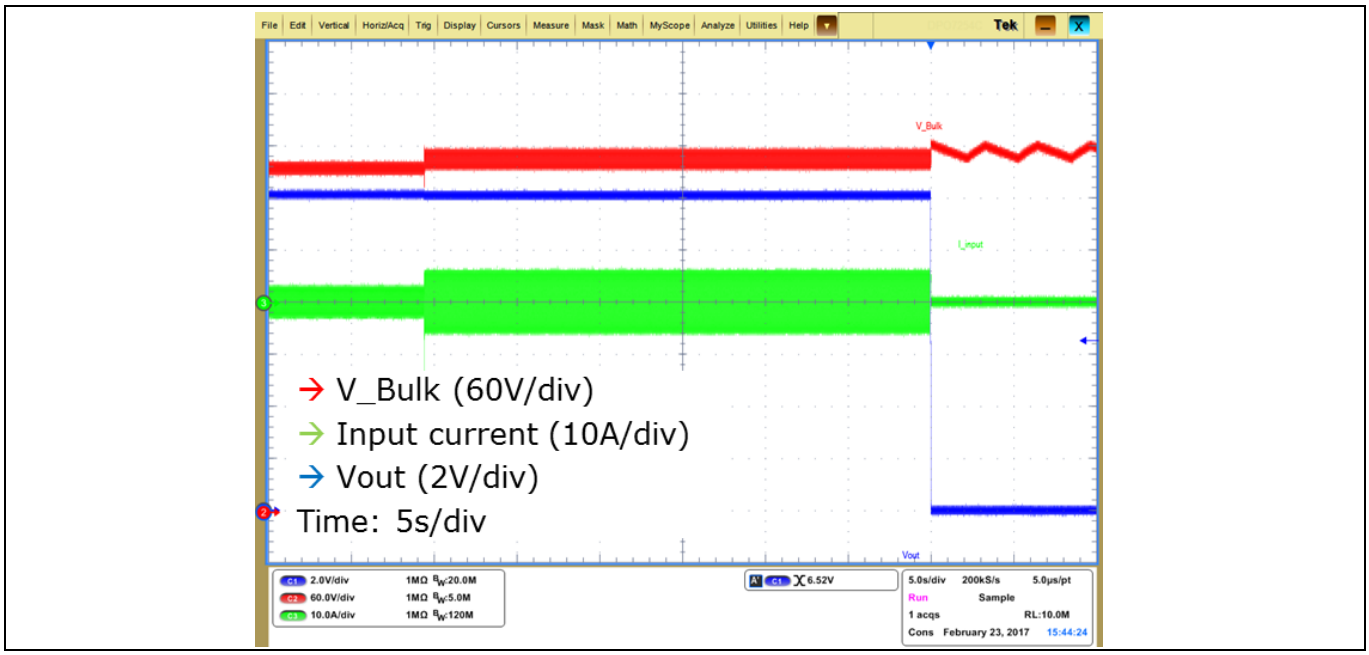


**Figure 71 OCP triggered after 30 s with 72 A. Step from half-load.**

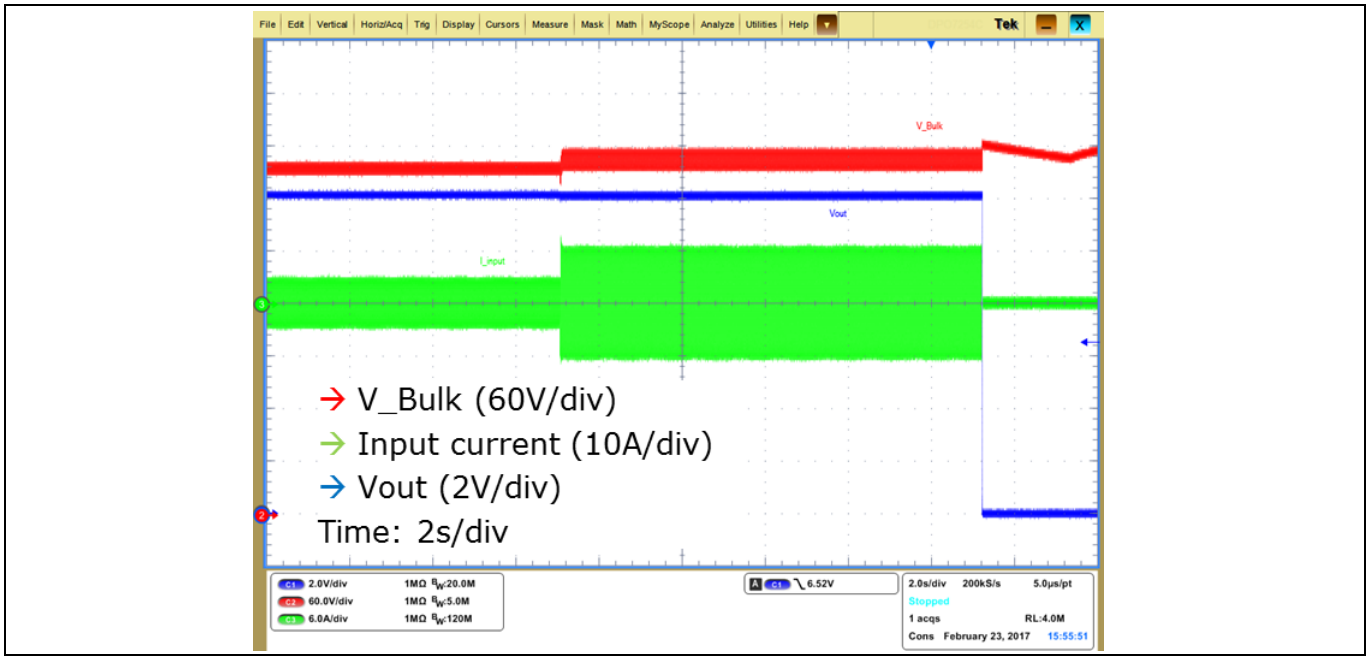


**Figure 72 OCP triggered after 10 s with 78 A. Step from half-load.**

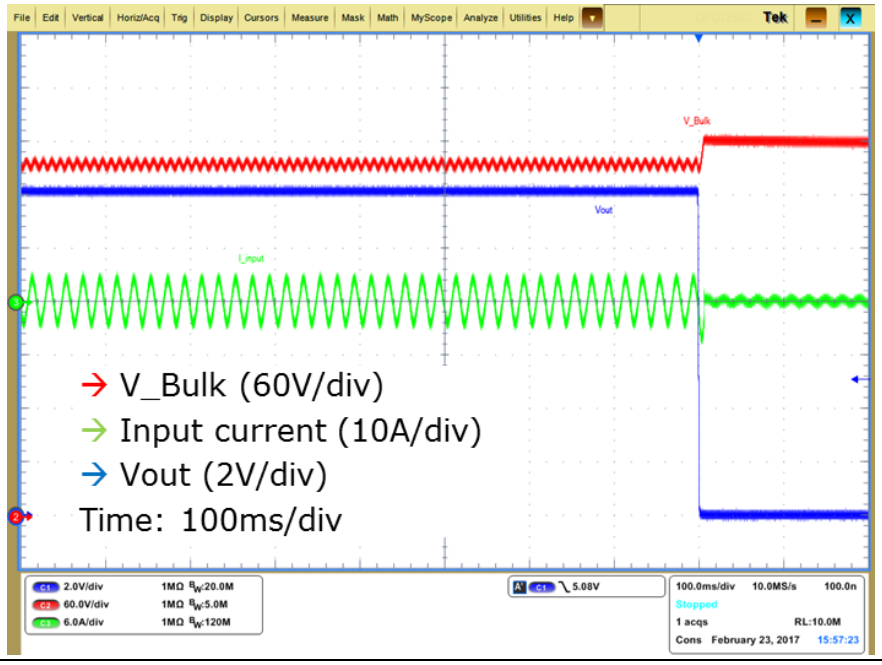


**Figure 73 OCP triggered with 100 A (load short-circuit). Step from half-load.**

### 6.7.1 Short-circuit

As explained in Sections 4.4.1 and 4.4.4, a resonant comparison protection is implemented. This enables fast detection of a short-circuit, given the quick reaction of the resonant current. Figure 74 shows how this protection is triggered when a short-circuit is applied directly in the power supply output, and the consequent LLC operation stop. A controller reset is required to resume PSU operation.

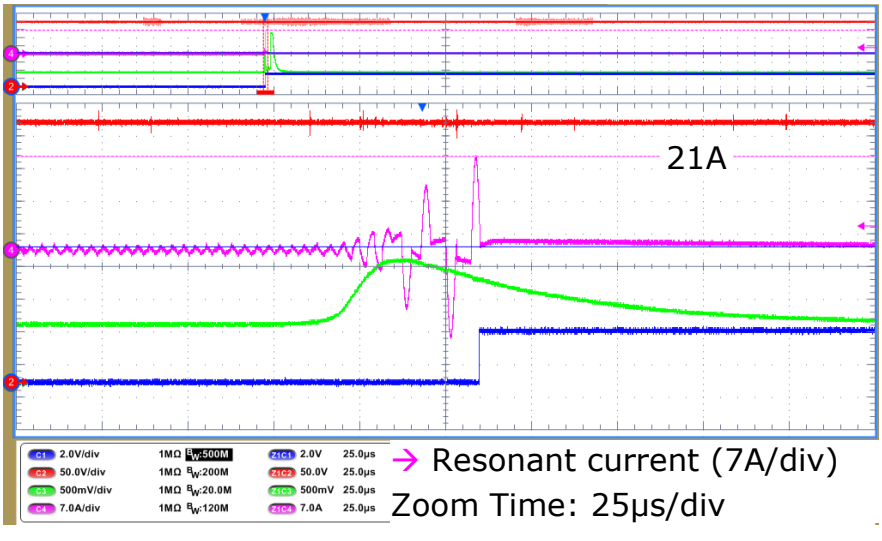


**Figure 74 Resonant current comparison as short-circuit protection trigger**

## 6.8 Conducted EMI (graphs)

The conducted EMI has been measured in the 800 W server power supply at full load using resistive load. The measurements are shown in Figure 75 and Figure 76 for 230 V and 90 V inputs respectively. In the figures both peak (yellow) and average (blue) measurements are shown, together with the corresponding class B limit.

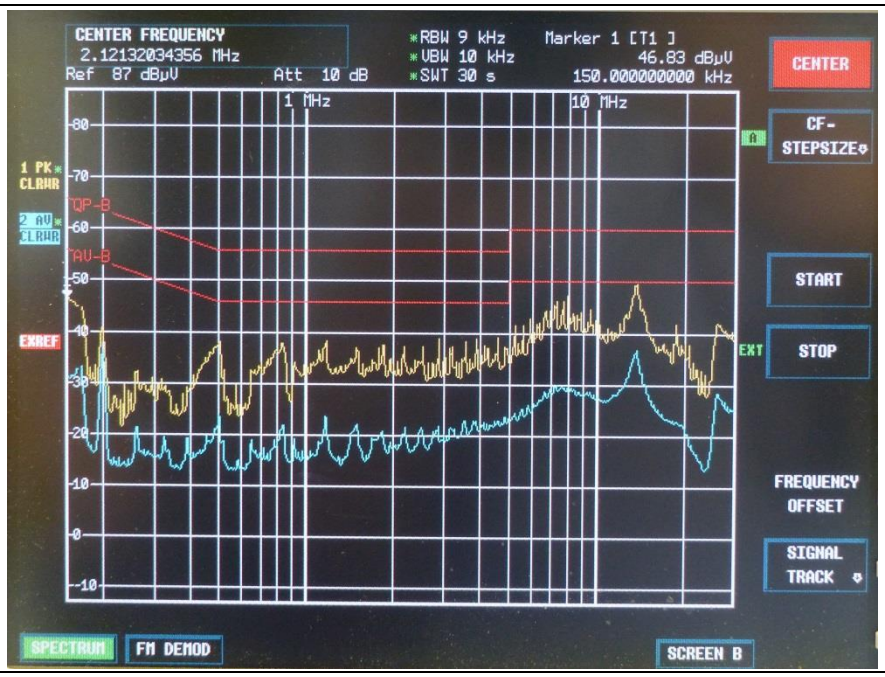


**Figure 75** **Peak (yellow) and average (blue) conducted EMI, measured with resistive load at full-load and 230 V input**

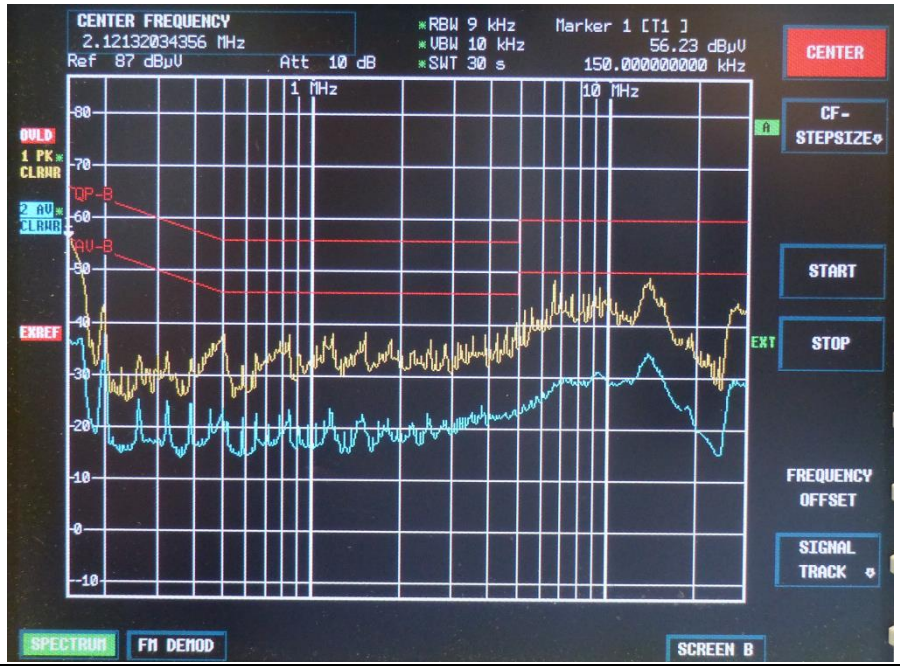


**Figure 76** **Peak (yellow) and average (blue) conducted EMI, measured with resistive load at full-load and 90 V input**

# 7 Schematics

## 7.1 Main board schematic

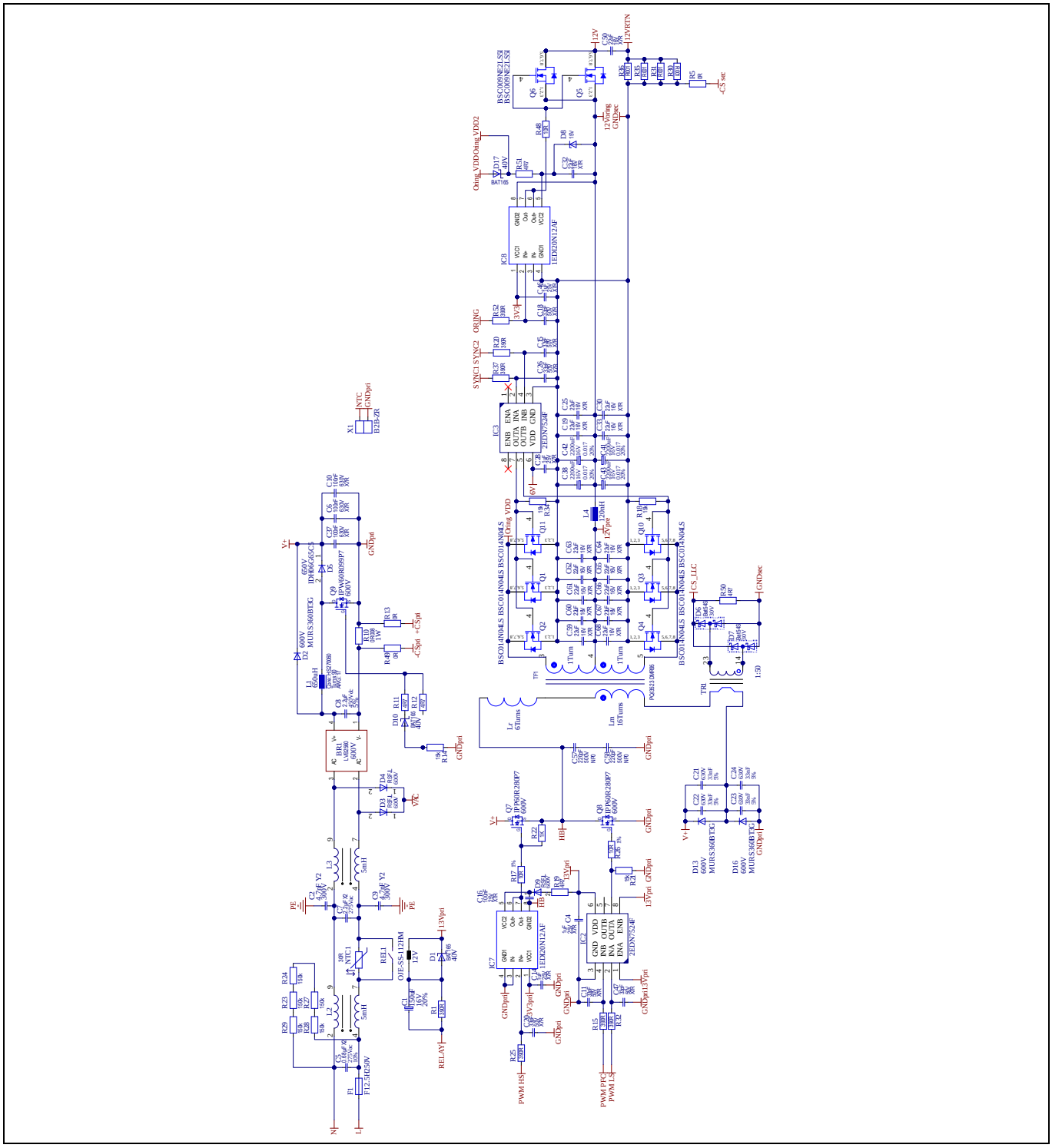

**Figure 77 PFC and LLC stage schematic of the 800 W server power supply with 600 V CoolMOS™ P7**

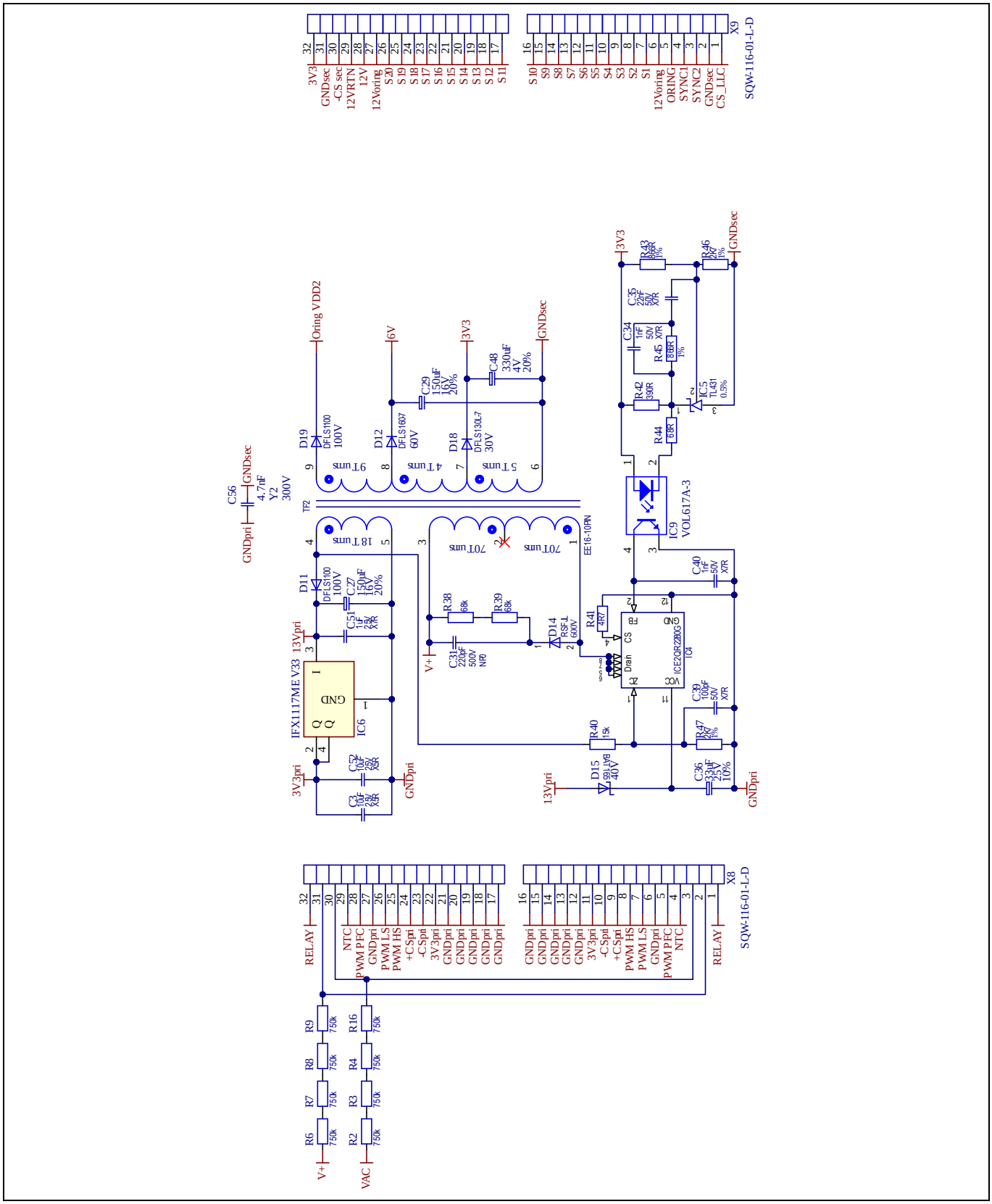


**Figure 78** **Auxiliary power supply schematic of the 800 W server power supply, including the connectors to the control board and the NTC temperature sensor**

## 7.2 Control board schematic

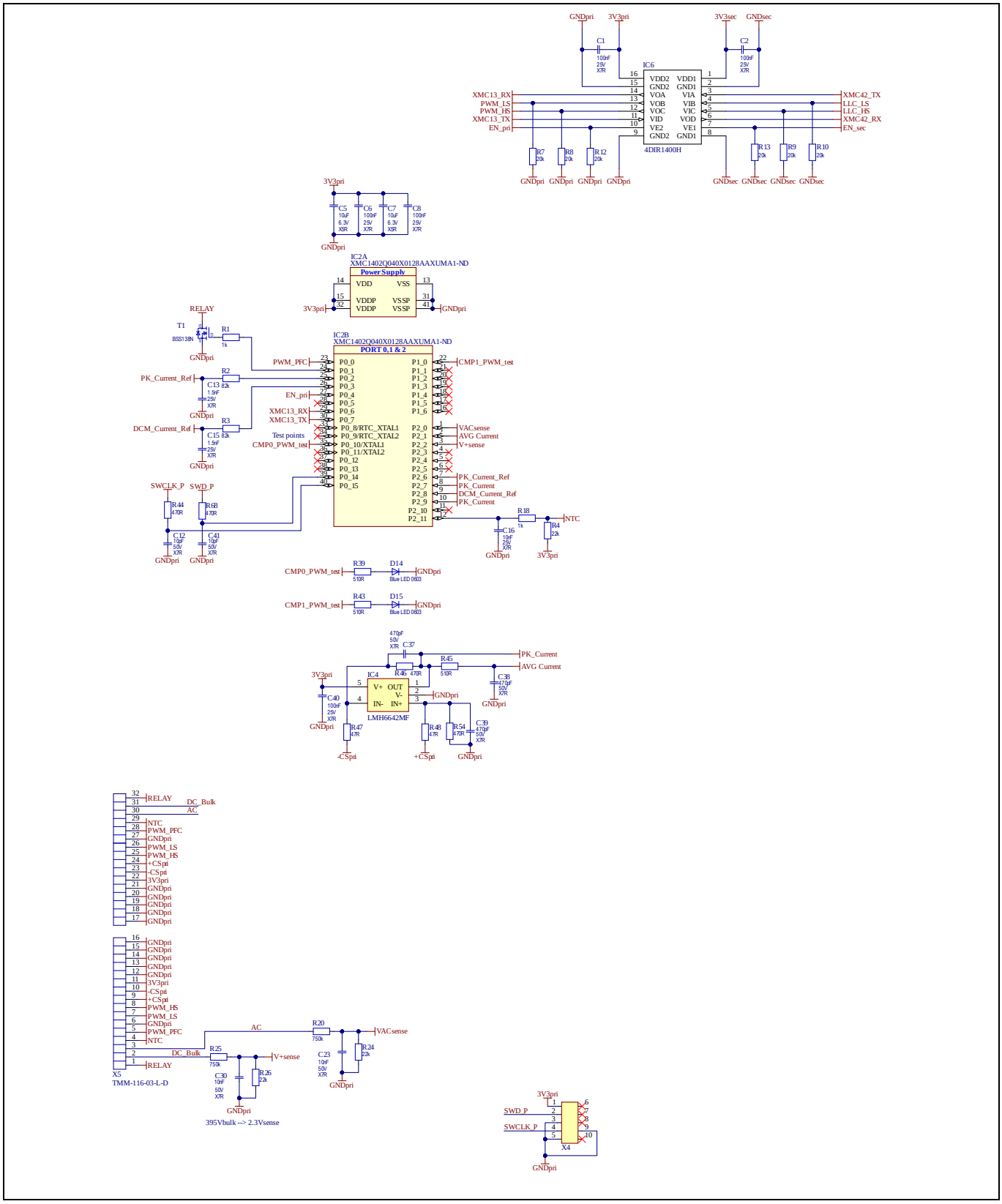


**Figure 79 Primary-side controller (XMC1402) schematic, including the ISOFACE™ 4DIR1400H for primary–secondary communication and the connector to the main board**

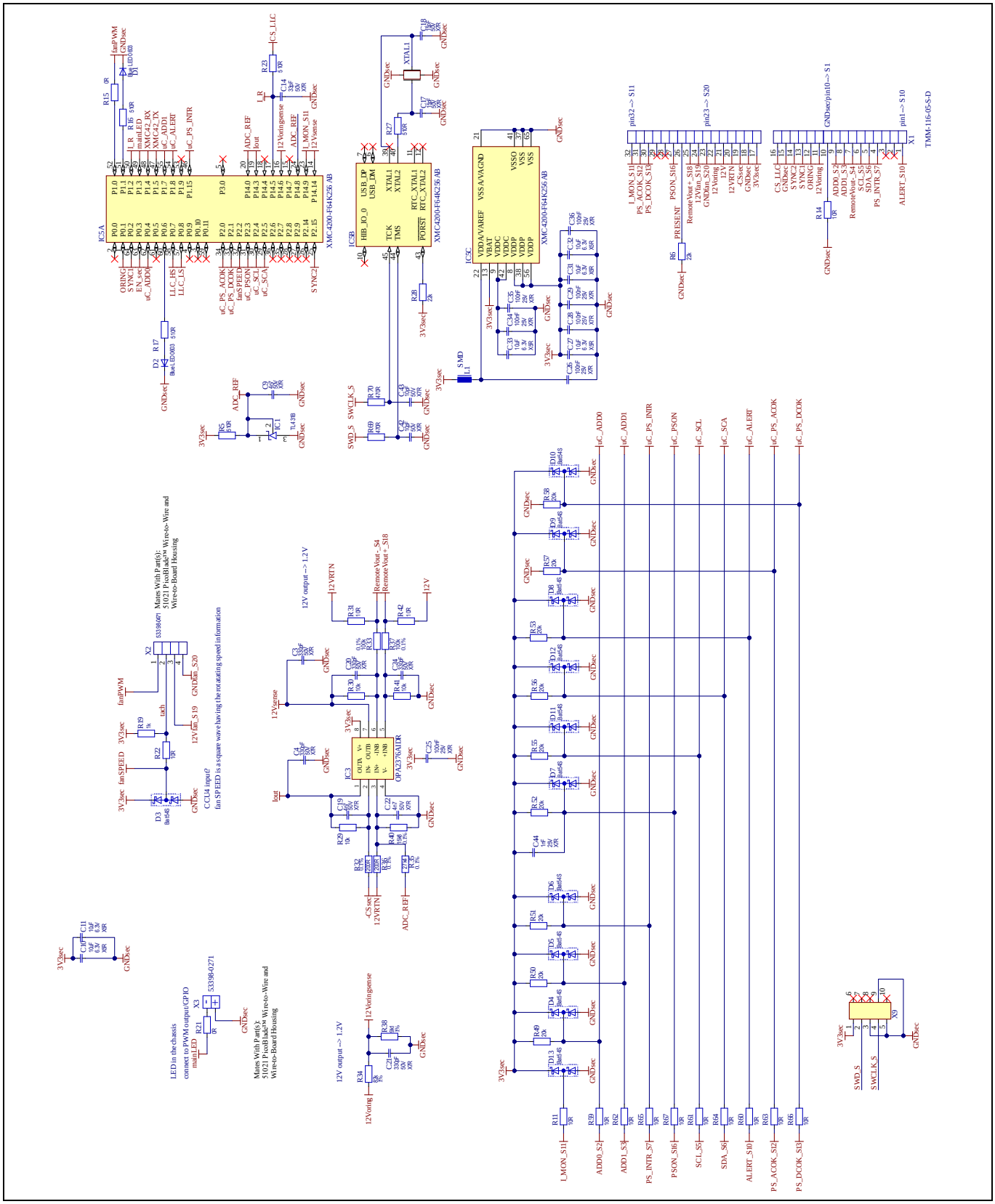

**Figure 80** **Secondary-side controller (XMC4200) schematic, including the signaling for the PSU output connector and connector to the main board**

# 8 Bill of Materials (BoM)

**Table 11 Main board components**

| Designator | Comment | Value | Tolerance | Voltage | Description |
|---|---|---|---|---|---|
| BR1 | THT | LVB2560 | | 600 V | |
| C1, C27, C29 | SMD | 150 µF | 20% | 16 V | Polarized capacitor |
| C2, C9, C56 | THT | 4.7 nF | Y2 | 300 V | Ceramic capacitor |
| C3, C52 | SMD | 10 µF | X5R | 25 V | Ceramic capacitor |
| C4, C14, C28, C46, C51 | SMD | 1 µF | X7R | 25 V | Ceramic capacitor |
| C5 | THT | 0.68 µF X2 | 10% | 275 V AC | Foil capacitor |
| C6, C10, C37 | SMD | 100 nF | X7R | 630 V | Ceramic capacitor |
| C7 | THT | 2.2 µF X2 | 20% | 275 V AC | Foil capacitor |
| C8 | THT | 2.2 µF | 5% | 450 V DC | Foil capacitor |
| C11, C15, C18, C20, C26, C47 | SMD | 33 pF | X7R | 50 V | Ceramic capacitor |
| C16 | SMD | 100 nF | X7R | 25 V | Ceramic capacitor |
| C19, C25, C30, C32, C33, C50, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68 | SMD | 22 µF | X7R | 16 V | Ceramic capacitor |
| C21, C22, C23, C24 | THT | 33 nF | 5% | 630 V | Foil capacitor |
| C31, C57, C58 | SMD | 220 pF | NP0 | 500 V | Ceramic capacitor |
| C34, C40 | SMD | 1 nF | X7R | 50 V | Ceramic capacitor |
| C35 | SMD | 22 nF | X7R | 50 V | Ceramic capacitor |
| C36 | SMD | 33 µF | 10% | 25 V | Polarized capacitor |
| C38, C41, C42, C43 | THT | 2200 µF | 20% | 16 V | Electrolytic capacitor |
| C39 | SMD | 100 pF | X7R | 50 V | Ceramic capacitor |
| C48 | SMD | 330 µF | 20% | 4 V | Polarized capacitor |
| D1, D10, D15, D17 | SMD | BAT165 | | 40 V | Schottky diode |

| Designator | Comment | Value | Tolerance | Voltage | Description |
|---|---|---|---|---|---|
| D2, D13, D16 | SMD | MURS360BT3G | | 600 V | Standard diode |
| D3, D4, D9, D14 | SMD | RSFJL | | 600 V | Diode |
| D5 | THT | IDH06G65C5 | | 650 V | SiC diode |
| D6, D7 | SMD | Bat54S | | 30 V | |
| D8 | SMD | BZT52C15 | | 15 V | Zener diode |
| D11, D19 | SMD | DFLS1100 | | 100 V | Standard diode |
| D12 | SMD | DFLS160-7 | | 60 V | Standard diode |
| D18 | SMD | DFLS130L-7 | | 30 V | Standard diode |
| F1 | THT | F12.5H250V | | | Sicherung |
| IC2, IC3 | SMD | 2EDN7524F | | | 2EDN752x/2EDN852x |
| IC4 | SMD | ICE2QR2280G | | | CoolSET™–Q1 |
| IC5 | SMD | TL431 | 0.5% | | TL431 – adjustable precision shunt regulator |
| IC6 | SMD | IFX1117MEV33 | | | Voltage regulator, 3.3 V output |
| IC7, IC8 | SMD | 1EDI20N12AF | | | Single-channel MOSFET gate driver IC |
| IC9 | SMD | VOL617A-3 | | | Optocoupler |
| L1 | THT | 650 µH | | | PFC choke |
| L2, L3 | THT | 5 mH | | | CM power line choke |
| L4 | SMD | 120 nH | | | Output filter choke |
| NTC1 | THT | 30 R | ±20% | | NTC resistor |
| Q1, Q2, Q3, Q4, Q10, Q11 | SMD | BSC014N04LS | | 40 V | N-channel OptiMOS™ 5 power transistor, 40 V VDS, 100 A ID, -55°C to 150°C, PG-TDSON-8-1, reel, green |
| Q5, Q6 | SMD | BSC009NE2LS5I | | 25 V | N-channel OptiMOS™ 5 power transistor, 40 V VDS, 100 A ID, -55°C to 150°C, PG-TDSON-8-1, reel, green |
| Q7, Q8 | THT | IPP60R280P7 | | 600 V | n-MOSFET |
| Q9 | THT | IPW60R099P7 | | 600 V | n-MOSFET |
| R1 | SMD | 390 R | 1% | | Resistor |
| R2, R3, R4, R6, R7, R8, R9, R16 | SMD | 750 k | 0.1% | | Resistor |
| R5, R13, R49 | SMD | 0 R | 1% | | Resistor |
| R10 | SMD | 0R008 | 1% | | Resistor |

| Designator | Comment | Value | Tolerance | Voltage | Description |
|---|---|---|---|---|---|
| R11, R12, R19, R41, R50, R51 | SMD | 4R7 | 1% | | Resistor |
| R14, R18, R21, R34, R40 | SMD | 15 k | 1% | | Resistor |
| R15, R20, R25, R32, R37, R42, R52 | SMD | 390 R | 1% | | Resistor |
| R17, R26, R48 | SMD | 10 R | 1% | | Resistor |
| R22 | SMD | 1 K | 1% | | Resistor |
| R23, R24, R27, R28, R29 | SMD | 150 k | 1% | | Resistor |
| R30, R31, R35, R36 | SMD | R001 | 1% | | Resistor |
| R38, R39 | SMD | 68 k | 1% | | Resistor |
| R43, R45 | SMD | 866 R | 1% | | Resistor |
| R44 | SMD | 68 R | 1% | | Resistor |
| R46, R47 | SMD | 2K7 | 1% | | Resistor |
| REL1 | THT | OJE-SS-112HM | | 12 V | Relais+ Schließer |
| TF1 | THT | PQI3523 DMR95 | | | |
| TF2 | THT | EE16-10PIN | | | Bias transformer |
| TR1 | THT | 1:50 | | | Current Sense Transformer |
| X1 | THT | B2B-ZR | | | Pin header, 2-pole |
| X8, X9 | THT | SQW-116-01-L-D | | | Pin header, 2 × 16 contacts |
| C69 | THT | 4700 µF | 20% | 450 V | Electrolytic capacitor |

**Table 12 Control board components**

| Designator | Comment | Value | Tolerance | Voltage | Description |
|---|---|---|---|---|---|
| C1, C2, C6, C8, C25, C26, C28, C29, C34, C35, C36, C40 | SMD | 100 nF | X7R | 25 V | Ceramic capacitor |
| C3, C4, C20, C21, C24 | SMD | 330 pF | X7R | 50 V | Ceramic capacitor |
| C5, C7, C10, C11, C27, C31, C32, C33 | SMD | 10 µF | X5R | 6.3 V | Ceramic capacitor |
| C9, C19, C22 | SMD | 4n7 | X7R | 50 V | Ceramic capacitor |
| C12, C41, C42, C43 | SMD | 10 pF | X7R | 50 V | Ceramic capacitor |
| C13, C15 | SMD | 1.5 nF | X7R | 25 V | Ceramic capacitor |

| Designator | Comment | Value | Tolerance | Voltage | Description |
|---|---|---|---|---|---|
| C14 | SMD | 33 pF | X7R | 50 V | Ceramic capacitor |
| C16 | SMD | 10 nF | X7R | 25 V | Ceramic capacitor |
| C17, C18 | SMD | 15 pF | X7R | 50 V | Ceramic capacitor |
| C23, C30 | SMD | 10 nF | X7R | 50 V | Ceramic capacitor |
| C37, C38, C39 | SMD | 470 pF | X7R | 50 V | Ceramic capacitor |
| C44 | SMD | 1 nF | X7R | 25 V | Ceramic capacitor |
| D1, D2, D14, D15 | SMD | Blue LED 0603 | | | Diode LED |
| D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13 | SMD | Bat54S | | | Diode |
| IC1 | SMD | TL431B | | | Integrated Circuit |
| IC2 | SMD | XMC1402Q040X0128AA | | | Integrated Circuit |
| IC3 | SMD | OPA2376AIDR | | | Integrated Circuit |
| IC4 | SMD | LMH6642MF | | | Integrated Circuit |
| IC5 | SMD | XMC4200-F64K256 AB | | | Integrated Circuit |
| IC6 | SMD | 4DIR1400H | | | Integrated Circuit |
| L1 | SMD | Ferrite bead 60 Ω at 100 MHz | | | Inductor |
| R1, R18, R19 | SMD | 1 k | 1% | | Resistor |
| R2, R3, R34 | SMD | 82 k | 1% | | Resistor |
| R4, R6, R24, R26, R28 | SMD | 22 k | 1% | | Resistor |
| R5, R16, R17, R23, R27, R39, R43, R45 | SMD | 510 R | 1% | | Resistor |
| R7, R8, R9, R10, R12, R13, R49, R50, R51, R52, R53, R55, R56, R57, R58 | SMD | 20 k | 1% | | Resistor |
| R11, R14, R22, R31, R42, R59, R60, R61, R62, R63, R64, R65, R66, R67 | SMD | 10 R | 1% | | Resistor |
| R15, R21 | SMD | 0 R | 1% | | Resistor |

## Bill of Materials (BoM)

| Designator | Comment | Value | Tolerance | Voltage | Description |
|---|---|---|---|---|---|
| R20, R25 | SMD | 750 k | 1% | | Resistor |
| R29, R30, R41 | SMD | 10 k | 0.1% | | Resistor |
| R32, R36 | SMD | 200 R | 0.1% | | Resistor |
| R33, R37 | SMD | 100 k | 0.1% | | Resistor |
| R35 | SMD | 27k4 | 0.1% | | Resistor |
| R38 | SMD | 9k1 | 1% | | Resistor |
| R40 | SMD | 15k8 | 0.1% | | Resistor |
| R44, R46, R54, R68, R69, R70 | SMD | 470 R | 1% | | Resistor |
| R47, R48 | SMD | 47 R | 1% | | Resistor |
| T1 | SMD | BSS138N | | | MOSFET |
| X1 | SMD | TMM-116-05-S-D | | | Pin header, 2 × 16 contacts |
| X2 | SMD | 53398-0471 | | | Pin header, 4 contacts |
| X3 | SMD | 53398-0271 | | | Pin header |
| X4, X9 | SMD | | | | Pin header, 2 × 5 contacts |
| X5 | SMD | TMM-116-03-L-D | | | Pin header, 2 × 16 contacts |
| XTAL1 | SMD | 12 MHz | | | Crystal oscillator |

# 9 References

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## Revision history

| Document revision | Date | Description of changes |
|---|---|---|
| V 1.0 | 2017-07-10 | Initial release |
| V 1.1 | 2023-10-25 | Added Section 4.3 - Isolation partitioning on the control board |
| | | |

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