42 W 12 V 5 V SMPS demo board with ICE5QR0680AZ

DEMO_5QR0680AZ_42W1

About this document

Scope and purpose

This document is an engineering report that describes a universal input 42 W, 12 V and 5 V off-line flyback converter using the latest 5th generation Infineon QR CoolSET™ ICE5QR0680AZ which offers high efficiency, low standby power with selectable entry and exit standby power options, wide V CC operating range with fast start up, robust line protection with input OVP and brownout and various modes of protection for a highly reliable system. This demo board is designed for users who wish to evaluate the performance of ICE5QR0680AZ and its ease of use.

Intended audience

This document is intended for power supply design engineers, application engineers, students, etc., who wish to design a low cost and highly reliable off-line SMPS. This can be an auxiliary power supply for white goods, PC, server and TV or an enclosed adapter for a blu-ray player, set-top box, game console, etc.

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1 Abstract

This application note is an engineering report for a 42 W 12 V and 5 V demo board designed in a QR flyback converter topology using a 5th generation QR CoolSET™ device, ICE5QR0680AZ. The target applications for the ICE5QR0680AZ include auxiliary power supplies for white goods, PC, server and TV or enclosed adapter, blu-ray player, set-top box, game console, etc. With the CoolMOS™ integrated into this IC, it greatly simplifies the design and layout of the PCB. The improved novel digital frequency reduction with proprietary QR operation offers lower EMI and higher efficiency for a wide AC range by reducing the switching frequency difference between low- and high-line.

The enhanced active burst mode power enables flexibility in standby power operation range selection and QR operation during active burst mode. As a result, the system efficiency, over the entire load range, is significantly improved compared to a conventional free running QR converter implemented with only maximum switching frequency limitation at light load. In addition, numerous adjustable protection functions have been implemented in the ICE5QR0680AZ to protect the system and customize the IC for the chosen application. In the case of a failure mode, such as brownout or line over-voltage, V CC over/under voltage, open control loop or overload, output overvoltage, over temperature, V CC short to ground and CS short to ground, the device enters a protection mode. By means of the cycle-by-cycle peak current limitation, the dimension of the transformer and current rating of the secondary diode can both be optimized. Thus, a cost effective solution can be easily achieved.

2 Demo board

This document contains a list of features, the power supply specification, schematic, BOM and the transformer construction documentation. Typical operating characteristics such as the performance curve and oscilloscope waveforms are shown at the end of the report.

Figure 1 DEMO_5QR0680AZ_42W1

3 Specifications of demo board

Table 1 Specifications of DEMO_5QR0680AZ_42W1

Input voltage and frequency	85 V AC (60 Hz) ~ 300 V AC (50 Hz)
Output voltage, current and power	(12 V x 3.41 A) +(5 V x 0.2 A) = 42 W
Dynamic load response (5 V at 0.2 A and 12 V load change from 10% to 100%, slew rate at 0.4 A/µs, 100 Hz)	±5% of nominal output voltage
Output ripple voltage (full load, 85 V AC ~ 300 V AC)	5 $V_{ripple\_p\_p}$< 100 mV 12 $V_{ripple\_p\_p}$< 100 mV
Active mode four point average efficiency (25%, 50%, 75%, 100% load)	> 85% at 115 V AC and 230 V AC
No load power consumption	< 100 mW at 230 V AC
Conducted emissions (EN55022 class B)	Pass with 10 dB margin for 115 V AC and 6 dB margin for 230 V AC
ESD immunity (EN61000-4-2)	Special Level (±10 kV for contact and air discharge)
Surge immunity (EN61000-4-5)	Installation class 4 (±2 kV for line to line and ±4 kV for line to earth)
Form factor case size (L x W x H)	(136 x 80 x 35) mm^3

Note: *"The demo board is designed for dual output with cross regulated loop feedback. It may not regulate properly if loading is applied only to single output. If the user wants to evaluate a single output (12 V only) condition, the following changes are necessary on the board.*

1. Remove D22, L22, C28, C210, R25A (to disable 5 V output)
2. Change R26 to 10 kΩ and R25 to 38 kΩ (to disable 5 V feedback and enable 100% weighted factor on 12 V output)

Since the board (especially the transformer) is designed for dual output with optimized cross regulation, single output efficiency might not be optimized. It is only intended for functional evaluation of the IC under a single output condition."

4 Circuit description

4.1 Line input

The AC line input side comprises the input fuse F1 as over-current protection. The choke L11, X-capacitor C11, C14 and Y-capacitor C12, C12A and C12B act as EMI suppressors. Optional spark gap devices SA1, SA2 and varistor VAR can absorb high voltage stress during a lightning surge test. A rectified DC voltage (120~424 V DC) is obtained through the bridge rectifier BR1 together with bulk capacitor C13.

4.2 Start-up

To achieve the fast and safe start-up, ICE5QR0680AZ has been implemented with a startup resistor and V CC short to GND protection. When V_{VCC} reaches the turn-on voltage threshold of 16 V, the IC begins with a soft-start. The soft-start implemented in ICE5QR0680AZ is a digital time-based function. The preset soft-start time is 12 ms with four steps. If not limited by other functions, the peak voltage on the CS pin will increase step by step from 0.3 V to 1 V. After the IC turns on, the V CC voltage is supplied by the auxiliary windings of the transformer. V CC short to GND protection is implemented during the startup time.

4.3 Integrated MOSFET and PWM control

ICE5QR0680AZ comprises a power MOSFET and the proprietary novel QR controller which enables higher average efficiency and low EMI. This integrated solution greatly simplifies the circuit layout and reduces the cost of PCB manufacturing. The PWM switch-on is determined by the zero-crossing detection input signal and the value of the up/down counter. The PWM switch-off is determined by the feedback signal V_{FB} and the current sensing signal V_{CS}. ICE5QR0680AZ also performs all necessary protection functions in flyback converters. Details about the information mentioned above are contained in the product datasheet.

4.4 RCD clamper circuit

A clamper network (R11, C15 and D11) dissipates the energy of the leakage inductance and suppress ringing on the SMPS transformer.

4.5 Output stage

There are two outputs on the secondary side, 12 V and 5 V. The power is coupled out via schottky diodes D21 and D22. The capacitors C22, C23 and C28 provide energy buffering followed by the L-C filters L21-C24 and L22-C210 to reduce the output ripple and prevent interference between the SMPS switching frequency and line frequency considerably. Storage capacitors C22, C23 and C28 are designed to have an internal resistance (ESR) as small as possible to minimize the output voltage ripple caused by the triangular current.

4.6 Feedback loop

For feedback, the output is sensed by the voltage divider of R26, R25, R25A and compared to the IC21 (TL431) internal reference voltage. C25, C26 and R24 comprise the compensation network. The output voltage of IC21 (TL431) is converted to a current signal via optocoupler IC12 and two resistors R22 and R23 for regulation control.

4.7 Primary side peak current control

The MOSFET drain source current is sensed via external resistors R14 and R14A. Since ICE5QR0680AZ is a current mode controller, it would have a cycle-by-cycle primary current and feedback voltage control which can ensure that the maximum power of the converter is controlled in every switching cycle.

For a QR flyback converter, the maximum possible output power is increased when a constant current limit value is used for all of the line input voltage range. This is usually not desired as this will increase the cost of the transformer and output diode in case of output over power conditions.

Internal current limitation with a line dependent V_{CS} curve and the proprietary novel QR switching which reduces the switching frequency difference between minimum and maximum line are implemented in the ICE5QR0680AZ. As a result, the maximum output power can be properly limited against the input voltage.

4.8 Digital frequency reduction

During normal operation, the switching frequency for ICE5QR0680AZ is digitally reduced with decreasing load. At light load, the MOSFET will be turned on not at the first minimum drain-source voltage time, but on the n^{th}. The counter is in the range of one to eight for low line and three to ten for high line, which depends on the feedback voltage in a time-base. The feedback voltage decreases when the output power requirement decreases, and vice-versa. Therefore, the counter is set by monitoring voltage V_{FB}. The counter will be increased with low V_{FB} and decreased with high V_{FB}. The thresholds are preset inside the IC.

4.9 Active burst mode

Active burst mode entry and exit power (two levels) can be selected in ICE5QR0680AZ. Details are contained in the product datasheet. Active burst mode power level one is used in this demo board (R17=open). At light load conditions, the SMPS enters into Active burst mode with QR switching. At this stage, the controller is always active but the V_{VCC} must remain above the switch-off threshold. During active burst mode, the efficiency increases significantly and at the same time it supports low ripple on V_{out} and fast response on load jump.

For determination of entering active burst mode operation, three conditions apply:

1. the feedback voltage is lower than the threshold of V_{FB_EBLX}
2. the up/down counter is eight for low line and ten for high line and
3. a certain blanking time (t_{FB_BEB}=20 ms).

Once all of these conditions are fulfilled, the active burst mode flip-flop is set and the controller enters active burst mode operation. This multi-condition determination for entering active burst mode operation prevents mis-triggering of entering active burst mode operation, so that the controller enters active burst mode operation only when the output power is really low during the preset blanking time.

During active burst mode, the maximum current sense voltage is reduced from V_{CS_N} to V_{CS_BLX} so as to reduce the conduction loss and the audible noise. During burst mode, the Feedback (FB) voltage represents a sawtooth between V_{FB_BOFF} and V_{FB_BON}.

The feedback voltage immediately increases if there is a high load jump. This is observed by one comparator. As the current limit is 31/35% during active burst mode a certain load is needed so that the FB voltage can exceed V_{FB_LB}. After leaving active burst mode, maximum current can now be provided to stabilize V_{out}. In addition, the up/down counter will be set to one (low line) or three (high line) immediately after leaving active burst mode. This is helpful to decrease the output voltage undershoot.

5 Protection features

Protection is one of the major factors to determine whether the system is safe and robust. Therefore sufficient protection is necessary. ICE5QR0680AZ provides a comprehensive protection to ensure the system is operating safely. The protections include line over-voltage, brownout, V CC over-voltage and under voltage, overload, output over-voltage, over temperature (controller junction), CS short to GND and V CC short to GND. When those faults are found, the system will go into the protection mode. It is then until the fault is removed, the system resumes to normal operation. A list of protections and the failure conditions are shown in the below table.

Table 2 Protection function of ICE5QR0680AZ

Protection function	Failure condition	Protection mode
Line over-voltage	V_{VIN} > 2.9 V	Non switch auto restart
Brownout	V_{VIN} < 0.4 V	Non switch auto restart
V CC over-voltage	V_{VCC} > 25.5 V	Odd skip auto restart
V CC under voltage	V_{VCC} < 10 V	Auto restart
Overload	V_{FB} > 2.75 V & last for 30 ms	Odd skip auto restart
Output over-voltage	V_{ZCD} > 2 V & last for 10 consecutive pulses	Odd skip auto restart
Over temperature (junction temperature of controller chip only)	T_J > 140 °C with 40°C hysteresis to reset	Non switch auto restart
CS short to GND	V_{CS} < 0.1 V, lasting for 5 µs and three consecutive pulses	Odd skip auto restart
V CC short to GND (V_{VCC}=0 V, $R_{StartUp}$=50 MΩ and V_{DRAIN}=90 V)	V_{VCC}< 1.1 V, $I_{VCC\_Charge1}$≈-0.2 A	Cannot start-up

6 Circuit diagram

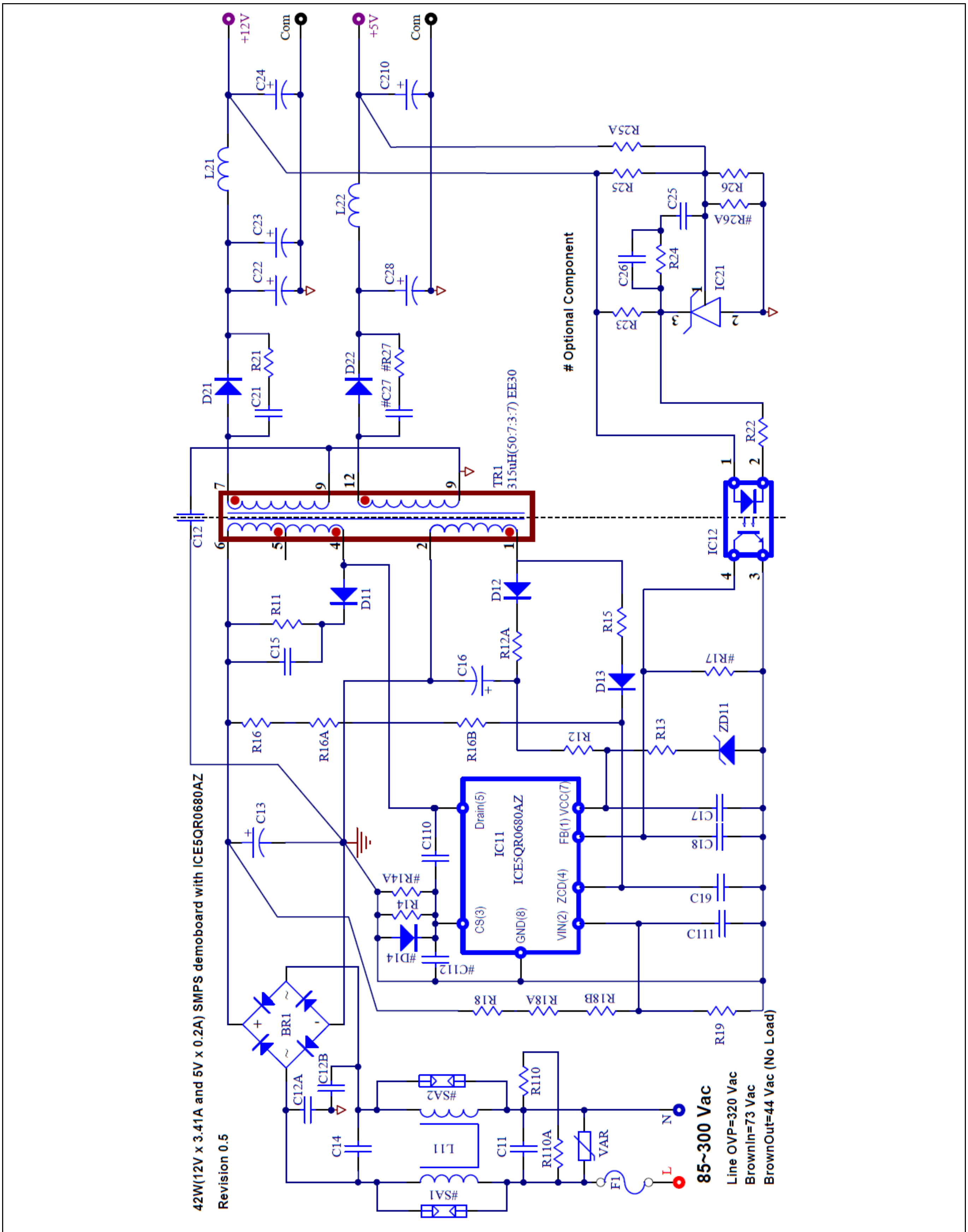


Figure 2 Schematic of DEMO_5QR0680AZ_42W1

Note: General guidelines for layout of PCB:

1. *Star ground at bulk capacitor C13: all primary grounds should be connected to the ground of bulk capacitor C13 separately at a single point. It can reduce the switching noise going into the sensitive pins of the CoolSET™ device effectively. The primary star ground can be split into four groups as follows,*
   i. *Combine signal (all small signal grounds connecting to the CoolSET™ GND pin such as filter capacitor ground C17, C18, C19, C111, C112 and opto-coupler ground) and power ground (current sense resistors R14 and R14A).*
   ii. *V CC ground includes the V CC capacitor ground C16 and the auxiliary winding ground, pin two of the power transformer.*
   iii. *EMI return ground includes Y capacitor C12.*
   iv. *DC ground from bridge rectifier, BR1*
2. *Filter capacitor close to the controller ground: Filter capacitors, C17, C18, C19, C11 and C112 should be placed as close to the controller ground and the controller pin as possible so as to reduce the switching noise coupled into the controller.*
3. *High voltage traces clearance: High voltage traces should maintain sufficient spacing to the nearby traces to avoid arcing.*
   i. *400 V traces (positive rail of bulk capacitor C13) to nearby trace: > 2.0 mm*
   ii. *600 V traces (drain voltage of CoolSET™ IC11) to nearby trace: > 2.5 mm*
4. *Recommended minimum of 232mm^2 copper area at the drain pin to add on PCB for better thermal performance.*
5. *Power loop area (bulk capacitor C13, primary winding of the transformer TR1 (Pin four and six), IC11 drain pin, IC11 CS pin and current sense resistor R14/R14A) should be as small as possible to minimize the switching emissions.*

7 PCB layout

7.1 Top side

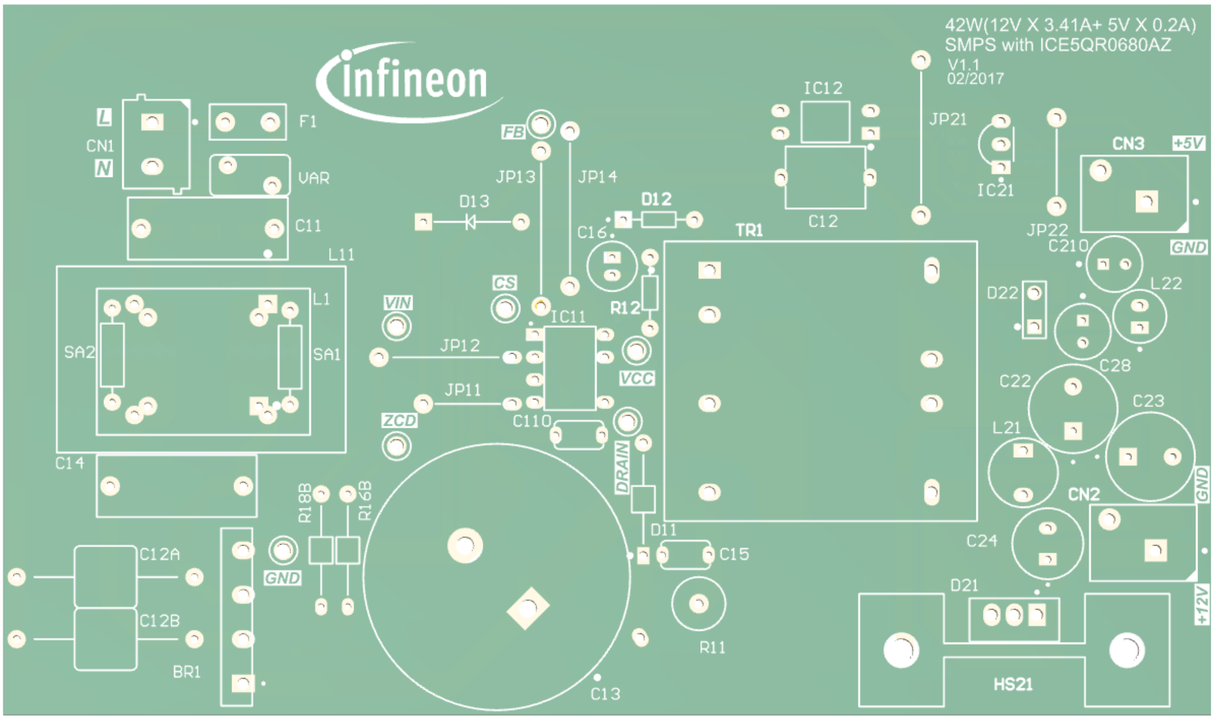


Figure 3 Top side component legend

7.2 Bottom side

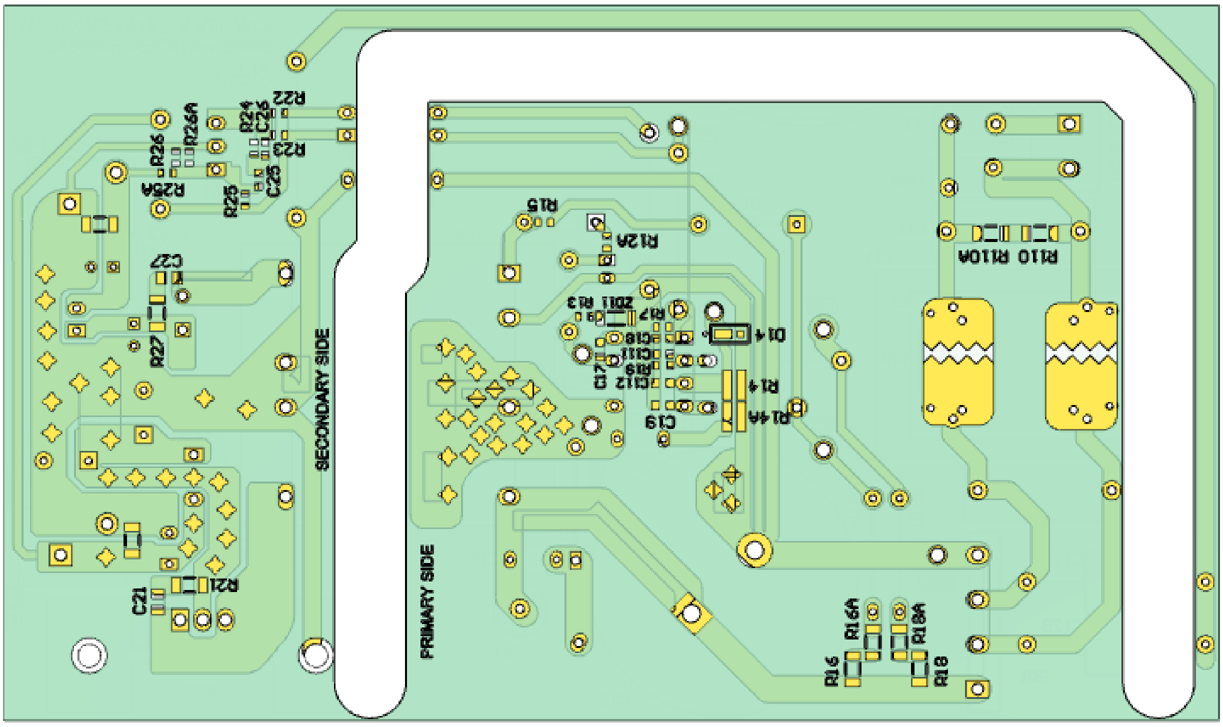


Figure 4 Bottom side copper and component legend

8 BOM

Table 3 BOM (R0.7)

No.	Designator	Description	Part Number	Manufacturer	Quantity
1	BR1	600 V/2 A	D2SB60A	Shindengen	1
2	C11	0.22 µF/310 V	890334024002	Wurth Electronics	1
3	C12	2.2 nF/500 V	DE1E3RA222MA4BQ	Murata	1
4	C12A, C12B	470 pF/400 V	DE2B3SA471KA3BY	Murata	2
5	C13	120 µF/500 V	LGN2H121MELB30		1
6	C14	47 nF/310 V	890334023015	Wurth Electronics	1
7	C15	4.7 nF/1000 V	RDE7U3A472J4K1H03	Murata	1
8	C16	33 µF/50 V	50PX33MEFC5X11	Rubycon	1
9	C17	100 nF/50 V	GRM188R71H104KA93D	Murata	1
10	C18, C26	1 nF/50 V	GRM1885C1H102GA01D	Murata	2
11	C19	47 pF/50 V	GRM1885C1H470GA01D	Murata	1
12	C110	22 pF/1000 V	RDE7U3A220J2K1H03	Murata	1
13	C111	22 nF/50 V	GCM188R71H223KA37D	Murata	1
14	C22, C23	1000 uF/16 V	16ZLH1000MEFC10X16	Rubycon	2
15	C24	470 uF/16 V	16ZLH470MEFC8X11.5	Rubycon	1
16	C25	220 nF/50 V	GRM188R71H224KAC4D	Murata	1
17	C28, C210	330 uF/10 V	10ZLH330MEFC6.3X11	Rubycon	2
18	D11	1 A/800 V	UF4006		1
19	D12	0.2 A/200 V	1N485B		1
20	D13	0.2 A/150 V/50 ns	FDH400		1
21	D21	30 A/100 V	VF30100SG		1
22	D22	1 A/50 V	SB150		1
23	F1	2 A/300 V	36912000000		1
24	HS21	Heatsink	513002B02500G		1
25	IC11	ICE5QR0680AZ	ICE5QR0680AZ	Infineon	1
26	IC12	Optocoupler	SFH617A-3		1
27	IC21	Shunt regulator	TL431BVLPG		1
28	JP11, JP12, JP13, JP14, JP21 and JP22	Jumper			6
29	L11	39 mH/1.4 A	B82734R2142B030	Epcos	1
30	L21	2.2 uH/6 A	744772022	Wurth Electronics	1
31	L22	4.7 uH/4.2 A	744 746 204 7	Wurth Electronics	1
32	R11	33 kΩ /2 W/350 V	ERG-2SJ333A	Panasonic	1
33	R12	27 Ω (Leaded Type)			1
34	R12A	0 Ω (0603)			1
35	R13	27 Ω (0603)			1
36	R14	0.43Ω /1 W/±1%	ERJ-B2BFR43V	Panasonic	1
37	R15	24 kΩ/ ±1% (0603)			1
38	R16, R16A	15 MΩ (1206)	RC1206JR-0715ML		2
39	R16B	20 MΩ (Axial,1/8 W)			1
40	R18, R18A	3 M Ω (1206)	RC1206FR-073ML		2

41	R18B	3 MΩ (Axial,1/8 W)			1
42	R19	59 kΩ /0.5% (0603)	ERJ-3RBD5902V		1
43	R110, R110A	1.5 MΩ/200 V (1206)			2
44	R22	820 Ω (0603)			1
45	R23	1.2 kΩ (0603)			1
46	R24	12 kΩ (0603)			1
47	R25	16 kΩ (0603)			1
48	R25A	6.2 kΩ (0603)			1
49	R26	2.5 kΩ (0603)			1
50	TR1	315 μH	750343401(R04)	Wurth Electronics	1
51	Test point of FB, VIN, CS, ZCD, Drain, Vcc, Gnd	Test point	5010		7
52	VAR	0.25 W/320 V	B72207S2321K101	Epcos	1
53	ZD11	22 V (SOD123)	MMSZ5251B-7-F		1
54	Con(L N)	Connector	691102710002	Wurth Electronics	1
55	Con(+12V Com), Con(+5V Com)	Connector	691 412 120 002B	Wurth Electronics	2

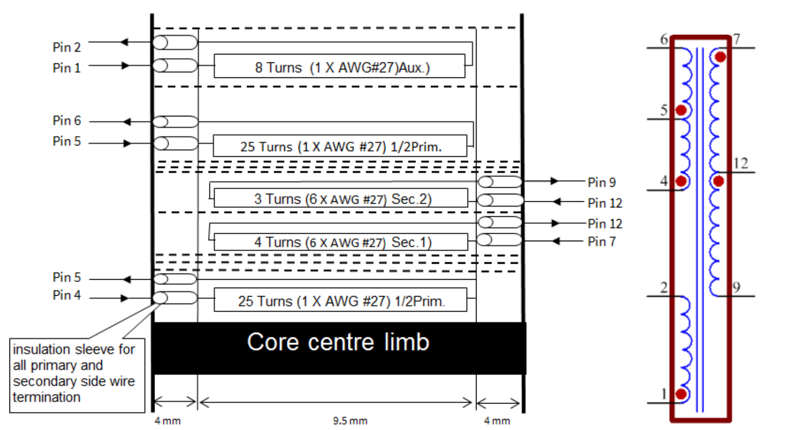
9 Transformer construction

Core and material: EE30/15/7 (EF30), TP4A (TDG)

Bobbin: 070-5313 (12 Pin, THT, horizontal version)

Primary inductance: Lp=315 µH (±10%), measured between pin four and pin six

Manufacturer and part number: Wurth Electronics Midcom (750343401 R04)



Start	Stop	No. of turns	Wire size	Layer
4	5	25	1XAWG#27	1/2 Primary
7	12	4	6XAWG#27	Secondary 1
12	9	3	6XAWG#27	Secondary 2
5	6	25	1XAWG#27	1/2 Primary
1	2	8	1XAWG#27	Auxiliary

Horizontal and vertical external shields are added and tied to Pin 2.

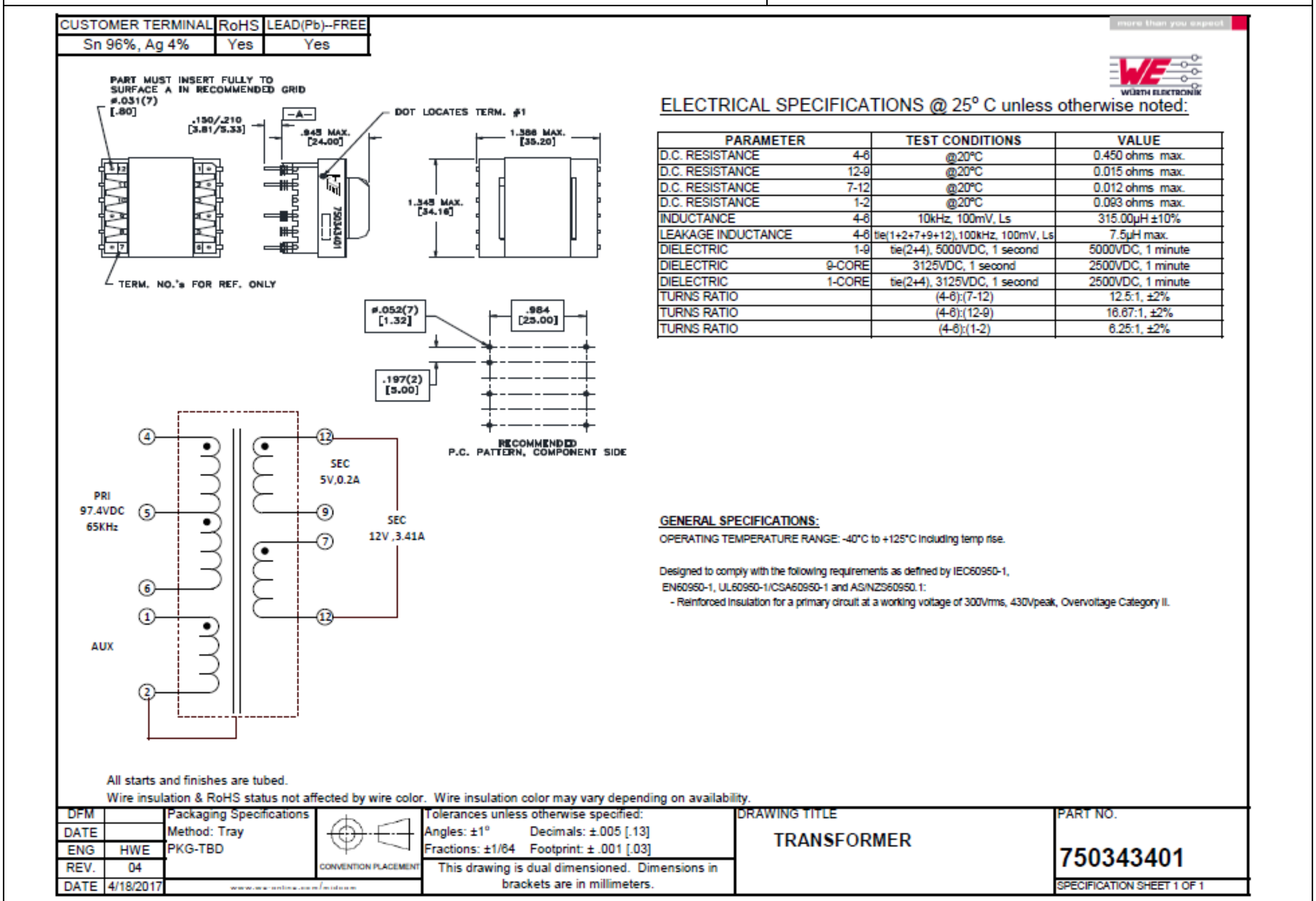


Figure 5 Transformer structure

10 Test results

10.1 Efficiency, regulation and output ripple

Table 4 Efficiency, regulation and output ripple

Input (V AC/Hz)	P_{in} (W)	V_5 (V DC)	I_5 (A)	V_{5RPP} (mV)	V_{12} (V DC)	I_{12} (A)	V_{12RPP} (mV)	P_{out} (W)	η (%)	Average η (%)	OLP P_{in} (W)	OLP $I_{out12\,V}$ Fixed 5 V at 0.2A (A)
85V AC/ 60 Hz	0.05	4.94	0.000	32	12.16	0.000	45				59.90	3.96
	0.08	4.66	0.006	95	12.84	0.000	25	0.03	32.91			
	14.81	4.98	0.060	14	12.04	1.010	28	12.46	84.13			
	12.19	4.98	0.050	14	12.03	0.834	24	10.29	84.38	83.99		
	24.77	4.99	0.100	14	12.04	1.700	34	20.97	84.65			
	37.34	4.99	0.150	18	12.04	2.552	45	31.47	84.29			
	51.02	4.99	0.200	20	12.05	3.416	57	42.16	82.64			
115V AC/ 60 Hz	0.05	4.93	0.000	32	12.17	0.000	67				66.00	4.60
	0.09	4.66	0.006	95	12.84	0.000	26	0.03	30.98			
	14.69	4.98	0.060	14	12.04	1.010	26	12.46	84.81			
	12.12	4.98	0.050	14	12.03	0.834	24	10.29	84.86	85.36		
	24.44	4.99	0.100	14	12.04	1.700	32	20.97	85.79			
	36.69	4.99	0.150	18	12.04	2.552	40	31.47	85.78			
	49.59	4.99	0.200	20	12.05	3.416	47	42.16	85.02			
230V AC/ 50 Hz	0.08	4.93	0.000	32	12.17	0.000	48				74.00	5.18
	0.12	4.64	0.006	95	12.92	0.000	29	0.03	22.84			
	14.83	4.98	0.060	14	12.04	1.010	29	12.46	84.01			
	12.29	4.98	0.050	14	12.03	0.834	24	10.29	83.69	85.52		
	24.43	4.97	0.100	14	11.93	1.705	34	20.84	85.30			
	36.36	4.99	0.150	18	12.04	2.552	42	31.47	86.56			
	48.73	4.99	0.200	20	12.05	3.416	48	42.16	86.52			
265V AC/ 50 Hz	0.09	4.93	0.000	32	12.17	0.000	67				76.00	5.38
	0.14	4.64	0.006	95	12.92	0.000	32	0.03	20.40			
	14.94	4.98	0.060	14	12.04	1.010	25	12.46	83.39			
	12.43	4.98	0.050	14	12.03	0.834	25	10.29	82.75	85.22		
	24.53	4.99	0.100	14	12.04	1.700	35	20.97	85.47			
	36.49	4.99	0.150	18	12.04	2.552	42	31.47	86.25			
	48.79	4.99	0.200	20	12.05	3.416	48	42.16	86.42			
300 V AC/ 50 Hz	0.11	4.93	0.000	32	12.17	0.000	51				79.00	5.50
	0.15	4.61	0.006	95	12.99	0.000	29	0.03	18.08			
	15.07	4.98	0.060	14	12.04	1.010	26	12.46	82.68			
	12.59	4.98	0.050	14	12.03	0.834	24	10.29	81.70	84.70		
	24.64	4.99	0.100	14	12.04	1.700	36	20.97	85.09			
	36.68	4.99	0.150	18	12.04	2.552	42	31.47	85.80			
	48.90	4.99	0.200	20	12.05	3.416	48	42.16	86.22			

Minimum load condition : 5 V at 6 mA

Typical load condition : 5 V at 60 mA and 12 V at 1 A

Maximum load condition : 5 V at 200 mA and 12 V at 3.41 A

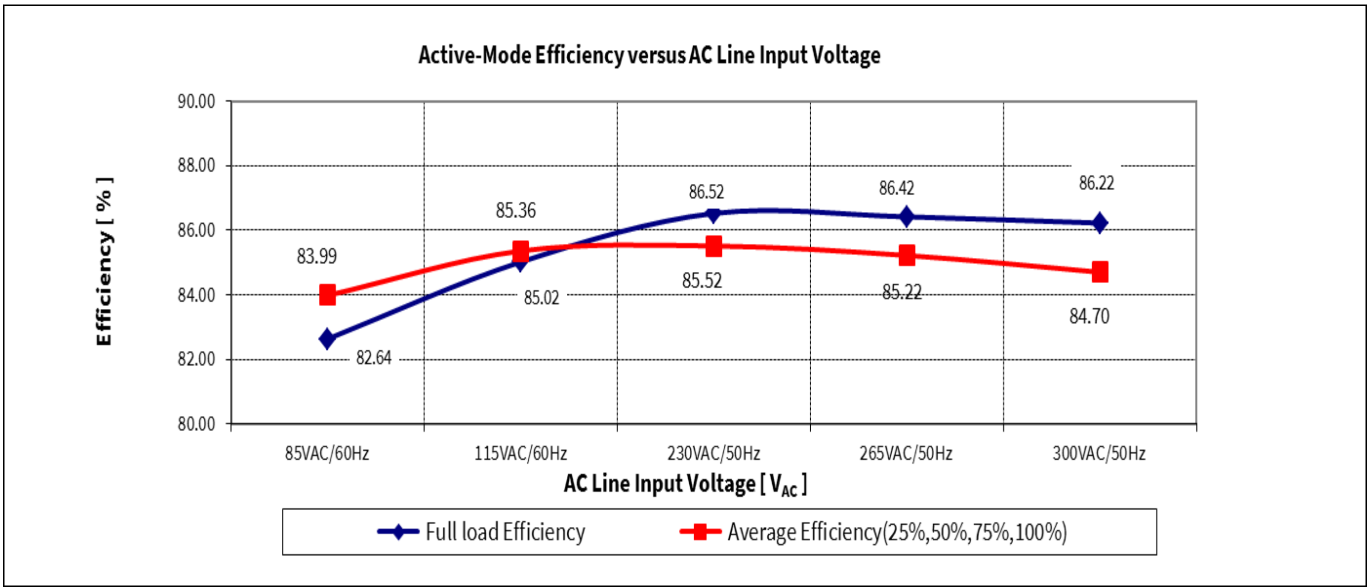


Figure 6 Efficiency vs AC line input voltage

10.2 Standby power

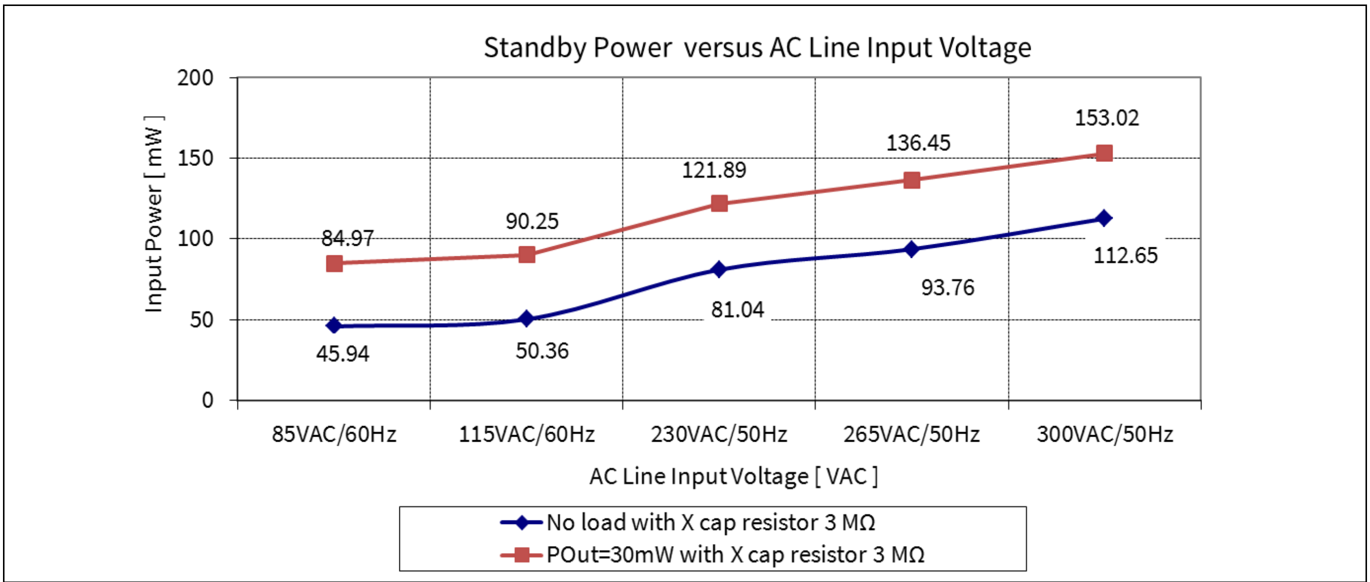


Figure 7 Standby power at no load and 30 mW load vs AC line input voltage (measured by Yokogawa WT210 power meter - integration mode)

10.3 Line regulation

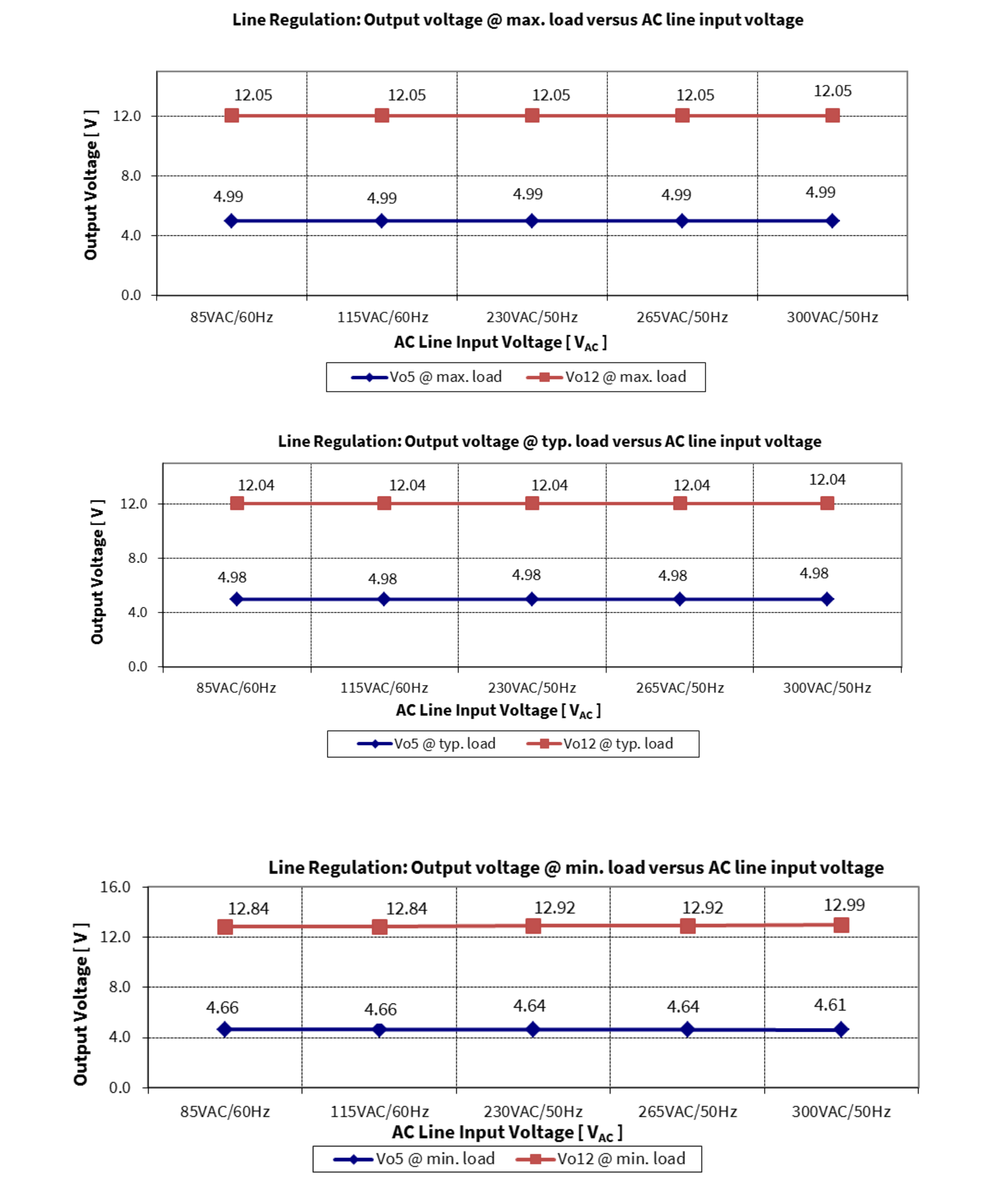


Figure 8 Line regulation V_{Out} vs AC line input voltage

10.4 Load regulation

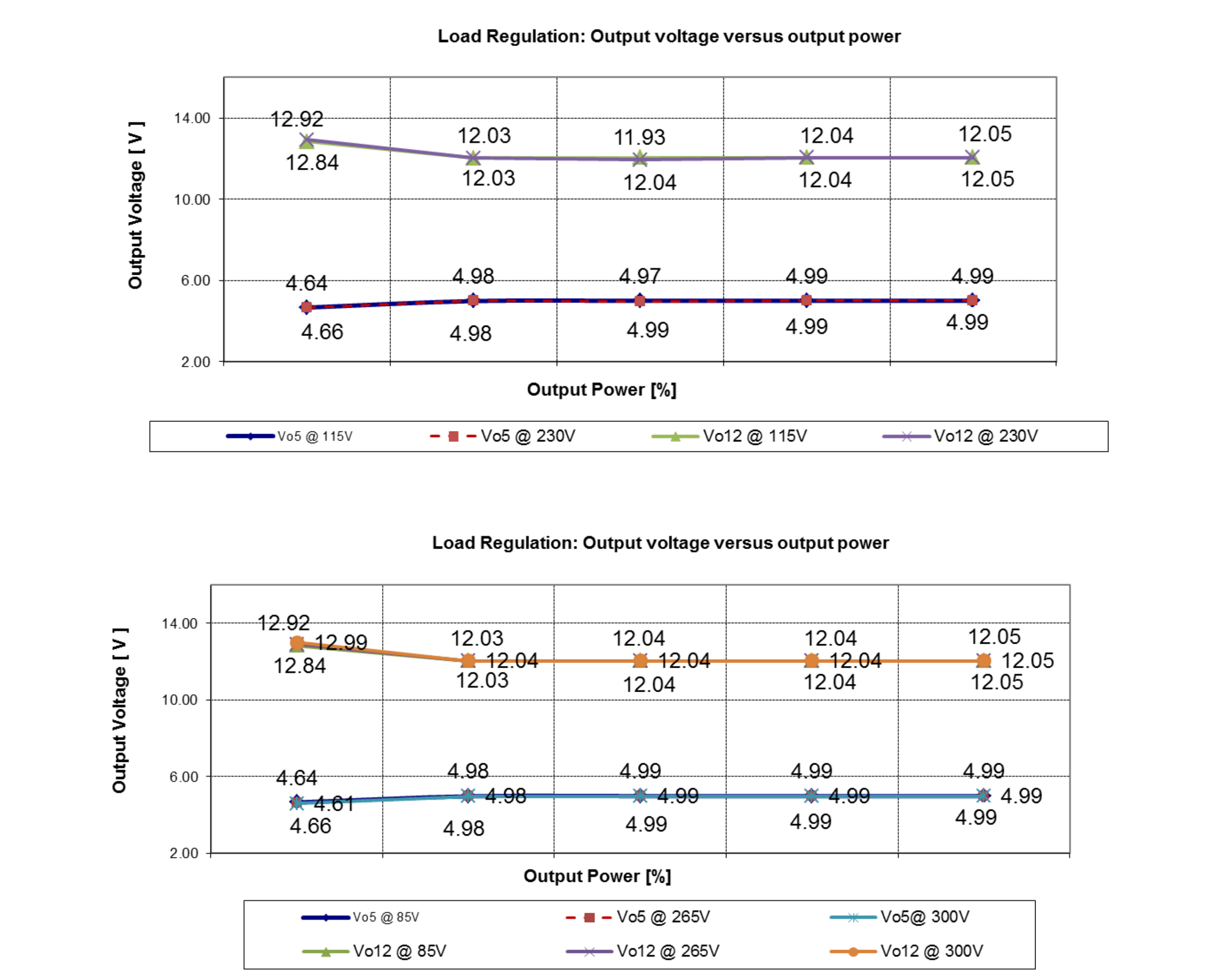


Figure 9 Load regulation V_{Out} vs output power

10.5 Maximum input power

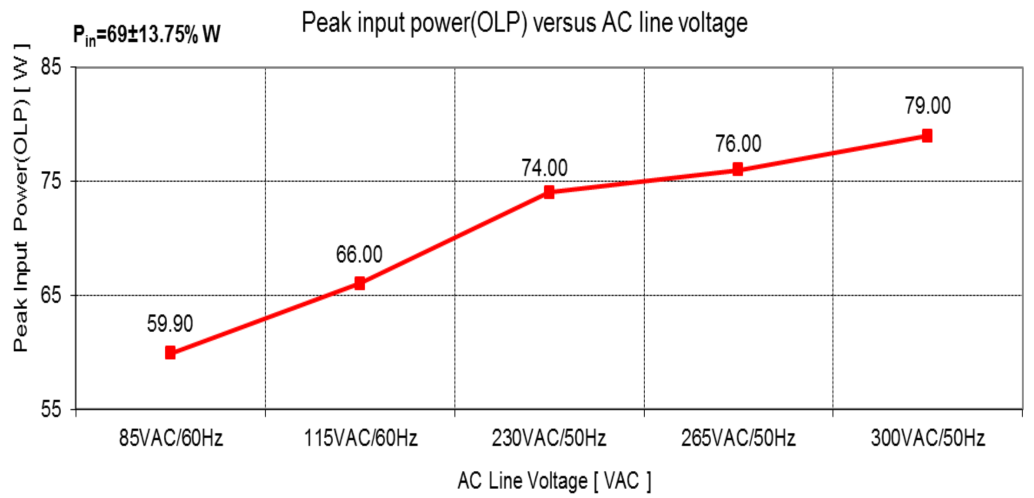


Figure 10 Maximum input power (before over-load protection) vs AC line input voltage

10.6 ESD immunity (EN61000-4-2)

Pass EN61000-4-2 special level (±10 kV for both contact and air discharge).

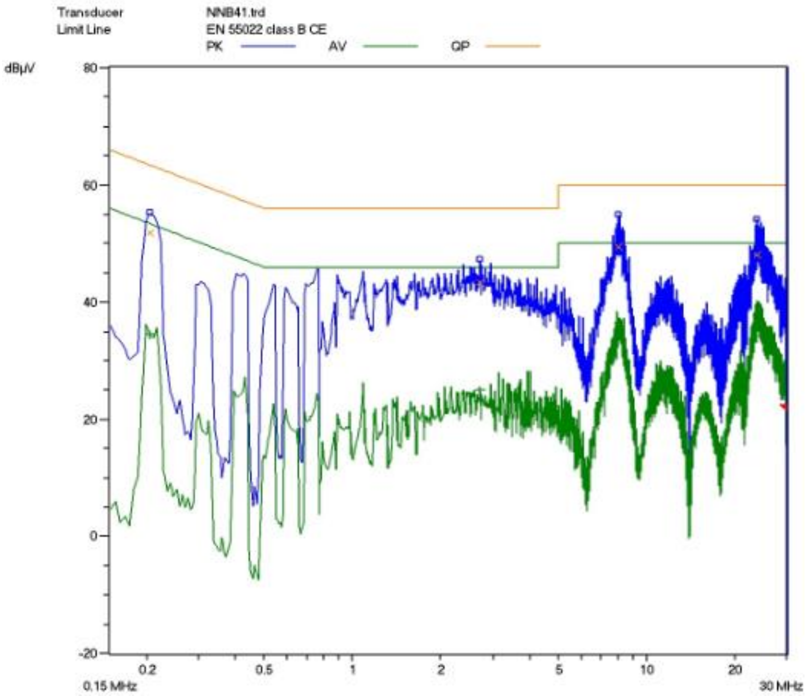
10.7 Surge immunity (EN61000-4-5)

Pass EN61000-4-5 Installation class 4 (±2 kV for line to line and ±4 kV for line to earth).

10.8 Conducted emissions (EN55022 class B)

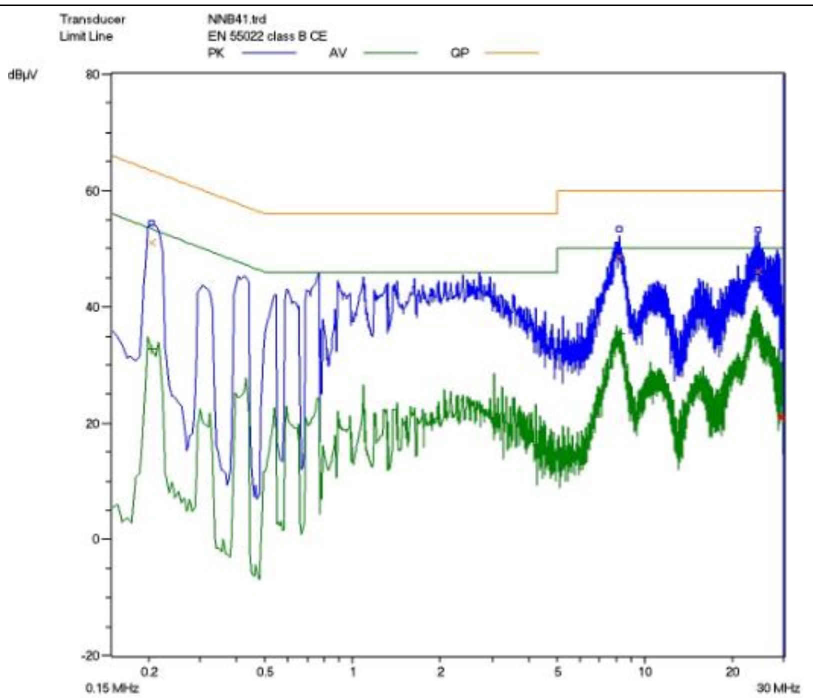
The conducted EMI was measured by Schaffner (SMR4503) in accordance with the test standard of EN55022 (CISPR 22) class B. The demo board was set up at maximum load (42 W) with input voltage of 115 V AC and 230 V AC.

Pass conducted emissions EN55022 (CISPR 22) class B with 10 dB margin for quasi peak measurement at low line (115 V AC) and 6 dB margin for high line (230 V AC).



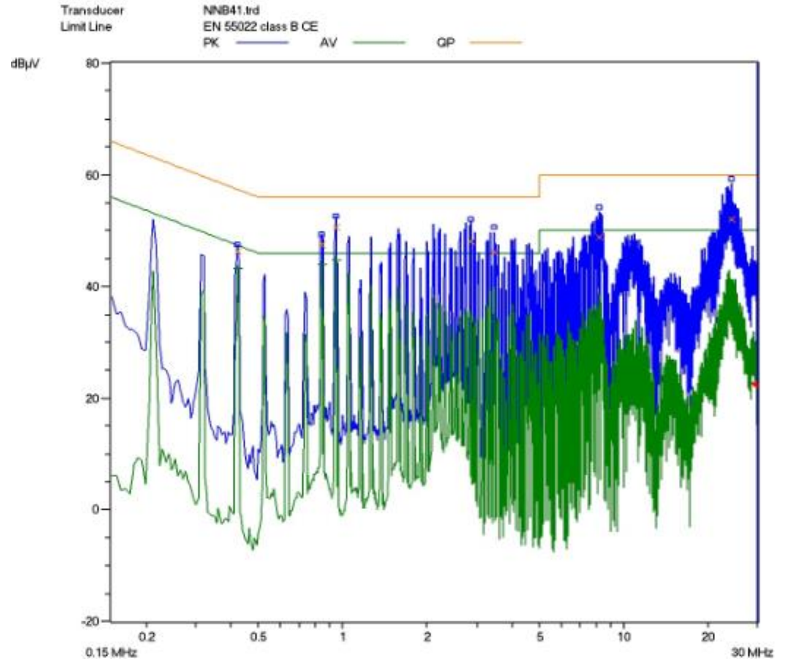
Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.2040	L	55.3	L	34.5	L	51.8	53.4	63.4
2.7180	L	47.3	L	25.1	L	43.3	46.0	56.0
8.0400	L	55.1	L	36.5	L	49.5	50.0	60.0
23.8400	L	54.2	L	37.8	L	48.1	50.0	60.0

Figure 11 Conducted emissions (line) at 115 V AC and maximum load



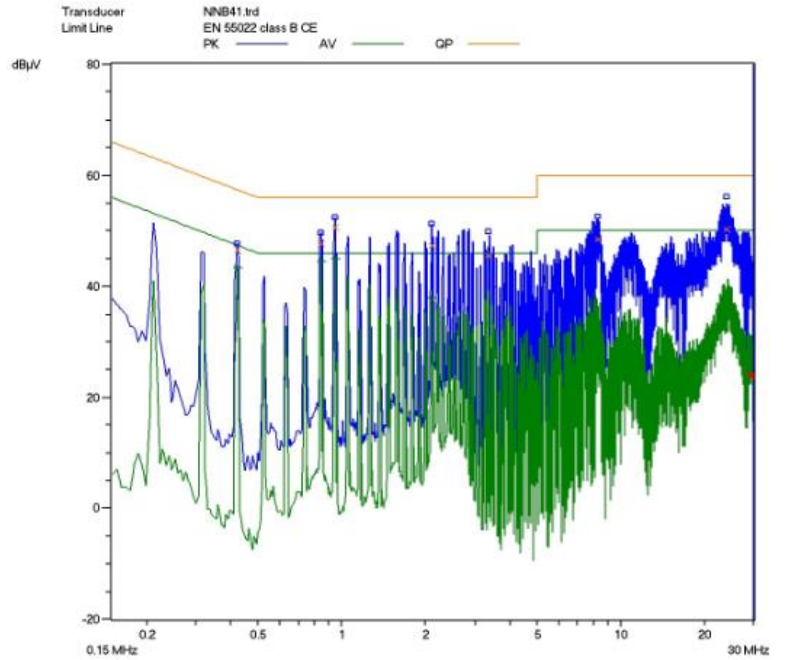
Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.2040	N	54.4	N	32.8	N	51.1	53.4	63.4
8.1760	N	53.5	N	35.4	N	48.6	50.0	60.0
24.6320	N	53.2	N	36.5	N	46.2	50.0	60.0

Figure 12 Conducted emissions (neutral) at 115 V AC and maximum load



Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.4200	L	47.5	L	43.2	L	46.4	47.4	57.4
0.8400	L	49.3	L	44.0	L	47.5	46.0	56.0
0.9420	L	52.6	L	44.8	L	50.0	46.0	56.0
2.8440	L	52.0	L	34.4	L	48.2	46.0	56.0
3.4720	L	50.6	L	33.8	L	46.2	46.0	56.0
8.2160	L	54.1	L	30.8	L	48.8	50.0	60.0
24.2400	L	59.4	L	37.8	L	52.0	50.0	60.0

Figure 13 Conducted emissions (line) at 230 V AC and maximum load



Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP
0.4200	N	47.7	N	43.3	N	46.5	47.4	57.4
0.8400	N	49.8	N	44.5	N	47.7	46.0	56.0
0.9420	N	52.4	N	45.0	N	50.0	46.0	56.0
2.0940	N	51.2	N	37.8	N	47.3	46.0	56.0
3.3680	N	49.9	N	33.4	N	45.5	46.0	56.0
8.2960	N	52.6	N	32.2	N	48.5	50.0	60.0
24.1040	N	56.3	N	38.0	N	50.2	50.0	60.0

Figure 14 Conducted emissions (neutral) at 230 V AC and maximum load

10.9 Thermal measurement

The thermal test of the open frame demo board was performed using an infrared thermography camera (FLIR-T62101) at an ambient temperature of 25°C. The measurements were taken after one hour running at full load.

Table 5 Hottest temperature of demo board

No.	Major component	85 V AC (°C)	300 V AC (°C)
1	IC11 (ICE5QR0680AZ)	82.9	82.4
2	R14 (current sense resistor)	68.2	59.8
3	TR1 (transformer)	60.9	67.0
4	BR1 (bridge diode)	59.3	39.0
5	R11(clamper resistor)	90.0	81.2
6	L11 (choke)	65.8	37.3
7	D21 (Secondary diode)	67.7	66.0
8	D22 (Secondary diode)	51.8	51.1
9	Ambient	25.0	25.0

85 V AC full load and 25°C ambient | **300 V AC full load and 25°C ambient**

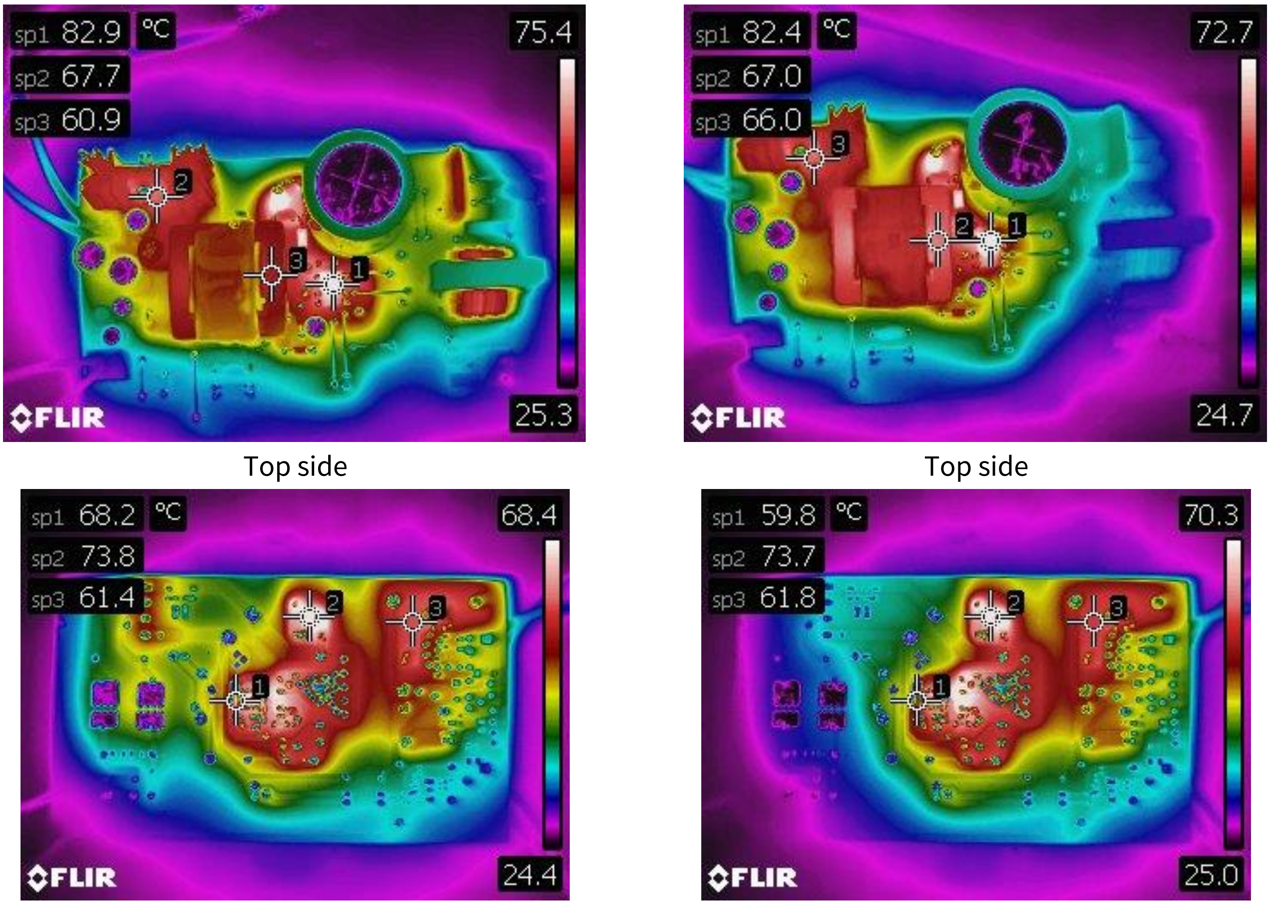


Figure 15 Infrared thermal image of DEMO_5QR0680AZ_42W1

11 Waveforms and oscilloscope plots

All waveforms and scope plots were recorded with a TELEDYNE LECROY 606Zi oscilloscope.

11.1 Start-up at low/high AC line input voltage with maximum load

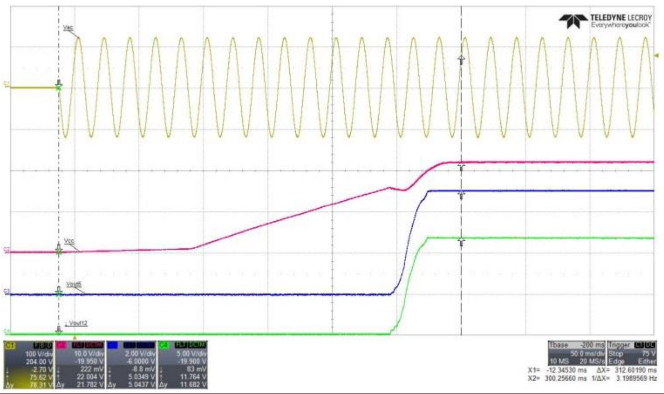
	
C1 (Yellow) : AC line voltage (V AC) C2 (Purple) : Supply voltage (V_{VCC}) C3 (Blue) : 5 V output voltage (V_{Out5}) C4 (Green) : 12 V output voltage (V_{Out12})	C1 (Yellow) : AC line voltage (V AC) C2 (Purple) : Supply voltage (V_{VCC}) C3 (Blue) : 5 V output voltage (V_{Out5}) C4 (Green) : 12 V output voltage (V_{Out12})
Startup time at 85 V AC and maximum load ≈ 312 ms	Startup time at 300 V AC and maximum load ≈ 262 ms

Figure 16 Startup

11.2 Soft-start

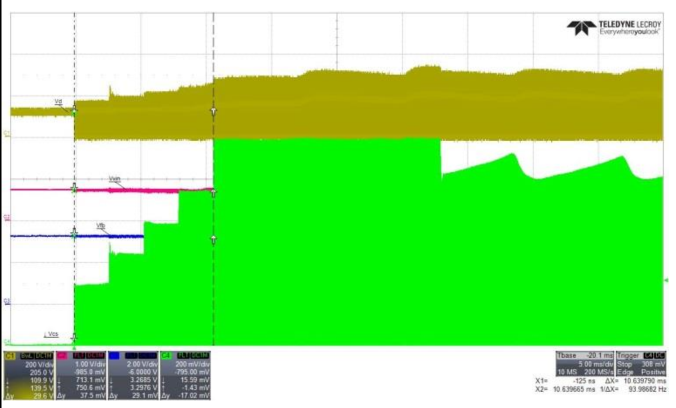
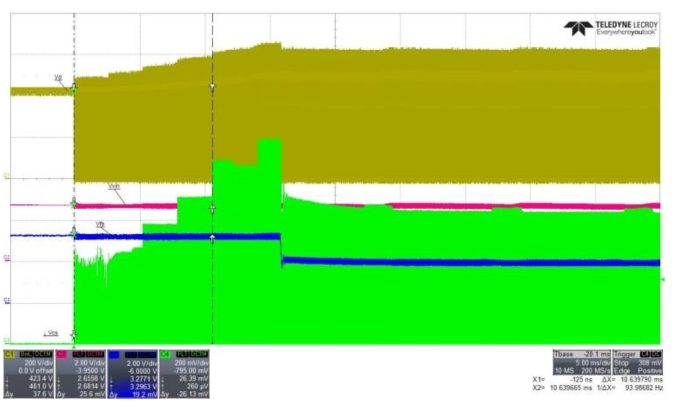
	
C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : VIN voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : VIN voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})
Soft start time at 85 V AC and maximum load ≈ 10 ms	Soft start time at 300 V AC and maximum load ≈ 10 ms

Figure 17 Soft-start

11.3 Drain and current sense voltage at maximum load

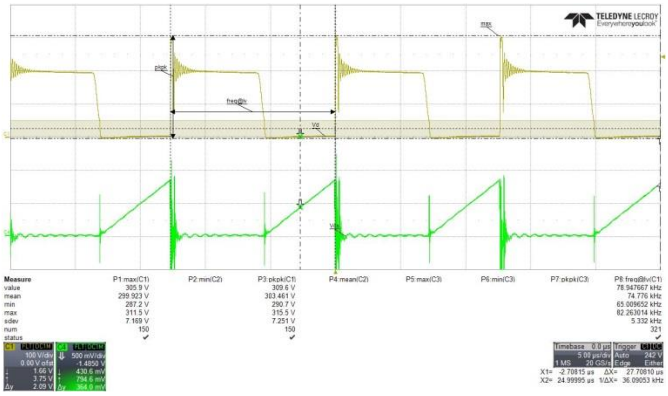
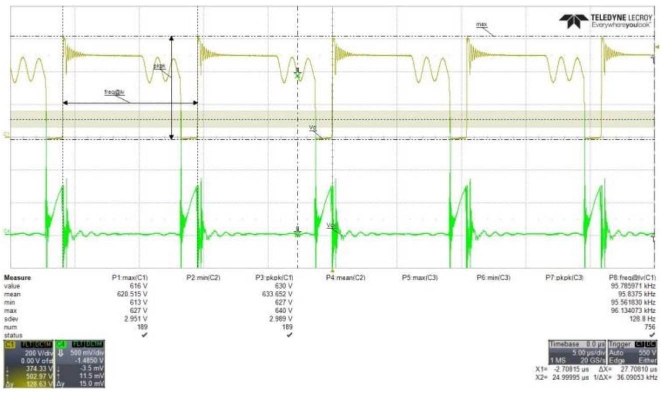
	
C1 (Yellow) : Drain voltage (V_D) C4 (Green) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_D) C4 (Green) : Current sense voltage (V_{CS})
V_{Drain_peak} at 85 V AC ≈ 315 V with 1st ZC and f_{S_Min} ≈ 65 kHz	V_{Drain_peak} at 300V AC ≈ 640 V with 3rd ZC and f_{S_Min} ≈ 95 kHz

Figure 18 Drain and current sense voltage at maximum load

11.4 Zero crossing point during normal operation

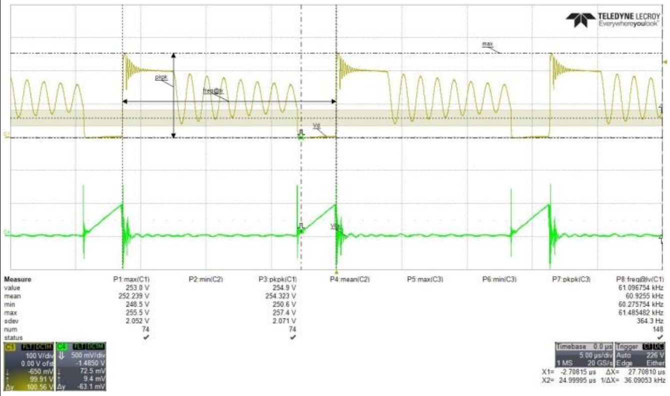
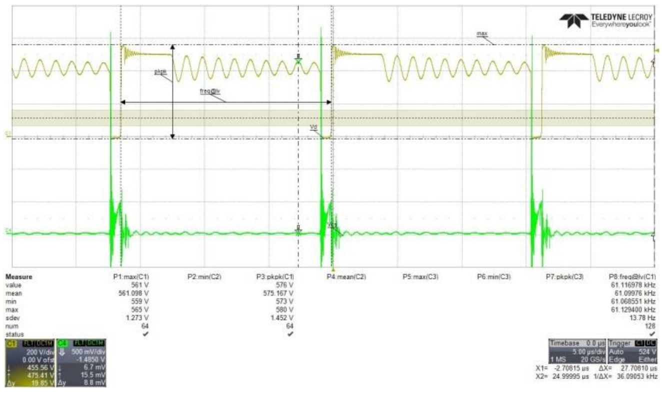
	
C1 (Yellow) : Drain voltage (V_D) C4 (Green) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_D) C4 (Green) : Current sense voltage (V_{CS})
8th zero crossing at 85 V AC and 25% load (5 V x 0.05 A +12 V x 0.853 A) (zero crossing varies from 1~8 for low line)	10th zero crossing at 300 V AC and 25% load (5 V x 0.05 A +12 V x 0.853 A) (zero crossing varies from 3~10 for high line)

Figure 19 Zero crossing

11.5 Load transient response (dynamic load from 10% to 100%)

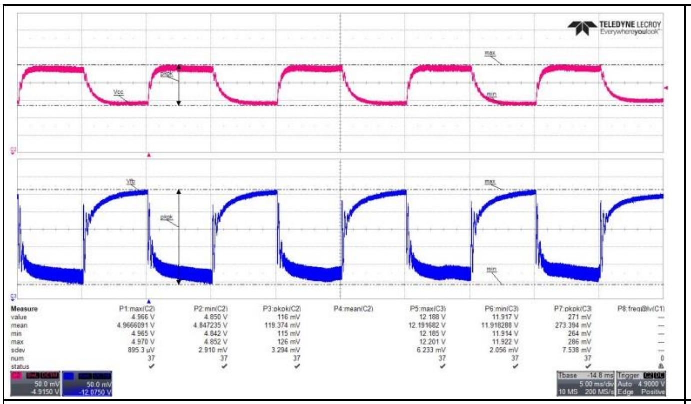
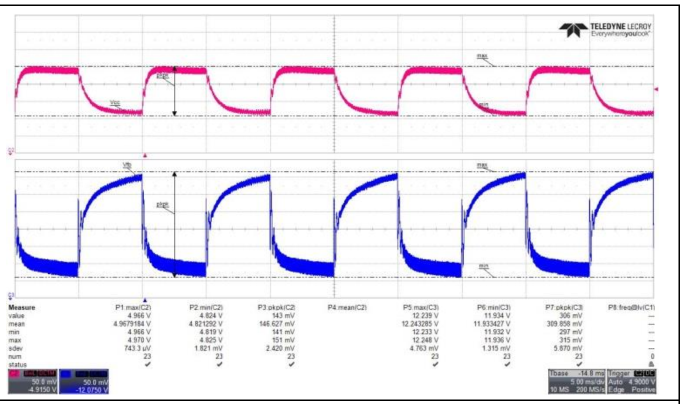
	
C2 (Purple) : 5 V output ripple voltage (V_{Out5}) C3 (Blue) : 12 V output ripple voltage (V_{Out12})	C2 (Purple) : 5 V output ripple voltage (V_{Out5}) C3 (Blue) : 12 V output ripple voltage (V_{Out12})
5 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 126 mV 12 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 286 mV (85 V AC , 12 V Load change from 10% to 100% and 5 V at 200 mA load, 100 Hz, 0.4 A/µs slew rate) Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	5 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 151 mV 12 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 315 mV (300 V AC , 12 V Load change from 10% to 100% and 5 V at 200 mA load, 100 Hz, 0.4 A/µs slew rate) Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 20 Load transient response

11.6 Output ripple voltage at maximum load

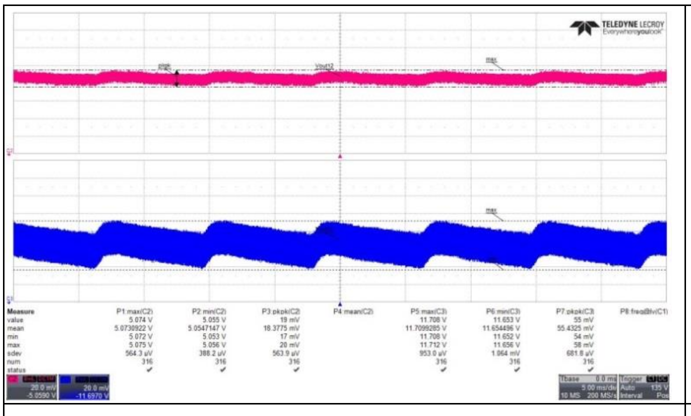
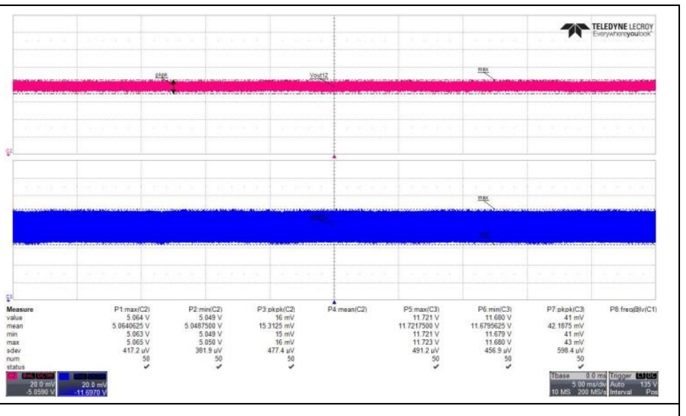
	
C2 (Purple) : 5 V Output ripple voltage (V_{Out5}) C3 (Blue) : 12 V Output ripple voltage (V_{Out12})	C2 (Purple) : 5 V Output ripple voltage (V_{Out5}) C3 (Blue) : 12 V Output ripple voltage (V_{Out12})
5 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 20 mV 12 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 56 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	5 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 16 mV 12 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 43 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 21 Output ripple voltage at maximum load

11.7 Output ripple voltage at burst mode 1 W load

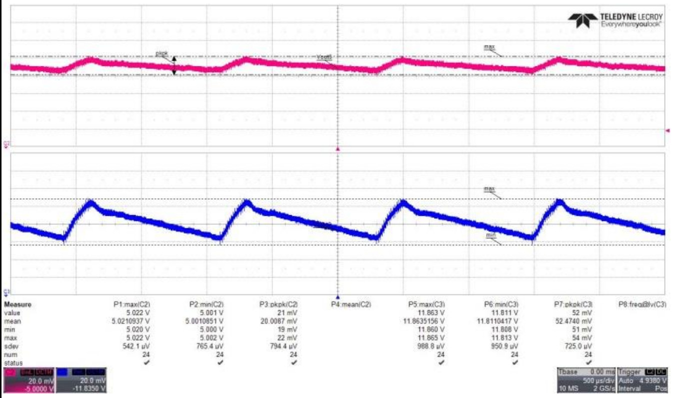
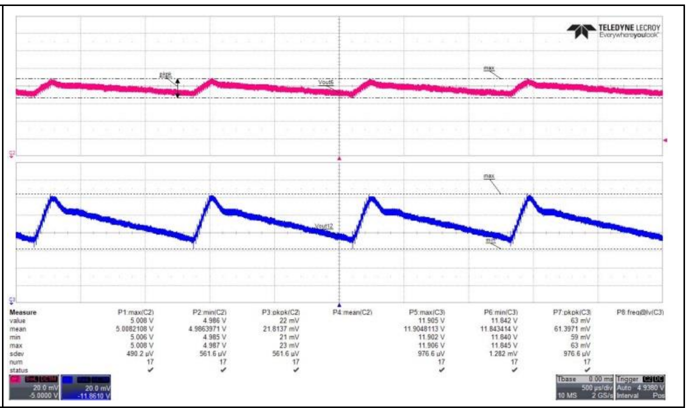
	
C2 (Purple) : 5 V Output ripple voltage (V_{Out5}) C3 (Blue) : 12 V Output ripple voltage (V_{Out12})	C2 (Purple) : 5 V Output ripple voltage (V_{Out5}) C3 (Blue) : 12 V Output ripple voltage (V_{Out12})
5 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 22 mV 12 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 54 mV Load: 5 V at 6 mA and 12 V at 80mA Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	5 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 23 mV 12 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 63 mV Load: 5 V at 6 mA and 12 V at 80mA Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 22 Output ripple voltage at burst mode 1 W load

11.8 Entering active burst mode

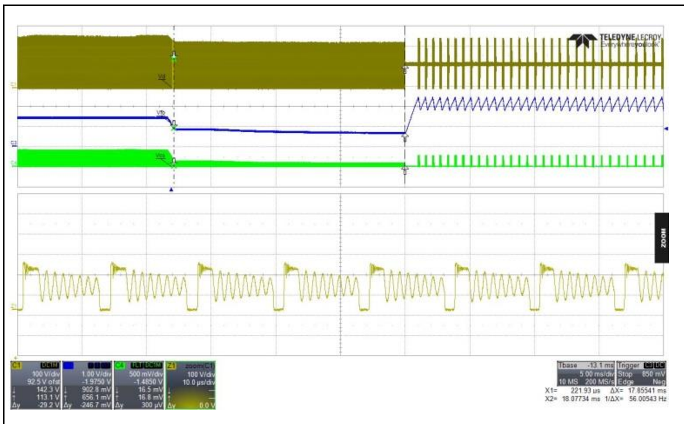
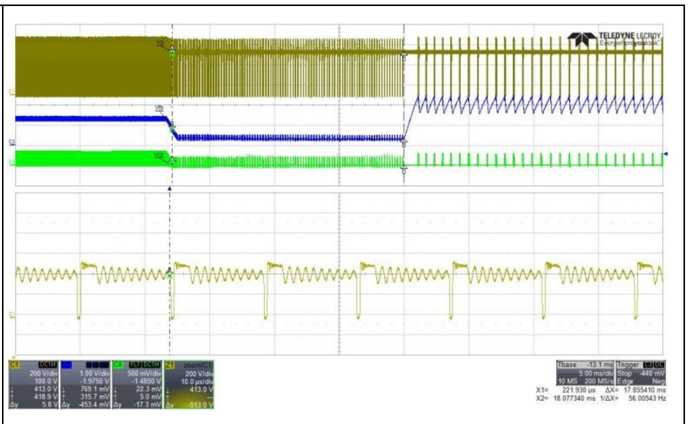
	
C1 (Yellow) : Drain voltage (V_D) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_D) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})
Condition to enter burst mode level 1 : V_{FB} < 0.9 V, N_{ZC} = 8 and $t_{blanking}$ = 20 ms (85 V AC, load change form 10.5 W to 1 W) (5Vx50mA+12Vx0.853A) to (5Vx50mA+12Vx0.0.062A)	Condition to enter burst mode level 1 : V_{FB} < 0.9 V, N_{ZC} = 10 and $t_{blanking}$ = 20 ms (300 V AC, load change form 10.5 W to 1 W (5Vx50mA+12Vx0.853A) to (5Vx50mA+12Vx0.0.062A)

Figure 23 Entering active burst mode

11.9 During active burst mode

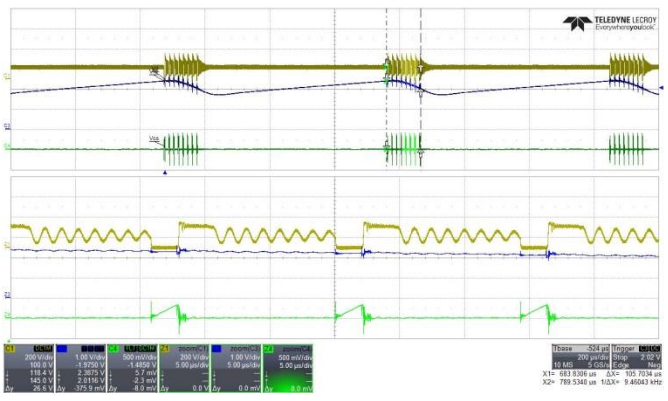
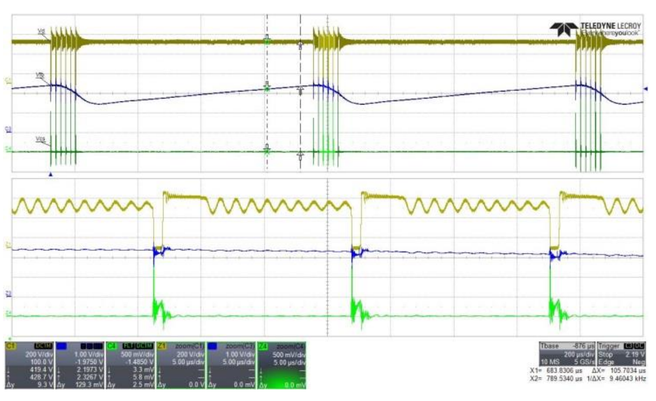
	
C1 (Yellow) : Drain voltage (V_D) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_D) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})
During active burst mode level 1 : V_{FB_BOn}=2.4 V, V_{FB_BOff} = 2.0 V, V_{CSBLP} = 0.31 V, N_{ZC} = 8 85 V AC,1 W (5Vx50mA+12Vx0.062A)	During active burst mode level 1 : V_{FB_BOn}=2.4 V, V_{FB_BOff} = 2.0 V, V_{CSBLP} = 0.31 V, N_{ZC} = 10 300 V AC,1 W (5Vx50mA+12Vx0.062A)

Figure 24 During active burst mode

11.10 Leaving active burst mode

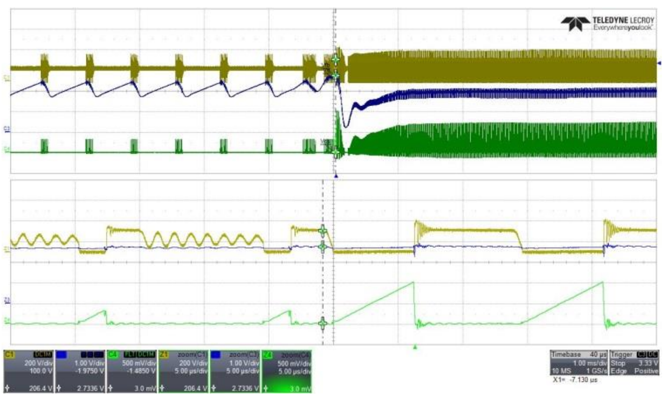
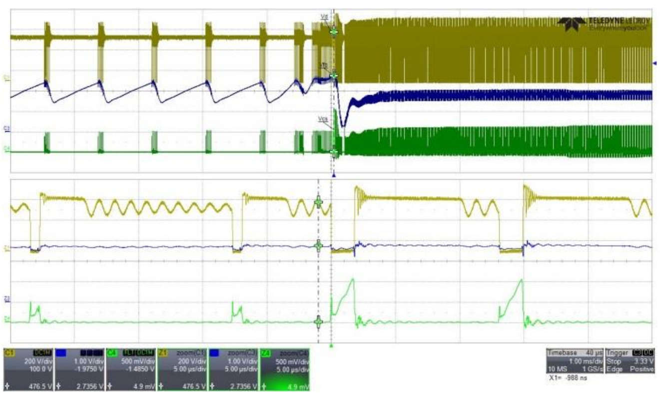
	
C1 (Yellow) : Drain voltage (V_D) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_D) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})
Condition to leave burst mode level 1 : V_{FB} >2.75 V 85 V AC, load change form 1 W to 41.25 W (5 Vx50 mA+12 Vx0.0.062 A) to (5 Vx50 mA+12 Vx3.41 A)	Condition to leave burst mode level 1 : V_{FB} >2.75 V 300 V AC, load change form 1 W to 41.25 W (5Vx50mA+12Vx0.0.062A) to (5Vx50mA+12Vx3.41A)

Figure 25 Leaving active burst mode

11.11 Line over voltage protection (non switch auto restart)

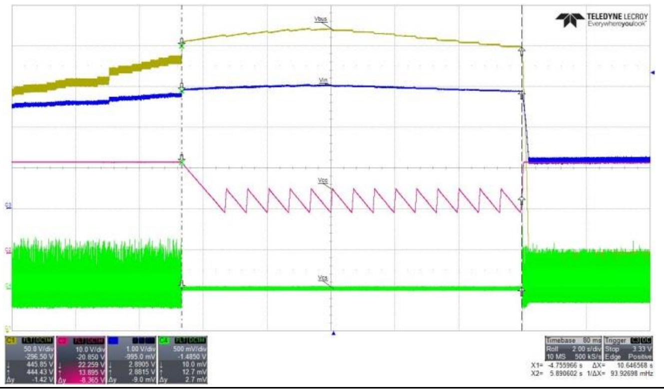
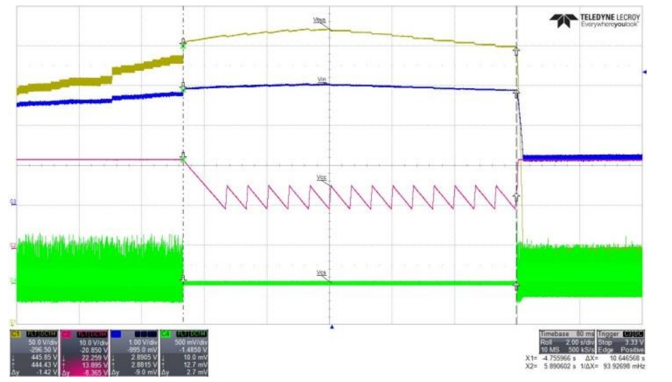
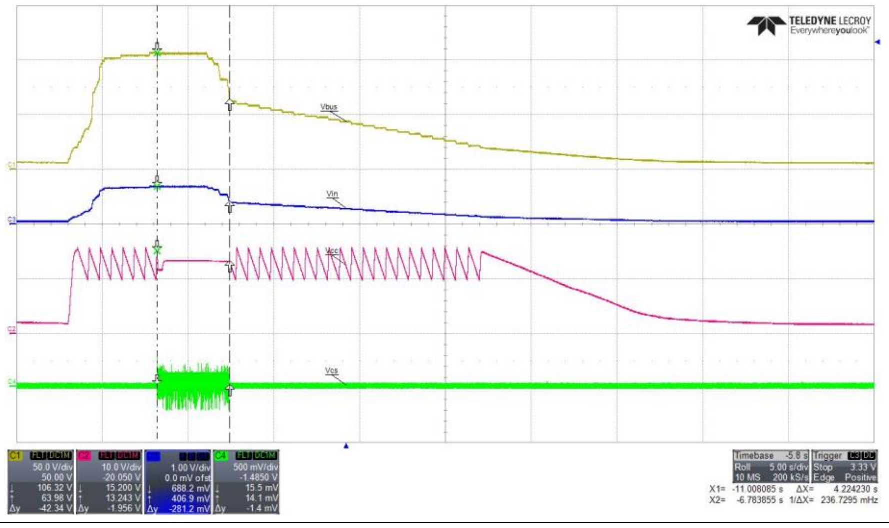
	
C1 (Yellow) : Bus voltage (V_{Bus}) C2 (Purple) : Supply voltage (V_{VCC}) C3 (Blue) : VIN voltage (V_{VIN}) C4 (Green) : Current sense voltage (V_{CS})	C1 (Yellow) : Bus voltage (V_{Bus}) C2 (Purple) : Supply voltage (V_{VCC}) C3 (Blue) : VIN voltage (V_{VIN}) C4 (Green) : Current sense voltage (V_{CS})
Condition to detect Line over voltage protection : V_{VIN} > 2.9 V (V_{BULK} > 445 V DC[≈320 V AC]) Condition to reset Line over voltage protection : V_{VIN} < 2.9 V (V_{BULK} < 445 V)	
(Gradually increase AC line voltage at full load till Line OVP detect and decrease AC line till Line OVP reset)	(Gradually increase AC line voltage at 1 W load (Active burst mode) till Line OVP detect and decrease AC line till Line OVP reset)

Figure 26 Line over voltage protection

11.12 Brownout protection (non switch auto restart)



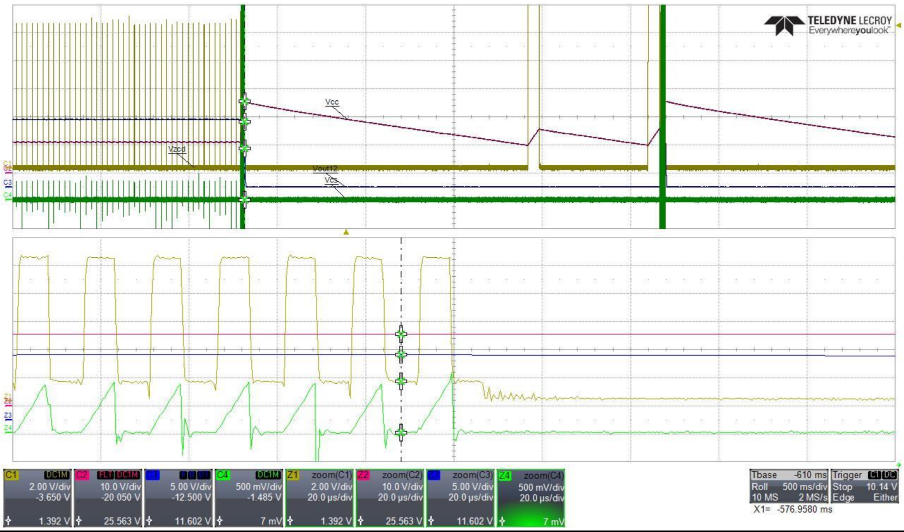
C1 (Yellow) : Bus voltage (V_{Bus})
C2 (Purple) : Supply voltage (V_{VCC})
C3 (Blue) : VIN voltage (V_{VIN})
C4 (Green) : Current sense voltage (V_{CS})

Condition to reset brownout protection (brownin) : V_{VIN} > 0.66 V (V_{BULK} > 106 V DC [≈75 V AC])
Condition to detect brownout protection : V_{VIN} < 0.4 V (V_{BULK} < 63 V DC [≈43 V AC])

(Gradually increase AC line voltage at 1 W (5 V at 6 mA and 12 V at 80 mA) load until system start and reduce the line until brownout detect)

Figure 27 Brownout protection

11.13 V_{CC} over-voltage protection (odd skip auto restart)

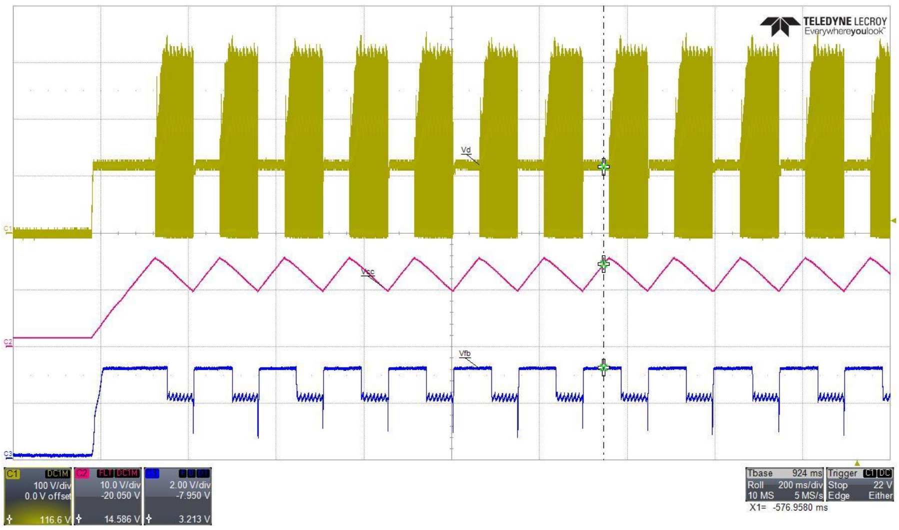


C1 (Yellow)	: Zero crossing detection voltage (V_{ZCD})
C2 (Purple)	: Supply voltage (V_{VCC})
C3 (Blue)	: 12 V output voltage (V_{O12})
C4 (Green)	: Current sense voltage (V_{CS})

Condition to enter V_{VCC} over voltage protection: $V_{VCC} > 25.5$ V
(85 V AC,remove R13 & load change from no load to full load)

Figure 28 V_{CC} over voltage protection

11.14 V_{CC} under voltage protection (auto restart)

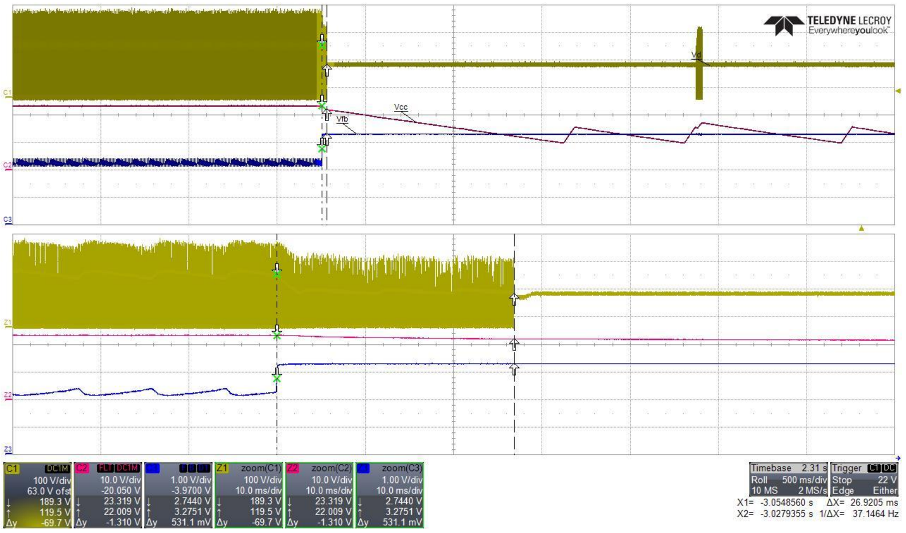


C1 (Yellow)	: Drain voltage (V_D)
C2 (Purple)	: Supply voltage (V_{VCC})
C3 (Blue)	: Feedback voltage (V_{FB})

Condition to enter V CC under voltage protection: $V_{CC} < 10$ V
(Remove R12A and power on the system with full load at 85 V AC)

Figure 29 V_{CC} under voltage protection

11.15 Over load protection (odd skip auto restart)

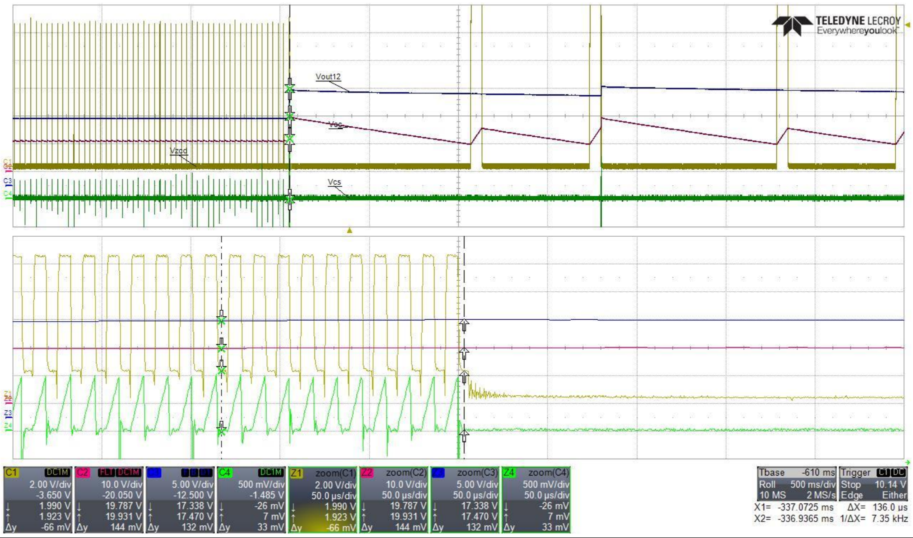


C1 (Yellow)	: Drain voltage (V_D)
C2 (Purple)	: Supply voltage (V_{VCC})
C3 (Blue)	: Feedback voltage (V_{FB})

Condition to enter over load protection: V_{FB} > 2.75 V & last for 30ms blanking time
(12 V output load change from full load to short at 85 V AC)

Figure 30 Over load protection

11.16 Output over voltage protection (odd skip auto restart)

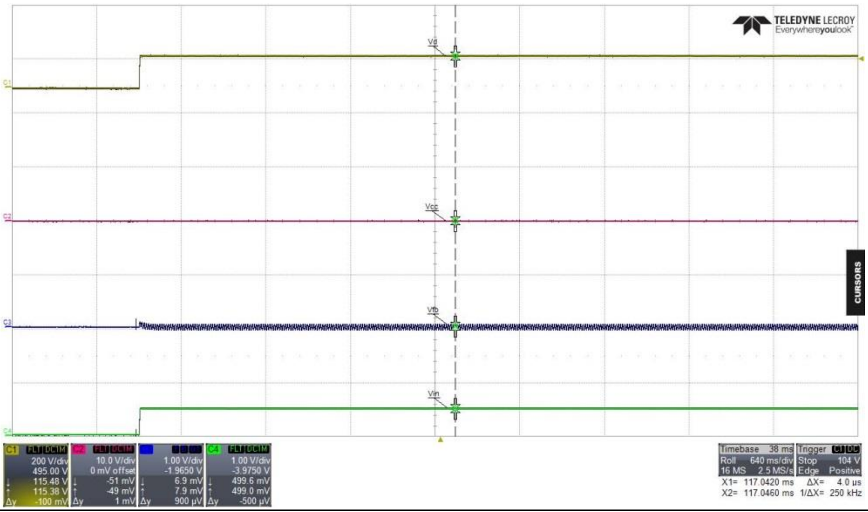


C1 (Yellow)	: Zero crossing detection voltage (V_{ZCD})
C2 (Purple)	: Supply voltage (V_{VCC})
C3 (Blue)	: 12 V output voltage (V_{O12})
C4 (Green)	: Current sense voltage (V_{CS})

Condition to enter output OVP: V_{O12} >17 V (V_{ZCD} > 1.9 V)
(85 V AC, short R26 during system operation at no load)

Figure 31 Output over voltage protection

11.17 V_{CC} short to GND protection



C1 (Yellow)	: Drain voltage (V_D)
C2 (Purple)	: V CC voltage (V_{VCC})
C3 (Blue)	: Feedback voltage (V_{FB})
C4 (Green)	: VIN voltage (V_{VIN})

Condition to enter V_{CC} short to GND : if $V_{CC} < V_{VCC\_SCP}$ → $I_{VCC} = I_{VCC\_Charge1}$
(Short V_{CC} pin to Gnd by multi-meter and measure the current, $I_{VCC} \approx 280$ µA and input power is ≈ 50 mW at 85 V AC and full load)

Figure 32 V_{CC} short to GND protection

12 References

[1] ICE5QRxxxxAx datasheet, Infineon Technologies AG

[2] AN-201609_PL83_026-5th Generation Quasi-Resonant Design Guide

[3] Calculation Tool Quasi Resonant CoolSET™ Generation 5

Revision history

Major changes since the last revision

Page or reference	Description of change
--	First release.

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