16 W 12 V 5 V SMPS demo board with ICE5QR4770AZ

AN-DEMO_5QR4770AZ_16W1

About this document

Scope and purpose

This document is an engineering report that describes universal input 16 W 12 V and 5 V off-line flyback converter using the latest 5th generation Infineon quasi resonant CoolSET™ ICE5QR4770AZ which offers high efficiency, low standby power with selectable entry and exit standby power option, wide V_{CC} operating range with fast start up, robust line protection with input OVP and brownout and various protections for a high reliable system. This demonstrator board is designed for users who wish to evaluate the performance of ICE5QR4770AZ in ease of use.

Intended audience

This document is intended for power supply design/application engineer, students, etc., who wish to design low cost and high reliable system of off-line Switched Mode Power Supply (SMPS), either auxiliary power supply of white goods, PC, server and TV or enclosed adapter, Blu-ray player, set-top box, game console, etc.

Table of contents

1 Abstract

This application note is an engineering report of 16 W 12 V and 5 V demo board designed in a quasi resonant flyback converter topology using the 5th generation quasi resonant CoolSET™, ICE5QR4770AZ. The target applications of ICE5QR4770AZ are either auxiliary power supply of white goods, PC, server and TV or enclosed adapter, Blu-ray player, set-top box, game console, etc. With the CoolMOS™ integrated in this IC, it greatly simplifies the design and layout of the PCB. The improved novel digital frequency reduction with proprietary quasi resonant operation offers lower EMI and higher efficiency for wide AC range by reducing the switching frequency difference between low and high line. The enhanced Active Burst Mode (ABM) power enables flexibility in standby power operation range selection and quasi resonant operation during ABM. As a result, the system efficiency, over the entire load range, is significantly improved compared to conventional free running quasi resonant converter implemented with only maximum switching frequency limitation at light load. In addition, numerous adjustable protection functions have been implemented in ICE5QR4770AZ to protect the system and customize the IC for the chosen application. In case of failure modes, like brownout or line over voltage, V_{CC} over/under voltage, open control-loop or over load, output overvoltage, over temperature, V_{CC} short to ground and CS short to ground, the device enters to protection mode. By means of the cycle-by-cycle peak current limitation, the dimension of the transformer and current rating of the secondary diode can both be optimized. Thus, a cost effective solution can be easily achieved.

2 Demonstrator board

This document contains the list of features, the power supply specification, schematic, bill of material and the transformer construction documentation. Typical operating characteristics such as performance curve and scope waveforms are showed at the rear of the report.

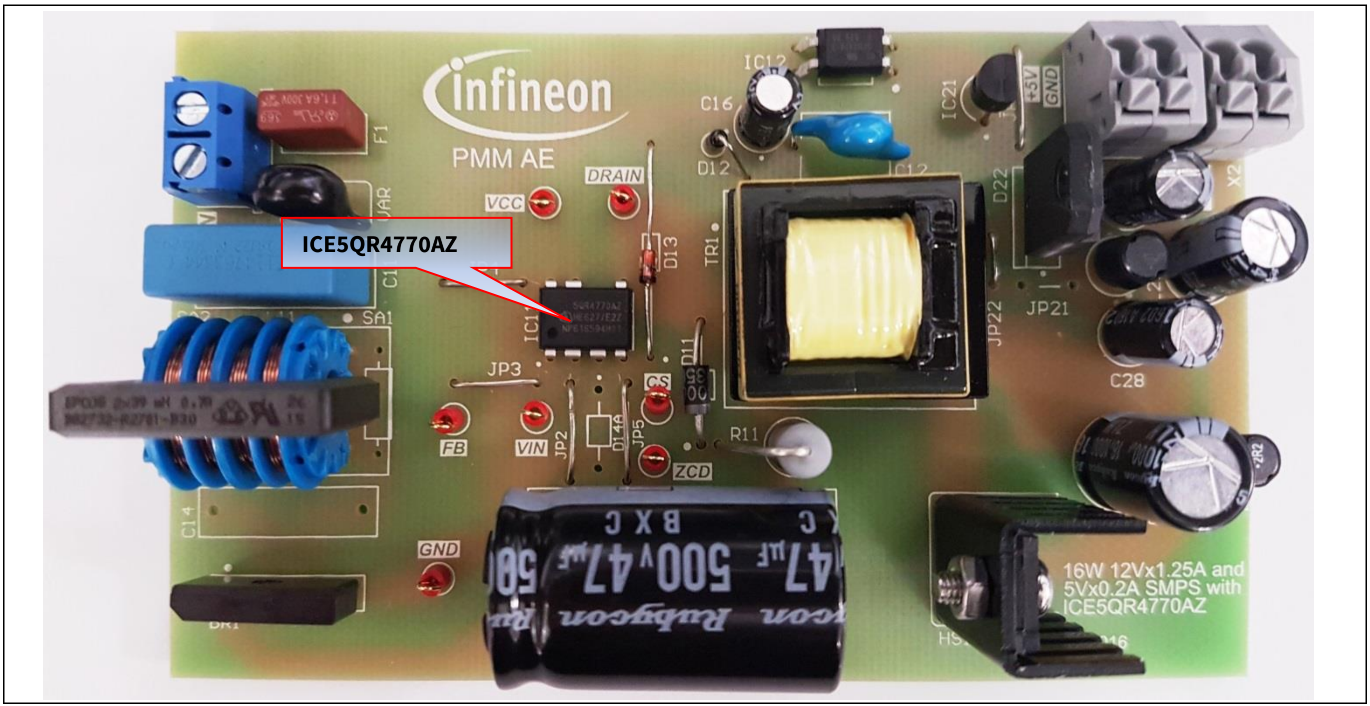


Figure 1 DEMO_5QR4770AZ_16W1

3 Specifications of demonstrator board

Table 1 Specifications of DEMO_5QR4770AZ_16W1

Input voltage and frequency	85 V_{AC} (60 Hz) ~ 300 V_{AC} (50Hz)
Output voltage, current and power	(12 V x 1.25 A) +(5 V x 0.2 A) = 16 W
Dynamic load response (5 V at 0.2 A and 12 V load change from 10% to 100%, slew rate at 0.4 A/µs, 100 Hz)	±5% of nominal output voltage
Output ripple voltage (full load, 85 V_{AC} ~ 300 V_{AC})	5 $V_{ripple\_p\_p}$< 100 mV 12 $V_{ripple\_p\_p}$< 100 mV
Active mode four point average efficiency (25%, 50%, 75%, 100% load)	> 84% at 115 V_{AC} and 230 V_{AC}
No load power consumption	< 100 mW at 230 V_{AC}
Conducted emissions (EN55022 class B)	Pass with 8 dB margin for 115 V_{AC} and 6 dB margin for 230 V_{AC}
ESD immunity (EN61000-4-2)	Special Level (±14 kV for contact and ±16 kV air discharge)
Surge immunity (EN61000-4-5)	Installation class 4 (±2 kV for line to line and ±4 kV for line to earth)
Form factor case size (L x W x H)	(110 x 66 x 27) mm^3

Note: *"The demo board is designed for dual output with cross regulated loop feedback. It may not regulate properly if loading is applied only to single output. If the user wants to evaluate for single output (12 V only) condition, the following changes are necessary on the board.*

1. Remove D22, L22, C28, C210, R25A (to disable 5 V output)
2. Change R26 to 10 kΩ and R25 to 38 kΩ (to disable 5 V feedback and enable 100% weighted factor on 12 V output)

Since the board (especially transformer) is designed for dual output with optimized cross regulation, single output efficiency might not be optimized. It is only for IC functional evaluation under single output condition."

4 Circuit description

4.1 Line input

The AC line input side comprises the input fuse F1 as over-current protection. The choke L11, X-capacitor C11 and Y-capacitor C12 act as EMI suppressors. Optional spark gap devices SA1, SA2 and varistor VAR can absorb high voltage stress during lightning surge test. A rectified DC voltage (120~424 V_{DC}) is obtained through the bridge rectifier BR1 together with bulk capacitor C13.

4.2 Start up

To achieve the fast and safe start up, ICE5QR4770AZ has implemented with startup resistor and V_{CC} short to GND protection. When V_{VCC} reaches the turn on voltage threshold 16 V, the IC begins with a soft-start. The soft-start implemented in ICE5QR4770AZ is a digital time-based function. The preset soft-start time is 12 ms with 4 steps. If not limited by other functions, the peak voltage on CS pin will increase step by step from 0.3 V to 1 V finally. After IC turns on, the V_{CC} voltage is supplied by auxiliary windings of the transformer. V_{CC} short to GND protection is implemented during the startup time.

4.3 Integrated MOSFET and PWM control

ICE5QR4770AZ is comprised of a power MOSFET and the proprietary novel quasi resonant controller which enables higher average efficiency and low EMI. This integrated solution greatly simplifies the circuit layout and reduces the cost of PCB manufacturing. The PWM switch-on is determined by the zero-crossing detection input signal and the value of the up/down counter. The PWM switch-off is determined by the feedback signal V_{FB} and the current sensing signal V_{CS}. ICE5QR4770AZ also performs all necessary protection functions in flyback converters. Details about the information mentioned above are illustrated in the product datasheet.

4.4 RCD clamper circuit

A clamper network (R11, C15 and D11) dissipates the energy of the leakage inductance and suppress ringing on the SMPS transformer.

4.5 Output stage

There are two outputs on the secondary side, 12 V and 5 V. The power is coupled out via schottky diodes D21 and D22. The capacitors C22 and C28 provide energy buffering followed by the L-C filters L21-C24 and L22-C210 to reduce the output ripple and prevent interference between SMPS switching frequency and line frequency considerably. Storage capacitors C22 and C28 are designed to have an internal resistance (ESR) as small as possible to minimize the output voltage ripple caused by the triangular current.

4.6 Feedback loop

For feedback, the output is sensed by the voltage divider of R26, R25, R25A and compared to IC21 (TL431) internal reference voltage. C25, C26 and R24 comprise the compensation network. The output voltage of IC21 (TL431) is converted to the current signal via optocoupler IC12 and two resistors R22 and R23 for regulation control.

4.7 Primary side peak current control

The MOSFET drain source current is sensed via external resistor R14 and R14A. Since ICE5QR4770AZ is a current mode controller, it would have a cycle-by-cycle primary current and feedback voltage control which can make sure the maximum power of the converter is controlled in every switching cycle.

For a quasi resonant flyback converter, the maximum possible output power is increased when a constant current limit value is used for all the line input voltage range. This is usually not desired as this will increase additional cost on transformer and output diode in case of output over power conditions.
Internal current limitation with line dependent V_{CS} curve and the proprietary novel quasi resonant switching which reduces switching frequency difference between minimum and maximum line are implemented in the ICE5QR4770AZ. As the result, the maximum output power can be well limited versus the input voltage.

4.8 Digital frequency reduction

During normal operation, the switching frequency for ICE5QR4770AZ is digitally reduced with decreasing load. At light load, the MOSFET will be turned on not at the first minimum drain-source voltage time, but on the n^{th}. The counter is in range of 1 to 8 for low line and 3 to 10 for high line, which depends on feedback voltage in a time-base. The feedback voltage decreases when the output power requirement decreases, and vice versa. Therefore, the counter is set by monitoring voltage V_{FB}. The counter will be increased with low V_{FB} and decreased with high V_{FB}. The thresholds are preset inside the IC.

4.9 Active Burst Mode (ABM)

Active Burst Mode entry and exit power (2 levels) can be selected in ICE5QR4770AZ. Details are illustrated in the product datasheet. Active burst mode power level 1 is used in this demo board (R17=open). At light load condition, the SMPS enters into ABM with quasi resonant switching. At this stage, the controller is always active but the V_{VCC} must be kept above the switch off threshold. During active burst mode, the efficiency increase significantly and at the same time it supports low ripple on V_{out} and fast response on load jump.

For determination of entering ABM operation, three conditions apply:

1. the feedback voltage is lower than the threshold of V_{FB_EBLX}
2. the up/down counter is 8 for low line and 10 for high line and
3. a certain blanking time (t_{FB_BEB} =20 ms).

Once all of these conditions are fulfilled, the ABM flip-flop is set and the controller enters active burst mode operation. This multi-condition determination for entering active burst mode operation prevents mis-triggering of entering active burst mode operation, so that the controller enters active burst mode operation only when the output power is really low during the preset blanking time.

During active burst mode, the maximum current sense voltage is reduced from 1 V_{CS_N} to V_{CS_BLX} so as to reduce the conduction loss and the audible noise. At the burst mode, the FB voltage is changing like a sawtooth between V_{FB_BOFF} and V_{FB_BON}.

The feedback voltage immediately increases if there is a high load jump. This is observed by one comparator. As the current limit is 31/35% during active burst mode a certain load is needed so that feedback voltage can exceed V_{FB_LB}. After leaving active burst mode, maximum current can now be provided to stabilize V_{out}. In addition, the up/down counter will be set to 1 (low line) or 3 (high line) immediately after leaving active burst mode. This is helpful to decrease the output voltage undershoot.

5 Protection features

Protection is one of the major factors to determine whether the system is safe and robust. Therefore sufficient protection is necessary. ICE5QR4770AZ provides a comprehensive protection to ensure the system is operating safely. The protections include line over voltage, brownout, V_{CC} over voltage and under voltage, over load, output over voltage, over temperature (controller junction), CS short to GND and V_{CC} Short to GND. When those faults are found, the system will go into the protection mode. It is then until the fault is removed, the system resumes to normal operation. A list of protections and the failure conditions are shown in the below table.

Table 2 Protection function of ICE5QR4770AZ

Protection function	Failure condition	Protection mode
Line over voltage	V_{VIN} > 2.9 V	Non switch auto restart
Brownout	V_{VIN} < 0.4 V	Non switch auto restart
V_{CC} over voltage	V_{VCC} > 25.5 V	Odd skip auto restart
V_{CC} under voltage	V_{VCC} < 10 V	Auto restart
Over load	V_{FB} > 2.75 V & last for 30 ms	Odd skip auto restart
Output over voltage	V_{ZCD} > 2 V & last for 10 consecutive pulses	Odd skip auto restart
Over temperature (junction temperature of controller chip only)	T_J > 140 °C with 40°C hysteresis to reset	Non switch auto restart
CS short to Gnd	V_{CS} < 0.1 V, last for 5 µs and 3 consecutive pulses	Odd skip auto restart
V_{CC} short to Gnd (V_{VCC}=0 V, $R_{StartUp}$=50 MΩ and V_{DRAIN}=90 V)	V_{VCC}< 1.1 V, $I_{VCC\_Charge1}$≈0.2 A	Cannot start up

6 Circuit diagram

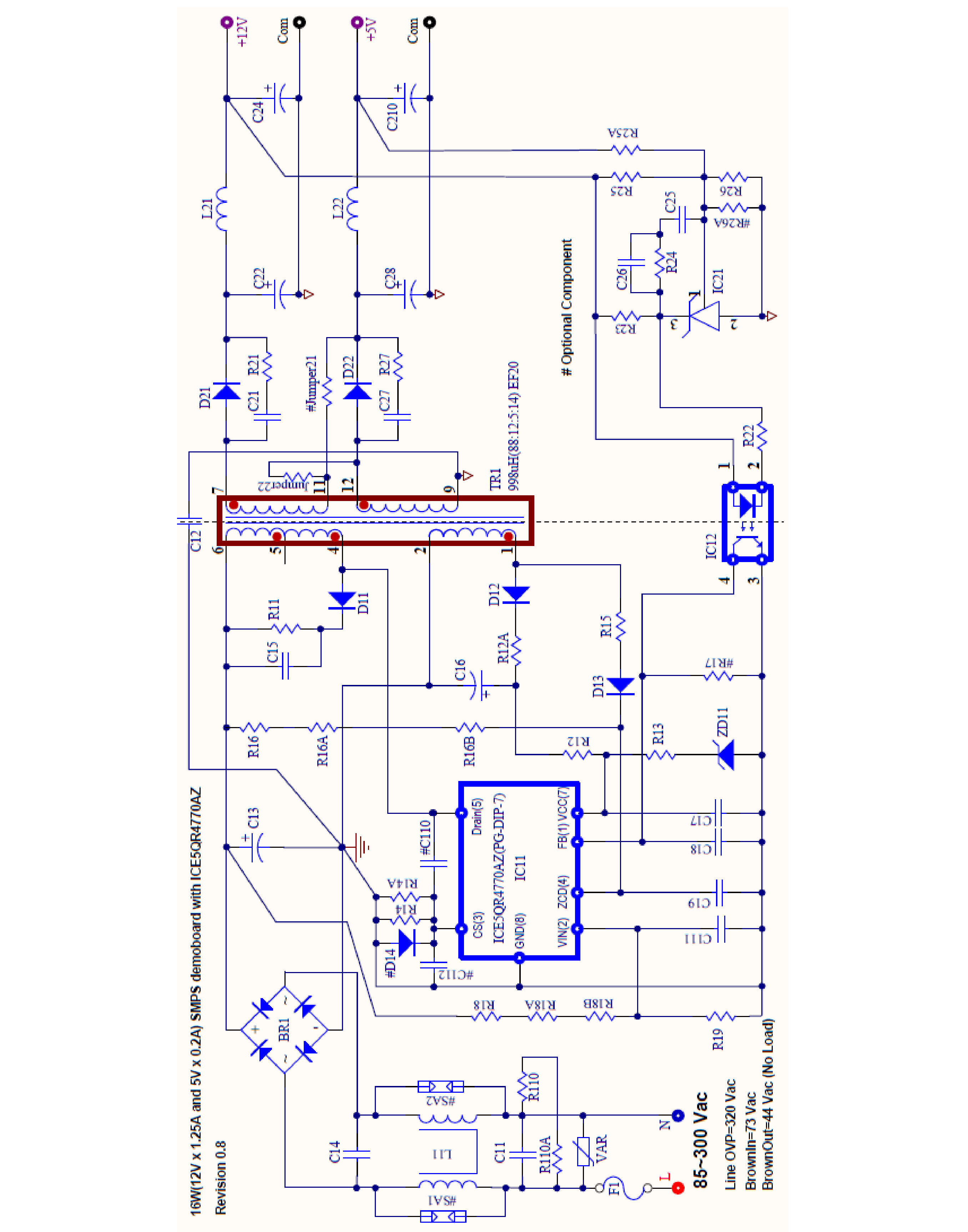


Figure 2 **Schematic of DEMO_5QR4770AZ_16W1**

Note: General guideline for layout design of Printed Circuit Board (PCB):

1. *Star ground at bulk capacitor C13: all primary grounds should be connected to the ground of bulk capacitor C13 separately in one point. It can reduce the switching noise going into the sensitive pins of CoolSET™ device effectively. The primary star ground can be split into four groups as follows,*
   i. *Combine signal (all small signal grounds connecting to the CoolSET™ GND pin such as filter capacitor ground C17, C18, C19, C111, C112 and opto-coupler ground) and power ground (current sense resistor R14 and R14A).*
   ii. *V_{CC} ground includes the V_{CC} capacitor ground C16 and the auxiliary winding ground, pin 2 of the power transformer.*
   iii. *EMI return ground includes Y capacitor C12.*
   iv. *DC ground from bridge rectifier, BR1*
2. *Filter capacitor close to the controller ground: Filter capacitors, C17, C18, C19 and C111 should be placed as close to the controller ground and the controller pin as possible so as to reduce the switching noise coupled into the controller.*
3. *High voltage traces clearance: High voltage traces should keep enough spacing to the nearby traces. Otherwise, arcing would incur.*
   i. *400 V traces (positive rail of bulk capacitor C13) to nearby trace: > 2.0 mm*
   ii. *600 V traces (drain voltage of CoolSET™ IC11) to nearby trace: > 2.5 mm*
4. *Recommended minimum 232 mm^2 copper area at drain pin to add on PCB for better thermal performance.*
5. *Power loop area (bulk capacitor C13, primary winding of the transformer TR1 (Pin 4 and 6), IC11 drain pin, IC11 CS pin and current sense resistor R14/R14A) should be as small as possible to minimize the switching emissions.*

7 PCB layout

7.1 Top side

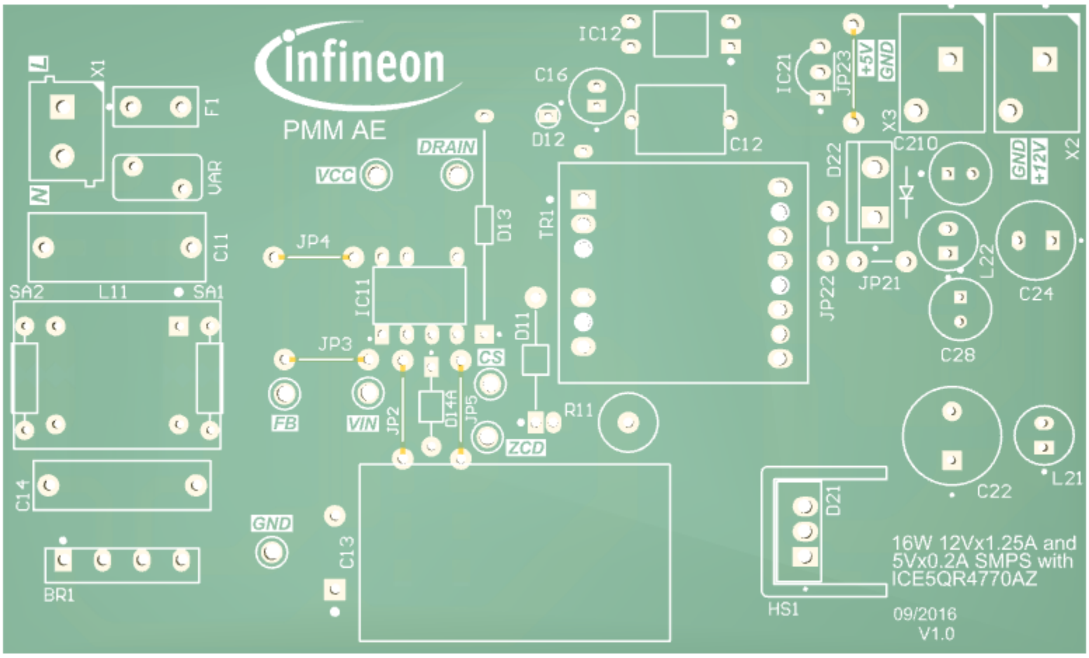


Figure 3 Top side component legend

7.2 Bottom side

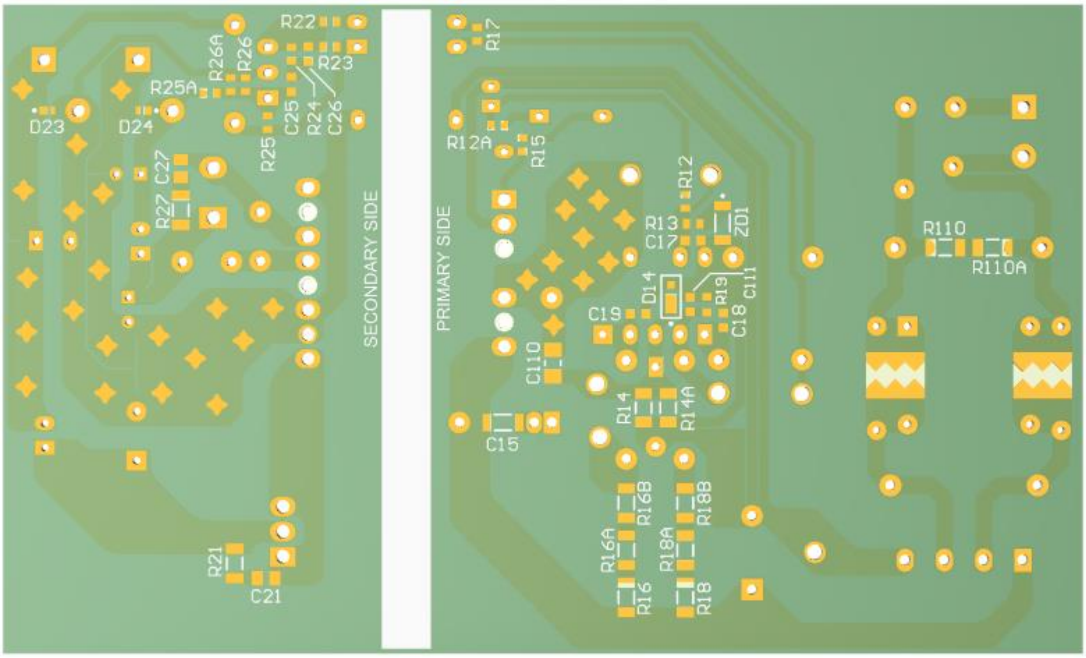


Figure 4 Bottom side copper and component legend

8 Bill of material

Table 3 Bill of material (V 0.8)

No.	Designator	Description	Part Number	Manufacturer	Quantity
1	BR1	600 V/ 1 A	S1VBA60	Shindengen	1
2	C11	0.22 µF/ 305 V	B32922C3224	Epcos	1
3	C12	1 nF/ 500 V	DE1E3RA102MA4BQ	Murata	1
4	C13	47 µF/ 500 V	500BXC47MEFC18X31.5	Rubycon	1
5	C15	1 nF/1000 V	GRM31BR73A102KW01#	Murata	1
6	C16	22 µF/50 V	50PX22MEFC5X11	Rubycon	1
7	C17	100 nF/ 50 V	GRM188R71H104KA93D	Murata	1
8	C18, C26	1 nF/ 50 V	GRM1885C1H102GA01D	Murata	2
9	C19	120 pF/ 50 V	GRM1885C1H121GA01D	Murata	1
10	C111	22 nF/ 50 V	GCM188R71H223KA37D	Murata	1
11	C21, C27	1 nF/ 100 V	GRM2162C2A102JA01#	Murata	2
12	C22	1000 uF/ 16 V	16ZLH1000MEFC10X16	Rubycon	1
13	C24	470 uF/ 16 V	16ZLH470MEFC8X11.5	Rubycon	1
14	C25	220 nF/ 50 V	GRM188R71H224KAC4D	Murata	1
15	C28	330 uF/ 10 V	10ZLH330MEFC6.3X11	Rubycon	1
16	C210	330 uF/ 10 V	10ZLH330MEFC6.3X11	Rubycon	1
17	D11	1 A/ 800 V	UF4006		1
18	D12	0.2 A/ 200 V	1N485B		1
19	D13	0.2 A/ 150 V/ 50 ns	FDH400		1
20	D21	20 A/ 100 V	STPS20M100SFP		1
21	D22	10 A/ 45 V	VFT1045BP		1
22	F1	1.6 A/ 300 V	36911600000		1
23	HS21	Heat sink	577202B00000G		1
24	IC11	ICE5QR4770AZ	ICE5QR4770AZ	Infineon	1
25	IC12	Optocoupler	SFH617A-3		2
26	IC21	Shunt regulator	TL431BVLPG		1
27	JP2, JP3, JP4, JP5, JP22 and JP23	Jumper			6
28	L11	39 mH/ 0.7 A	B82732R2701B030	Epcos	1
29	L21	2.2uH/ 4.3 A	744 746 202 2	Wurth Electronics	1
30	L22	4.7 uH/ 4.2 A	744 746 204 7	Wurth Electronics	1
31	R11	68 kR/ 2 W/ 350 V	ERG-2SJ683A	Panasonic	1
32	R12, R13	27 Ω(0603)			2
33	R12A	0 Ω(0603)			1
34	R14	2.2 R/ 0.33 W/ ±1%	ERJ8BQF2R2V	Panasonic	1
35	R14A	2R/ 0.33 W/ ±1%	ERJ8BQF2R0V	Panasonic	1
36	R15	27 k Ω ±1% (0603)			1
37	R16, R16A, R16B	15MR/ 0.25 W/5%	RC1206JR-0715ML		3
38	R18, R18A, R18B	3MR/ 0.25 W/1%	RC1206FR-073ML		3
39	R19	58.3kR/0.1 W/0.5%	RT0603DRE0758K3L		1
40	R110, R110A	2M Ω/5%/200 V	RC1206JR-072ML		2
41	R21	51R/ 0.25 W/ ±1%	ERJ8ENF51R0V	Panasonic	1
42	R22	820Ω (0603)			1

43	R23	1.2 kΩ (0603)			1
44	R24	12 kΩ (0603)			1
45	R25	16 kΩ (0603)			1
46	R25A	6.2 kΩ (0603)			1
47	R26	2.5 kΩ (0603)			1
48	R27	13R/ 0.25W/ ±1%	ERJ8ENF13R0V	Panasonic	1
49	TR1	998 µH	750343074(Rev 0.2)	Wurth Electronics	1
50	Test point of FB, VIN, CS, ZCD, Drain, V_{CC}, Gnd	Test point	5010		7
51	VAR	0.3 W/ 320 V	ERZE07A511	Panasonic	1
52	ZD1	22VZener			1
53	Con(L N)	Connector	691102710002	Wurth Electronics	1
54	Con(+12V Com), Con(+5V Com)	Connector	691 412 120 002B	Wurth Electronics	2

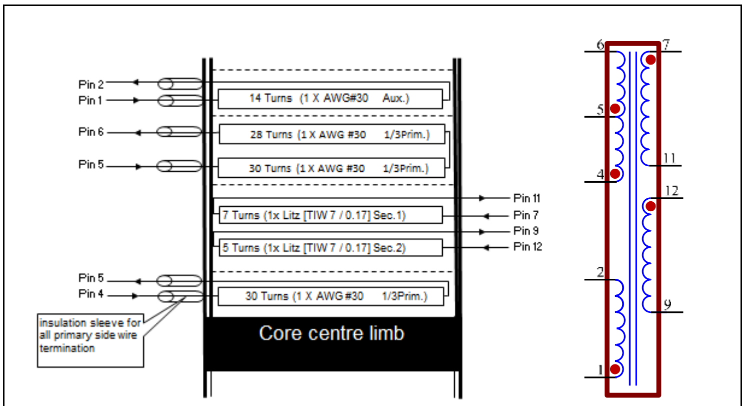
9 Transformer construction

Core and material: EE20/10/6(EF20), TP4A (TDG)

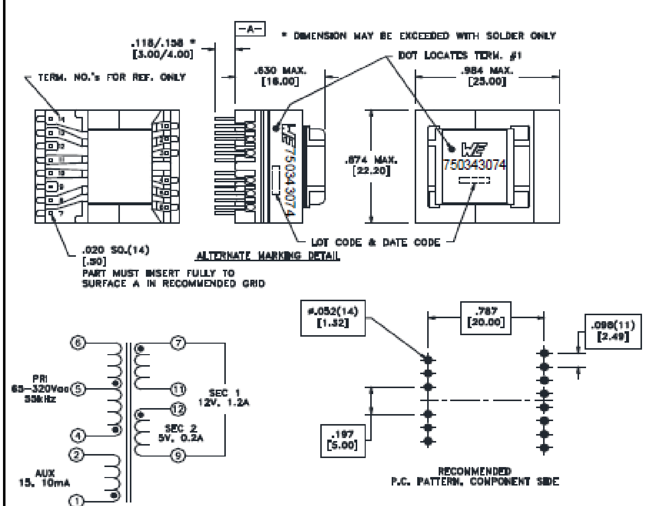
Bobbin: 070-5643 (14 Pin, THT, horizontal version)

Primary inductance: Lp=998 µH (±10%), measured between pin 4 and pin 6

Manufacturer and part number: Wurth Electronics Midcom (750343074)



Start	Stop	No. of turns	Wire size	Layer
4	5	30	1XAWG#30	1/3 Primary
12	9	5	1 x Litz [TIW 7 / 0.17]	Secondary 2
7	11	7	1 x Litz [TIW 7 / 0.17]	Secondary 1
5	6	58	1XAWG#30	2/3 Primary
1	2	14	1XAWG#30	Auxiliary



CUSTOMER TERMINAL	RoHS	LEAD(Pb)-FREE
Sn 96%, Ag 4%	Yes	Yes

ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	1-2	@20°C	0.250 ohms max.
D.C. RESISTANCE	4-6	@20°C	1.320 ohms max.
D.C. RESISTANCE	7-11	@20°C	0.040 ohms max.
D.C. RESISTANCE	12-9	@20°C	0.025 ohms max.
INDUCTANCE	4-6	50kHz, 100mV, Ls	998.0uH ±10%
LEAKAGE INDUCTANCE	4-6	tie(1+2+7+9+11+12),100kHz, 100mV, Ls	9uH typ., 15uH max.
DIELECTRIC	6-7	tie(2+4, 11+12), 3750VAC, 1 second	
DIELECTRIC	7-core	tie(11+12), 3750VAC, 1 second	
TURNS RATIO		(4-6):(1-2)	6.29:1, ±2%
TURNS RATIO		(4-6):(7-11)	12.57:1, ±2%
TURNS RATIO		(4-6):(12-9)	17.6:1, ±2%

GENERAL SPECIFICATIONS:

OPERATING TEMPERATURE RANGE: -40°C to +125°C including temp rise.

Designed to comply with the following requirements as defined by IEC60950-1, EN60950-1, UL60950-1/CSA60950-1 and AS/NZS60950.1:

- Reinforced insulation for a primary circuit at a working voltage of 320Vrms, Overvoltage Category II.

Wire insulation & RoHS status not affected by wire color. Wire insulation color may vary depending on availability.

DFM		Packaging Specifications	
DATE		Method: Tray	
ENG	NWA	PKG-0736	
REV.	02		
DATE	2016-03-16		

Tolerances unless otherwise specified: Angles: ±1° Decimals: ±.005 [.13] Fractions: ±1/64 Footprint: ± .001 [.03]

This drawing is dual dimensioned. Dimensions in brackets are in millimeters.

DRAWING TITLE: TRANSFORMER

PART NO. 750343074

SPECIFICATION SHEET 1 OF 1

Figure 5 Transformer structure

10 Test results

10.1 Efficiency, regulation and output ripple

Table 4 Efficiency, regulation & output ripple

Input (V_{AC}/Hz)	P_{in} (W)	V_{out1} (V_{DC})	I_{out1} (A)	V_{ORPP1} (mV)	V_{out2} (V_{DC})	I_{out2} (A)	V_{ORPP2} (mV)	P_{out} (W)	Efficiency η (%)	Average η (%)	OLP P_{in} (W)	OLP I_{out2} (Fixed 5 V at 0.2 A) (A)
85 V_{AC}/ 60 Hz	0.04156	4.90	0.00	20	12.17	0.00	36				25.12	1.55
	0.07992	4.76	0.006	56	12.52	0.00	18	0.03	35.74			
	9.01	4.93	0.06	19	12.11	0.60	20	7.56	83.93			
	4.67	4.90	0.05	15	12.17	0.30	15	3.90	83.43	83.03		
	9.27	4.91	0.10	19	12.16	0.60	18	7.79	84.00			
	14.09	4.90	0.15	22	12.18	0.90	19	11.70	83.02			
	19.84	4.90	0.20	25	12.18	1.25	24	16.21	81.68			
115 V_{AC}/ 60 Hz	0.04650	4.90	0.00	21	12.16	0.00	39				28.00	1.82
	0.08458	4.76	0.006	58	12.52	0.00	17	0.03	33.77			
	8.89	4.93	0.06	19	12.09	0.60	19	7.55	84.92			
	4.64	4.90	0.05	16	12.17	0.30	16	3.90	83.97	84.67		
	9.16	4.91	0.10	19	12.15	0.60	18	7.78	84.95			
	13.76	4.91	0.15	21	12.16	0.90	20	11.68	84.89			
	19.06	4.91	0.20	23	12.16	1.25	20	16.18	84.90			
230 V_{AC}/ 50 Hz	0.07107	4.90	0.00	22	12.17	0.00	38				28.40	1.90
	0.11151	4.75	0.006	59	12.54	0.00	18	0.03	25.56			
	8.94	4.93	0.06	20	12.09	0.60	19	7.55	84.45			
	4.78	4.90	0.05	18	12.16	0.30	17	3.89	81.44	84.05		
	9.22	4.91	0.10	21	12.15	0.60	19	7.78	84.39			
	13.71	4.93	0.15	21	12.12	0.90	20	11.65	84.96			
	18.92	4.92	0.20	23	12.14	1.25	21	16.16	85.41			
265V_{AC}/ 50Hz	0.08232	4.89	0.00	21	12.19	0.00	40				29.20	1.96
	0.12324	4.75	0.006	57	12.56	0.00	17	0.03	23.13			
	9.02	4.94	0.06	20	12.08	0.60	19	7.54	83.64			
	4.87	4.90	0.05	16	12.17	0.30	16	3.90	80.00	83.30		
	9.28	4.91	0.10	21	12.15	0.60	19	7.78	83.85			
	13.83	4.93	0.15	21	12.12	0.90	19	11.65	84.22			
	18.97	4.92	0.20	24	12.13	1.25	22	16.15	85.12			
300 V_{AC}/ 50 Hz	0.09631	4.89	0.00	22	12.18	0.00	39				30.13	2.03
	0.14497	4.76	0.006	56	12.54	0.00	17	0.03	19.70			
	9.12	4.94	0.06	20	12.08	0.60	19	7.54	82.72			
	4.96	4.90	0.05	15	12.18	0.30	14	3.90	78.61	82.48		
	9.39	4.91	0.10	21	12.15	0.60	19	7.78	82.86			
	13.91	4.92	0.15	22	12.13	0.90	21	11.66	83.79			
	19.06	4.93	0.20	25	12.12	1.25	23	16.14	84.66			

Minimum load condition : 5 V at 6 mA

Typical load condition : 5 V at 60 mA and 12 V at 0.6 A

Maximum load condition : 5 V at 200 mA and 12 V at 1.25 A

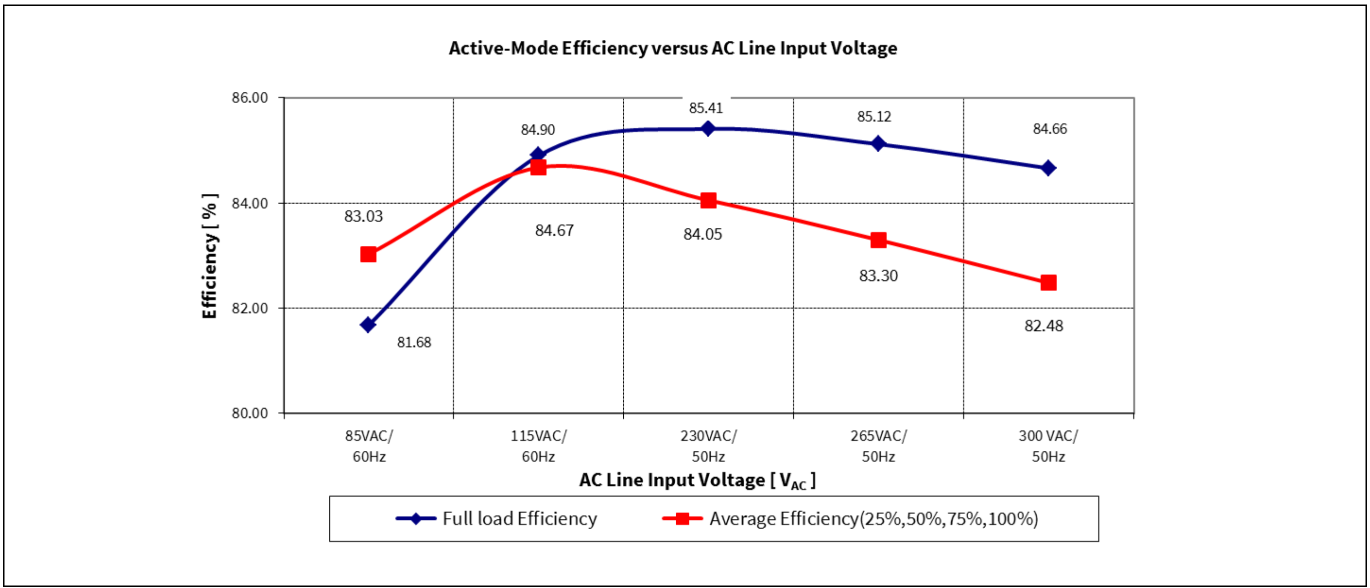


Figure 6 Efficiency vs AC line input voltage

10.2 Standby power

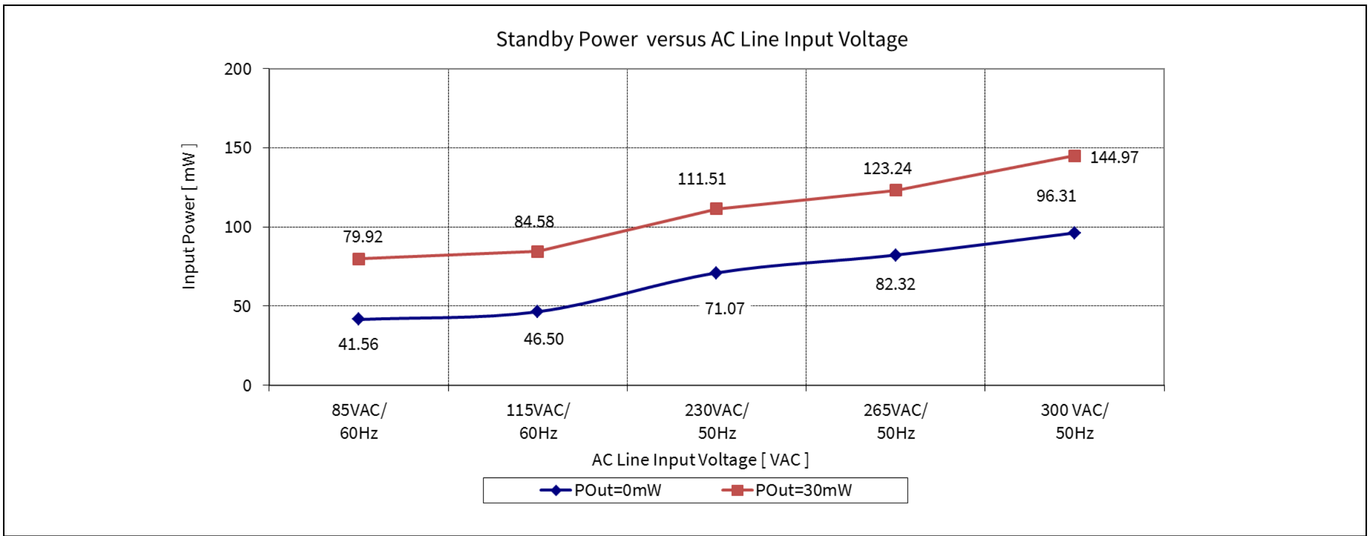


Figure 7 Standby power at no load and 30 mW load vs AC line input voltage (measured by Yokogawa WT210 power meter - integration mode)

10.3 Line regulation

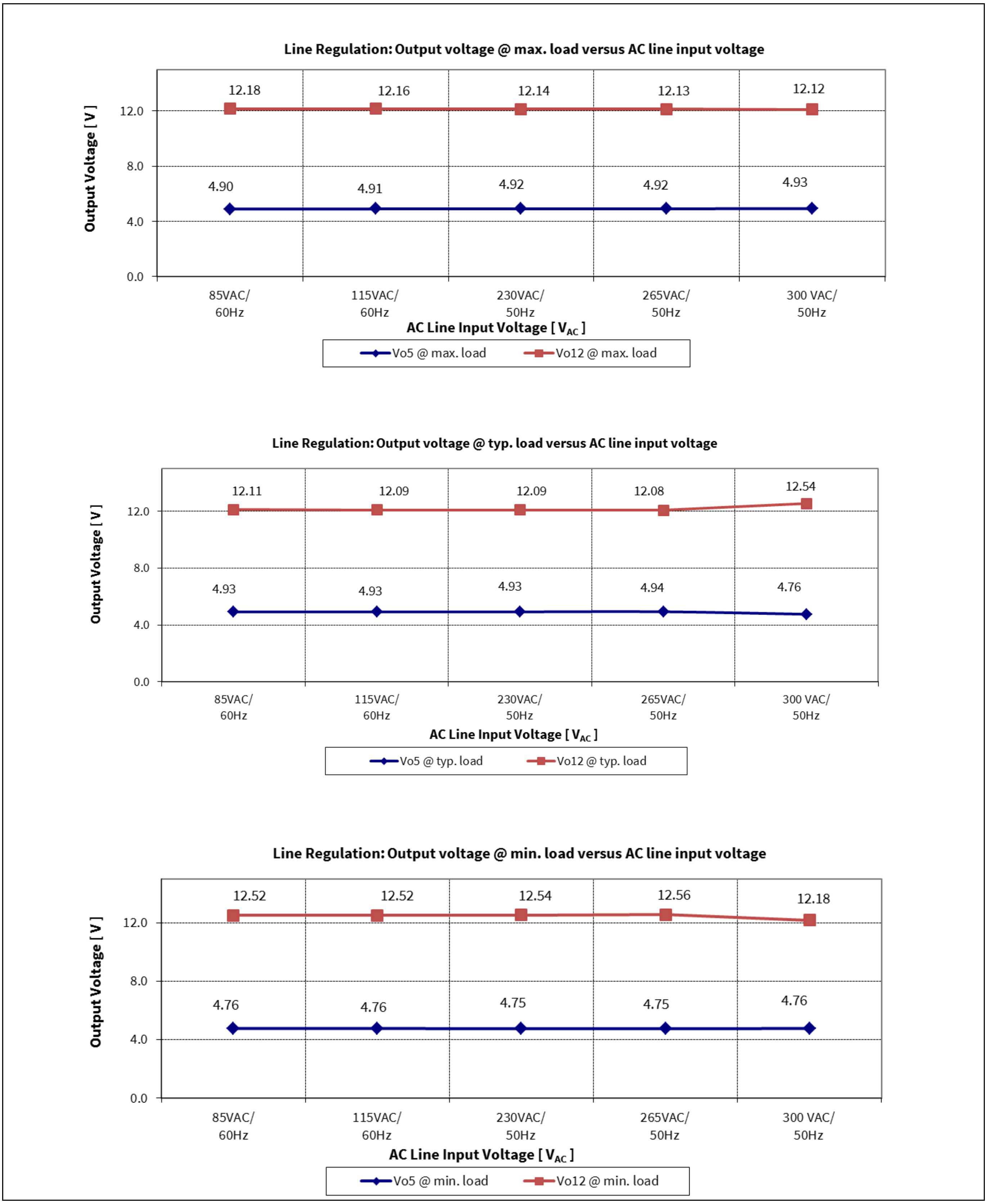


Figure 8 Line regulation V_{Out} at full load vs AC line input voltage

10.4 Load regulation

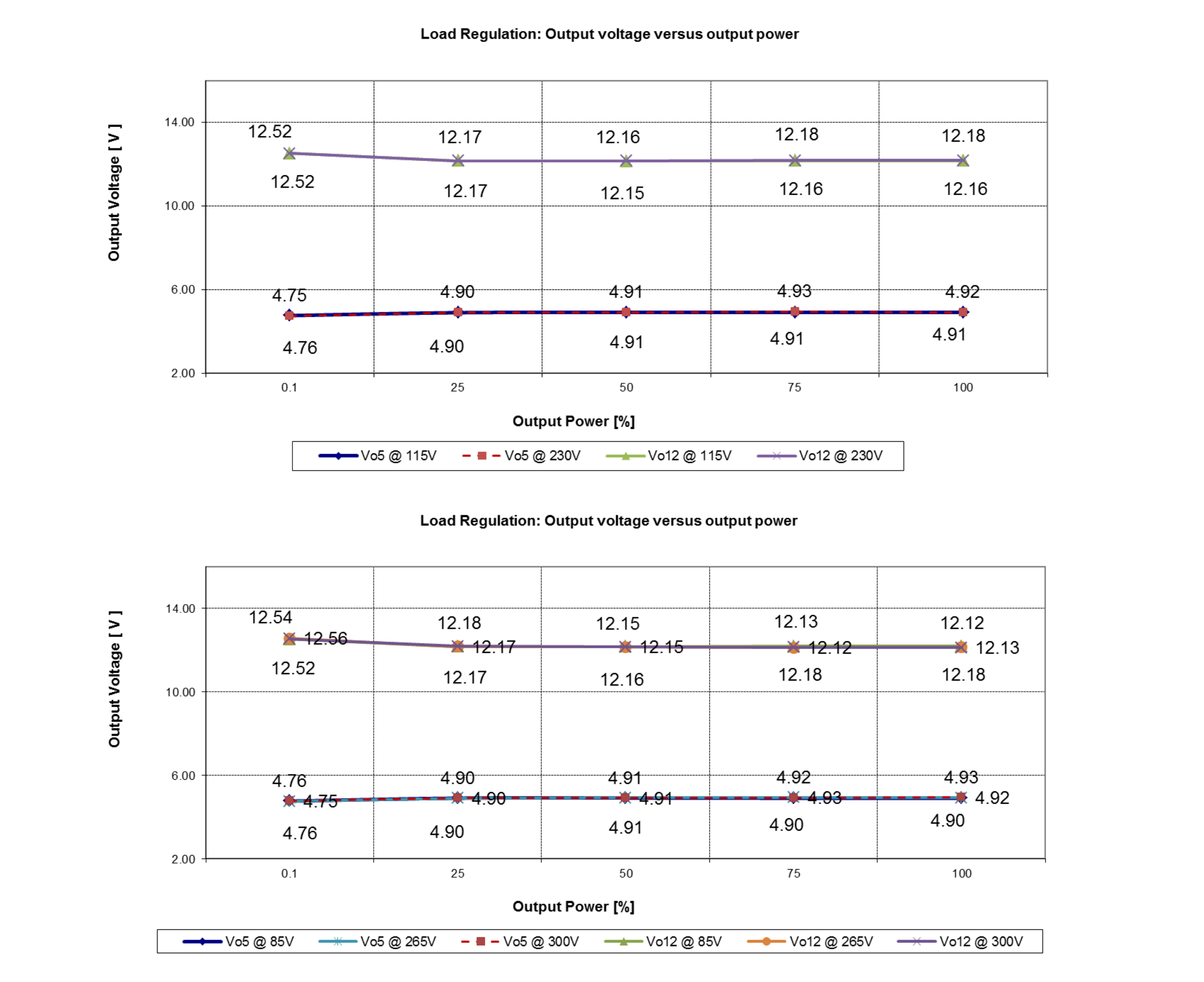


Figure 9 Load regulation V_{Out} vs output power

10.5 Maximum input power

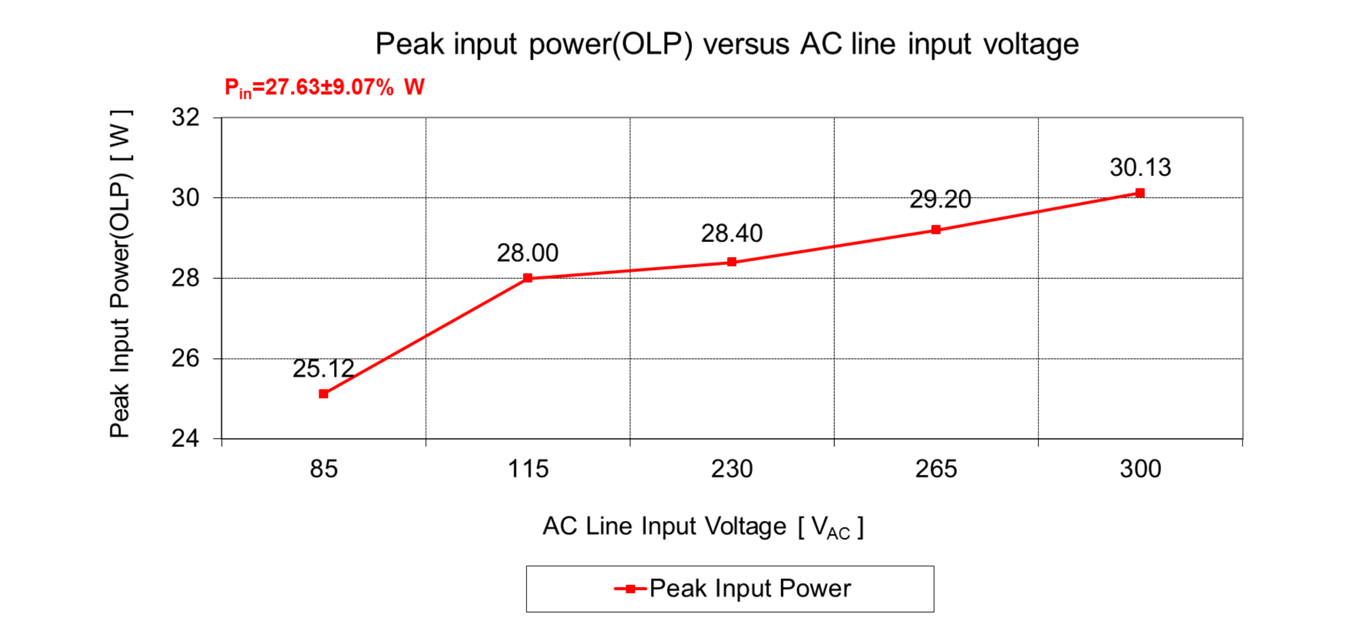


Figure 10 Maximum input power (before over-load protection) vs AC line input voltage

10.6 ESD immunity (EN61000-4-2)

Pass EN61000-4-2 Special Level (±14 kV for contact discharge and (±16 kV air discharge).

10.7 Surge immunity (EN61000-4-5)

Pass EN61000-4-5 Installation class 4 (±2 kV for line to line and ±4 kV for line to earth)[1].

10.8 Conducted emissions (EN55022 class B)

The conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN55022 (CISPR 22) class B. The demo board was set up at maximum load (16 W) with input voltage of 115 V_{AC} and 230 V_{AC}.

[1] PCB spark gap distance needs to reduce to 0.5 mm and C13 change to 120 µF.

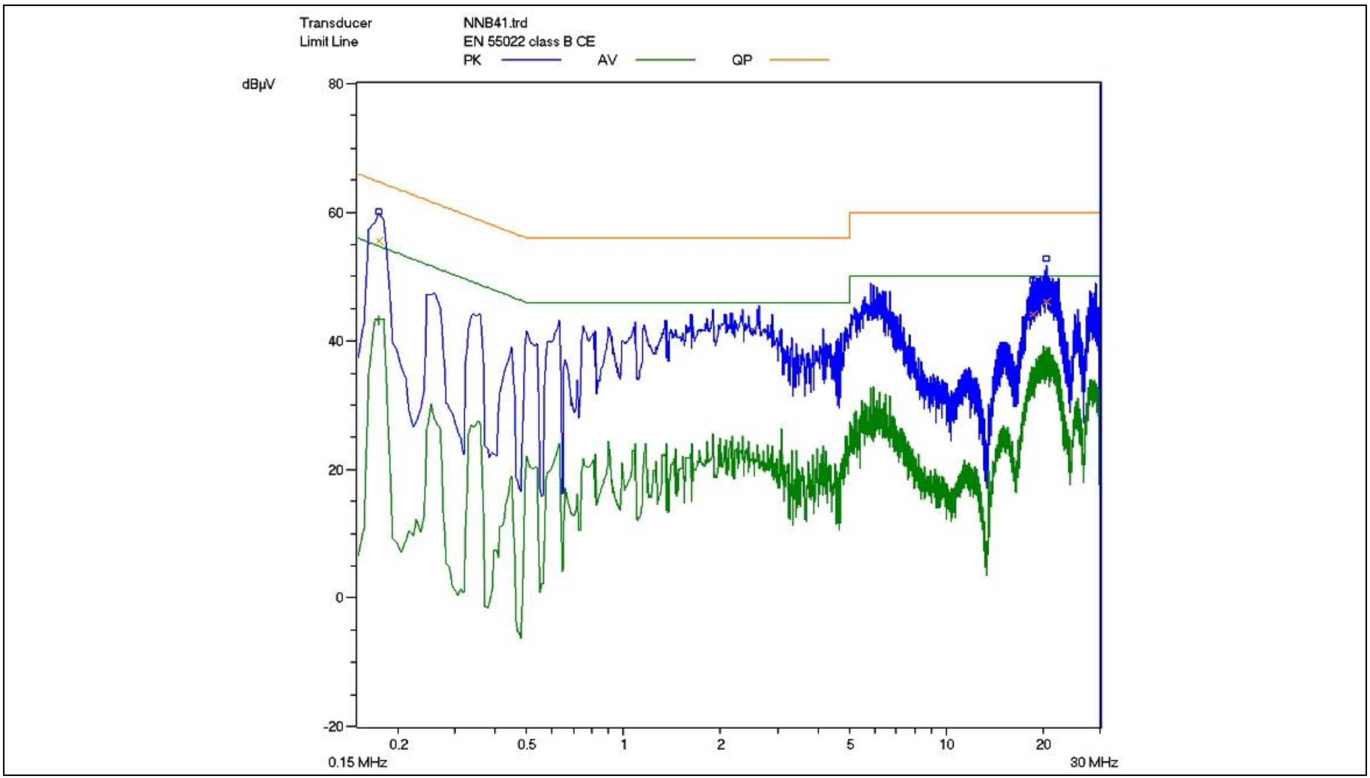


Figure 11 Conducted emissions(line) at 115 V_{AC} and maximum load

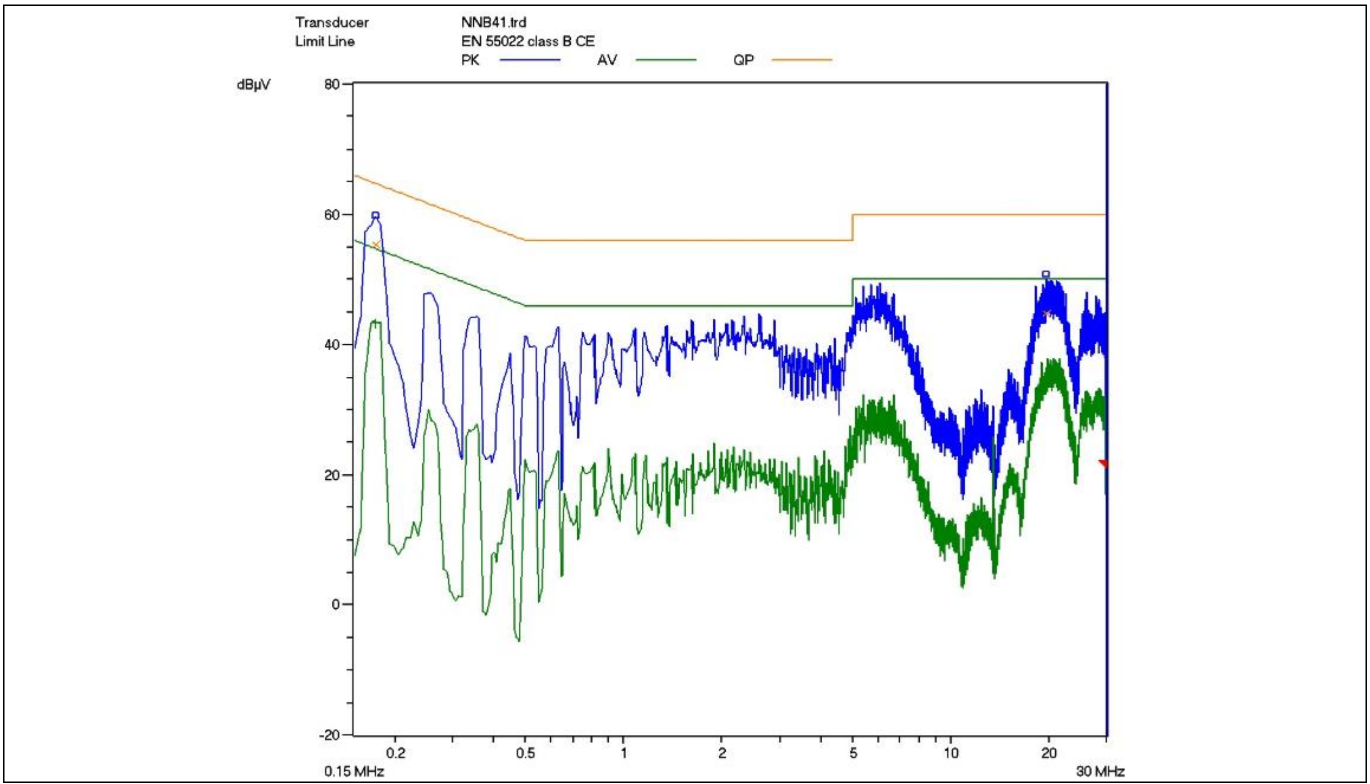


Figure 12 Conducted emissions(neutral) at 115 V_{AC} and maximum load

Pass conducted emissions EN55022 (CISPR 22) class B with 8 dB margin for quasi peak measurement at low line (115 V_{AC}).

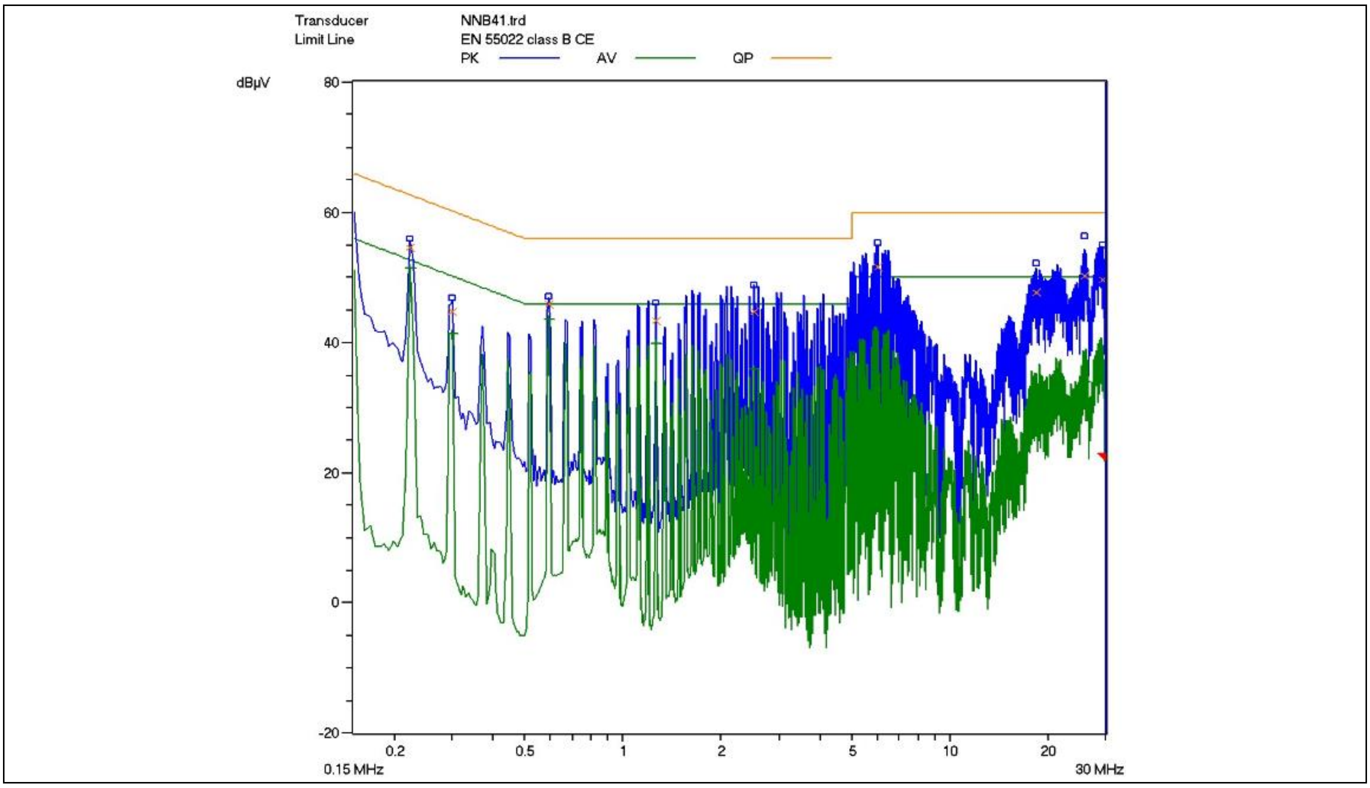


Figure 13 **Conducted emissions(line) at 230 V_{AC} and maximum load**

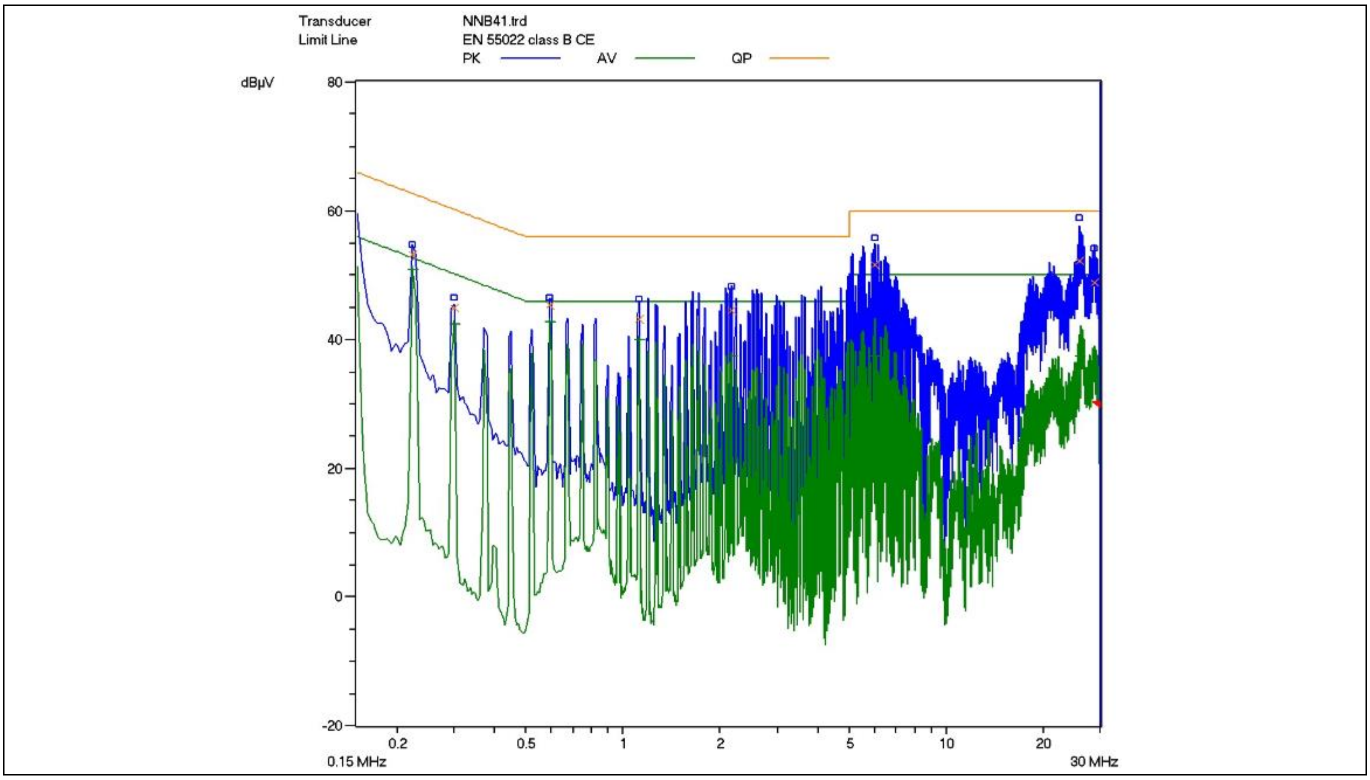


Figure 14 **Conducted emissions(neutral) at 230 V_{AC} and maximum load**

Pass conducted emissions EN55022 (CISPR 22) class B with 6 dB margin for quasi peak measurement at high line (230 V_{AC}).

10.9 Thermal measurement

The thermal test of open frame demo board was done using an infrared thermography camera (TVS-500EX) at ambient temperature 25°C. The measurements were taken after one hour running at full load.

Table 5 Hottest temperature of demo board

No.	Major component	85 V_{AC} (°C)	300 V_{AC} (°C)
1	IC11 (ICE5QR4770AZ)	78.2	53.8
2	R14A (current sense resistor)	54.9	40.7
3	TR1 (transformer)	54.5	65.0
4	BR1 (bridge diode)	45.7	33.4
5	R11(clamper resistor)	57.3	53.6
6	L11 (choke)	47.3	31.6
7	D21 (Secondary diode)	49.3	56.2
8	D22 (Secondary diode)	37.2	42.0
9	Ambient	25.0	25.0

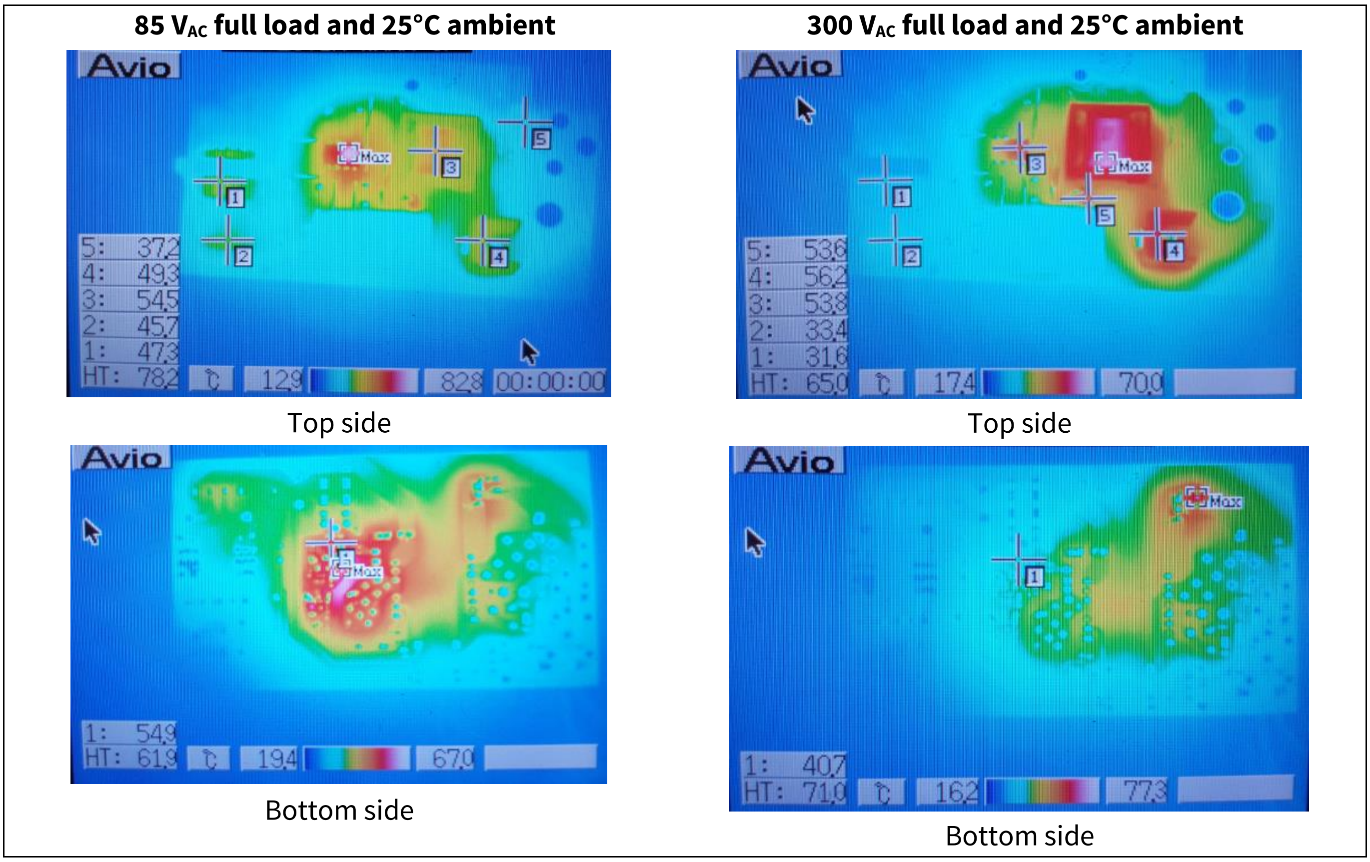


Figure 15 Infrared thermal image of DEMO_5QR4770AZ_16W1

11 Waveforms and scope plots

All waveforms and scope plots were recorded with a TELEDYNELECROY 606Zi oscilloscope.

11.1 Startup at low/high AC line input voltage with maximum load

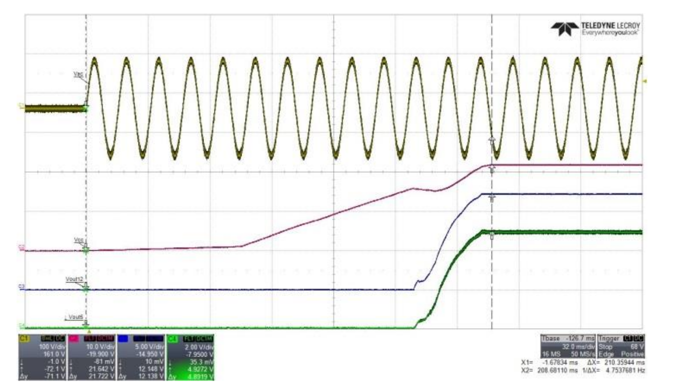
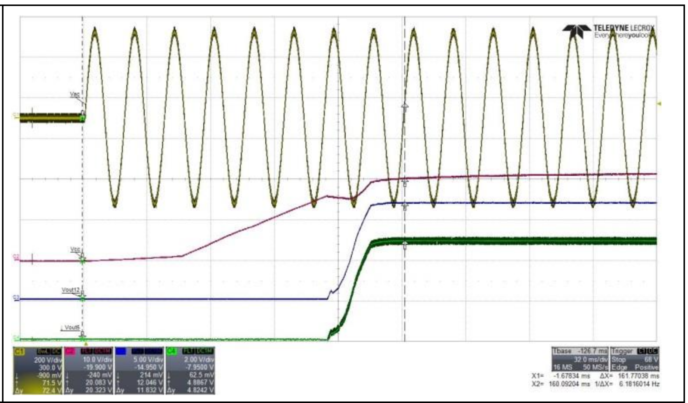
	
C1 (Yellow) : AC line voltage (V_{AC}) C2 (Purple) : Supply voltage (V_{VCC}) C3 (Blue) : 12 V output voltage (V_{Out12}) C4 (Green) : 5 V output voltage (V_{Out5})	C1 (Yellow) : AC line voltage (V_{AC}) C2 (Purple) : Supply voltage (V_{VCC}) C3 (Blue) : 12 V output voltage (V_{Out12}) C4 (Green) : 5 V output voltage (V_{Out5})
Startup time at 85 V_{AC} and maximum load ≈ 210 ms	Startup time at 300 V_{AC} and maximum load ≈ 160 ms

Figure 16 Startup

11.2 Soft start

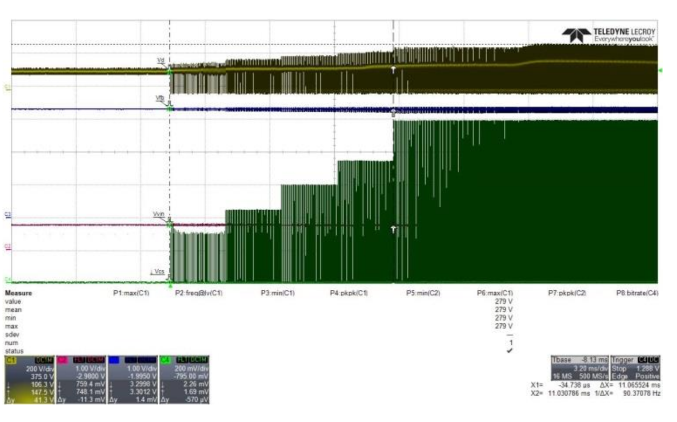
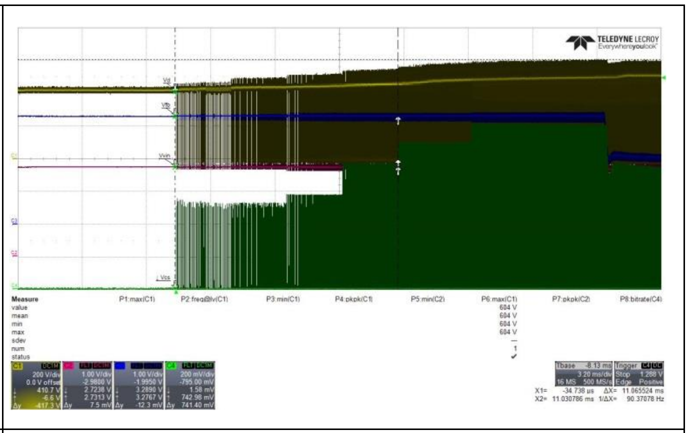
	
C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : V_{IN} voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : V_{IN} voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})
Soft start time at 85 V_{AC} and maximum load ≈ 11 ms	Soft start time at 300 V_{AC} and maximum load ≈ 11 ms

Figure 17 Soft start

11.3 Drain and current sense voltage at maximum load

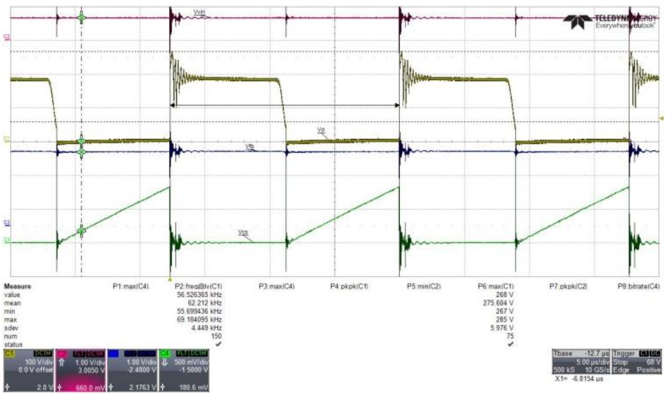
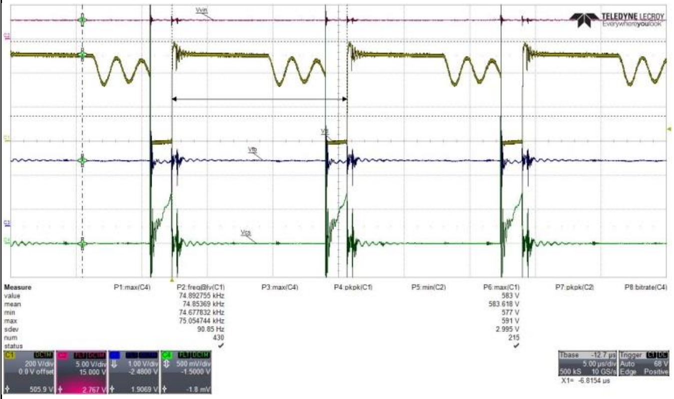
	
C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : V_{IN} voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : V_{IN} voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})
V_{Drain_peak} at 85 V_{AC} ≈ 268 V with 1^{st} ZC and f_S ≈ 62 kHz	V_{Drain_peak} at 300V_{AC} ≈ 591 V with 3^{rd} ZC and f_S ≈ 74 kHz

Figure 18 Drain and current sense voltage at maximum load

11.4 Zero crossing point during normal operation

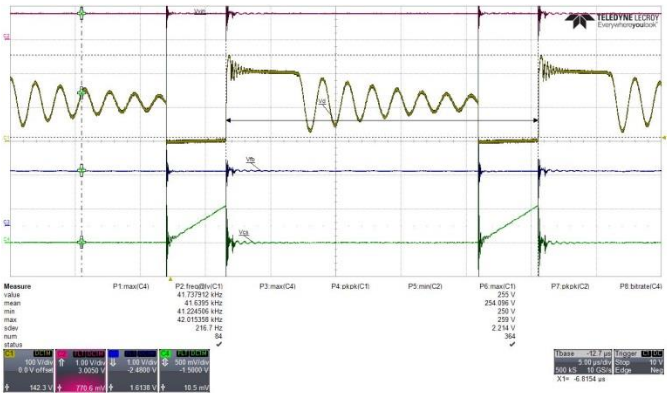
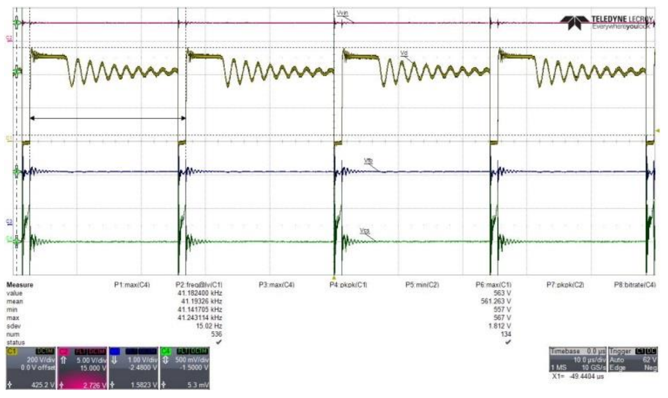
	
C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : V_{IN} voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : V_{IN} voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})
8^{th} zero crossing at 85 V_{AC} and 25% load (5 V x 0.05 A +12 V x 0.31 A) (zero crossing varies from 1~8 for low line)	10^{th} zero crossing at 300 V_{AC} and 25% load (5 V x 0.05 A +12 V x 0.31 A) (zero crossing varies from 3~10 for high line)

Figure 19 Zero crossing

11.5 Load transient response (dynamic load from 10% to 100%)

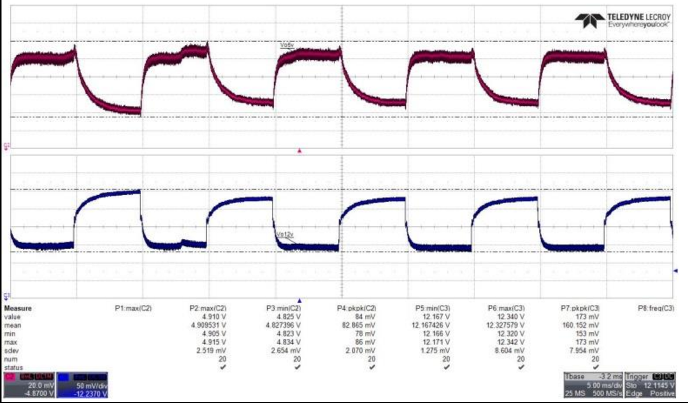
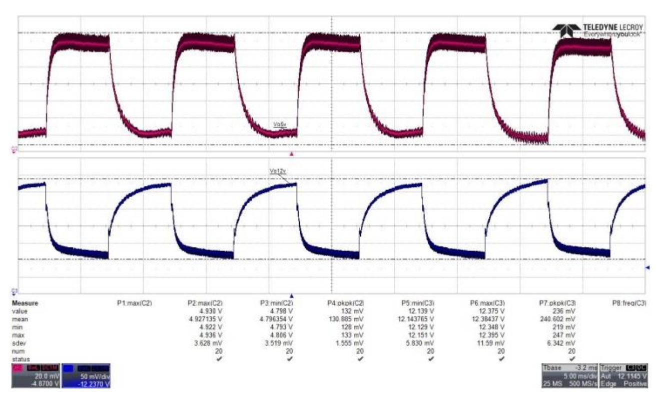
	
C2 (Purple) : 5 V Output ripple voltage (V_{Out5}) C3 (Blue) : 12 V Output ripple voltage (V_{Out12})	C2 (Purple) : 5 V Output ripple voltage (V_{Out5}) C3 (Blue) : 12 V Output ripple voltage (V_{Out12})
5 $V_{ripple\_pk\_pk}$ at 85 V_{AC} ≈ 86 mV 12 $V_{ripple\_pk\_pk}$ at 85 V_{AC} ≈ 173 mV (85 V_{AC} , 12 V Load change from 10% to 100% and 5 V at 200 mA load, 100 Hz, 0.4 A/µs slew rate) Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	5 $V_{ripple\_pk\_pk}$ at 300 V_{AC} ≈ 133 mV 12 $V_{ripple\_pk\_pk}$ at 85 V_{AC} ≈ 247 mV (300 V_{AC} , 12 V Load change from 10% to 100% and 5 V at 200 mA load, 100 Hz, 0.4 A/µs slew rate) Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 20 Load transient response

11.6 Output ripple voltage at maximum load

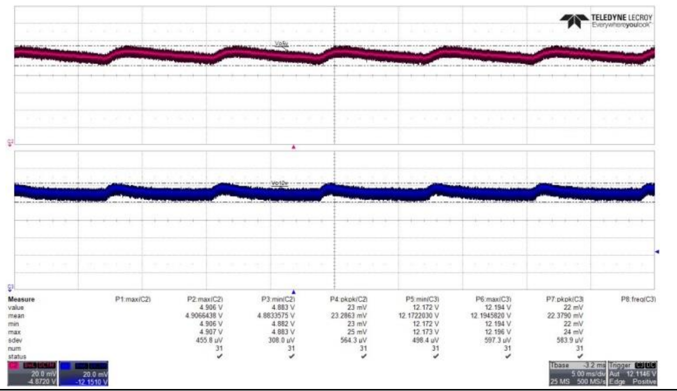
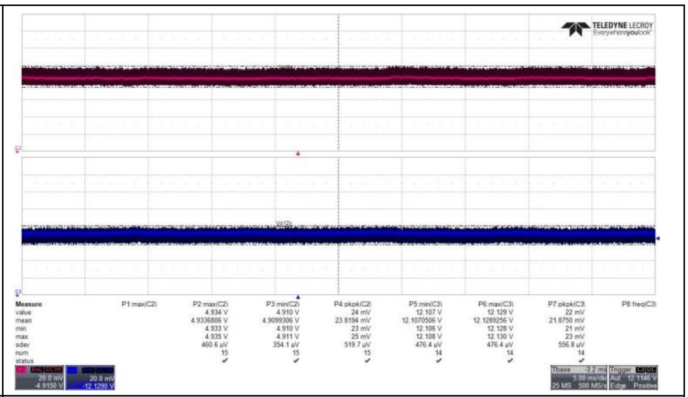
	
C2 (Purple) : 5 V Output ripple voltage (V_{Out5}) C3 (Blue) : 12 V Output ripple voltage (V_{Out12})	C2 (Purple) : 5 V Output ripple voltage (V_{Out5}) C3 (Blue) : 12 V Output ripple voltage (V_{Out12})
5 $V_{ripple\_pk\_pk}$ at 85 V_{AC} ≈ 25 mV 12 $V_{ripple\_pk\_pk}$ at 85 V_{AC} ≈ 24 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter	5 $V_{ripple\_pk\_pk}$ at 300 V_{AC} ≈ 25 mV 12 $V_{ripple\_pk\_pk}$ at 300 V_{AC} ≈ 23 mV Probe terminal end with decoupling capacitor of 0.1 µF(ceramic) and 1 µF(Electrolytic), 20 MHz filter

Figure 21 Output ripple voltage at maximum load

11.7 Output ripple voltage at burst mode 1 W load

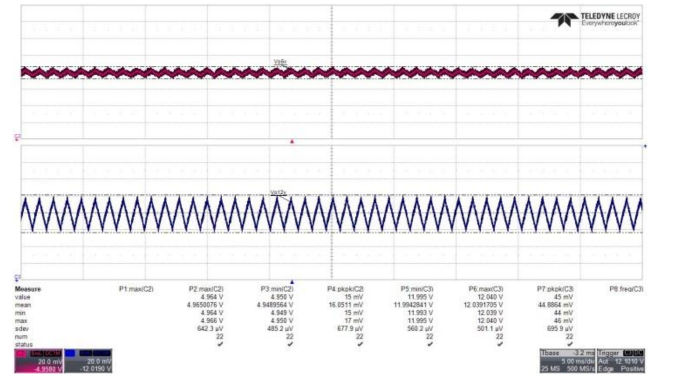
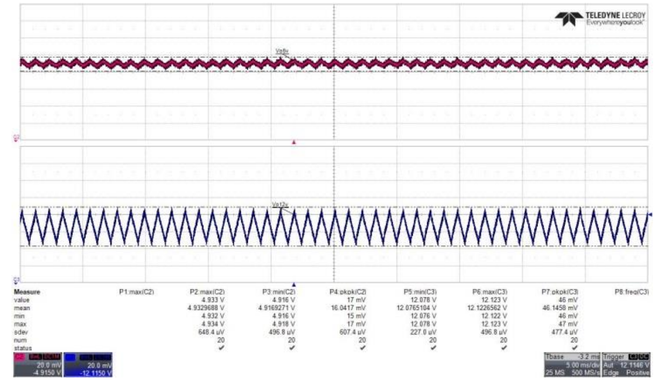
	
C2 (Purple) : 5 V Output ripple voltage (V_{Out5}) C3 (Blue) : 12 V Output ripple voltage (V_{Out12})	C2 (Purple) : 5 V Output ripple voltage (V_{Out5}) C3 (Blue) : 12 V Output ripple voltage (V_{Out12})
5 $V_{ripple\_pk\_pk}$ at 85 V_{AC} ≈ 17 mV 12 $V_{ripple\_pk\_pk}$ at 85 V_{AC} ≈ 46 mV Load: 5 V at 6 mA and 12 V at 80mA Probe terminal end with decoupling capacitor of 0.1 μF(ceramic) and 1 μF(Electrolytic), 20 MHz filter	5 $V_{ripple\_pk\_pk}$ at 300 V_{AC} ≈ 17 mV 12 $V_{ripple\_pk\_pk}$ at 300 V_{AC} ≈ 47 mV Load: 5 V at 6 mA and 12 V at 80mA Probe terminal end with decoupling capacitor of 0.1 μF(ceramic) and 1 μF(Electrolytic), 20 MHz filter

Figure 22 Output ripple voltage at burst mode 1 W load

11.8 Entering active burst mode

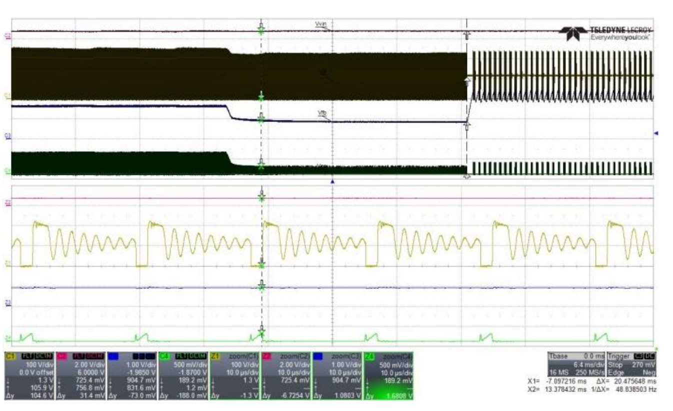
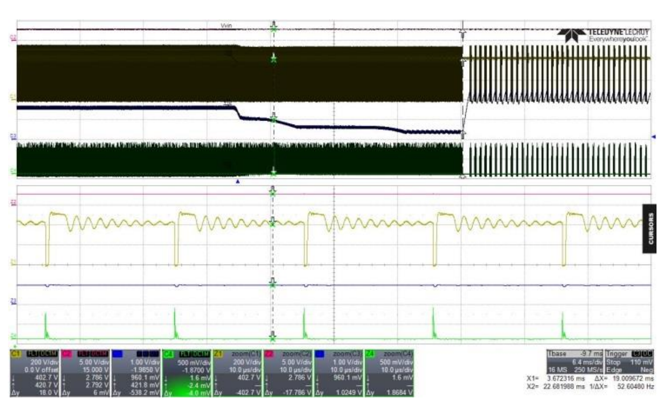
	
C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : V_{IN} voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : V_{IN} voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})
Condition to enter burst mode level 1 : V_{FB} < 0.9 V, N_{ZC} = 8 and $t_{blanking}$ = 20 ms (load change form 5 W to 0.5 W at 85 V_{AC})	Condition to enter burst mode level 1 : V_{FB} < 0.9 V, N_{ZC} = 10 and $t_{blanking}$ = 20 ms (load change form 5 W to 0.5 W at 300 V_{AC})

Figure 23 Entering active burst mode

11.9 During active burst mode

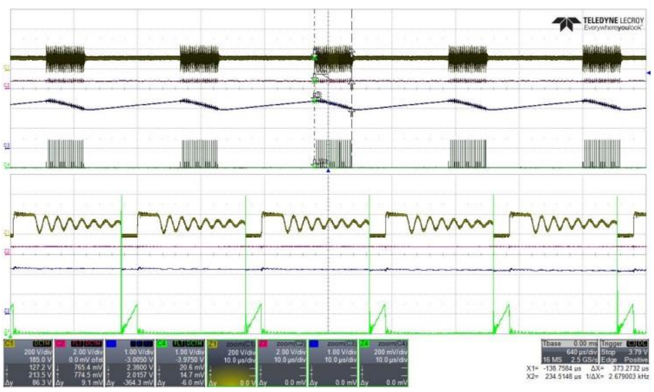
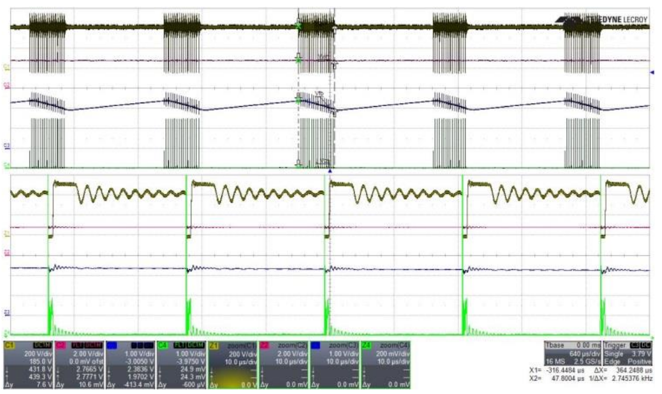
	
C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : V_{IN} voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : V_{IN} voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})
During active burst mode level 1 : V_{FB_BOn}=2.4 V, V_{FB_BOff} = 2.0 V, V_{CSBLP} = 0.31 V, N_{ZC} = 8 (0.5 W at 85 V_{AC})	During active burst mode level 1 : V_{FB_BOn}=2.4 V, V_{FB_BOff} = 2.0 V, V_{CSBLP} = 0.31 V, N_{ZC} = 10 (0.5 W at 300 V_{AC})

Figure 24 During active burst mode

11.10 Leaving active burst mode

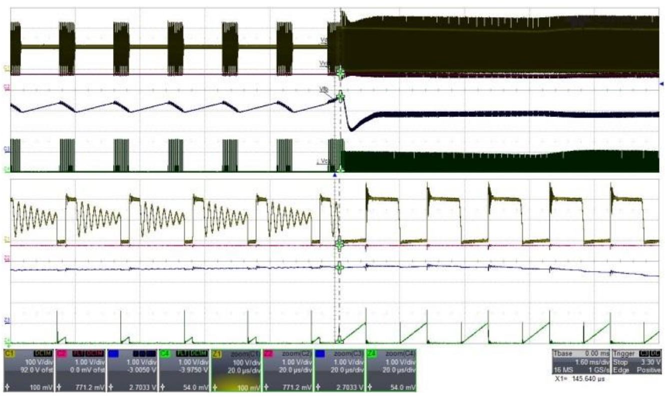
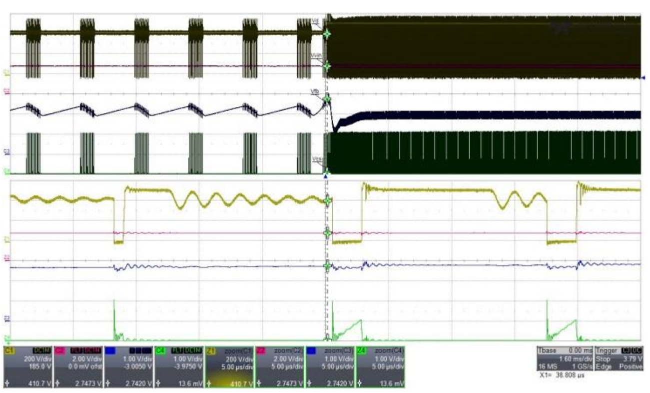
	
C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : V_{IN} voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})	C1 (Yellow) : Drain voltage (V_D) C2 (Purple) : V_{IN} voltage (V_{VIN}) C3 (Blue) : Feedback voltage (V_{FB}) C4 (Green) : Current sense voltage (V_{CS})
Condition to leave burst mode level 1 : V_{FB} >2.75 V (load change form 0.5 W full load at 85 V_{AC})	Condition to leave burst mode level 1 : V_{FB} >2.75 V (load change form 0.5 W full load at 300 V_{AC})

Figure 25 Leaving active burst mode

11.11 Line over voltage protection (non switch auto restart)

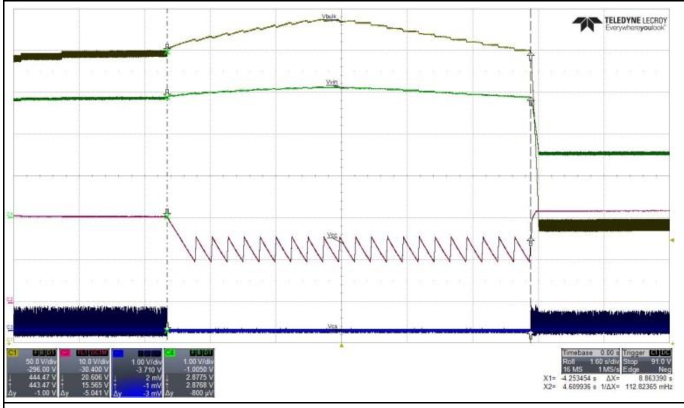
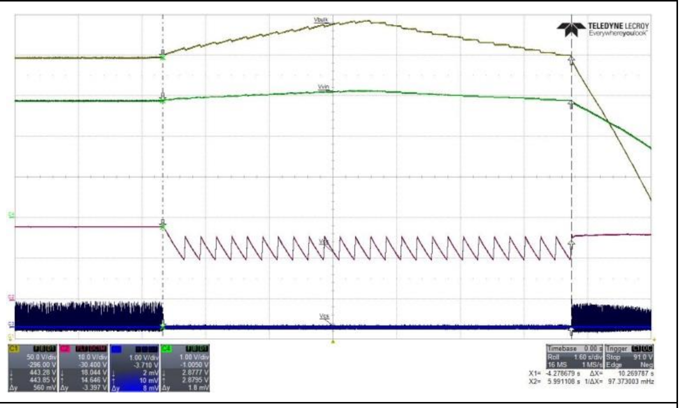
	
C1 (Yellow) : Bulk voltage (V_{Bulk}) C2 (Purple) : Supply voltage (V_{VCC}) C3 (Blue) : Current sense voltage (V_{CS}) C4 (Green) : V_{IN} voltage (V_{VIN})	C1 (Yellow) : Bulk voltage (V_{Bulk}) C2 (Purple) : Supply voltage (V_{VCC}) C3 (Blue) : Current sense voltage (V_{CS}) C4 (Green) : V_{IN} voltage (V_{VIN})
Condition to detect Line over voltage protection : V_{VIN} > 2.9 V (V_{BULK} > 442 V_{DC}[≈320 V_{AC}]) Condition to reset Line over voltage protection : V_{VIN} < 2.9 V (V_{BULK} < 442 V)	
(Gradually increase AC line voltage at full load till Line OVP detect and decrease AC line till Line OVP reset)	(Gradually increase AC line voltage at 1 W load(Active Burst Mode) till Line OVP detect and decrease AC line till Line OVP reset)

Figure 26 Line over voltage protection

11.12 Brownout protection (non switch auto restart)

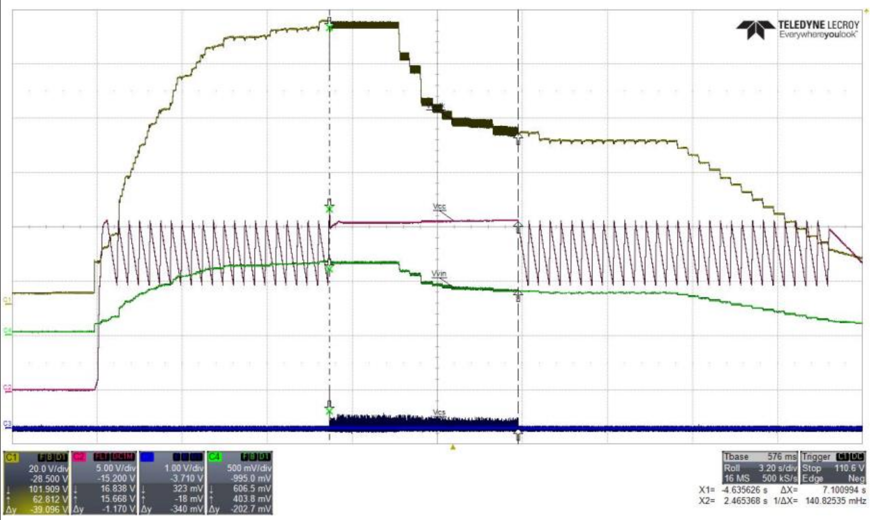
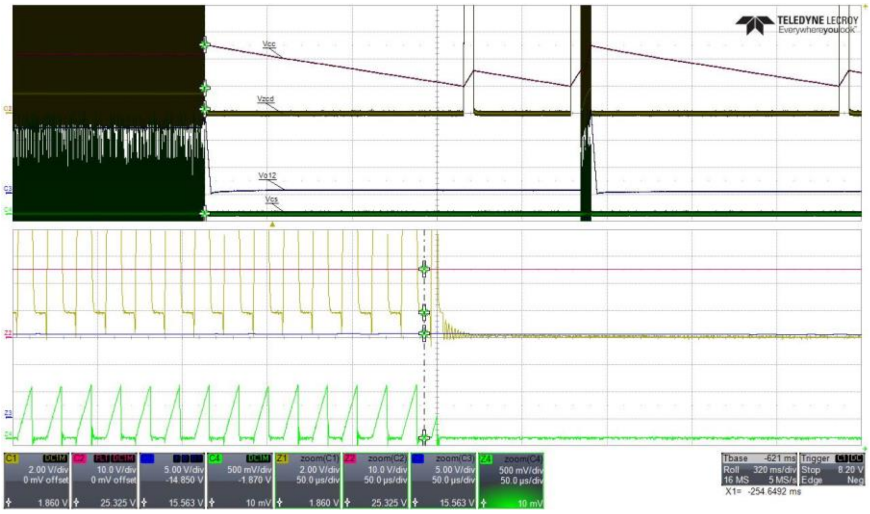

C1 (Yellow) : Bulk voltage (V_{Bulk}) C2 (Purple) : Supply voltage (V_{VCC}) C3 (Blue) : Current sense voltage (V_{CS}) C4 (Green) : V_{IN} voltage (V_{VIN})
Condition to reset Brownout protection(Brownin) : V_{VIN} > 0.66 V (V_{BULK} > 100 V_{DC} [≈73 V_{AC}]) Condition to detect Brownout protection : V_{VIN} < 0.4 V (V_{BULK} < 61 V_{DC} [≈44 V_{AC}])
(Gradually increase AC line voltage at 1 W load till system start and reduce the line till brownout detect)

Figure 27 Brownout protection

11.13 V_{CC} over voltage protection (odd skip auto restart)

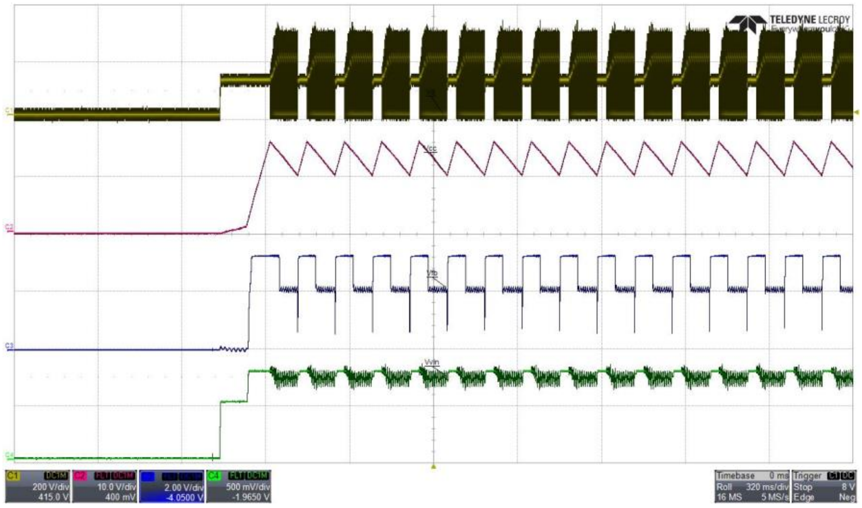


C1 (Yellow) : Zero crossing detection voltage (V_{ZCD})
C2 (Purple) : Supply voltage (V_{VCC})
C3 (Blue) : 12 V output voltage (V_{O12})
C4 (Green) : Current sense voltage (V_{CS})

Condition to enter V_{VCC} over voltage protection: $V_{VCC} > 25.5$ V
(85 V_{AC} and remove R13, load change form 13 W to full load)

Figure 28 V_{CC} over voltage protection

11.14 V_{CC} under voltage protection (auto restart)

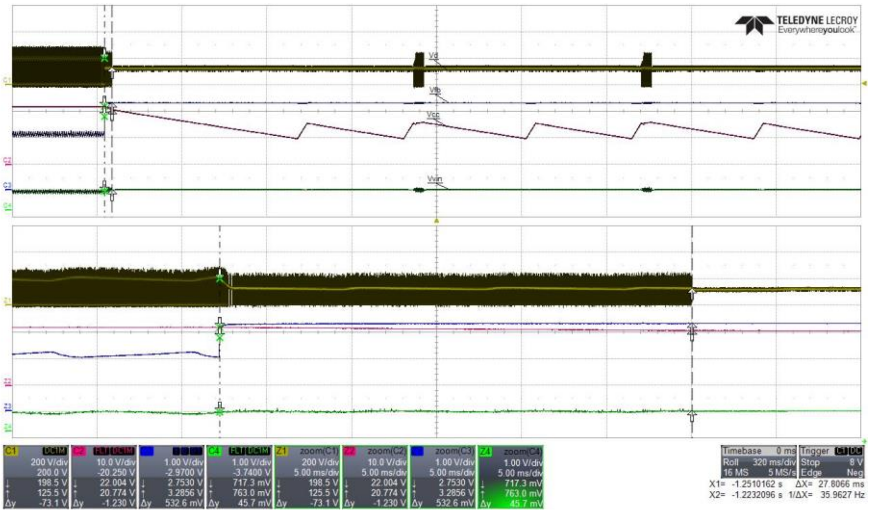


C1 (Yellow) : Drain voltage (V_D)
C2 (Purple) : Supply voltage (V_{VCC})
C3 (Blue) : Feedback voltage (V_{FB})
C4 (Green) : V_{IN} voltage (V_{VIN})

Condition to enter V_{CC} under voltage protection: $V_{CC} < 10$ V
(Remove R12A and power on the system with full load at 85 V_{AC})

Figure 29 V_{CC} under voltage protection

11.15 Over load protection (odd skip auto restart)

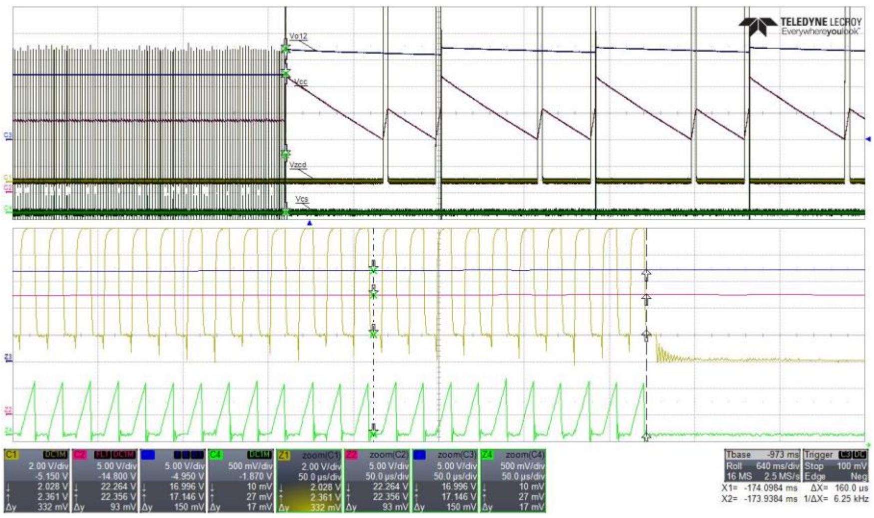


C1 (Yellow) : Drain voltage (V_D)
C2 (Purple) : Supply voltage (V_{VCC})
C3 (Blue) : Feedback voltage (V_{FB})
C4 (Green) : V_{IN} voltage (V_{VIN})

Condition to enter over load protection: V_{FB} > 2.75 V & last for 30 ms blanking time
(12 V output load change from full load to short at 85 V_{AC})

Figure 30 Over load protection

11.16 Output over voltage protection (odd skip auto restart)

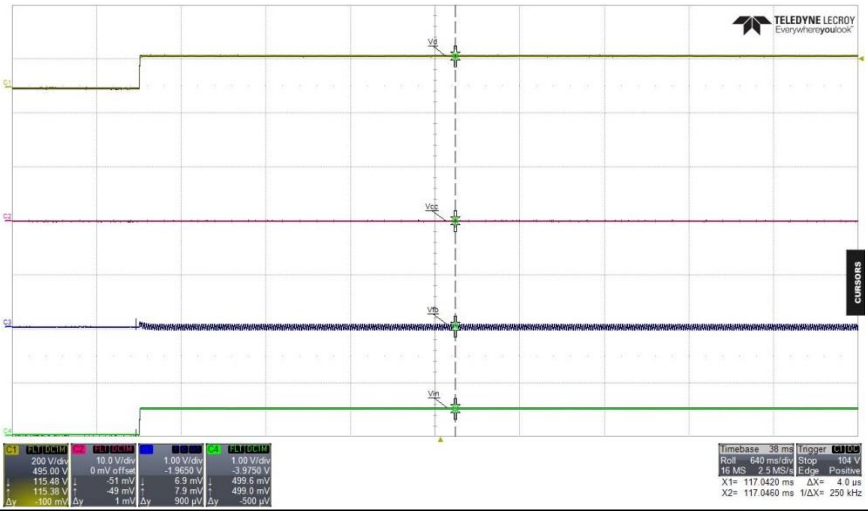


C1 (Yellow) : Zero crossing detection voltage (V_{ZCD})
C2 (Purple) : Supply voltage (V_{VCC})
C3 (Blue) : 12 V output voltage (V_{O12})
C4 (Green) : Current sense voltage (V_{CS})

Condition to enter output OVP: V_{O12} >16.8 V (V_{ZCD} > 2 V)
(85 V_{AC}, short R26 during system operation at no load)

Figure 31 Output over voltage protection

11.17 V_{CC} short to GND protection



C1 (Yellow) : Drain voltage (V_D)
C2 (Purple) : V_{CC} voltage (V_{VCC})
C3 (Blue) : Feedback voltage (V_{FB})
C4 (Green) : V_{IN} voltage (V_{VIN})

Condition to enter V_{CC} short to GND : if $V_{CC} < V_{VCC\_SCP} \rightarrow I_{VCC} = I_{VCC\_Charge1}$
(Short V_{CC} pin to Gnd by multi-metre and measure the current, $I_{VCC} \approx$ 280 µA and input power is ≈ 50 mW at 85 V_{AC} and full load)

Figure 32 V_{CC} short to GND protection

12 References

[1] ICE5QRxxxxAx datasheet, Infineon Technologies AG

[2] AN-201609_PL83_026-5th Generation Quasi-Resonant Design Guide

Revision history

Major changes since the last revision

Page or Reference	Description of change
--	First release.

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