

Driving CoolGaN™ 600 V high electron mobility transistors

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About this document

Scope and purpose

This document deals with the preferred driving scheme for Infineon's first-generation 600 V e-mode gallium nitride (GaN) transistor, a p-GaN-type switch with non-isolated gate, referred to here as CoolGaN™ 600 V High Electron Mobility Transistor (HEMT). A driving concept based on Infineon's driver IC 1EDI20N12AF together with a dedicated coupling network is described and thoroughly analyzed. Both physical GaN properties and application-specific considerations are taken into account. Theory and simulation results are shown to be in agreement with the measurements.

The purpose of this document is to enable the reader to understand and optimize the driving circuitry according to their particular goals and needs.

Intended audience

This application note is mainly aimed at readers with a basic knowledge of switching circuits and power transistors. However, any particular familiarity with GaN HEMTs is neither assumed nor required.

Table of contents

About this document.....	1
Table of contents.....	1
1 Introduction	3
2 General gate-driving considerations	4
2.1 Isolated gate (MOSFET)	4
2.2 Non-isolated gate (p-GaN)	5
3 Infineon's e-mode GaN solution	8
3.1 GaN HEMT properties	8
3.2 Driver properties	9
3.3 Interface circuit	10
4 Dimensioning of the RC interface	11
4.1 Basic relations	11
4.2 Driving real GaN transistor gates	13
5 Application-specific considerations.....	16
5.1 Hard-switched applications (totem-pole PFC)	16
5.1.1 Totem-pole PFC topology	16
5.1.2 GaN transistor in reverse conduction (diode)	17
5.1.3 Particular effects in hard-switched topologies	18
5.1.4 Example totem-pole PFC	18
5.2 Soft-switched applications (LLC)	23
6 Measurement results	25

Driving CoolGaN™ 600 V high electron mobility transistors

Introduction

7	Summary and guidelines.....	26
8	References	27
	Revision history.....	28

1 Introduction

Gallium nitride (GaN) is a very promising material for power semiconductors. Although known for decades, the need for exotic and expensive substrate materials has severely limited its useful application areas. However, this situation has changed in recent years. Efforts worldwide have led to significant progress in the realization of reliable GaN transistors on cheap silicon substrates and this has been key to their economic success. Technically, the wide bandgap of GaN allows higher electric field strengths and thus results in more compact HV switches compared to silicon, thus far surpassing state-of-the-art silicon transistors in terms of all relevant Figures of Merit (FOM).

More importantly, GaN switches are so-called heterojunction High Electron Mobility Transistors (HEMTs). The conducting channel is formed at an AlGaN/GaN interface by a highly conductive two-dimensional electron gas (2DEG). Therefore the device is purely lateral and does not contain physical pn-junctions. And that is why GaN transistors can be operated not only as power switches, but also as diodes, i. e. in reverse direction with negligible reverse recovery charge Q_{rr} . This is not possible with silicon MOSFETs due to the high Q_{rr} of their intrinsic pn-junction diode. A further consequence is the possible substitution of diodes by switches, which enables the utilization of new power topologies with significant advantages in terms of cost and efficiency [1].

But as ever, there is no such thing as a free lunch. In the case of GaN, the payment consists of a property that is not appreciated by engineers dealing with the application of power switches. A GaN HEMT is inherently “normally on”, i.e. the electron gas is formed without the need for any external voltage. To interrupt the channel and switch the transistor off, however, a negative voltage at the gate with respect to the source is required. Obviously, if this voltage is not available, e.g. in failure modes or during power-up or down, this behavior can cause power shorts and might even be destructive. The most common solution to this problem is to add a low-voltage e-mode silicon MOSFET in series with the GaN HEMT in a cascode configuration [2]; however, significant drawbacks in terms of additional losses and HV stresses are associated with this approach.

So many attempts have been made to modify GaN transistors in such a way as to achieve a positive threshold voltage. The most mature concept uses a layer of p-doped GaN beneath the gate (Figure 1a). This shifts the device's threshold voltage to a positive, although typically relatively low, value (1 to 1.5 V). And, more importantly, this concept only works satisfactorily without an insulating layer under the gate. That means the gate forms a pn-diode with a forward voltage of about 3 V and a resistance of a few Ohms (Figure 1b). And this gate characteristic has significant impact on the driving method of such a transistor.

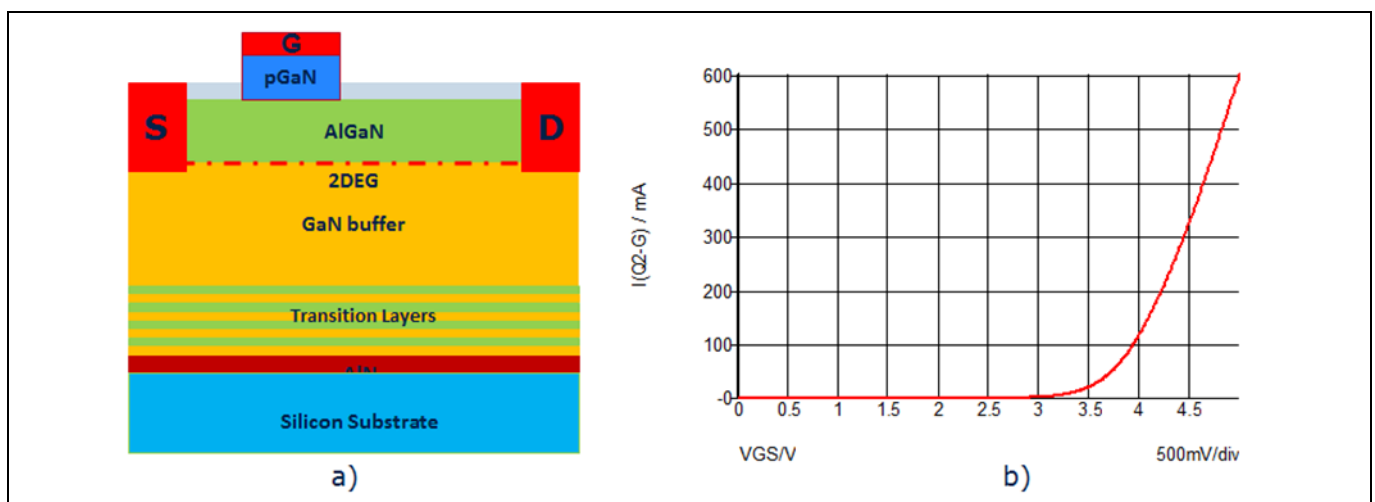


Figure 1 Cross-section (a) and gate characteristics (b) of p-GaN transistor

2 General gate-driving considerations

2.1 Isolated gate (MOSFET)

For a better understanding let's start with a summary of the classic MOSFET gate-driving process. Figure 2a depicts the relevant elements of the equivalent switch and driver circuit. The switch consists of an ideal transistor, i.e. a voltage-controlled current source with the three associated non-linear capacitances C_{GS} , C_{GD} and C_{DS} . In spite of its distributed nature the resistance of the gate electrode is usually modeled by a simple lumped resistor R_{int} . In most applications this approximation is sufficiently accurate.

The driver itself consists of two switches that are utilized to alternately connect the gate to either the positive or the negative driver supply voltage, V_P and V_N , respectively. These voltages are related to the source node of the switch, regardless of whether this is fixed or switching with respect to the system ground. Here the more general case of a bipolar supply voltage is assumed, although often a unipolar voltage V_P is used. As will be explained later, switching dynamics call for a certain minimum resistance in the gate-driving loop, and this is normally realized by adding external gate resistors. If the driver provides separated outputs for the two switches (as the proposed IFX-driver does), these resistors R_{on} and R_{off} can be chosen independently to optimize the switching performance.

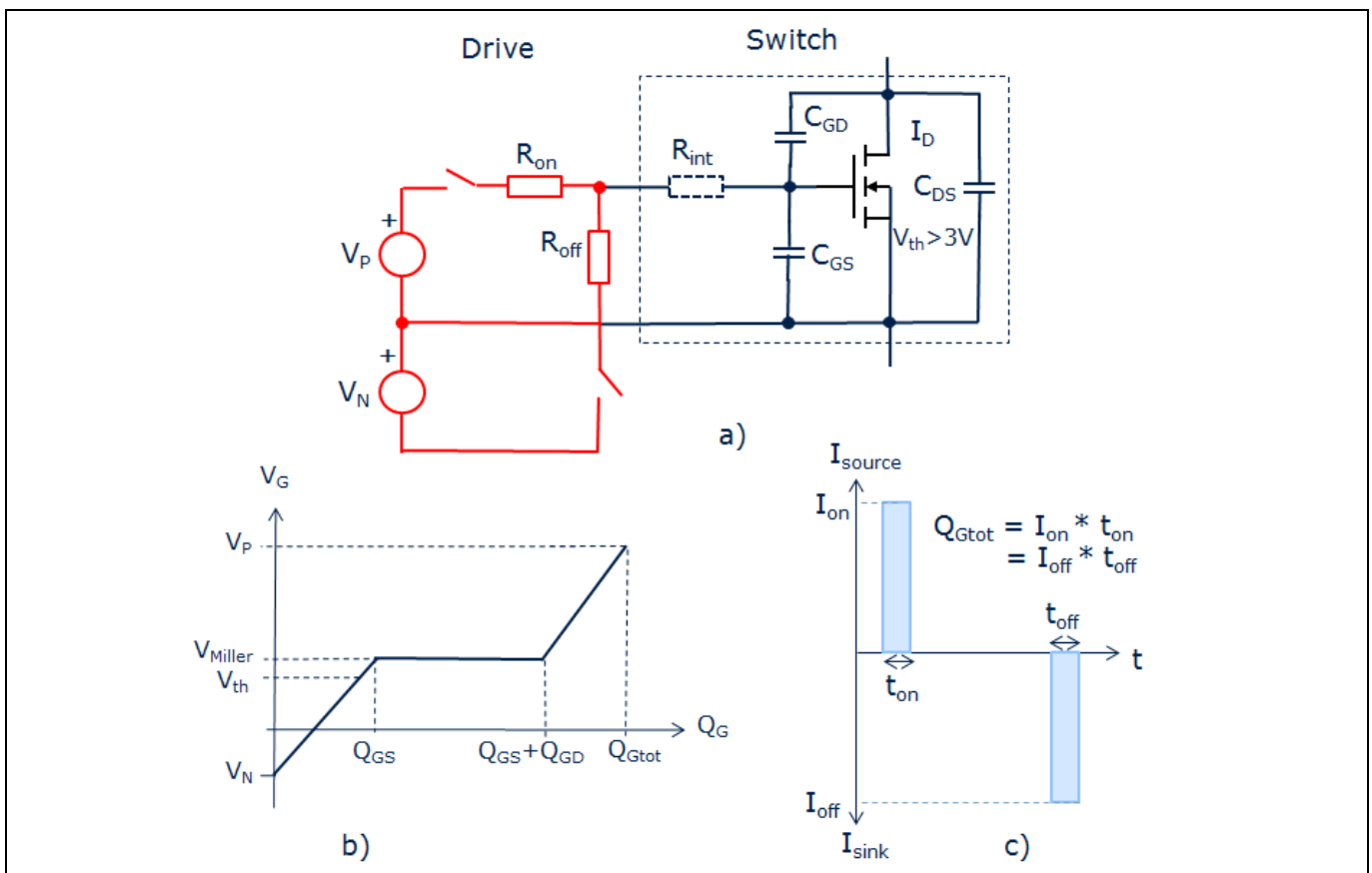


Figure 2 MOSFET: equivalent circuit (a), gate-charge characteristic (b) and gate-charge current (c)

Driving CoolGaN™ 600 V high electron mobility transistors

General gate-driving considerations

The associated gate-charging curve is shown in Figure 2b. During switch-on first C_{GS} has to be charged to the Miller plateau voltage V_{Miller} , i.e. the gate voltage level corresponding to the actual switching current I_D (which can be derived from transfer characteristics). This requires a charge Q_{GS} to be delivered from the driver. Then, to allow a change in drain voltage, C_{GD} has to be charged accordingly, resulting in gate-charge component Q_{GD} . The time needed to provide Q_{GD} via the gate loop limits the achievable switching speed. When the drain voltage does not change any more, the gate is finally charged up to V_S , and the total gate charge reaches its final value Q_{Gtot} .

The resulting gate-drive current over time is given in Figure 2c, and essentially consists of short positive and negative current peaks of area Q_{Gtot} for each switching event. The higher the switching current, the faster the switching transient. The current values are given by

$$I_{on} = \frac{V_P - V_{Miller}}{R_{on} + R_{int}} \quad (1)$$

for switching on, and similarly by

$$I_{off} = \frac{V_{Miller} - V_N}{R_{off} + R_{int}} \quad (2)$$

for switching off. As already mentioned, V_N is often zero; this is possible, if a sufficiently high V_{th} ensures a sufficiently high I_{off} .

2.2 Non-isolated gate (p-GaN)

How does our e-mode GaN switch now differ from the described behavior? Clearly the main difference is that physical pn junction diodes are formed between gate and source and also between gate and drain. The forward voltage V_F of these diodes is defined by the physical band structure of GaN and is in the 3 to 3.5 V range. It is evident that V_F always has to be higher than the Miller voltage. This is guaranteed from device physics, although the actual difference $V_F - V_{Miller}$ depends on temperature and current, and is subject to statistical variations. Besides, the achievable GaN threshold voltage is in the 1 V range and thus is significantly lower than a typical MOSFET threshold. So the equivalent circuit of a GaN switch as depicted in Figure 3a is again composed of an ideal MOSFET with low threshold V_{th} , the voltage-dependent non-linear capacitances C_{GS} , C_{GD} and C_{DS} and the internal gate resistor R_{int} . But now two diodes from gate-to-source and gate-to-drain, respectively, have to be added. And it is these diodes that preclude the structure from being driven like a conventional MOSFET.

Looking now at the gate-charge diagram of Figure 3b, the switching process takes place as with a conventional MOSFET. The only difference is that after having gone through the Miller plateau, the gate node is clamped by the diode to a voltage close to the diode threshold V_F . As before, the switching speed depends on the gate current available in the Miller plateau according to eqs (1) and (2), respectively. But now, even when the switching transition is over, a permanent current

$$I_{ss} = \frac{V_P - V_F}{R_{on} + R_{int}} \quad (3)$$

flows into the gate diode during the on-state, with R_{ss} denoting the associated drive impedance. This current causes additional losses and thus has to be kept as small as possible. Figure 3c depicts the gate current

Driving CoolGaN™ 600 V high electron mobility transistors

General gate-driving considerations

waveform. And the rather obvious goal is to provide large peak currents I_{on} and I_{off} at a small steady-state current I_{ss} .

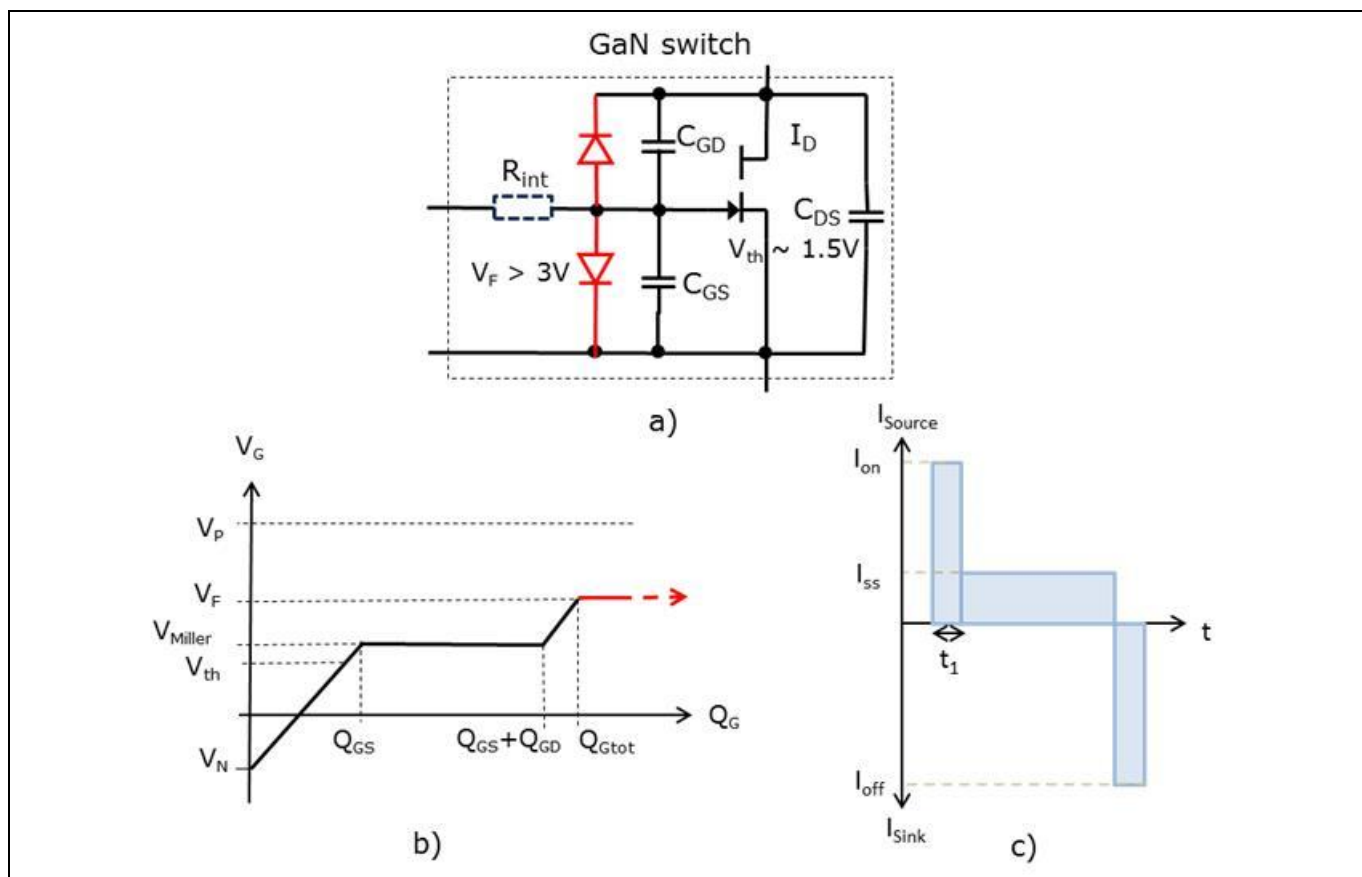


Figure 3 E-mode GaN HEMT: equivalent circuit (a), gate-charge characteristic (b) and gate-charge current (c)

But how can this be achieved?

Let's start with the switch-off process. Here the small V_{th} would only allow a small I_{off} current, if no negative supply voltage is used. This is particularly important in hard-switching half-bridge applications with fast transients of the drain voltage of a transistor in the "off" state. The resulting current through C_{GD} has to be sunk by the driver with V_{GS} staying below V_{th} , otherwise the resulting cross-current flow leads to increased losses ("return-on" effect) and can even be destructive. To avoid this, in hard-switched applications a negative driving voltage V_N of typically a few Volts is required.

For switching on it is evident that the standard driving scheme of Figure 2a cannot do the job. From eqs (1) and (3), a fixed gate-drive impedance ($R_{ss} = R_{on}$) would limit the ratio of I_{on} and I_{ss} to low values, only depending on the difference between V_F and V_{Miller} . In order to achieve a high ratio between I_{on} and I_{ss} , a significant difference in the driving impedance during the off-/on-transient and the steady on-state is required. Theoretically this could be achieved utilizing two different driver stages for transients and steady-state with different impedance and/or supply voltage. However, any solution of this kind means high hardware effort, as dedicated integrated drivers do not exist.

That is why Infineon recommends use of the gate-drive concept depicted in Figure 4. Here the R_{on} of the classic drive concept is substituted by an RC network that provides two parallel paths. A small resistor R_{on} is coupled to the gate via a capacitance C_{on} , while a high resistor R_{ss} provides a direct path. If dimensioned properly, the on-transient current I_{on} is defined by R_{on} , while R_{ss} determines the steady-state diode current.

Driving CoolGaN™ 600 V high electron mobility transistors

General gate-driving considerations

It seems that in Figure 4 the negative supply V_N is missing, but this is not true. In fact, V_N is not needed, as through C_{on} a shift of the gate-drive levels to negative values can be achieved.

Details of how to dimension this network will be given in chapter 4. Prior to this, chapter 3 will summarize the main features of the switch and driver.

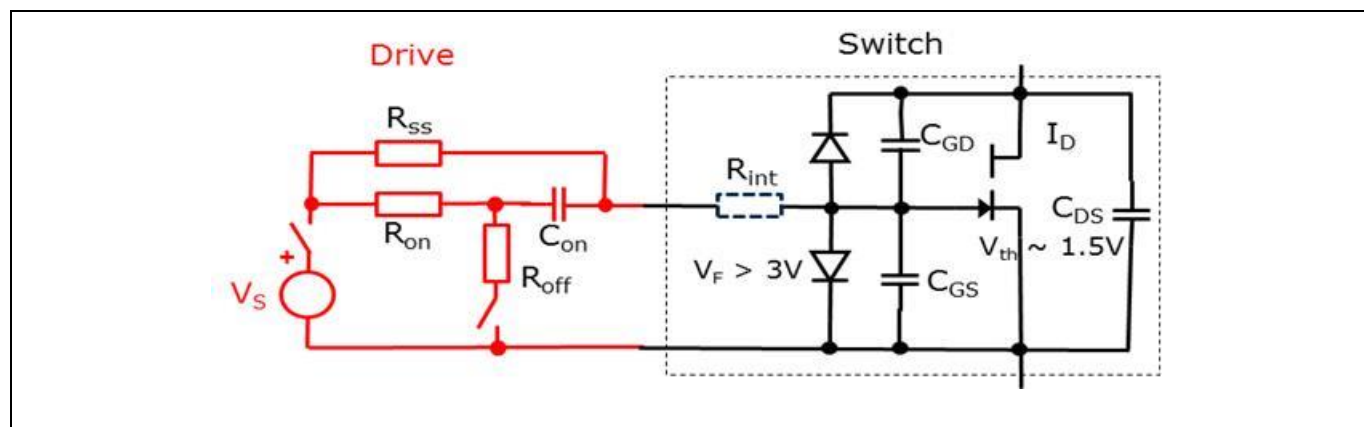


Figure 4 Proposed gate-driving scheme of e-mode GaN HEMT

Driving CoolGaN™ 600 V high electron mobility transistors

Infineon's e-mode GaN solution

3 Infineon's e-mode GaN solution

3.1 GaN HEMT properties

Infineon provides a family of 600 V-rated GaN power switches based on the p-GaN concept. The first family of devices available is IGx60R070D1 with a nominal $R_{DS(on)}$ of 70 mΩ [3]. The most important transistor parameters are summarized in Table 1.

Table 1 Main parameters of 600 V/70 mΩ GaN transistor

IGO60R070D1				
Parameter	Name	Value	Unit	Condition
Operating voltage	V_{DS}	600	V	
On-resistance	$R_{DS(on)}$	70	mΩ	$T = 25^{\circ}\text{C}$
Threshold voltage	V_{th}	1.2	V	$T = 25^{\circ}\text{C}$
Gate charge	$Q_{GS} + Q_{GD}$	2 + 3	nC	$V_{DS} = 400\text{ V}$
Gate diode forward voltage	V_F	3.5	V	$I_{gate} = 20\text{ mA}$
Gate resistance	R_{int}	1	Ω	
Transconductance dI_D/dV_{GS}	g_m	30	A/V	
Output charge	Q_{oss}	45	nC	$V_{DS} = 400\text{ V}$
Energy stored in output capacitance	E_{oss}	7	μJ	$V_{DS} = 400\text{ V}$

As already mentioned, the threshold voltage V_{th} is positive, but it is quite low. This impacts the required gate-drive levels. Besides, all terminal capacitances and the associated stored charges are very low, thus enabling extremely fast switching transients. Figure 5 shows the typical voltage dependence of these capacitances with their highly non-linear nature.

To drive the gate, the input capacitance C_{iss} of several hundred pF has to be charged up to the diode voltage V_F resulting in a gate-charge contribution of around 2 nC. The remaining part of the total gate charge then is due to charging of $C_{GD} = C_{rss}$. Assuming a drain voltage swing of 400 V, integration of the C_{rss} curve over voltage gives an additional 3 nC, resulting in a total gate charge of approximately 5 nC.

The GaN die is packaged into a 20-pin DSO package with an exposed bottom-side/top-side cooling die pad. A separate source pin is utilized as the reference for the gate driver to minimize the critical source inductance [4]. The package combines very low parasitic inductances with an excellent thermal behavior.

All GaN HEMTs data in this document refer to IGOT60R070D1, the DSO-20 CoolGaN™ optimized for bottom-side cooling.

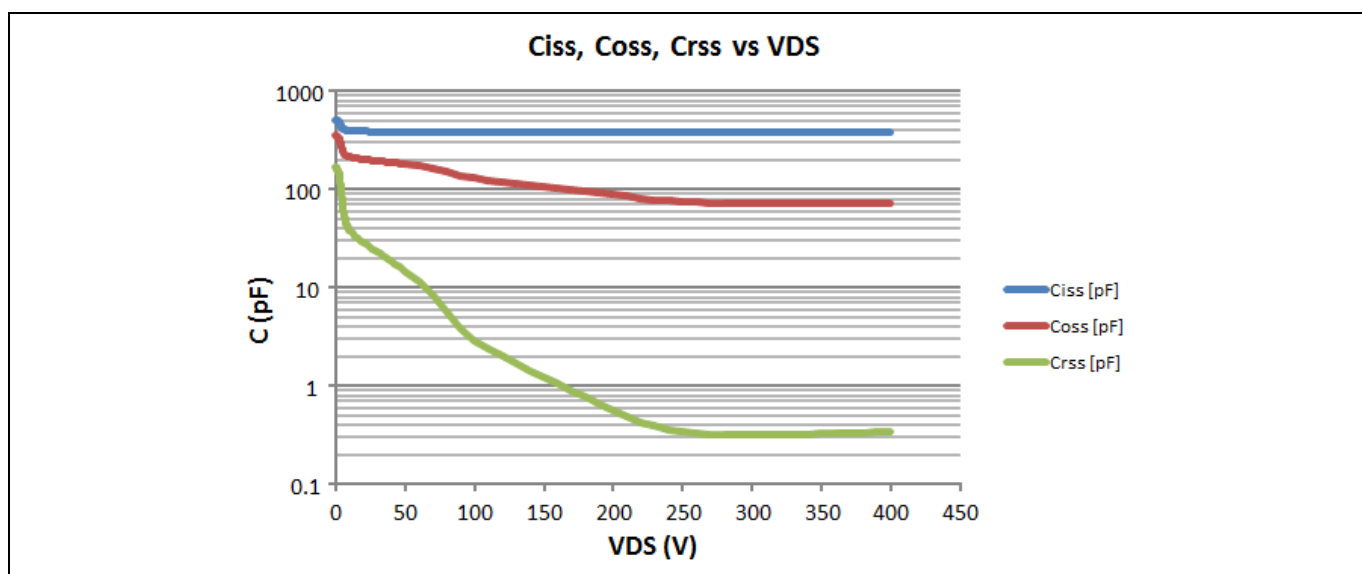


Figure 5 Voltage dependence of terminal capacitances for IGOT60R070D1

3.2 Driver properties

We recommend driving the GaN switches with Infineon's 1EDI20N12AF, an integrated galvanically isolated gate-driver IC in a PG-DSO-8 package. Separated sink-and-source outputs are able to provide driving currents up to 2 A. The driver is a member of Infineon's EiceDRIVER™ Compact family and is particularly well suited to very fast switching, as it realizes the isolation barrier by means of Coreless Transformer Technology (CTT), which among all isolation methods provides the best Common Mode Transient Immunity (CMTI). Table 2 summarizes the key driver parameters [5].

Table 2 Main parameters of 1EDI20N12AF gate driver

1EDI20N12AF				
Parameter	Name	Value	Unit	Comment
Maximum supply voltage	VCC	35	V	
Minimum supply voltage	UVLO	9	V	Under Voltage Lockout (UVLO) function
Input-to-output isolation		+/- 1200	V	
Minimum output current	I _{out}	2	A	
Output impedance	R _{out}	2	Ω	Resistive region of output characteristics
Rise/fall times	t _r /t _f	15	ns	
Propagation delay matching	Δt _d	20	ns	
Common Mode Transient Immunity	CMTI	100	V/ns	

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Infineon's e-mode GaN solution

3.3 Interface circuit

Figure 6 shows the switch, driver and the proposed RC interface together with all relevant parasitic elements.

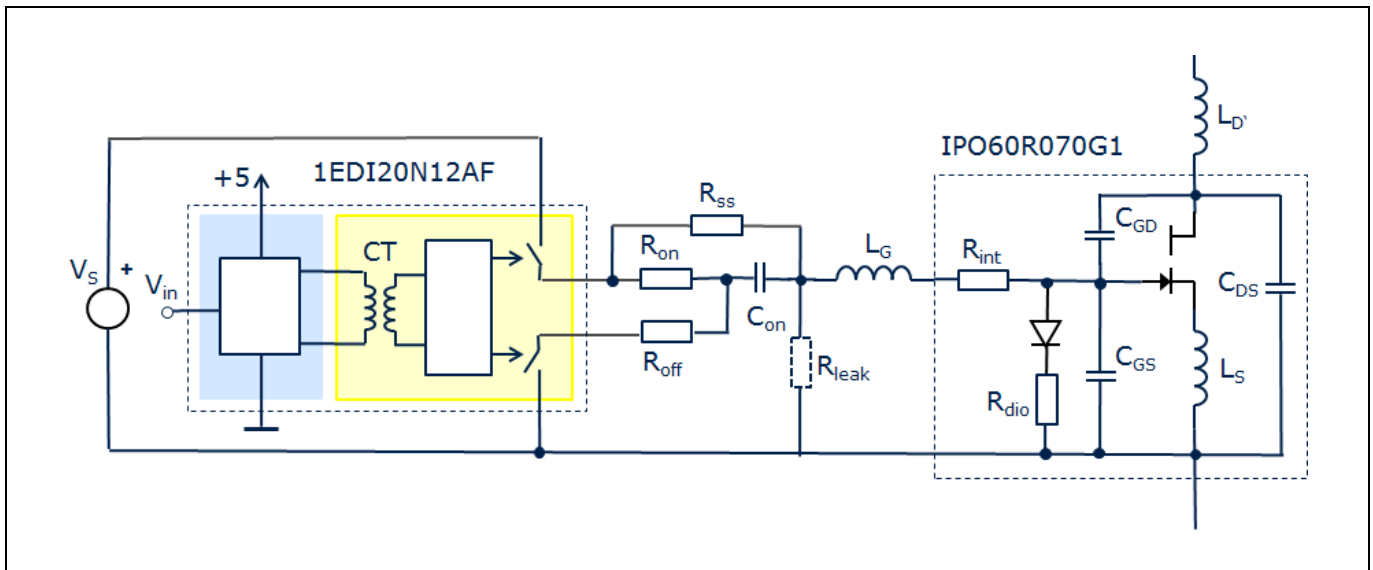


Figure 6 Switch, driver and interface with parasitic elements

As indicated, the driver integrates two dies in a package, coupled by an on-chip transformer CT. The driver outputs can be regarded as switches with a rise and fall time of 15 ns, an on-resistance of 2 Ω and a current limit of 2 A. The detailed behavior of the RC circuit will be described in chapter 4. An optional resistor R_{leak} between gate and source may be used to sink potential leakage currents without turning on the switch even under worst-case static conditions (continuous high drain voltage, high temperature). A resistor value of 5 k Ω is recommended. The equivalent switch circuit has been extended by the diode series resistance R_{dio} and the parasitic inductances. L_S denotes the part of the source inductance within the gate loop only. Due to the source sense concept this critical parasitic can be kept negligibly small. The remaining part of L_S can be lumped with the drain inductance to form the effective drain inductance $L_{D'}$. Finally also the gate loop inductance L_G influences gate-drive dynamics.

Typical values for these parasitics are:

- $R_{dio} = 2 \Omega$
- $L_S < 0.1 \text{ nH}$
- $L_D = 3 \text{ nH}$
- $L_G = 10 \text{ nH}$

The inductance values are lower than expected, but they could be practically achieved by combining a highly optimized PCB layout with inductance canceling techniques in the power loop [6].

4 Dimensioning of the RC interface

4.1 Basic relations

In order to understand how the proposed interface works, it is helpful to have a closer look at the simple circuit given in Figure 7. Here the transistor is substituted by a constant capacitance C_G of 2 nF in parallel with an ideal diode with a forward voltage of 3.5 V and a series resistance R_{dio} of 3 Ω . A voltage source switching between zero and V_S is connected via a coupling capacitance C_{on} of 2 nF and a small series resistor R_{on} of 10 Ω as the low-impedance AC-path. The parallel DC path is formed by a 500 Ω resistor. For simplicity, the driving voltage is assumed to behave like a step function.

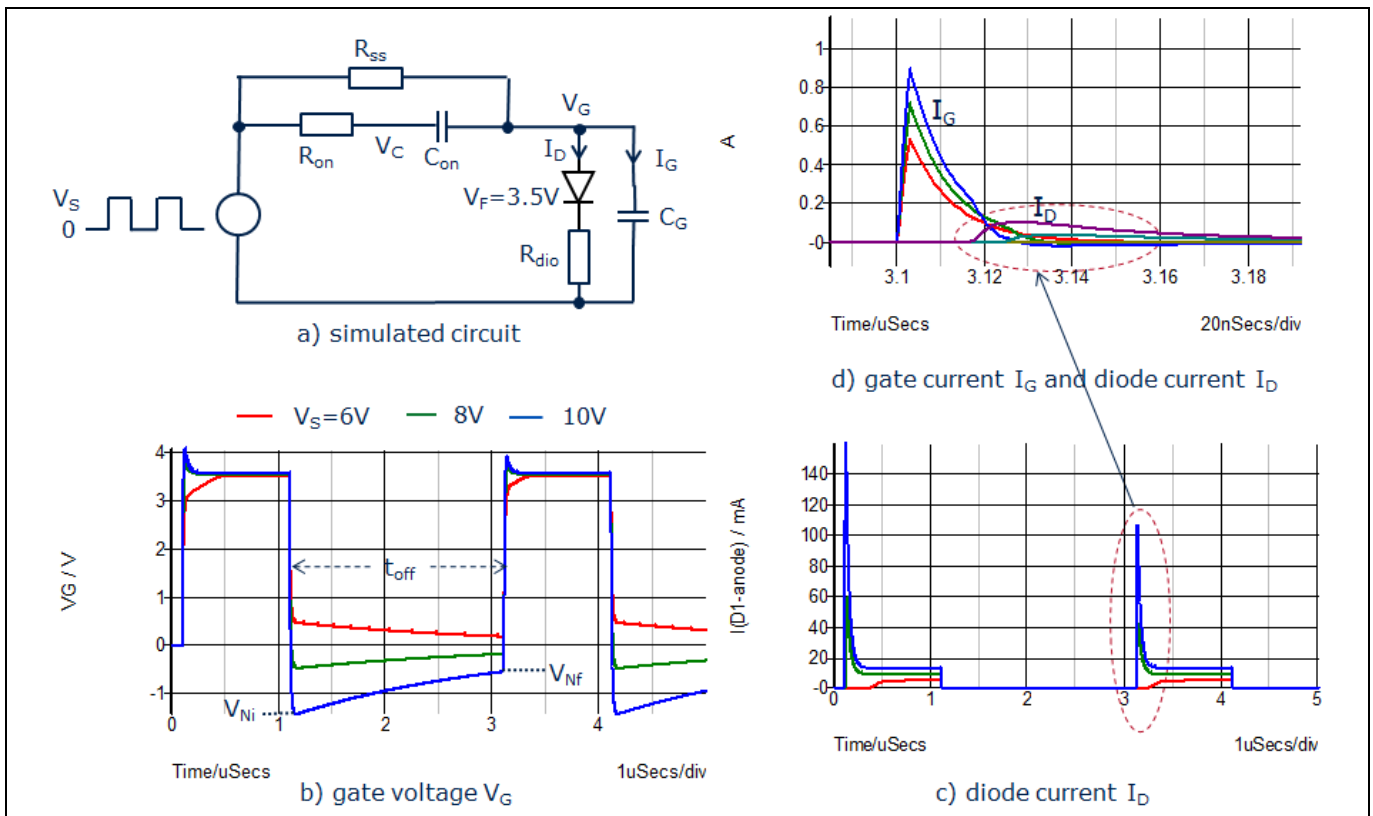


Figure 7 Simulation results of simplified gate-charge circuit (a) with gate voltage (b), diode current (c) and gate current (d)

Before the first switching event both C_G and C_{on} are uncharged. With the driving voltage transition from zero to the “on” level V_S , both capacitances are charged until V_G reaches 3.5 V at a charging current:

$$I_G(t) = \frac{V_S - V_C(t)}{R_{on}} \quad (4)$$

As long as no diode current is flowing, the charge in C_G equals the charge in C_{on} :

$$(V_C - V_G) \cdot C_{on} = V_G \cdot C_G$$

$$V_C = V_G \cdot \left(1 + \frac{C_G}{C_{on}}\right) \quad (5)$$

Driving CoolGaN™ 600 V high electron mobility transistors

Dimensioning of the RC interface

Here, as an example, C_{on} has been chosen equal to C_G . Then $V_C = 2 \cdot V_G$ for V less than V_F . As soon as the diode starts conducting, V_G is clamped to a value close to 3.5 V, corresponding to a V_C of 7 V. If V_S exceeds this value, C_{on} is further charged until V_C reaches V_S . The final charge in C_{on} is thus larger than that in C_G by an amount of $(V_S - 7 \text{ V}) \cdot C_{on}$. If, on the other hand, V_S is not sufficiently large (here V_S is less than 7 V), then V_G is charged to a level below V_G via the capacitive path, while the remaining gate charge is provided by the resistor R_{ss} .

This behavior is illustrated in Figure 7b. Looking at the first switch-on event, obviously $V_S = 6 \text{ V}$ is too low to fully charge C_G via the fast path. As expected, V_G goes up to 3 V, and is then slowly charged to 3.5 V via the 500 Ω resistor. If V_S is higher than 7 V, charging of C_G to V_F is fast and there is no significant difference in the gate voltage behavior at a V_S of 8 and 10 V, respectively. In general, the steady on-state is characterized by:

$$V_G = V_F \rightarrow Q(C_G) = V_F \cdot C_G \quad (6)$$

$$V_C = V_S \rightarrow Q(C_{on}) = (V_S - V_F) \cdot C_{on} \quad (7)$$

$$I_{ss} = \frac{V_S - V_F}{R_{ss}} \quad (8)$$

If the driving voltage is now switching back to zero (switch-off, assuming $t = 0$), the difference in gate voltage behavior is evident. With 0 V applied externally, fast balancing of the charges in C_G and C_{on} via R_{on} takes place, causing a gate voltage:

$$V_G(0) = - \frac{Q(C_{on}) - Q(C_G)}{C_{on} + C_G} \quad (9)$$

If $Q(C_{on})$ is smaller than $Q(C_G)$, the charge difference causes a positive gate voltage at the begin of the off phase (red curve in Figure 7b) that is discharged slowly via R_{ss} . Due to the low threshold voltage of GaN such a situation is unacceptable and thus $Q(C_{on})$ greater than $Q(C_G)$ is a mandatory condition to safely turn off the transistor.

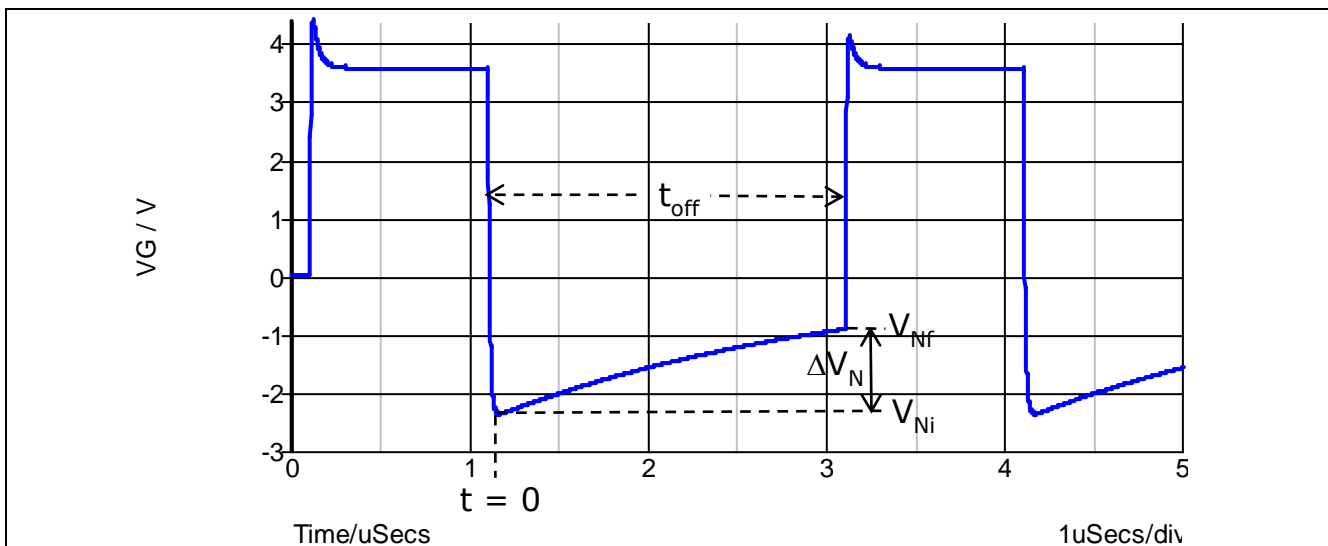


Figure 8 Gate-voltage waveform for $V_S = 12 \text{ V}$

Figure 8 shows the gate voltage behavior of Figure 7a once more with $V_S = 12 \text{ V}$. The charge difference in C_{on} and C_G causes V_G to go negative. The initial negative voltage V_{Ni} can be calculated by inserting eqs (6) and (7) into (9) to yield:

$$V_G(0) = V_{Ni} = V_F - V_S \cdot \frac{C_{on}}{C_{on} + C_G} \quad (10)$$

Driving CoolGaN™ 600 V high electron mobility transistors

Dimensioning of the RC interface

This initial value V_{Ni} decreases with a time constant:

$$\tau = R_{SS} \cdot (C_{on} + C_G) \quad (11)$$

At the end of the off-phase ($t = t_{off}$) the final value V_{Nf} is reached:

$$V_G(t_{off}) = V_{Nf} = V_{Ni} \cdot e^{-t_{off}/\tau} \quad (12)$$

Thus during the off-phase C_{on} is discharged by an amount:

$$\Delta V_N = V_{Nf} - V_{Ni} = -V_{Ni} \cdot (e^{-t_{off}/\tau} - 1) \quad (13)$$

The next switching-on event thus starts at the negative gate voltage value V_{Nf} . Due to this pre-charging, the extra charge required to fully charge C_{on} after V_G has reached V_F is now smaller. This can be seen in the diode current I_D given in Figure 7c, which is lower for the second switching pulse than for the first one. Note also that the gate voltage peak visible at switch-on is no more than the voltage drop I_D causes over the diode's on-resistance R_{dio} . From Figure 7c it is also clear that no diode current is flowing during the switching transient, if V_S is too small (red curve). In any case I_D slowly approaches the steady-state value of eq. (8).

But also the gate-charging current I_G , as shown in Figure 7d at a higher time resolution, depends on V_{Nf} of the previous off phase. Due to the remaining charge in C_{on} , V_C during the charging phase (V_G is less than V_F) is now increased by $-V_{Nf}$ and eq. (5) has to be modified to:

$$V_C(t) = V_G(t) \cdot \left(1 + \frac{C_G}{C_{on}}\right) - V_{Nf} \quad (14)$$

According to eq. (4) this also means a reduction of the gate-charging current I_G compared with the initial switching with discharged C_G . From eq. (12), this effect varies with t_{off} . At start-up or with very long t_{off} , C_{on} gets completely discharged ($V_{Nf} = 0$), while for short t_{off} $V_{Nf} \sim V_{Ni}$ and the gate-charging current is smallest. This leads to a variation of switching behavior with duty cycle. To keep this variation small, the minimum necessary V_{Ni} should be chosen (see section 5.1).

4.2 Driving real GaN transistor gates

Essentially the considerations given above also hold, if we are not driving a constant capacitance by an ideal step-voltage source, but a real switching transistor by a real gate driver. First, the driving voltage is no step function, but has finite rise and fall times. This effect can partly compensate the duty-cycle dependence of the driving current, as will be shown in section 5.1.4. Second, the Q_G vs V_G characteristic changes from a straight line for a constant capacitance to the well-known step-charging curve as given in Figure 2b. The Miller plateau indicates the charge in C_{GD} associated with the voltage swing at the drain; in this region the gate behaves like a huge capacitance, whereas below and above the Miller level it shows the physical capacitance as depicted in Figure 5.

The total gate charge Q_{Gtot} denotes the charge required to change V_{GS} from 0 to V_F . For a given transistor and switching voltage this value is fixed and close to the specified gate charge of 7 nC for the switch described in 3.1 (as charging from Miller level to V_F only gives a small contribution). V_{Ni} can again be calculated by the charge redistribution relation of eq. (9). However, in contrast to the constant capacitance case, C_G is now the physical capacitance, i.e. $C_G = C_{iss}$, while $Q(C_G)$ is the total gate charge Q_{Gtot} . Eq. (10) thus becomes:

$$V_{Ni} = -\frac{C_{on} \cdot (V_S - V_F) - Q_{Gtot}}{C_{on} + C_{iss}} \quad (15)$$

The optimum value of V_{Ni} depends on application, but once a target value is defined, eq. (15) can be used to find possible combinations of V_S and C_{on} with a trade-off between faster switching and higher steady-state current

Driving CoolGaN™ 600 V high electron mobility transistors

Dimensioning of the RC interface

as described by eqs (4), (8), (11), (12) and (14). Figure 9 gives a graphical representation of eq. (15), assuming a total gate charge of 5 nC.

Regarding the time constant for discharging, again C_G of eq. (11) has to be substituted by the actual gate capacitance, thus:

$$\tau = R_{ss} \cdot (C_{on} + C_{iss})$$

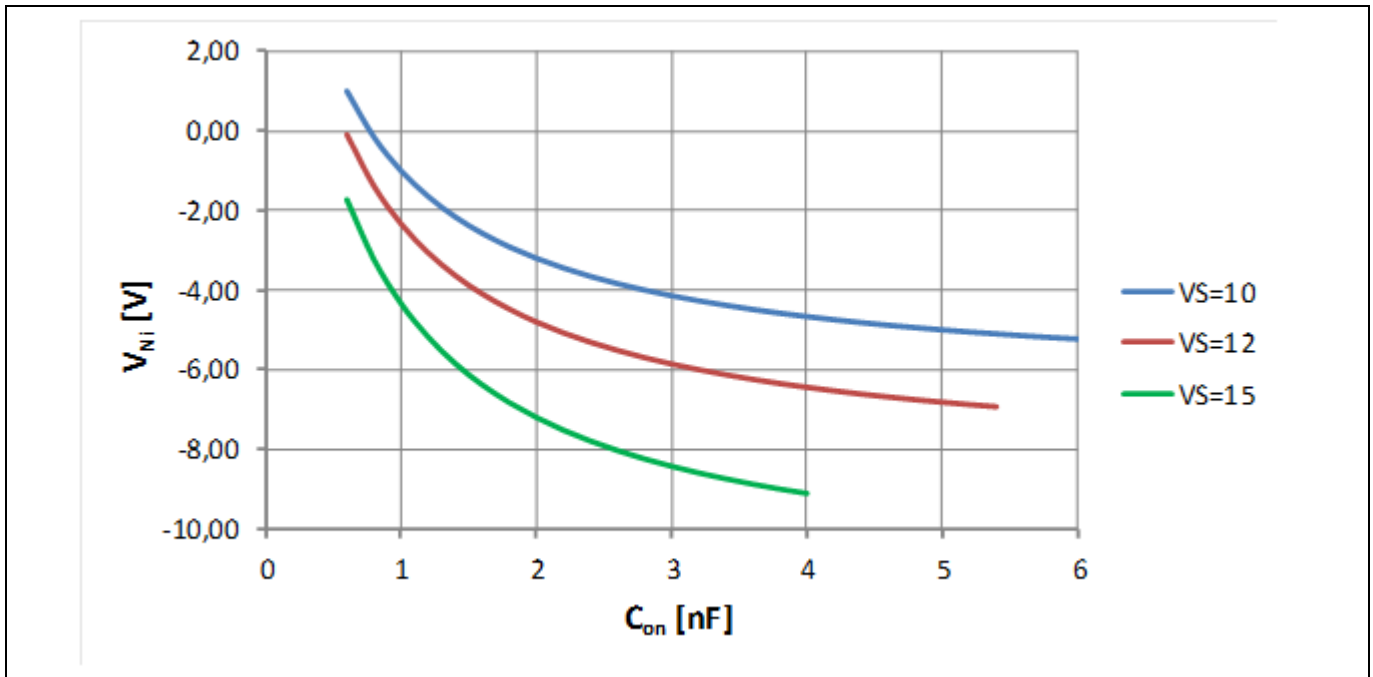


Figure 9 V_{Ni} as a function of C_{on} and V_S according to eq. (15)

Besides the strongly non-linear behavior of real transistor capacitances, further differences exist between the simplified circuit of Figure 7a and the more realistic one in Figure 6. It is easy to discern that these are the parasitic inductances. It is not so easy to identify all the effects they are responsible for. And it is very difficult to quantify these effects.

There are certainly two well-known effects that strongly influence gate drive. Both result in minimum values for R_{on} .

1. From Figure 6, the gate loop is essentially an LC circuit formed by the parasitic gate inductance L_G and the series connection of C_{GS} and C_{on} . To avoid oscillations in this loop, a sufficiently high damping resistance R is needed. From simple oscillator theory the aperiodic case (no overshoot) requires a minimum resistance:

$$R = 2 \cdot \sqrt{L/C}$$

Although our loop is non-linear and more complex, this can be used for rough estimations. From Figure 5 we know that the gate capacitance is in the 0.5 to 1 nF range. A realistic gate loop inductance ranges from 10 to 20 nH, which yields a damping resistance range of roughly 6 to 12 Ω . This is the total loop resistance including the driver resistance of approximately 2 Ω and the internal gate resistance R_{int} . Although the static R_{int} is typically small ($\sim 1 \Omega$), the distributed nature of R_{int} limits the validity of the simple model. Anyhow, in most applications a small external gate resistor in the 5 to 10 Ω range should help to avoid unwanted oscillations.

2. Yet there is another effect setting limits to the switching speed. This is caused by the inductances in the power loop (in Figure 6 lumped in L_D). Fast switching transients typically happen in only a few ns. The

Driving CoolGaN™ 600 V high electron mobility transistors

Dimensioning of the RC interface

associated di/dt values can reach some tens of Amps per ns with an associated high voltage drop across the power-loop inductance. This voltage is subtracted from the drain-to-source voltage for rising current, but added for falling currents. Thus particular care has to be taken that the voltage limitation for the GaN switch is not exceeded. This may require reducing switching speed, i.e. increasing R_{on} , as typically the highest di/dt values are seen at switch-on leading to voltage stress for the diode part in a half-bridge configuration.

5 Application-specific considerations

With the theoretical background given in the previous chapter we are now able to dimension the proposed gate-drive network in a reasonable manner. As requirements and properties may vary widely, examples covering the most important and also the most promising applications for GaN switches shall be given in the following.

5.1 Hard-switched applications (totem-pole PFC)

5.1.1 Totem-pole PFC topology

The most significant advantage of a GaN HEMT is not the small area and capacitance, but the lack of a body diode. This simply means that a GaN transistor can be operated not only as a switch, but also as a diode, i.e. with negative polarity of V_{DS} . This is not valid for MOSFETs due to the slow physical pn diode between source and drain. And it is essentially this feature of GaN that causes the decisive benefits.

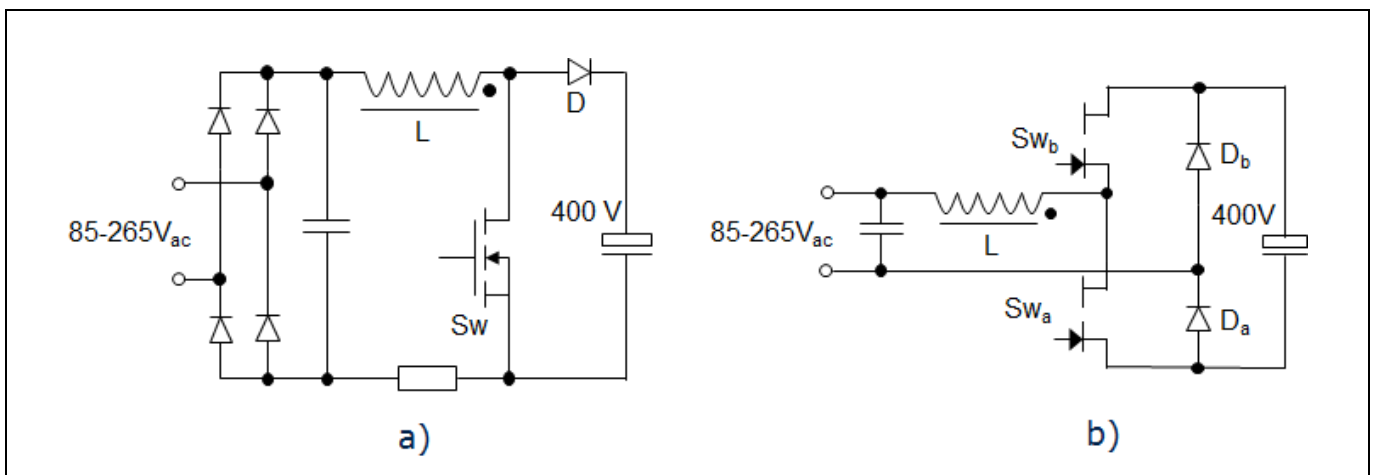


Figure 10 Classic (a) and totem-pole PFC (b)

Figure 10 a shows a classical Power Factor Correction (PFC) stage. The AC input voltage is rectified and boosted to 400 V. As usual, the boost converter consists of switch Sw, inductance L and diode D. The (continuous) current in L is switched between Sw and D at a frequency in the 100 kHz range. During the transients the switch sees both high voltage and high current, resulting in high switching power. Thus in such a “hard-switched” case the transient should be as short as possible.

If the diode could be substituted by a transistor, the so called totem-pole topology of Figure 10 b is made possible to fulfill the same function. The main idea behind this is that, if both transistors Sw_a and Sw_b can take over both switch and diode function, a diode bridge for rectification is not needed any more; it can be substituted by the two diodes D_a and D_b in Figure 10 b. During the positive half-wave of the input voltage, Sw_a is the active switch, while Sw_b takes over the diode functionality. The return path is formed by diode D_a. In the negative half-wave Sw_a and Sw_b interchange their function and the current flows via D_b. As D_a and D_b change their state at a very low rate (with the mains polarity change), they can also easily be substituted by standard MOSFETs operating as synchronous rectifiers. Thus in the totem-pole topology the losses caused by the input rectifier are reduced significantly.

5.1.2 GaN transistor in reverse conduction (diode)

Figure 1a shows a GaN transistor as quite a simple lateral device. Functionally it is symmetrical with respect to source and drain, i.e. it operates in basically the same way for positive and negative voltage between drain and source. However, as the distance between gate and drain is larger than between gate and source, slight differences in electrical parameters between normal and reverse mode can be observed. The reverse behavior of a GaN transistor is in clear contrast to a normal MOSFET with its inherent body diode, and results in an electrical behavior as shown in Figure 11.

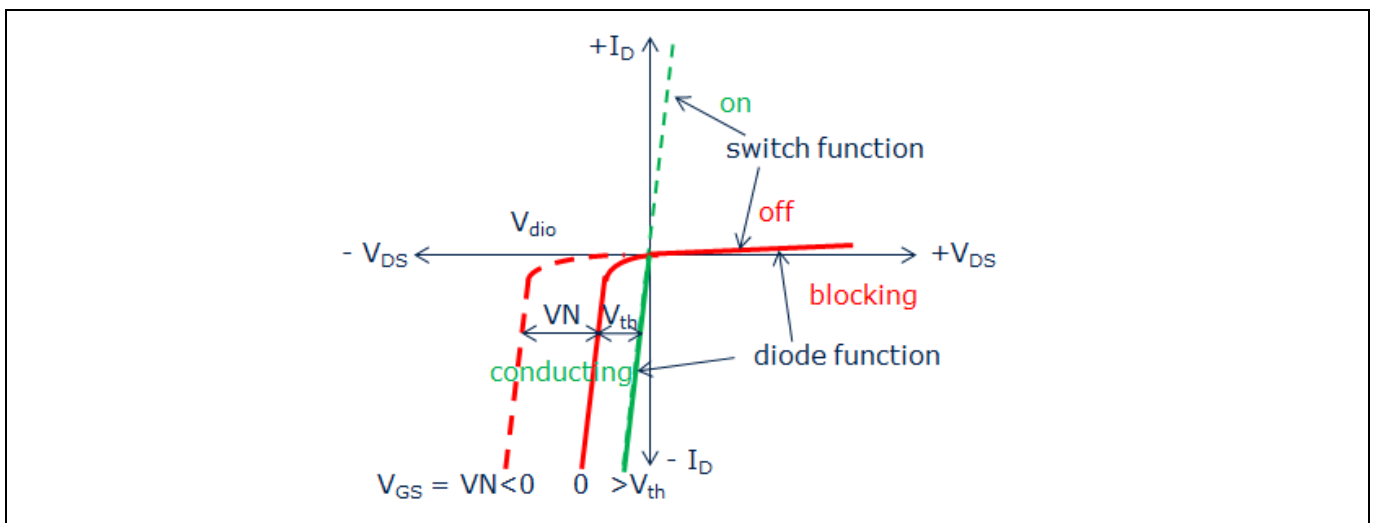


Figure 11 Basic electrical characteristics of GaN transistor in normal (switch) and reverse (diode) operation

Basically a switch is operated in the first quadrant of V_{DS} and I_D only. It is either on or off (low or high impedance). A diode, however, always has to block voltage in one polarity and has to conduct in the other. An ideal diode behavior is thus characterized by the red branch in the first quadrant and the low-impedance green branch in the third. This corresponds to a switched-on transistor (V_{GS} is greater than V_{th}), whereas a real diode follows the solid red curve, i.e. it exhibits a higher voltage drop due to its threshold voltage. This basic advantage of a transistor switch compared with a diode is often utilized in power circuits (synchronous rectification).

However, such a “diode” transistor must never be switched on when the associated active switch is on to avoid high and potentially destructive shoot-through current. As a consequence, a certain time delay between the “switch off” and “diode on” transitions is required. During this time, often called dead-time t_d , the gate of the diode transistor is maintaining its off level. This causes increased voltage drop in reverse operation (V_{DS} is less than 0), as shown by the red curves in Figure 11.

The reason is simple. A transistor always conducts if the gate exceeds the threshold V_{th} with respect to the more negative of the source and drain electrode, respectively. In normal operation this means V_{GS} greater than V_{th} , in reverse operation V_{GD} greater than V_{th} . As V_{GS} greater than V_{th} obviously causes V_{GD} greater than V_{th} for V_{SD} greater than 0, a transistor in the on-state remains on also in reverse direction. This is reflected in the symmetrical characteristic in Figure 11 (green line). With $V_{GS} = 0$, apparently in normal operation the transistor is off. In the reverse direction, it starts conducting, if V_{SD} exceeds V_{th} , as then $V_{GD} = V_{GS} + V_{SD}$ greater than V_{th} (solid red line). Similarly, if V_{GS} in the off-state is the negative voltage V_N , V_{SD} has to exceed $V_{th} - V_N$ to start conduction. The characteristic is thus further shifted to the left by an amount of V_N (dashed red line).

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Application-specific considerations

This means that a GaN transistor exhibits a diode-like behavior in the reverse direction, when it is in the off-state. The associated diode voltage drop V_{dio} is determined by the difference of transistor threshold and off-state gate voltage level:

$$V_{dio} = V_{th} - V_{GS,off}$$

Thus, if a negative voltage V_N is applied at the gate to switch a GaN transistor off, it is still able to conduct in the reverse direction, but the voltage drop will increase by V_N . This is not a GaN-specific behavior, as any lateral symmetric transistor would behave similarly.

5.1.3 Particular effects in hard-switched topologies

As explained, hard-switching calls for fast transients. If in Figure 10b switch Sw_a is switched on, the switching node swings from 400 V to 0 at a very steep slope that might exceed 200 V/ns. Clearly the passive switch Sw_b then has to be kept off during this transient, otherwise cross-conduction and high losses would result. A falling switching node is equivalent to a fast rising drain node of Sw_b . From Figure 6, a rising drain leads to current into C_{GD} , which has to be sunk by the gate driver. If the voltage drop between gate and source exceeds V_{th} , the transistor turns on, thereby increasing switching current and losses. This effect is often called “re-turn-on”. It can be minimized by a low driving impedance and, more efficiently, by a low driving voltage level in the off-state.

Obviously, e-mode GaN HEMTs are particularly sensitive to re-turn-on due to their low threshold voltage. And this is why the shift to a negative off voltage, resulting from the proposed gate drive, is highly valuable in hard-switching. It is the initial negative voltage V_{Ni} , as discussed in section 4.1, that appears at the gate of the passive transistor (diode) and helps to avoid re-turn-on during the switching transient.

A further effect of hard-switching is voltage overshoot. The worst situation happens at the passive transistor (“diode”) during the falling edge of the switched current. It must therefore be ensured that even in the worst case with $V_{Nf} = 0$ at the switch (fastest switching) the voltage ratings are not exceeded. Besides, situations with both transistors in the off-state for extended periods require careful consideration, as a switch-on event with $V_N = 0$ at the diode leads to a significant re-turn-on. As such situations only happen at low rates, if at all, the resulting high switching loss is of minor importance; however, the increased current may lead to higher voltage overshoot, although strong re-turn-on also has a damping effect on over-voltage. Anyway, the situation can be avoided, if after long off-times for both switches the diode is always the first to be switched on.

5.1.4 Example totem-pole PFC

Now a concrete example for dimensioning the gate-drive network can be given. The totem-pole PFC of Figure 10b shall be switched at 100 kHz with operating current levels going up to 10 A (the maximum current to be handled is 30 A, but only for several tenths of a ms. Dead-times are assumed to be two times 100 ns per switching period of 10 μ s. Both switches Sw_a and Sw_b consist of the elements shown in Figure 6.

Switching simulations as well as measurements indicate that a V_{Ni} of a few Volts is required to minimize re-turn-on. On the other hand, during the dead-time the inductor current is flowing over a diode with negative gate voltage V_{Ni} (before “switch on”) and V_{Nf} (before “diode on”), respectively, causing additional losses by the increased voltage drop. From these considerations the best strategy is to minimize V_{Ni} and maximize ΔV_N .

Simulations have been carried out according to the schematic given in Figure 12. As a reference $C_{on} = 2$ nF and $V_S = 12$ V have been chosen to yield a V_{Ni} of about -4 V (see Figure 9). From switching simulations, a total gate resistor of 10 Ω seems adequate to limit the drain and gate voltage overshoots to safe values (with 6 nH of total power-loop and 10nH of gate-loop inductance). Taking into account driver and intrinsic gate resistance, 5 Ω for R_{on} and R_{off} are the initial choice. An R_{ss} of 1 k Ω leads to a discharge time constant τ of 2 μ s. This is a reasonable

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Application-specific considerations

value, as at 100 kHz the total switching period is 10 μ s; so even for short off-times some discharge occurs (duty cycles are typically restricted to a minimum of 0.1).

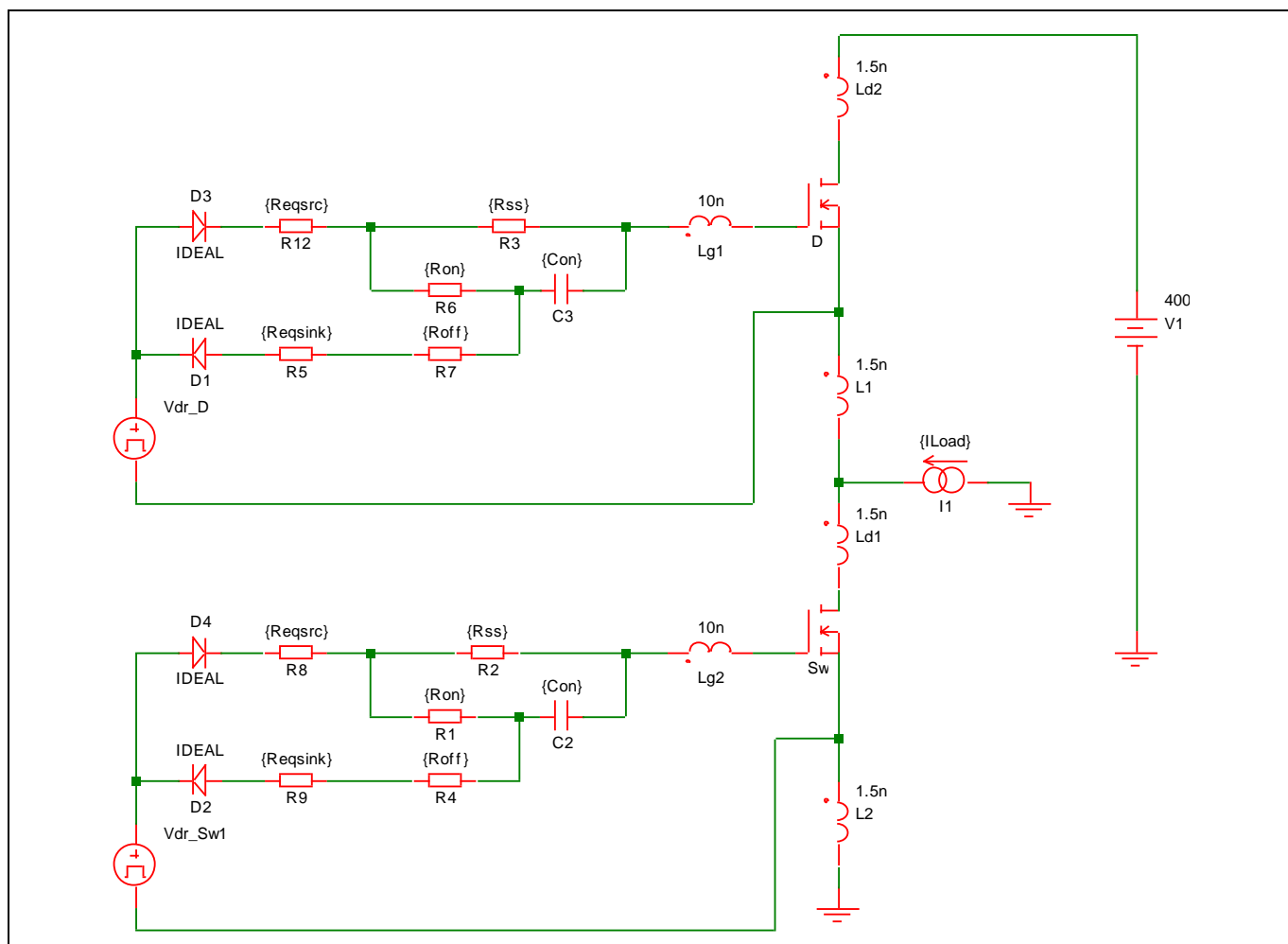


Figure 12 Simulation circuit for totem-pole PFC stage

The simulated waveforms of switching currents and voltages are depicted in Figure 13. Obviously before first switch-on (“on1”), C_{on} of switch Sw is completely discharged. The diode transistor D is switched from the on- to the off-state, resulting in a negative voltage V_{Ni_D} at its gate. Current I_{Load} (10 A) is still flowing through the “diode”, causing a relatively high voltage drop of about 8 V that can even be seen as a small step in V_{DS} (graph d). After a dead-time of 100 ns Sw is switched and causes the associated switching node transients. Charging of the output capacitances by the switch current peak seen in graph c is mainly responsible for the switching losses. 1 μ s after “on1” Sw is switched off and I_{Load} causes the switching node to go up. After a short off-state of only 0.5 μ s the second switch-on event “on2” takes place. As C_{on} is now still charged, the gate voltage does not start at zero, but at approximately -4 V. From the previous considerations, we would expect a significantly slower transient due to a reduced gate-charge current, as can be seen in Figure 13 b. However, this seems not to be reflected in the transients of Figures 13 c and d.

Even at a significantly higher time resolution (Figure 14) the two switching transients look rather similar in spite of the obvious differences in the respective gate voltage and current waveforms. The reason is the limited rise time of the driving voltage that definitely cannot be considered as a step function. Thus, when the gate voltage of Sw is at the Miller plateau, the driving voltage V_{dr_Sw} has not reached its final value for the “on1” transient (left graph of Figure 14 a). “On2” starts from a negative V_{GS} , thus the time required to reach the Miller plateau increases. This leads to a higher V_{dr_Sw} in the transient phase (right graph of Figure 14 a) thereby partly

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Application-specific considerations

compensating for the effect of the pre-charged C_{on} . As a result the switching waveforms of Figure 14 c and d look rather similar, with a slightly slower “on2” transient. We also will see that the impact of the duty cycle on switching losses is less severe than expected.

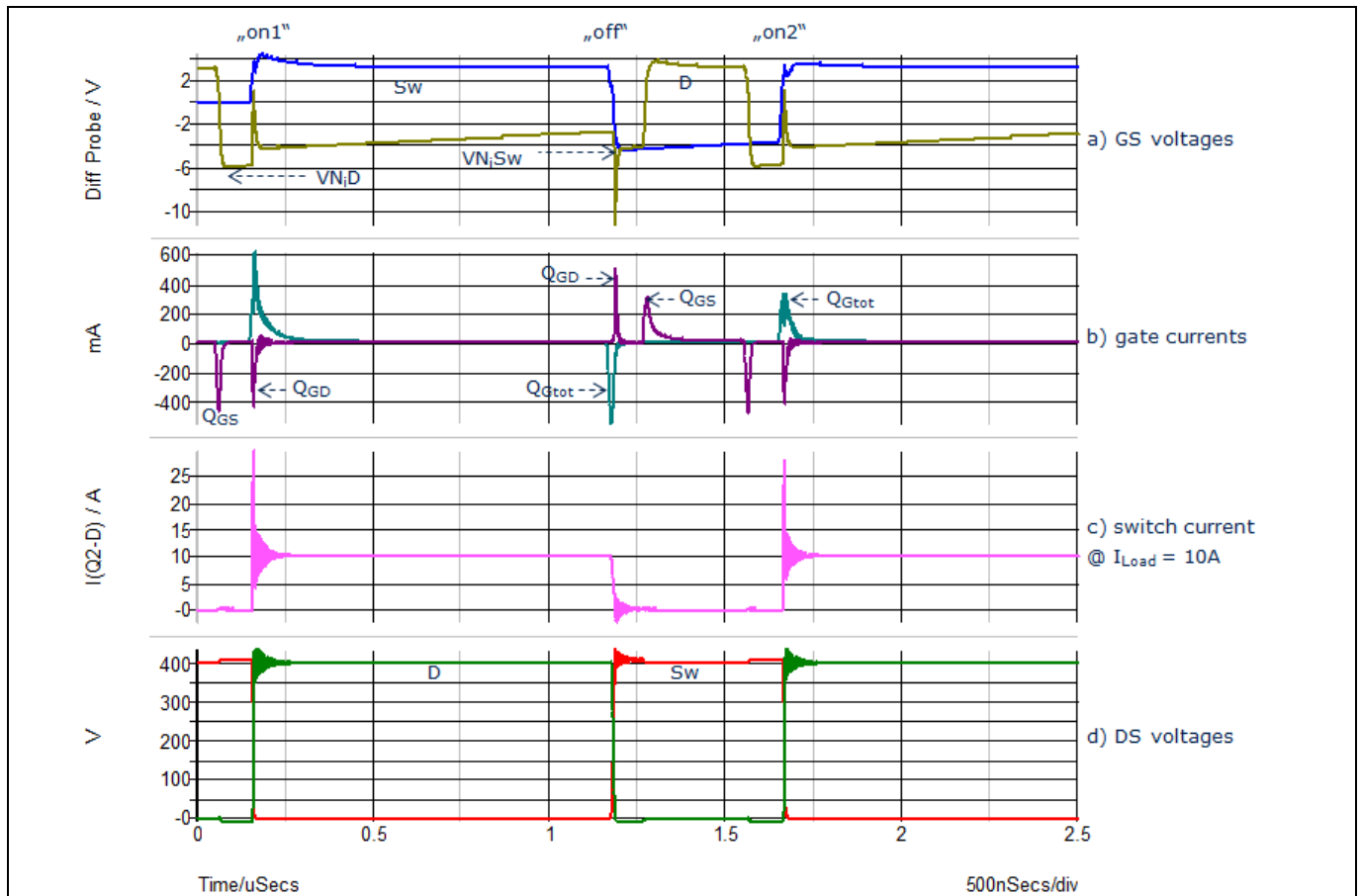


Figure 13 Simulated waveforms of PFC stage: gate-to-source voltages (a), gate currents (b), switch drain current (c) and drain-to-source voltages (d)

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Application-specific considerations

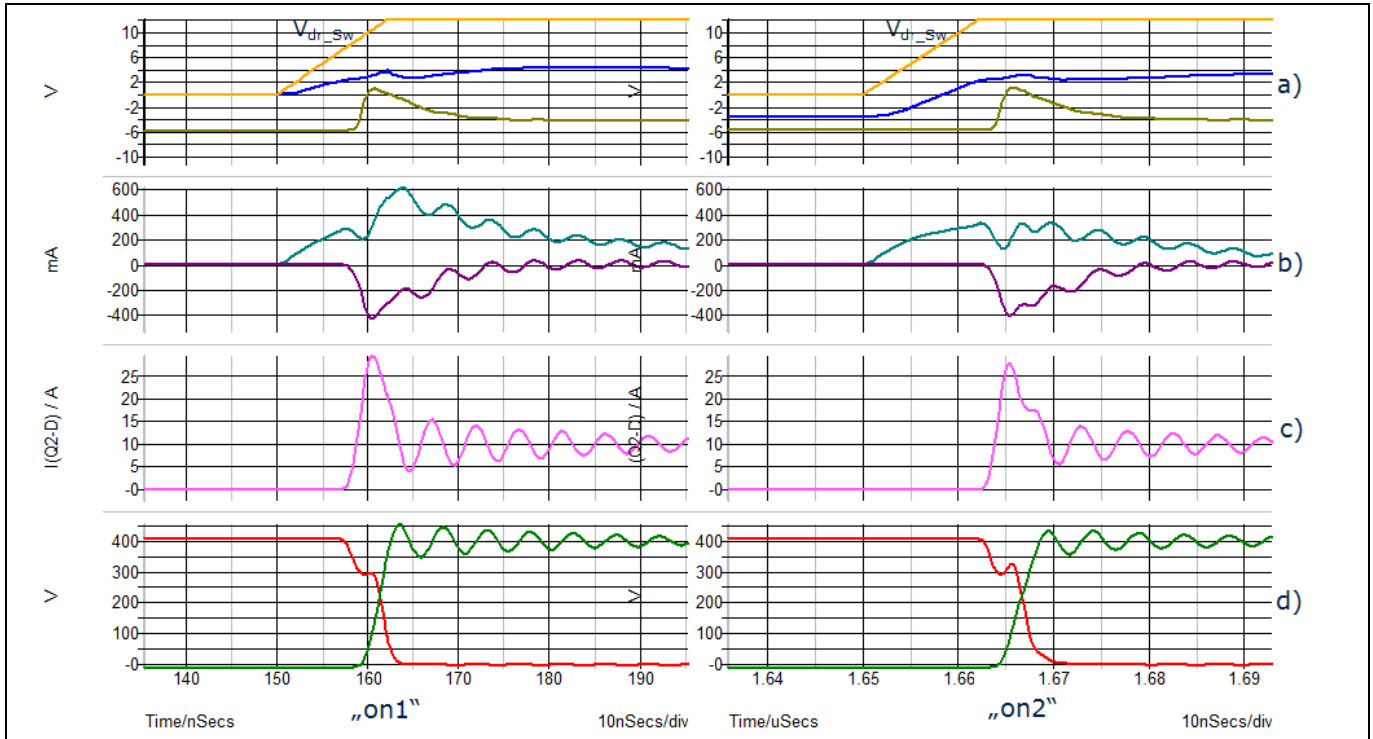


Figure 14 Details of “on1” and “on2” transients of Figure 13

The waveforms of Figure 13 deserve an even closer look. As can be seen, the gate current stays at a relatively low level of several hundred mA. Due to the very small capacitances this is sufficient to achieve the fast transients of Figure 14 with voltage slew rates close to 200 V/ns. Of course the question arises of whether a higher gate-charging current would make sense. From our perspective it would not, as an increase in switching speed means higher peak current, thus higher di/dt and higher voltage peaks compared to those observed in Figure 14c. And it should be pointed out that the assumed power-loop inductance value of only 6 nH is not easy to achieve. So, even if there seems to be some margin, it cannot be recommended to significantly exceed voltage overshoots of 100 V, even in the worst case. A more ideal driving voltage would in practice result in the need for higher gate resistors, leaving only very limited potential for the reduction of switching losses.

A further interesting detail can be derived from the gate-current waveforms in Figure 13b. Obviously there is a difference in the behavior of the switch and the diode. The gate current for the switch shows a single peak that provides the total gate charge Q_{Gtot} , whereas the diode waveform exhibits two smaller peaks. The reason is evident: diode gate voltage and switching node transient do not coincide. So the diode is switched on leading to the associated Q_{GS} peak 100 ns before the on-transient, which is responsible for the second peak with charge Q_{GD} . This is also reflected in the V_{GS} waveform. The gate voltage for the diode shows a lower initial voltage V_{Ni_D} with a step after the switching transient. V_{Ni_D} can still be calculated by eq. (15), but Q_{Gtot} has to be replaced by Q_{GS} to yield the correct value during the dead-time. This is important, as the diode's reverse voltage drop is thus increased by $Q_{GD}/(C_{on} + C_{iss})$, in our case by approximately 1.5 V.

Figure 15 shows the total energy dissipated in the two transistors; the graphs result from integration and summing of the respective current-voltage products of Figure 13 c and d for I_{Load} of 1 and 10 A. The different types of losses can be easily distinguished. The total switching energy per period E_{tot} is about 22 μJ at low current and increases to 33 μJ at 10 A. It is only the latter that could eventually be reduced by a few μJ through faster switching. Figure 15 also indicates that the relatively high negative V_{GS} leads to high reverse voltage and diode conduction losses during the dead-times.

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Application-specific considerations

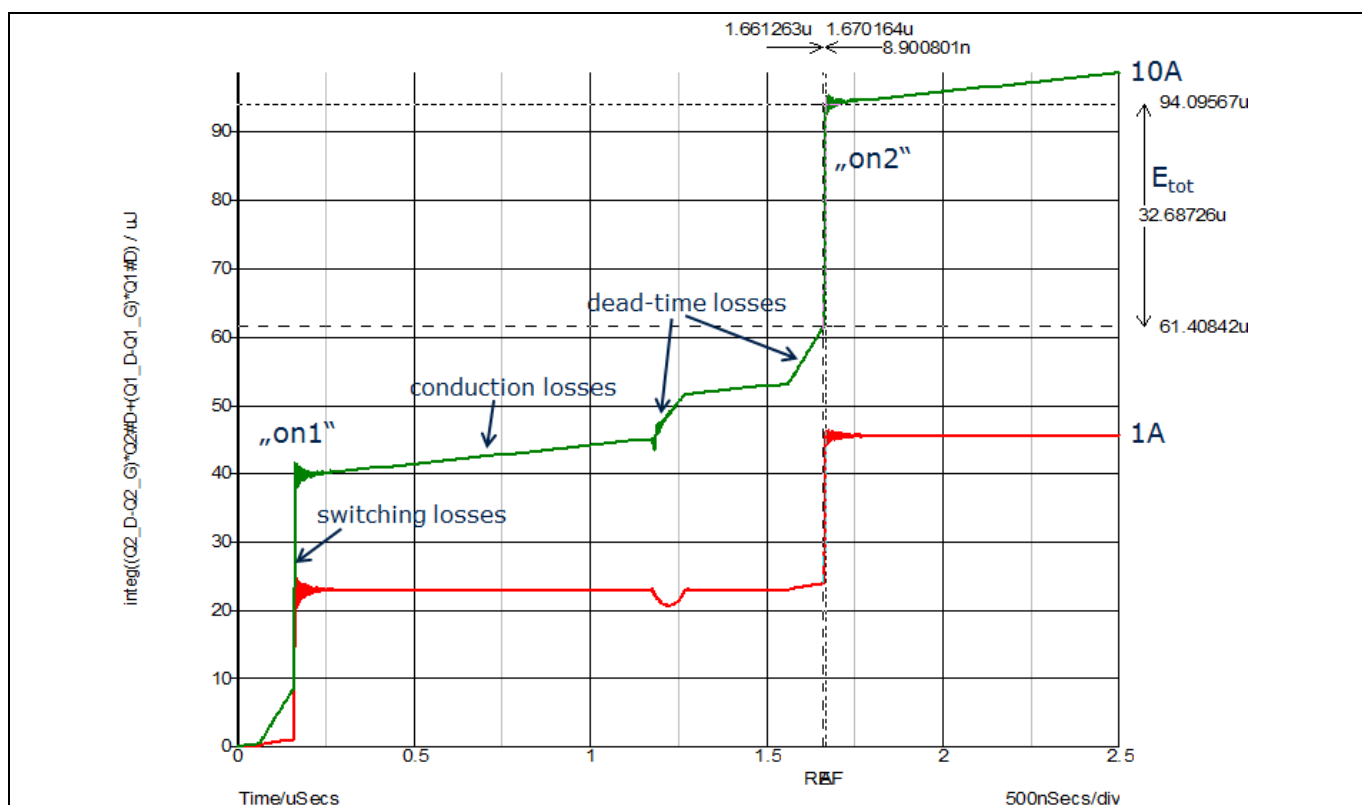


Figure 15 Total switching loss associated with waveforms of Figure 13 for $I_{Load} = 1$ and 10 A

Based on similar simulations, in Tables 3 and 4 different parameter combinations together with the resulting switching losses P_{sw} are listed. Also included are the simulated dead-time losses P_{dio} and the losses caused by the steady-state gate current P_{ss} . For P_{dio} two dead-times t_d of 100 ns each are assumed per switching period. The losses can be calculated to be:

$$P_{sw} = f_{sw} \cdot E_{tot}$$

$$P_{dio} = f_{sw} \cdot I_L \cdot (2 \cdot (V_{th} - V_{Ni_D}) - \Delta V_N) \cdot t_d$$

$$P_{ss} = I_{ss} \cdot V_S$$

Table 3 Drive-circuit parameter combinations used for loss simulations

Drive circuit	R_{on}/R_{off} [Ω]	V_S [V]	C_{on} [nF]	R_{ss} [Ω]	V_{Ni_D} [V]	$\Delta V_N(1\text{ }\mu\text{s})$ [V]	I_{ss} [mA]
A	5 / 5	12	2	1000	-5.9	1.5	9
B	5 / 5	12	2	500	-5.6	2.6	17
C	10 / 10	12	2	1000	-6	1.6	9
D	5 / 5	12	3.3	1000	-7	1.5	9
E	5 / 5	12	1.5	1000	-5.2	1.5	9
F	5 / 5	15	1	1000	-6	2	12

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Application-specific considerations

Table 4 Simulated power losses in Watts of 400 V/100 kHz totem-pole PFC stage for drive circuits in Table 3

	P_{sw}	P_{dio}	P_{ss}	P_{cond}	$P_{sw1/2}$	P_{dio}	P_{ss}	P_{cond}
	$I_{Load} = 1\text{ A}$				$I_{Load} = 10\text{ A}$			
A	2.2	.1	.1	.07	3.0 / 3.3	1.4	.1	7
B	2.2	.1	.2	.07	3.0 / 3.1	1.3	.2	7
C	2.2	.1	.1	.07	3.1 / 3.5	1.4	.1	7
D	2.2	.1	.1	.07	3.1 / 3.6	1.7	.1	7
E	2.2	.1	.1	.07	3.1 / 3.1	1.35	.1	7
F	2.2	.1	.18	.07	3.0 / 3.0	1.45	.18	7

For comparison purposes in Table 4 the conduction losses

$$P_{cond} = I_{Load}^2 \cdot R_{dson}$$

have also been included (at room temperature). Obviously at low current the switching losses are dominant and they are independent of the gate-drive circuitry used. At larger I_{Load} the switching losses also increase and a slight dependence on gate-drive circuitry can be observed. In Table 4 therefore P_{sw1} and P_{sw2} denote the respective losses for long and short diode off-times, corresponding to the “on1” and “on2” transitions in the previous graphs. Although in the 10 A range conduction losses dominate, both switching and diode dead-time losses are significant. The loss values clearly confirm the theoretical considerations. Drive circuitry A, B, E and F show similar small losses, whereas C trades slightly higher losses for reduced voltage overshoots. A further increase in V_N as resulting from circuit D is neither required nor recommended.

5.2 Soft-switched applications (LLC)

“Soft-switching” means to avoid simultaneous high current and high voltage in a power switch, i.e. to operate the switch at either zero voltage or zero current. This can be achieved by utilizing resonant transitions to charge the switching node capacitance, as is done in the well-known LLC topology of the DC-DC converter stage following the PFC stage in today’s most common SMPS architecture [7].

As soft-switching yields much slower voltage transients with typical slopes of only a few V/ns, the RC driving network should be slightly changed to optimize performance. In particular there is no need for significant negative off-voltages, and thus V_{Ni} should be chosen to be as low as possible. Safe operation is a must, and thus a slightly negative V_{Ni} in the -1 V range is recommended. R_{on} and R_{off} are obviously less critical and can be chosen higher than in hard-switched applications, e.g. 10 to 20 Ω . The total gate charge stays the same, as it depends only on the overall voltage swing. Thus, from Figure 9 we find 12 V/1 nF or 10 V/1.5 nF to be reasonable V_S/C_{on} combinations. Unfortunately, as explained above, the negative gate voltage V_{Ni_D} during the diode’s dead-time is increased by approximately Q_{GD}/C_{on} and thus still stays in the -4 V range. Although the dead-time losses per cycle can be slightly reduced, the significance of P_{dio} increases, as LLC circuits are switched at frequencies going up to 300 kHz. Switching losses are determined by the energy stored in the output capacitances and thus correspond to P_{sw} at low current, as given in Table 4.

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Application-specific considerations

As already mentioned, soft-switched systems are much less sensitive to re-turn-on in regular operation. Thus, if the reverse diode losses P_{dio} are still considered too high, clamping of the negative V_{GS} could be an option. However, the details of such an approach are beyond the scope of this application note.

6 Measurement results

To verify the theory and simulation results given in the previous chapters, a commutation board with two IGOT60R070D1. GaN switches and two 1EDI20N12AF gate drivers has been designed (Figure 16). Particular compensation techniques are used to minimize the power-loop inductance. Q3D simulations finally yielded a very low value of 6 to 7 nH.

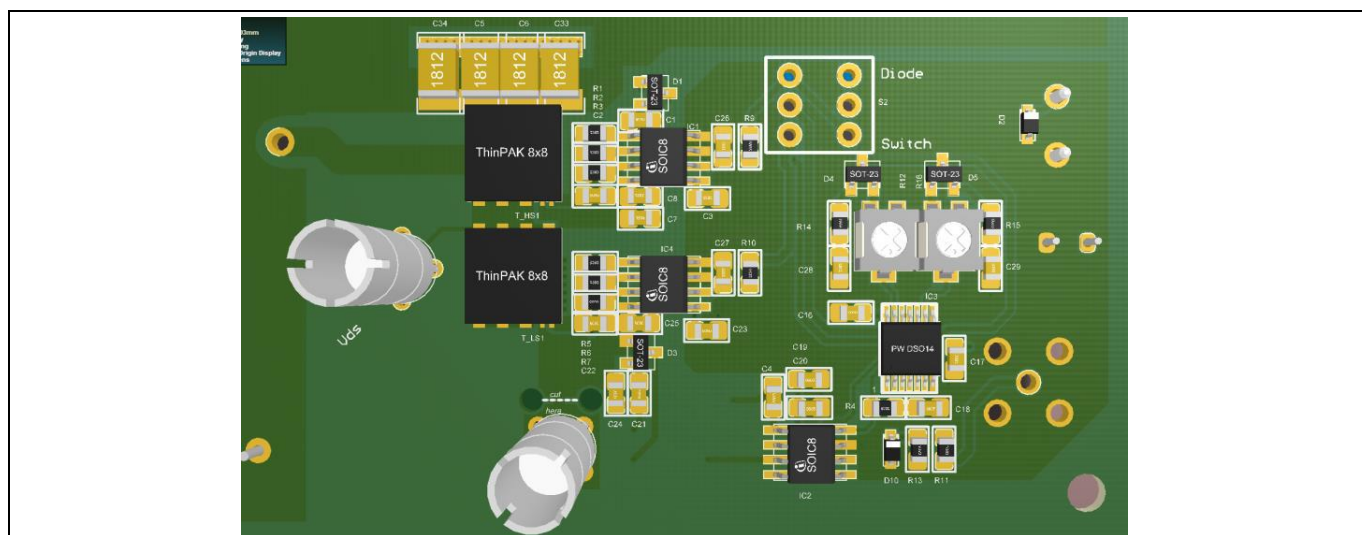


Figure 16 PCB for switching measurements

Although the accurate measurement of switching transients at the extreme speed of GaN is a critical task and would merit a dedicated application note, our results so far agree with the theory. As an example Figure 17 shows measured switch-on waveforms for a load current of 10 A using driving circuit D of Table 3. Although it is difficult to reproduce the exact waveforms seen in simulation, the main parameters like peak current, voltage overshoot, switching times and switching losses are in agreement. This enables prediction of the performance of real systems with sufficient accuracy.

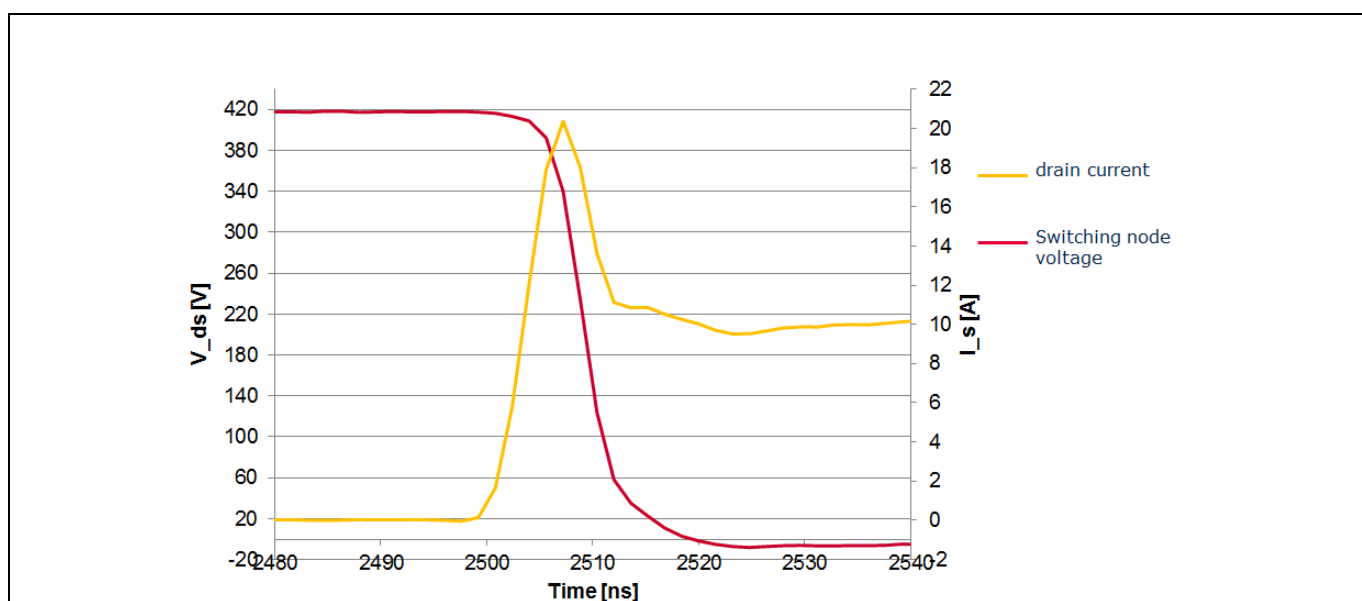


Figure 17 Measured switching voltage and current for $I_{Load} = 10 \text{ A}$

7 Summary and guidelines

To achieve optimum switching performance with Infineon's e-mode GaN HEMTs driven by Infineon's isolated gate-drive IC 1EDI20N12AF, we recommend the following:

- Choose the minimum possible gate resistors R_{on} and R_{off} . The actual values depend on the power-loop design. As a criterion, voltage stress must not exceed specified limits even with a completely discharged C_{on} .
- Choose a combination of supply voltage V_s and coupling capacitance C_{on} that fulfills the requirements for the initial negative switch-off voltage V_{Ni} . As a rule of thumb, $V_{Ni} = -3$ to -4 V for hard-switching and $V_{Ni} = -1$ to -2 V for soft-switching are good choices.
- At a given V_{Ni} , high V_s and low C_{on} is preferable with hard-switching, whereas low V_s and high C_{on} are recommended for soft-switching.
- Driver and switch dynamic properties are well balanced, resulting in robust operation, and relatively insensitive with respect to the driving-circuit parameters.
- Choice of R_{ss} is therefore not critical; a time-constant $\tau = R_{ss} * (C_{on} + C_{iss})$ in the range of a few μs is recommended.
- In soft-switching applications clamping of the negative V_{GS} can be a worthwhile option.
- If the system allows long off-times for both switches (both C_{on} discharged), it is recommended to start switching with the "diode" to avoid an excessive current peak due to re-turn-on.

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Revision history

Revision history

Document version	Date of release	Description of changes

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Edition 2018-05-03

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference

AN_201702_PL52_012

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