CoolMOS™ CFDA

650 V rated superjunction MOSFET with fast body diode for automotive

About this document

Scope and purpose

Nowadays, there is a growing need of resonant topologies in automotive applications, in topologies like main inverter, DC-DC converter, flyback converter, LLC resonant topologies, HID lighting and onboard battery charger. This application note sets its focus on describing the CoolMOS™ CFDA[1] generation of superjunction MOSFETs[2] which is especially optimized for these applications and is also suitable for non-resonant topologies giving a higher margin in repetitive hard commutation of the body diode limited by the junction temperature. Additionally the CFDA automotive qualified generation are the first 650 V high voltage devices on the market with an integrated fast body diode. This paper will prove that the two major goals, high efficiency and high reliability, are completely reached and Infineon Technologies sets a new reference in the market for high voltage automotive qualified MOSFETs. Furthermore, a detailed comparison between CFDA and the former CoolMOS™ generations CPA and C3A will be demonstrated in different kind of application conditions.

Intended audience

This application note was designed to give an engineer the opportunity to see improvements of the CFDA automotive qualified CoolMOS™ family in comparison to CPA and C3A CoolMOS™ families.

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1 Introduction

According to the construction of the MOSFET different theoretical improvements will be analyzed and verified by measurements. These improvements are for example a significant reduction of reverse parameters like the Q_G[3], t_{rr}[4]and Q_{rr}[5] values, cost down for customers and other features and benefits which will be described in the next chapters of this application note. The following table shows the typical topologies and applications in which this product comes into operation.

Table 1 Target topologies and applications

Topology	Application
ZVS[6]phase shifted full bridge	DC-DC converter as ZVS full bridge
LLC resonant topology	DC-DC converter
	On-board / off-board battery charger
	HID[7] lighting lamp ballast
	LED[8] lighting
H4 bridge	DC-DC converter, HID[7] lighting
Flyback	DC-DC converter
	PFC stages

Now that the target topologies and applications are listed, the table below illustrates the features and benefits of the CFDA.

Table 2 Main features and benefits

Features	Benefits
Significant Q_G reduction	less gate drive capability necessary
	reduced turn ON and turn OFF time (better usage for ZVS window)
Reduced Q_{rr}[9]	repetitive hard commutation (limited by $T_{junction}$[10])
Defined $t_{rr,max}$ and $Q_{rr,max}$ values	design advantages
Overall	Automotive qualification and lower price compared to C3[11] technology based industrial CFD family

The CFDA is based on the C6[12] technology which, therefore, includes all improvements of the C6 technology compared to the previous C3 technology (the C3 technology is described in a comparison in the Infineon application note AN 2010-11: “650 V CoolMOS™ C6/E6”, see:
http://www.infineon.com/dgdl/Infineon-ApplicationNote_PowerMOSFETs_650VCoolMOSC6E6.pdf

1.1 Introduction to superjunction MOSFET

With the increasing demand for higher power density, especially soft switching topologies like half bridge (e.g. HID half bridge or LLC) and full bridge concepts (e.g. ZVS bridge) seem to be the ideal solution. These topologies reduce the switching losses and increase the reliability of the system due to less dynamic di/dt and dv/dt stress on the power device. Such high stresses occur predominantly in light-load operation [1]. It is already shown that superjunction devices like the CoolMOS™ help to overcome this problem by inherent optimized charge carrier removal during reverse recovery and eliminating the problem of latch-up of the parasitic npn-bipolar transistor [1]. A significant reduction of the reverse recovery charge can be achieved by an

enhanced recombination rate of the injected carriers resulting in lower reverse recovery peak currents during turn-off and strongly reduced reverse recovery charge by almost a factor of 10. For optimized body diode (Figure 1) performance in hard switching conditions, especially the shape of the resulting reverse recovery waveform and the design conditions of the printed circuit board are important [2],[3]. The new CoolMOS™ 650 V CFDA is designed in this manner with improved reverse recovery behaviour together with increased safety margin in breakdown voltage, compared to the former Infineon CoolMOS™ family of CPA type.

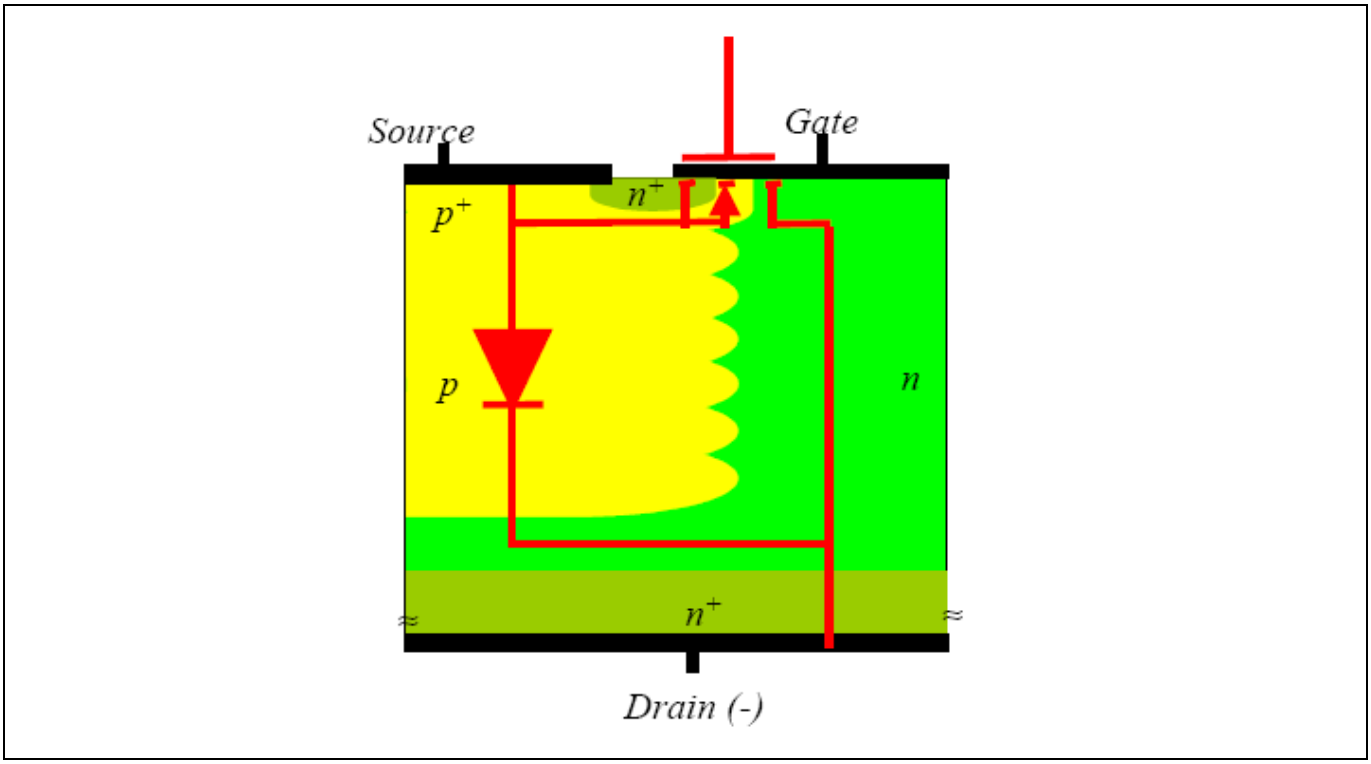

Figure 1 Schematic cross section of the CoolMOS™ high voltage power MOSFET and its integral body diode

1.1.1 Superjunction principle

The Infineon CoolMOS™ technology is a revolutionary approach for high voltage power MOSFETs and designed according to the superjunction (SJ) principle [4], which in turn is based on the RESURF [5] ideas being successfully used for decades in lateral power MOSFETs. Conventional power MOSFETs suffer from the limitation of the so-called silicon limit [6], which means that doubling the voltage blocking capability typically leads to an increase in the on-state resistance by a factor of five. The silicon limit is shown in Figure 2, where the area specific on-state resistance of state-of-the-art standard MOSFETs as well are indicated. SJ technology may lower the on-state resistance of a power MOSFET virtually towards zero. The basic idea is to allow the current to flow from top to bottom of the MOSFET in very high doped vertically arranged regions. In other words, a lot more charge is available for current conduction compared to what is the case in a standard MOSFET structure. In the blocking state of the SJ MOSFET, the charge is counterbalanced by exactly the same amount of charge of the opposite type. The two charges are separated locally in the device by a very refined technology, and the resulting structure shows a laterally stacked fine-pitched pattern of alternating arranged p- and n-areas, see Figure 3. The finer the pitch can be made, the lower the on-state resistance of the device will be. With every CoolMOS™ generation the pitch is reduced, moving ever closer to the zero resistance point without losing voltage blocking capability.

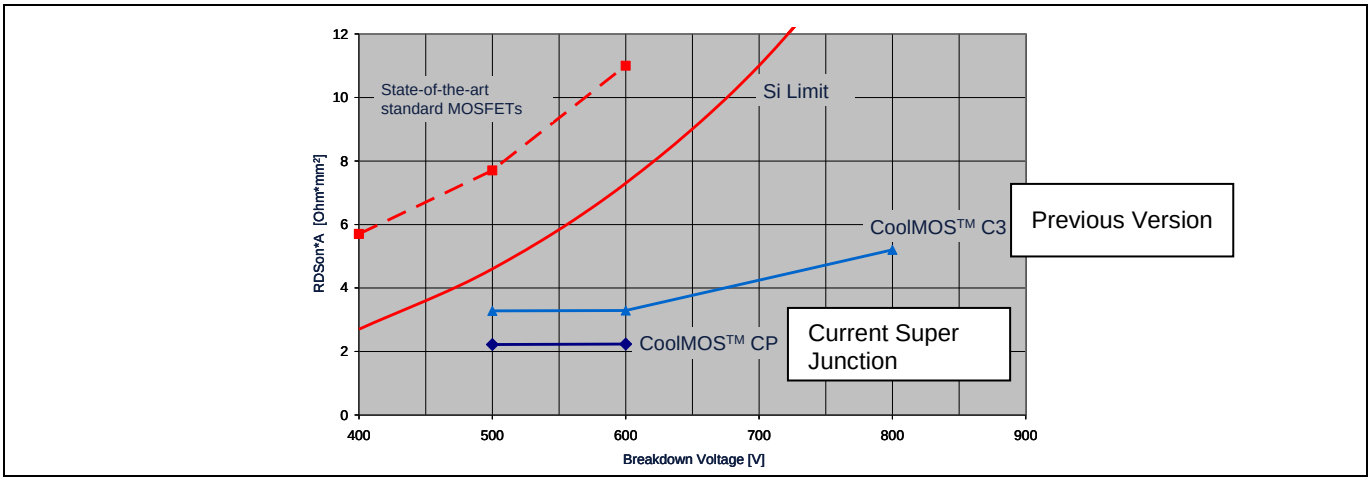

Figure 2 Area-specific $R_{DS(on)}$ [1] versus breakdown voltage for standard MOSFET and CoolMOS™

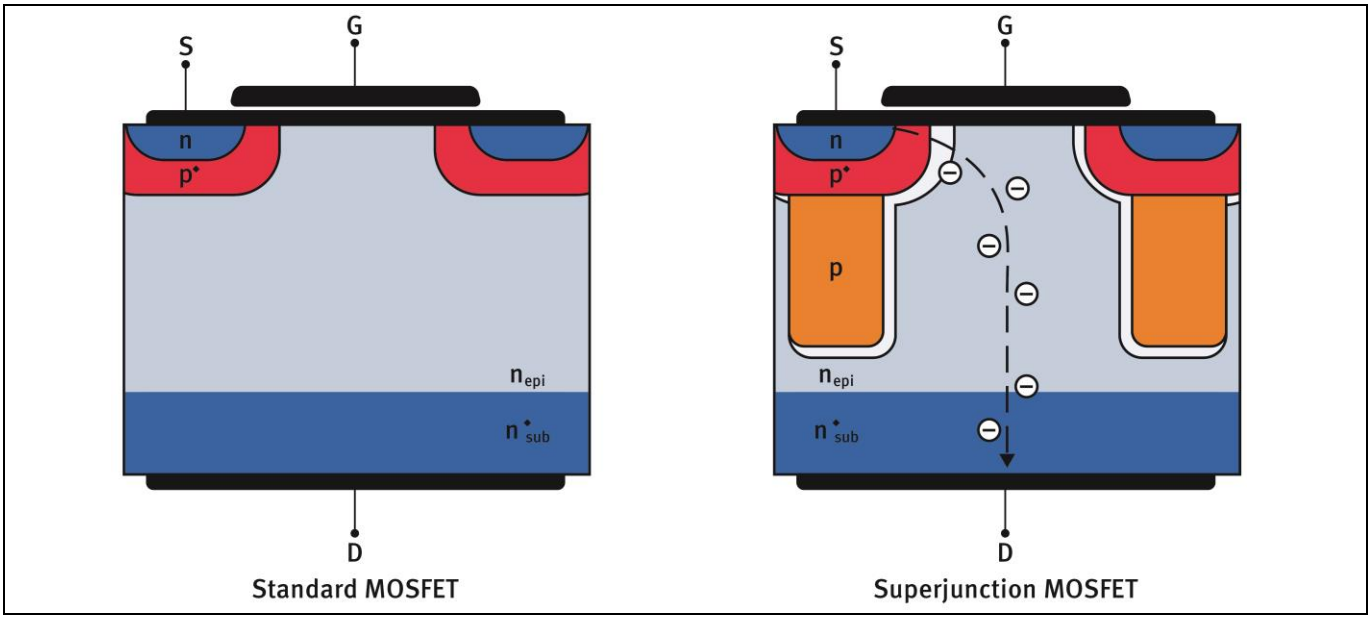

Figure 3 Schematic cross-section of a standard power MOSFET versus a superjunction MOSFET

Another signature of SJ technology is the extremely fast switching speed. The turn-off behaviour of a SJ MOSFET is not characterized by the relatively slow voltage driven vertical expansion of the space charge layer but by a sudden nearly intrinsic depletion of the laterally stacked p-n structure. This unique behaviour makes the device very fast. The neutralization of these depletion layers is done via the MOS controlled turn-on of the load current for the n-areas and via a voltage driven drift current for the p-areas. SJ devices reach therefore theoretical switching speeds in the range of few nanoseconds.

Figure 4 shows a comparison of the figure-of-merit $R_{DS(on)}$*Q_g between the most advanced MOSFET technologies available in the market today.

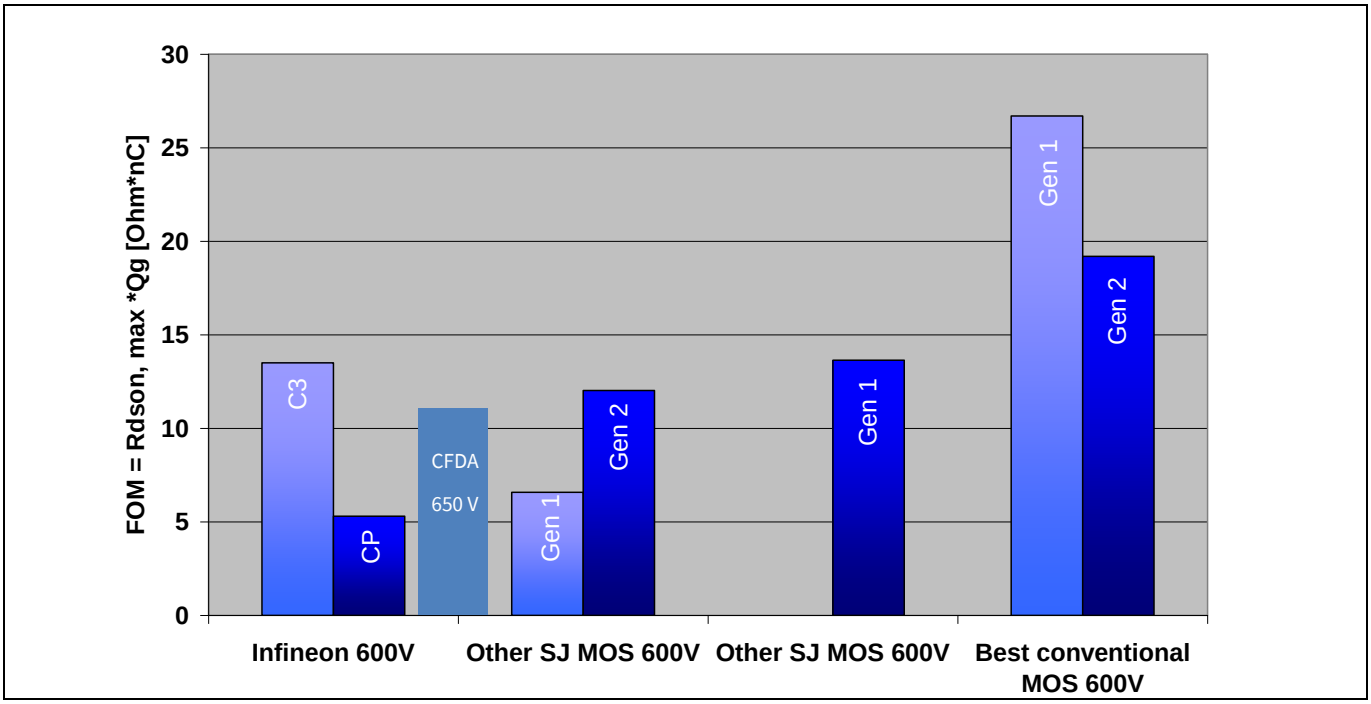

Figure 4 **Comparison of figure-of-merit $R_{DS(on)}$,max*Q_G for most advanced 600 V MOSFETs available in the market, vs. Infineon industrial families (600 V) and automotive CFDA family (650 V)**

The listed CoolMOS™ families CP and C3 shown in Figure 4 above are cross reference industrial types and comparable with the related (automotive qualified) CPA and C3A families according to the FOM (figure-of-merit).

2 Main differences of CFDA vs. C3A / CPA

This chapter is going to analyze the most important differences between the high voltage CoolMOS™ families: CFDA (C6 CoolMOS™ technology based, automotive qualified), C3 and C3A (both C3 CoolMOS™ technology based, C3 industrial qualified, C3A automotive qualified) and CPA (C5 CoolMOS™ technology based, automotive qualified).

2.1 Voltage rating ($V_{(BR)DSS}$)

As visible in the datasheet there is a minimum drain-source breakdown voltage ($V_{(BR)DSS}$)[13] of 600 V for CPA, 650 V of CFDA and 800 V for C3A. The 650 V CFDA family is going to complement the 600 V CPA family. This increase of the breakdown voltage was decided to address the automotive market which needs 650 V devices. This requirement is claimed to have a higher margin on the input stage of a DC-DC converter due to the occurring voltage peaks at the DC link.

2.2 Key parameter comparision CFDA

Below is a comparison of typical key parameters for the CFDA family vs. CPA and C3A family, based on a reference type with an $R_{DS(on)}$ of approximately 190 mΩ.

Table 3 Key parameter comparison CFDA versus C3A/CPA families

Specification	Symbol	CFDA	C3A	CPA
Breakdown voltage (Drain – Source)	$V_{(BR)DSS}$	650 V	800 V	600 V
Reference type on-state resistance, maximum rating, 25°C	$R_{DS(on)}$	190 mΩ	190 mΩ	199 mΩ
Drain current rating, max.	I_D	17.5 A	20.7 A	16.0 A
Pulse current rating, max.	$I_{D,pulse}$	57.2 A	62.1 A	51.0 A
Typ. gate source charge	Q_{GS}	12 nC	11 nC	8 nC
Typ. gate drain charge	Q_{GD}	37 nC	33 nC	11 nC
Total gate charge	Q_G	68 nC	87 nC	32 nC
Gate Miller-plateau	$V_{Plateau}$	6.4 V	5.5 V	5 V
Energy stored in output capacitance @400 V	E_{OSS}	5.7 µJ	10 µJ	7.5 µJ
Gate threshold voltage min. ... max.	V_{thr}	3.5 / 4.5 V	2.1 / 3.9	2.5 / 3.5 V
Body diode, reverse recovery charge	Q_{rr}	0.7 µC	11 µC	5.5 µC
Body diode, di/dt	dI_F/dt	900 A / µs	400 A / µs	200 A / µs
Body diode, dv/dt	dV /dt	50 V /ns	4 V /ns	15 V /ns

Note: Listed values for the 190 mΩ reference type in C3A family column (grey marked) are taken from the C3 family (equates to corresponding non automotive C3 Industrial type of same technology), for performance comparison only.

2.3 Internal gate resistor $R_{g,int}$, selflimiting di/dt and dv/dt

CoolMOS™ CFDA comes with an integrated gate resistor in order to achieve self-limiting di/dt and dv/dt characteristics. Internal gate resistors have the advantage to be a low inductive type and lead to the self limiting di/dt and dv/dt.

This integrated $R_{G,int}$ [23] allows fast turn ON and turn OFF at normal operating current conditions but limits the di/dt and dv/dt in case of peak current conditions. The values of integrated $R_{G,int}$ [23] scales inversely with the gate charge respectively device capacitances.

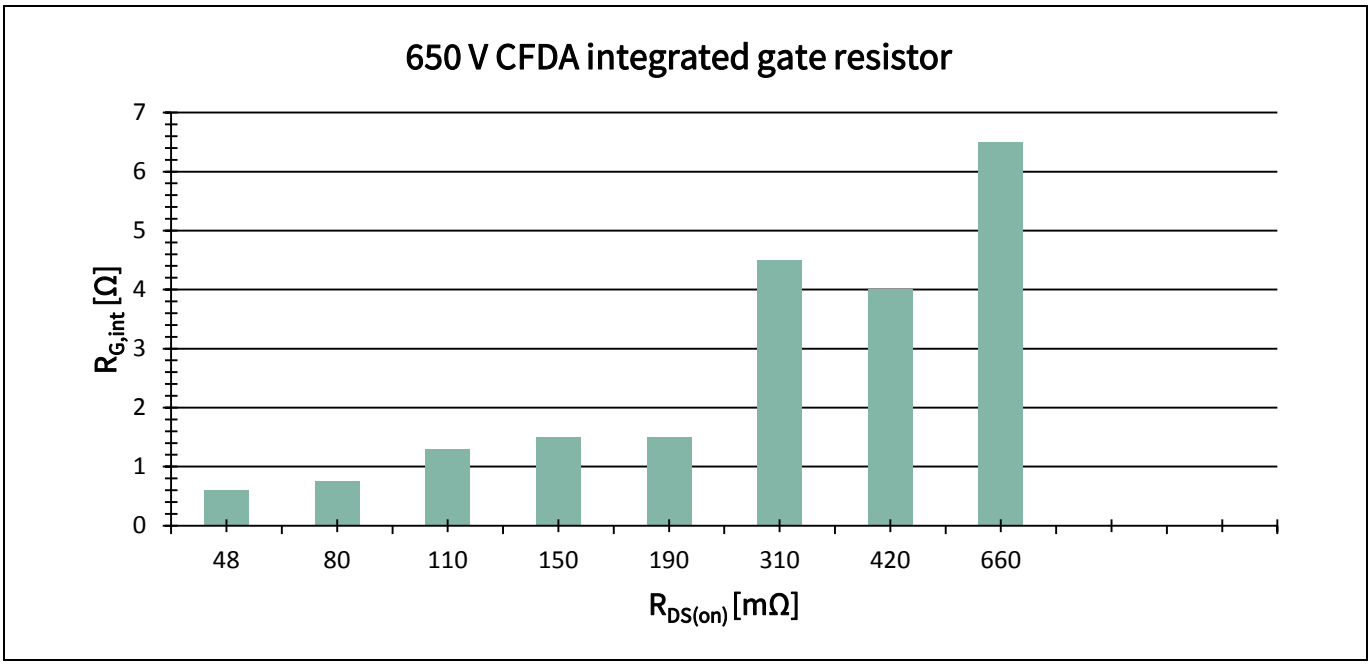

Figure 5 Integrated gate resistor ($R_{g,int}$) for CoolMOS™ CFDA family

The CFDA devices with $R_{DS(on)}$ values below 150 mΩ come with no built-in gate resistances. Low $R_{DS(on)}$ values require larger silicon area and thus exhibit larger device capacitances. For those parts it is usually not necessary to additionally limit the di/dt and dv/dt values. Low ohmic CFDA parts are therefore ideally suited for applications with highest efficiency requirements, like e.g. DC-DC converters.

Please note that the listed internal gate resistor $R_{G,int}$ in Figure 5 above is showing the sum of all internal gate resistor parts (build-in gate resistor, bond wire, bond finger, solder resistance etc.). In the application the additional external gate resistor $R_{G,ext}$ [25] allows to control the final dv/dt.

The CFDA is designed for “ease-of-use” feature and provides a stable switching behaviour. Due to its self limiting behaviour the C6 technology can be easier implemented in a parasitic layout environment. These ease-of-use requirements are: the C_{rss} [24] of C6 is close to C3A level, and the implementation of an internal gate resistor brings the advantage of stable switching, and switching losses are comparable to C3A. As the CFDA is based on the C6 technology, it also shows a stable and self-limiting switching behaviour and is easy to design-in, even in layouts which are not perfectly optimized with respect to their parasitic environment.

The following diagrams, in Figure 6, represent the CFDA CoolMOS™ switching behaviour for the 80 mΩ type PW65R080CFDA:

- di/dt and dv/dt , for turn OFF slopes
- di/dt and dv/dt , for turn ON slopes

All combined with different external gate resistors $R_{g,ext}$ [25].

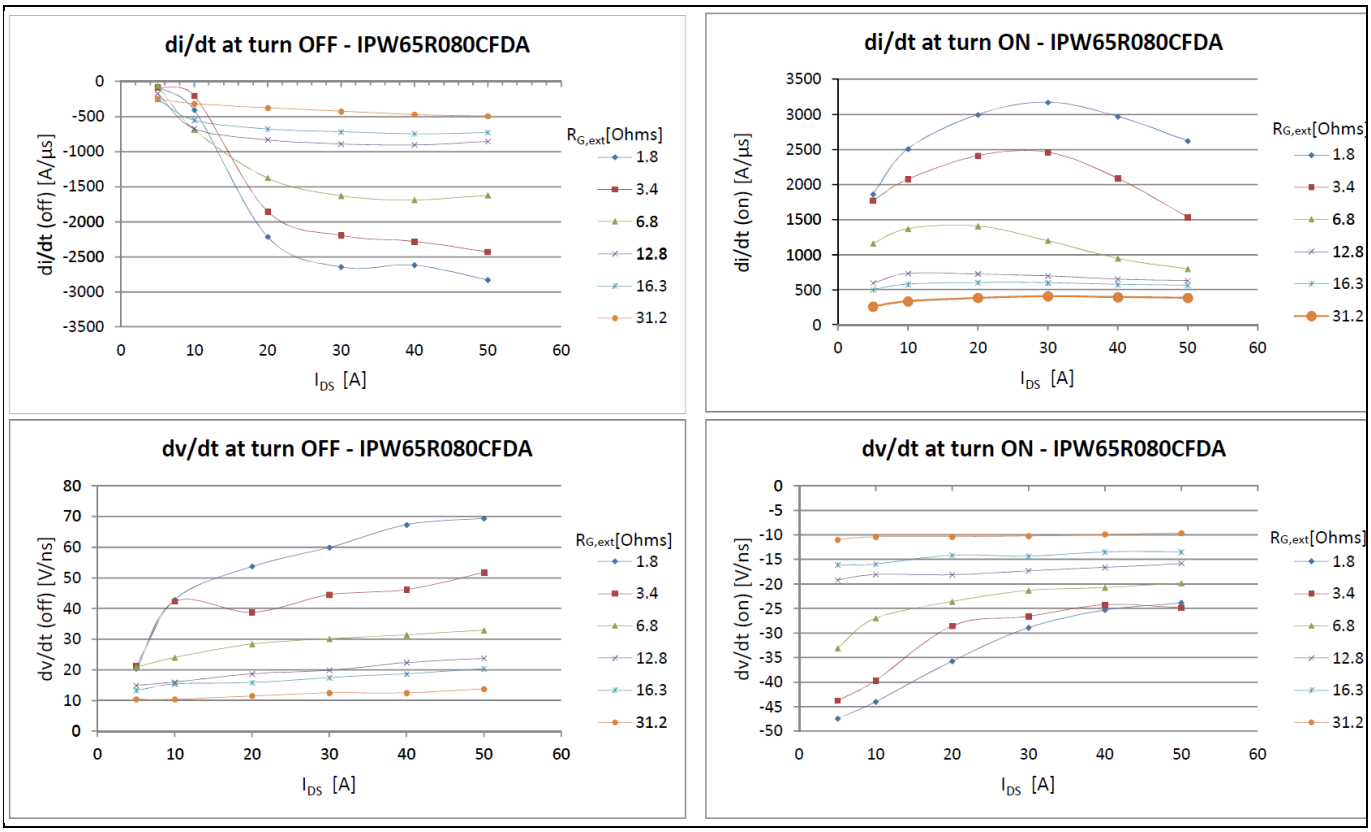

Figure 6 CoolMOS™ CFDA measurements for di/dt and dv/dt (OFF / ON slopes)

After the analysis of the most important improvements this application note is going to describe some measurements of CFDA in target applications, see:

- Chapter 4.1(HID lighting bridge)
- Chapter 4.2 (DC-DC Converter (ZVS phase shifted full bridge))

2.4 Diode reverse recovery charge; time and current (Q_{rr}, t_{rr}, I_{rrm})

Compared to CFD/C3 industrial family, the Q_{rr} of CFDA was further reduced. As consequence t_{rr}[34][19] is shortened and the I_{rrm}[20] is also reduced which brings a higher margin in repetitive hard commutation of the body diode limited by the junction temperature which is allowed by the datasheet. Figure 7 shows the improved behaviour of a lowered Q_{rr} in a theoretical way.

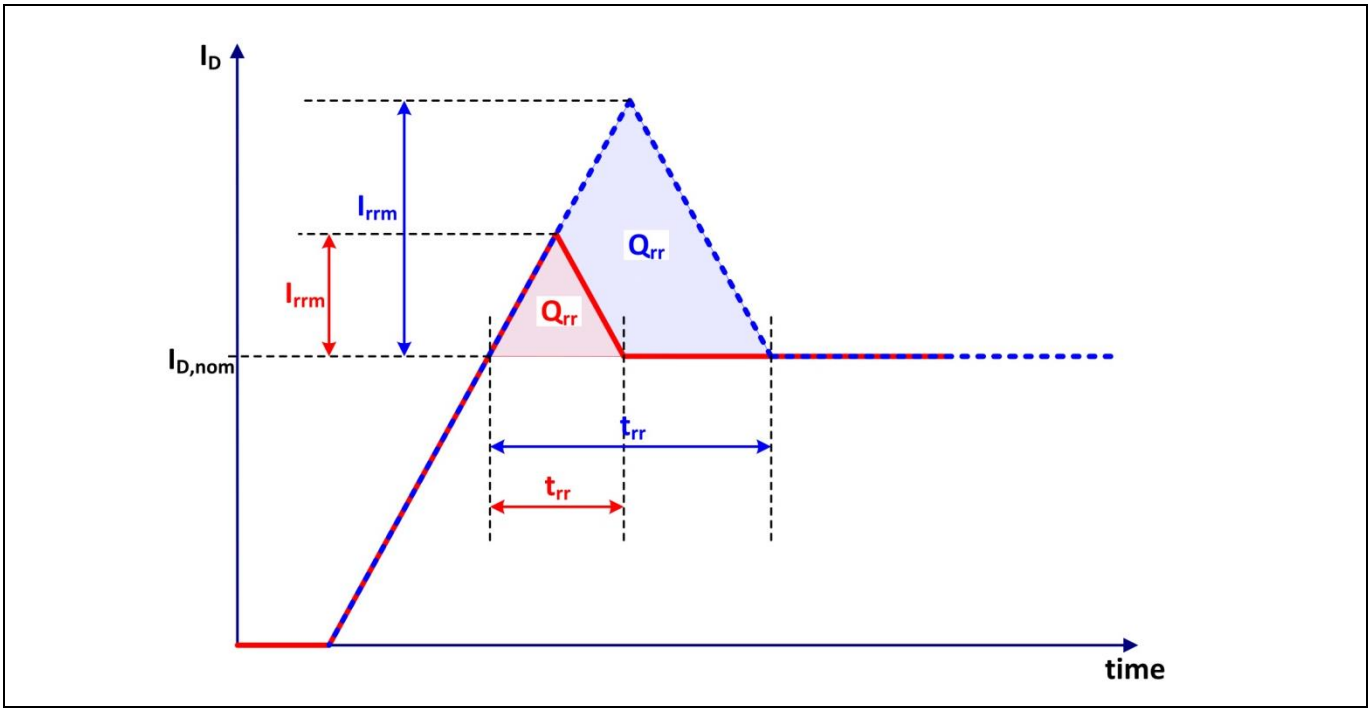

Figure 7 Simplified I_D waveform depending on Q_{rr}, t_{rr}, I_{rrm}

Figure 9 illustrates the Q_{rr} value of CFDA in comparison to a CFD/C3 industrial type and a competitor technology by showing the example of an 80 mΩ product. It is visible that CFDA has the lowest Q_{rr} values from 10 A to 25 A in a half bridge configuration with a supply voltage of 400 V, like seen in Figure 8. The high side switch is used to load the inductance to the specified current. After switching OFF the high side MOSFET current is commutating to the body diode of the low side MOSFET which corresponds to the DUT (device under test).

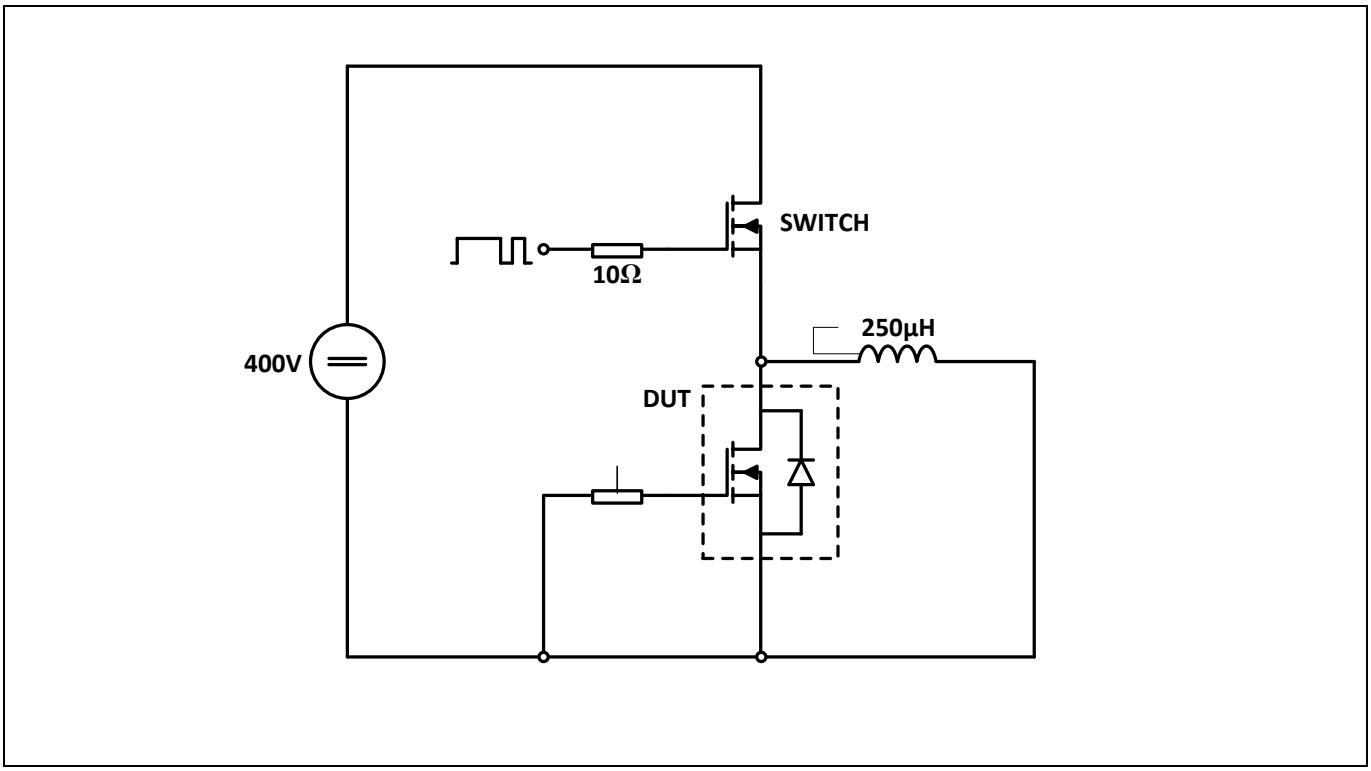

Figure 8 Half bridge configuration

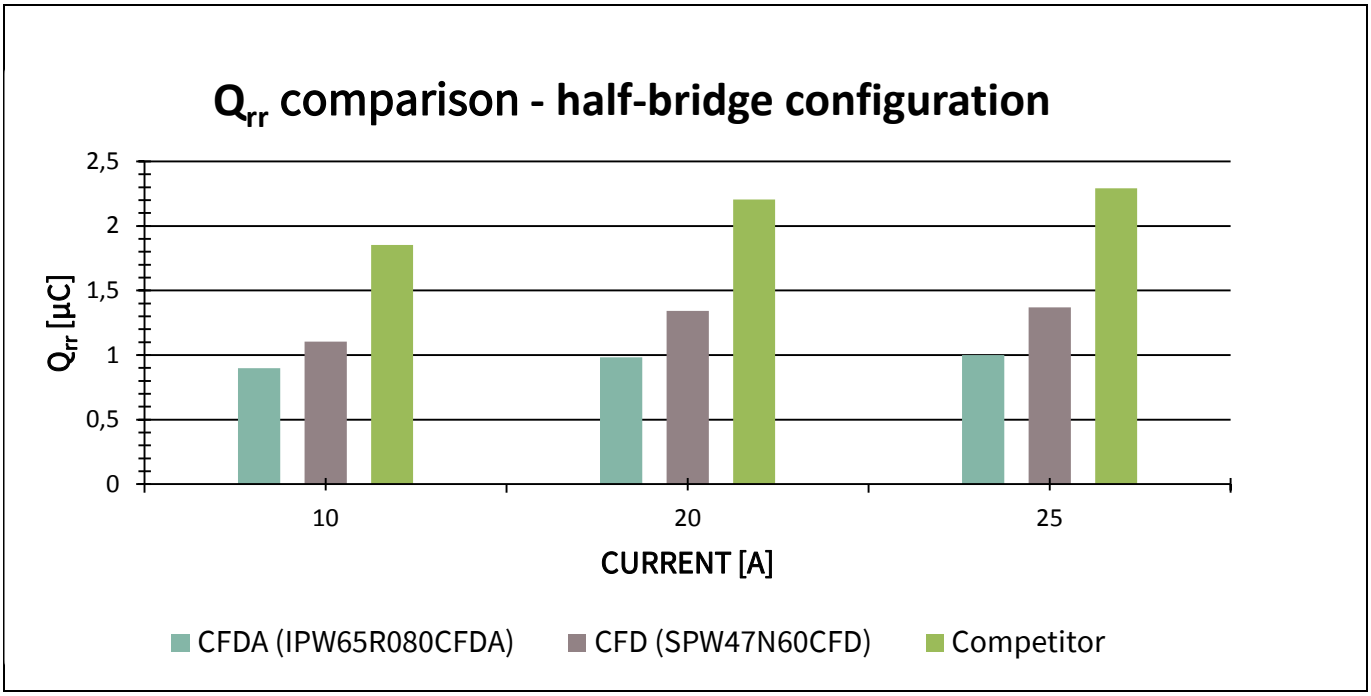

Figure 9 **Q_{rr} comparison of low side MOSFET in a half bridge configuration**

Furthermore, due to an improved production process of the CFDA the t_{rr} and Q_{rr} values will be given in the datasheet which results in a major benefit in the design of e.g. HID lamp ballast applications, where the reduced Q_{rr} and t_{rr} is also of advantage. An HID application example is listed in Chapter 4, Specific target applications.
The absolute measured reverse recovery behaviour of the new CoolMOS™ 650 V CFD(A) is shown in Figure 10. It appears that the new CoolMOS™ 650 V CFDA devices have a very low reverse recovery charge Q_{rr}, reverse recovery time trr and reverse recovery current I_{rrm} when compared to the standard CFD device.

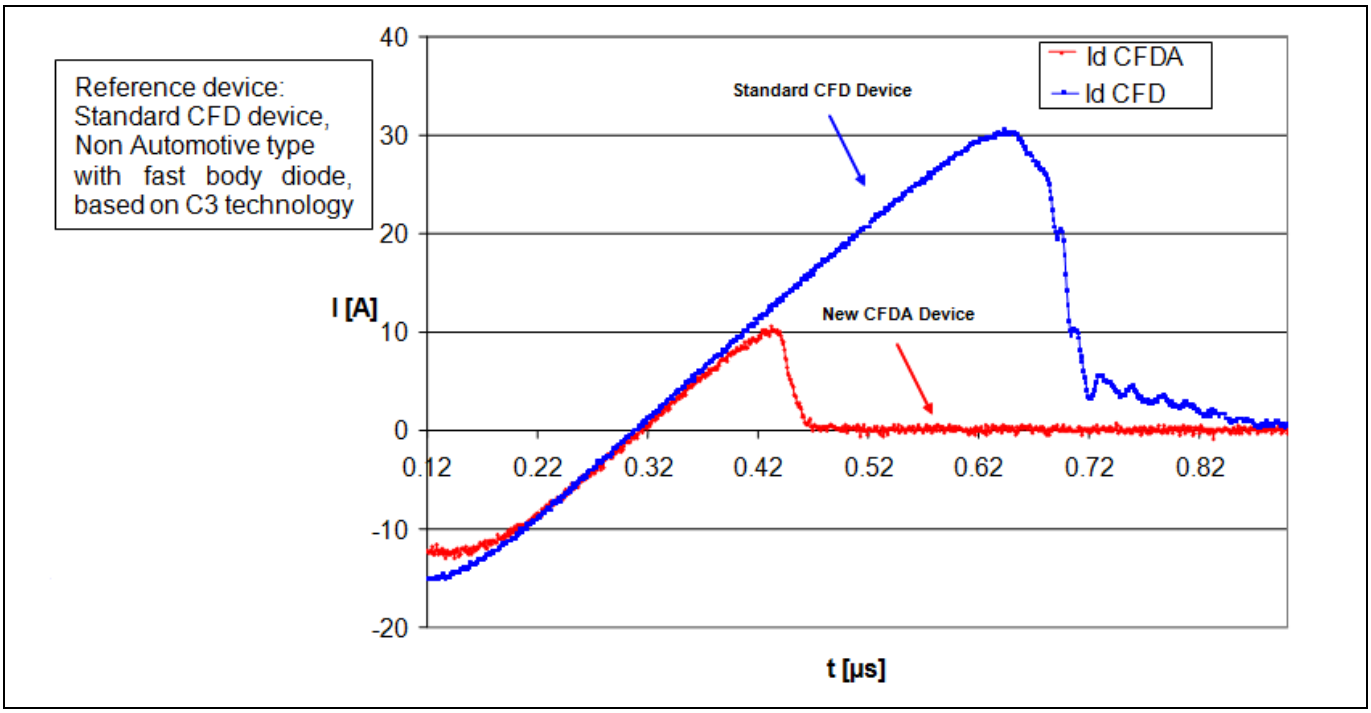

Figure 10 **Measured reverse recovery waveforms at di/dt = 100A/µs, 25°C, V_r = 400 V. The new CFDA device (red curve) shows very low Q_{rr}, t_{rr} and I_{rrm} compared to the standard CFD device (blue curve).**

Additional the blue standard CFD device shows a waveform with a hard slope transition. In comparison, the red waveforms of the new CFDA device shows a soft slope characteristic, in spite of the strongly reduced Q_{rr}, t_{rr} and I_{rrm}. This characteristic is highly desirable during hard commutation in order to avoid voltage overshoot and to ensure reliable device operation.

2.4.1 Dependence of Q_{rr} and t_{rr} with temperature

Of importance for the designer is the dependence of Q_{rr} and t_{rr} on temperature. The Q_{rr} and t_{rr} values tend to increase with temperature, due to increased carrier generation in the device. This dependence is shown in Figure 11 for the 310 mΩ 650 V CFDA type. An almost linear increase of Q_{rr} and t_{rr} with temperature is observed.

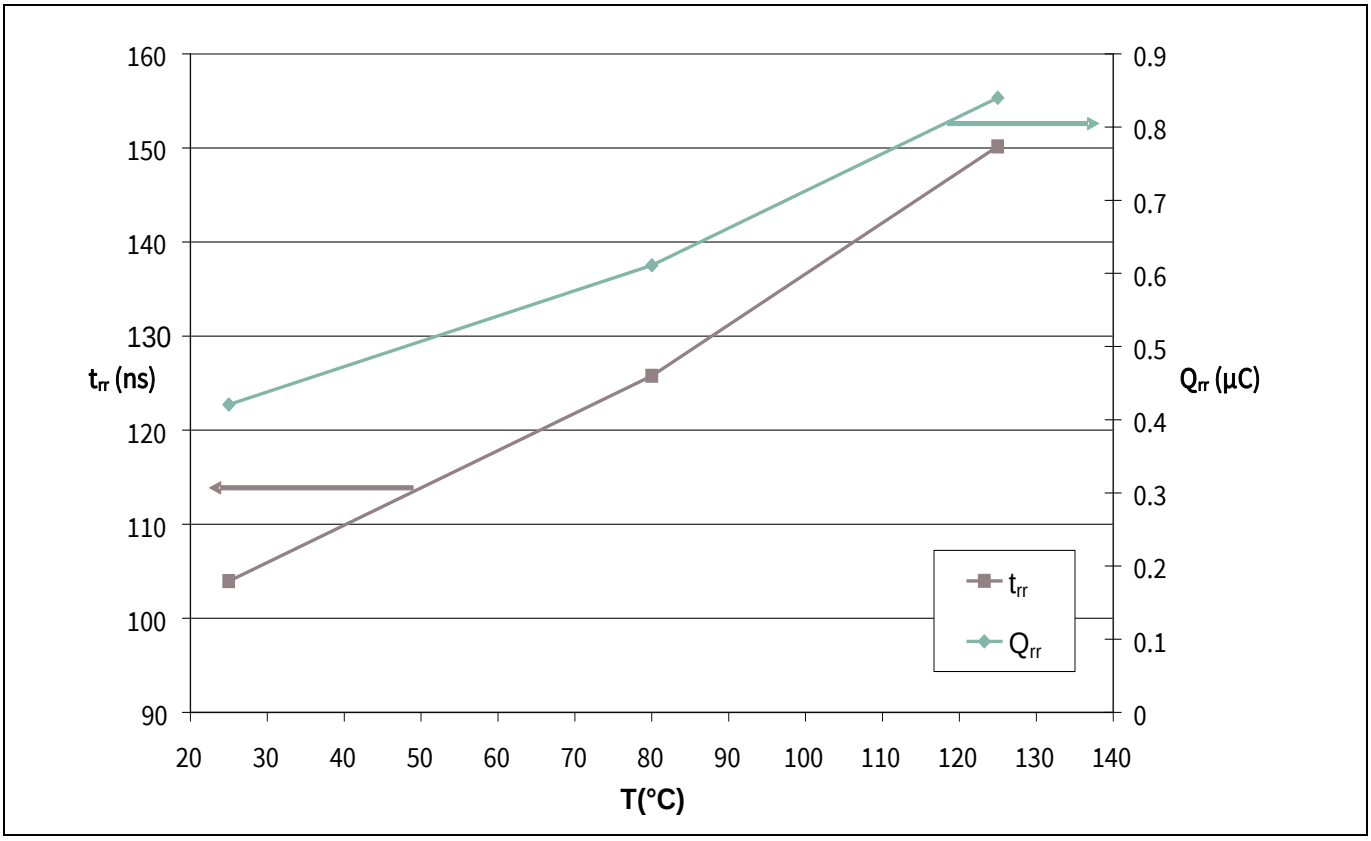

Figure 11 Dependence of Q_{rr} and T_{rr} with temperature, for the 310 mΩ CFDA device

2.4.2 Dependence of Q_{rr} and t_{rr} with $R_{DS(on)}$, comparison with CFD device

Another important aspect to be considered is the dependence of Q_{rr} and t_{rr} on the devices $R_{DS(on)}$. This can be seen in Figure 12 and Figure 13 respectively, where the new 650 V CFDA device is compared with the former Infineon's CoolMOS™ CFD (non automotive, fast diode) technology.

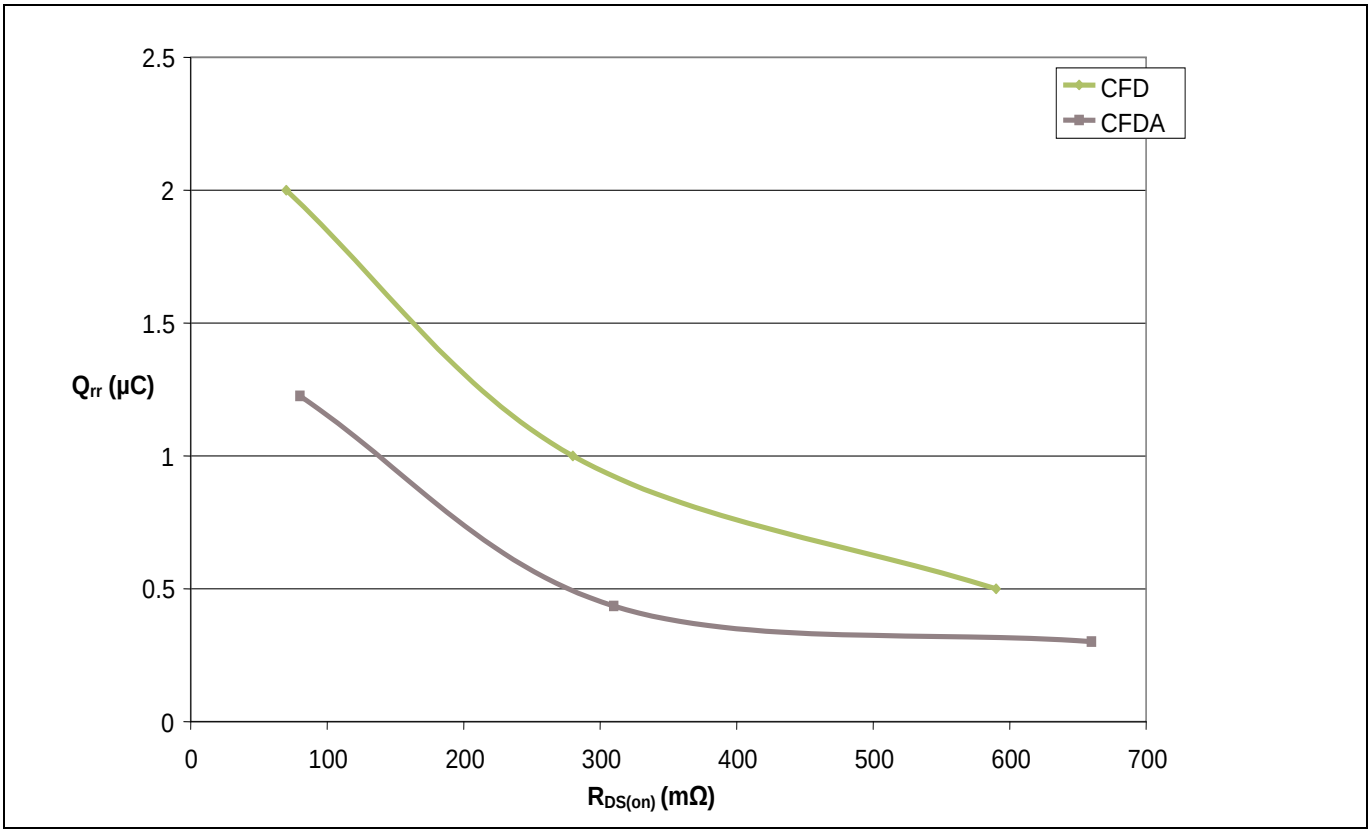

Figure 12 Dependency of Q_{rr} versus $R_{DS(on)}$, measured at 25°C and for the 80 mΩ, 310 mΩ and 660 mΩ 650 V CFDA devices , in comparison with the former 600 V industrial CFD (non automotive) technology

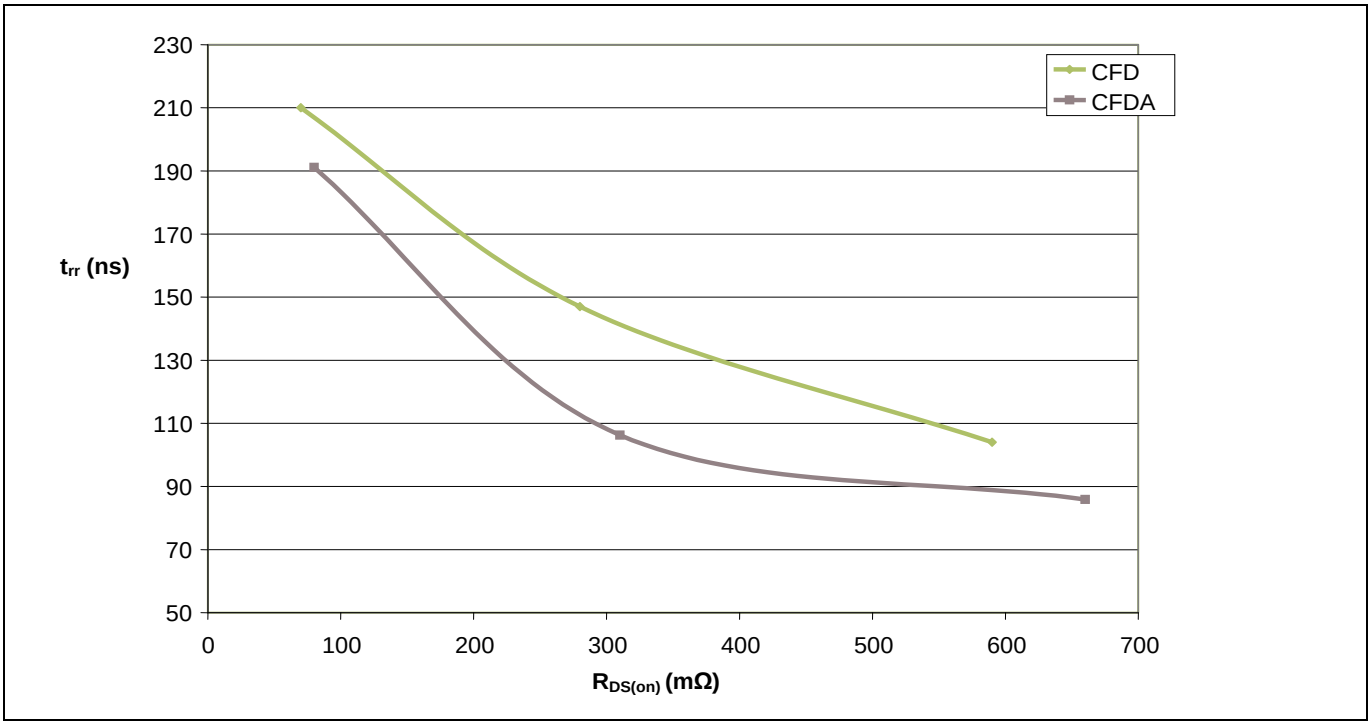

Figure 13 Dependence of t_{rr} on $R_{DS(on)}$, measured at 25°C and for the 80 mΩ, 310 mΩ and 660 mΩ 650 V CFDA devices in comparison with the former 600 V industrial (non automotive) CFD technology

The new 650 V CFDA device clearly offers an even better trade-off than the former technology between dynamical characteristics (Q_{rr},t_{rr}) and lowest $R_{DS(on)}$.

2.5 Commutation behaviour (hard switching of fast body diode)

The behaviour analyzed in Chapter 2.4 brings a more stable and rugged behaviour during commutation of the body diode. The following figure represents the maximum V_{DS} overshoot ($V_{DS,max}$[22]) which occurs during commutation. Root is a voltage drop over inductances in the commutation loop, due to a change in the slope of the body diode current.

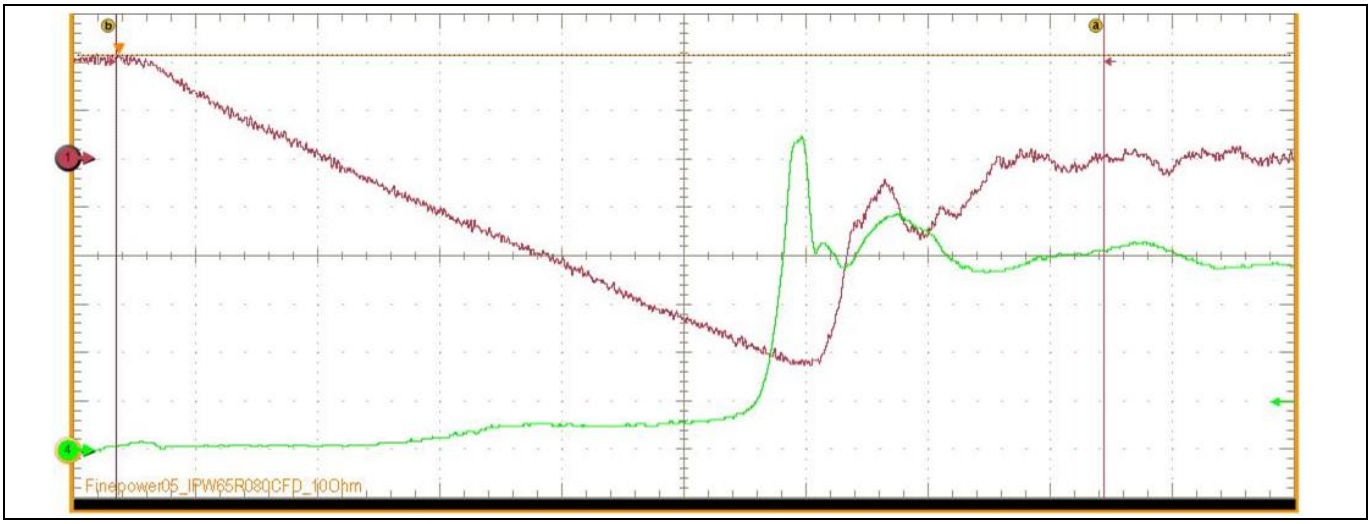

Figure 14 Measured $V_{DS,max}$ in a half bridge configuration represented in Figure 16 of the IPW65R080CFDA

Parameter:

- Y (C1, brown, Current) 10 A/div.
- Y (C4, green, VDS) 100 V/div
- X 200 ns/div
- Delta t (b-a) 107.9 ns

This waveform was acquired in a half bridge configuration where the low side MOSFET is the device under test which is shown in Figure 16. This figure also illustrates the values of $V_{DS,max}$ of CFDA (at temperature T_j = 25°C) in comparison to industrial CFD type and a comparable competitor product with a maximum $R_{DS(on)}$ of 80 mΩ.

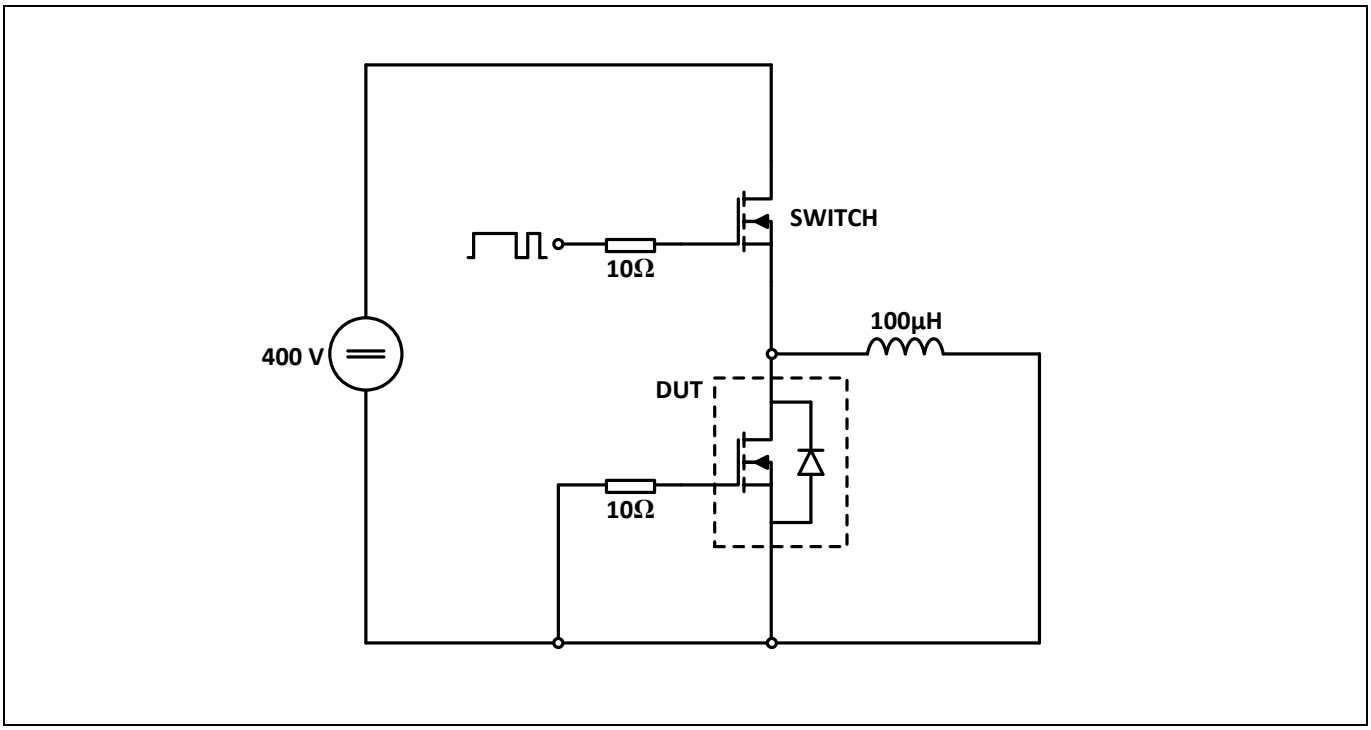

Figure 15 Half bridge configuration

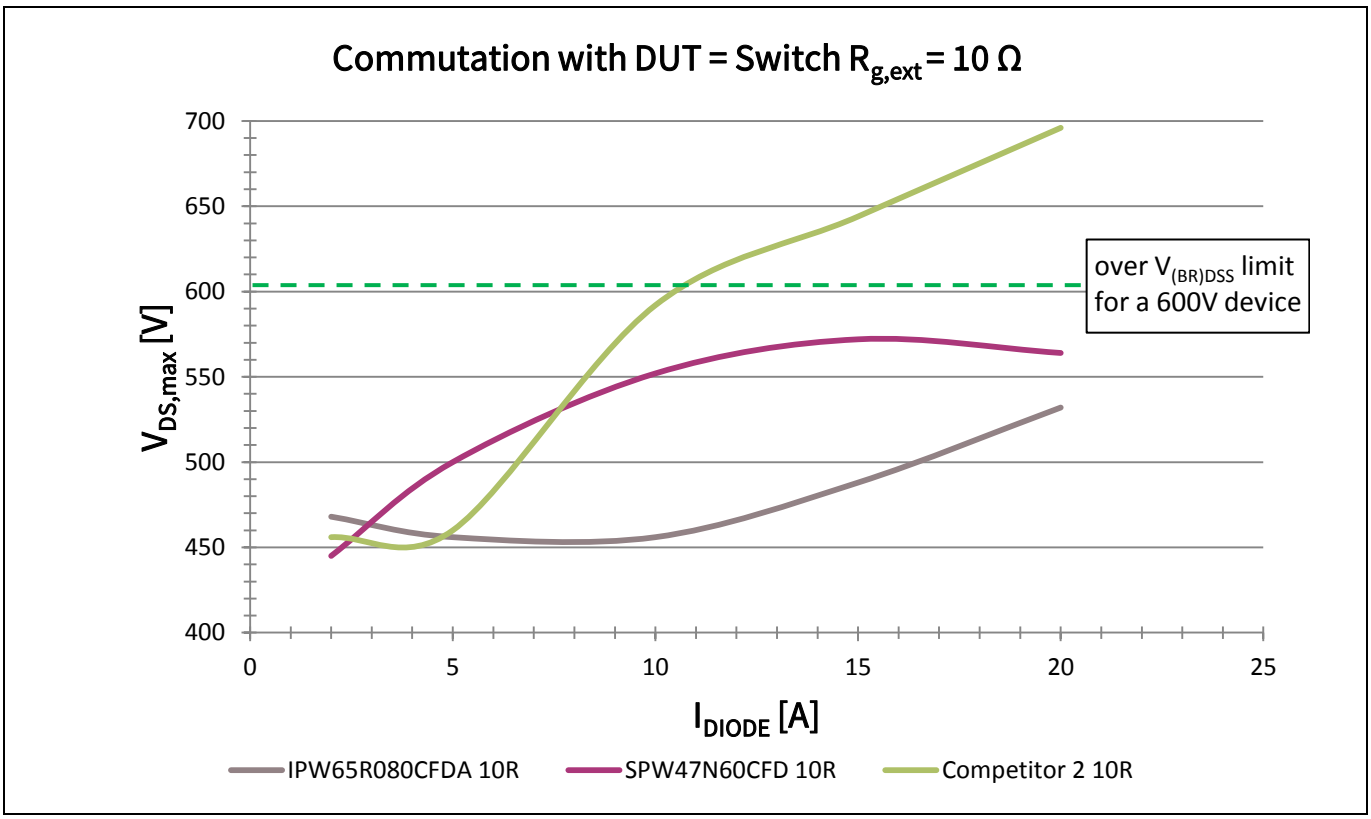

Figure 16 $V_{DS,max}$ comparison CFDA, CFD and Competitor 2

Figure 16 describes that even when reaching high loads (20 A) the CFDA has a voltage peak of only at about 535 V which is at about 115 V lower than the maximum breakdown voltage of 650 V (only CFDA). As can be seen in the diagram the competitor product reaches approximately 700 V at this high current which is 100 V higher than the breakdown voltage of the product ($V_{(BR)DSS}$ = 600 V) which could lead to the failure of the device.

The commutation ruggedness of the CoolMOS™ 650 V CFDA device is demonstrated in reverse recovery measurements in Figure 17, where the devices were tested up to di/dt ≈ 2000 A/µs.

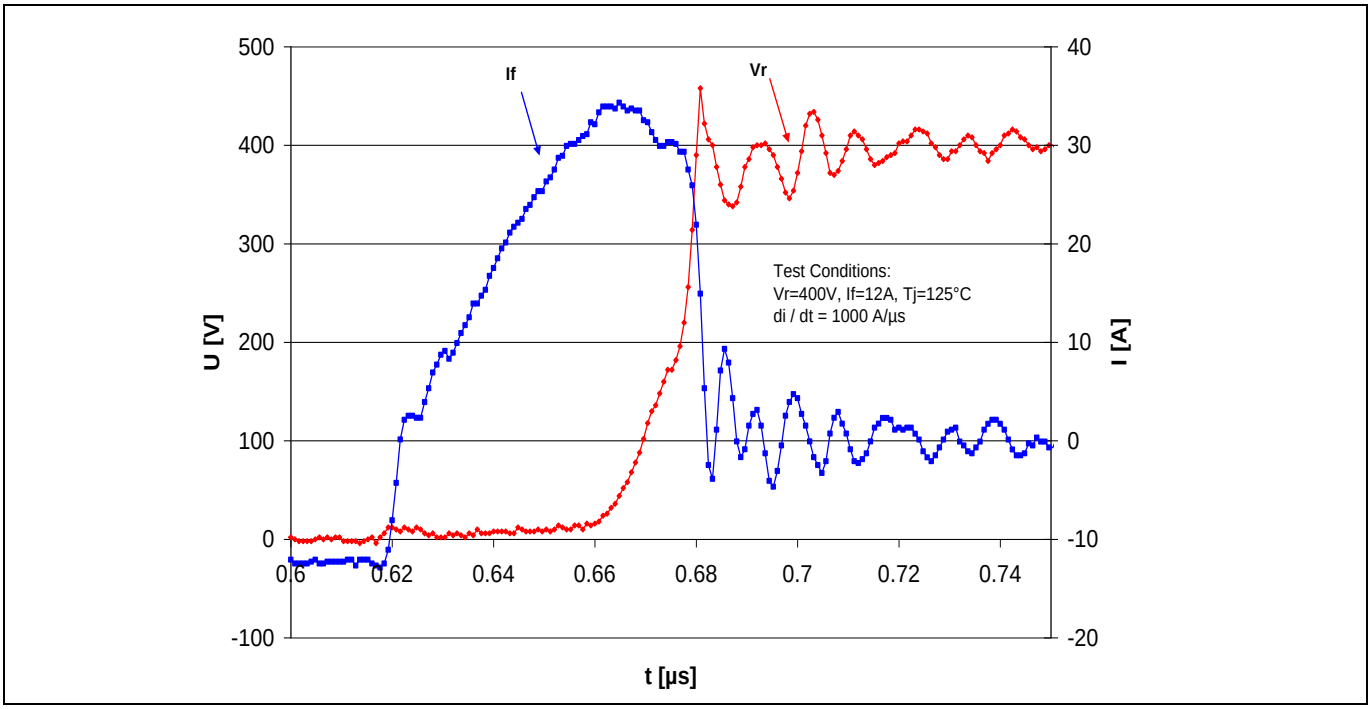

Figure 17 Measured reverse recovery waveforms for the new CoolMOS™ 650 V CFDA device. The devices could not be destroyed even at the maximum capability of the tester.

No device could be destroyed under these conditions and the waveforms show still a soft characteristic, compared to snappy waveforms for other superjunction devices. This is a clear advantage for the designer, once one can optimize its application for maximum performance without being concerned with device destruction during hard commutation of the body diode.

2.6 Input gate charge (Q_g)

This section of the application note will describe another improvement of the CFDA family, the reduced Q_g compared to the industrial types C3, automotive types C3A and CFD types. The following figure describes what happens if the MOSFET has a lower Q_g.

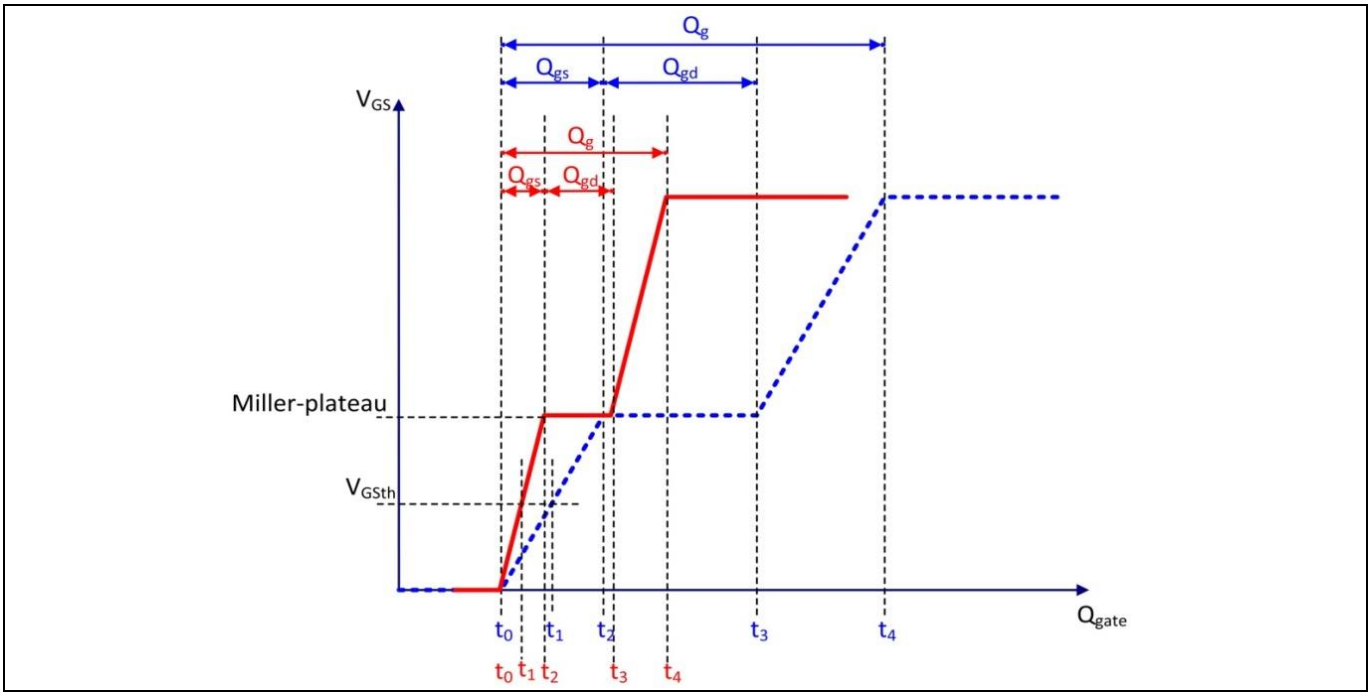

Figure 18 Simplified Gate charge

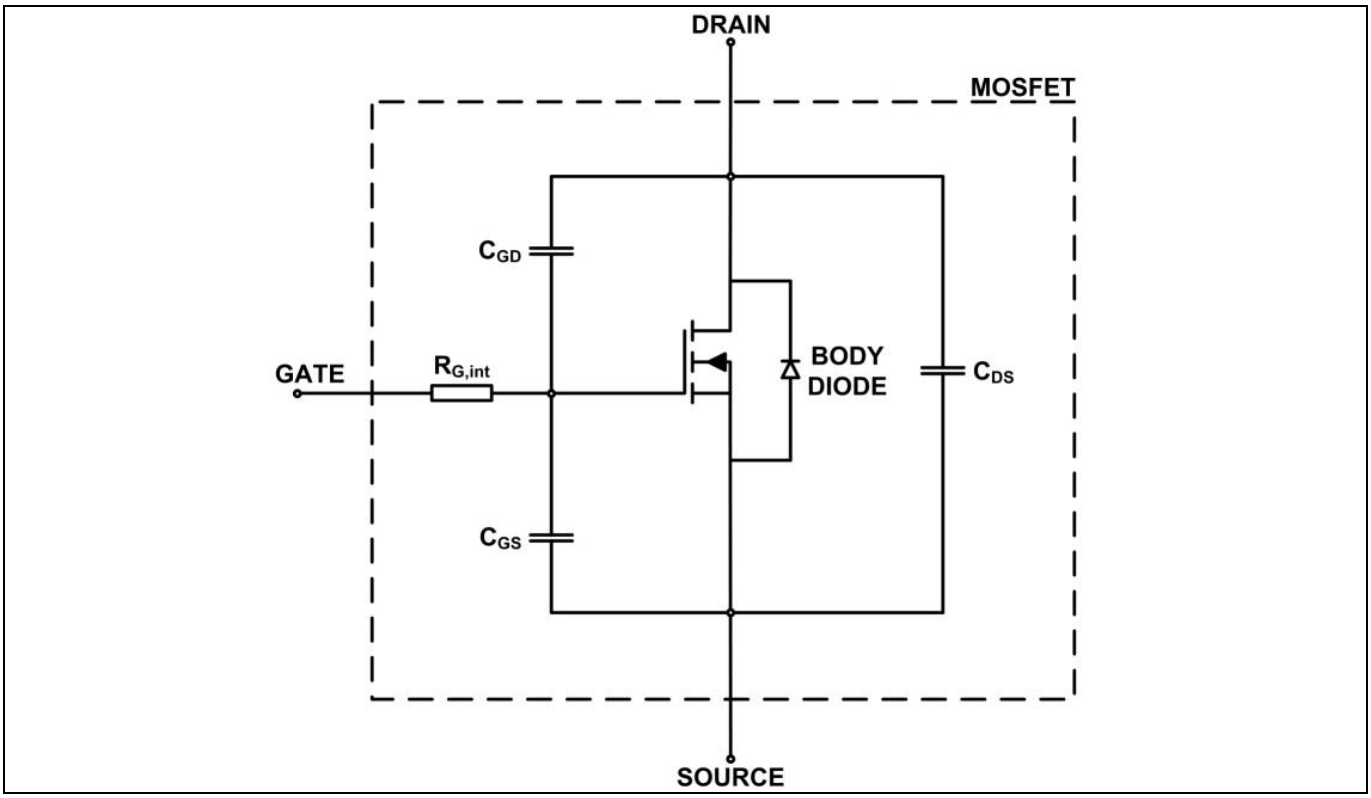

Figure 19 Simplified small signal MOSFET equivalent circuit

As visible in Figure 18 due to a reduced gate charge it is possible to switch the device ON and OFF faster or reach the same performance with lower driver capability. The length of the Miller-plateau is dependent on the relation between the internal C_{GS}[14] and C_{GD}[15]. “In order to simplify the clarification of the Miller-plateau it is assumed that the voltage supply has a value of 400 V and the gate driver is represented as a constant current source. During t0 till t2 the current from the gate driver is charging C_{GS} and discharging C_{GD}. Directly after t2 the

MOSFET switches ON and V_{DS} decreases to nearly 0 V. At this time the V_{GS}[16] has the value of about 6.3 V (this is an assumed value for easier description). During the period from t2 to t3 when V_{DS}[17] drops from a supply voltage of 400 V, C_{GD} has to be discharged until the voltage over C_{GD} reaches 6.4 V. Because C_{GD} is discharged from 393.7 V to -6.3 V a lot of energy is needed from the driver. For this reason C_{GS} cannot be charged due to the fact that nearly the whole current from the driver flows through C_{GD} until t3. From t3 to t4 V_{DS} stays constant at nearly 0 V and the current from the driver is able to charge C_{GS} until the defined voltage is reached."[7]

As mentioned before it is possible to switch the MOSFET ON and OFF faster, which leads to a wider window to achieve zero voltage switching. The next figure is going to represent this behaviour in a theoretical way where only the Q_g is decreasing and all other characteristics of the same part stay the same.

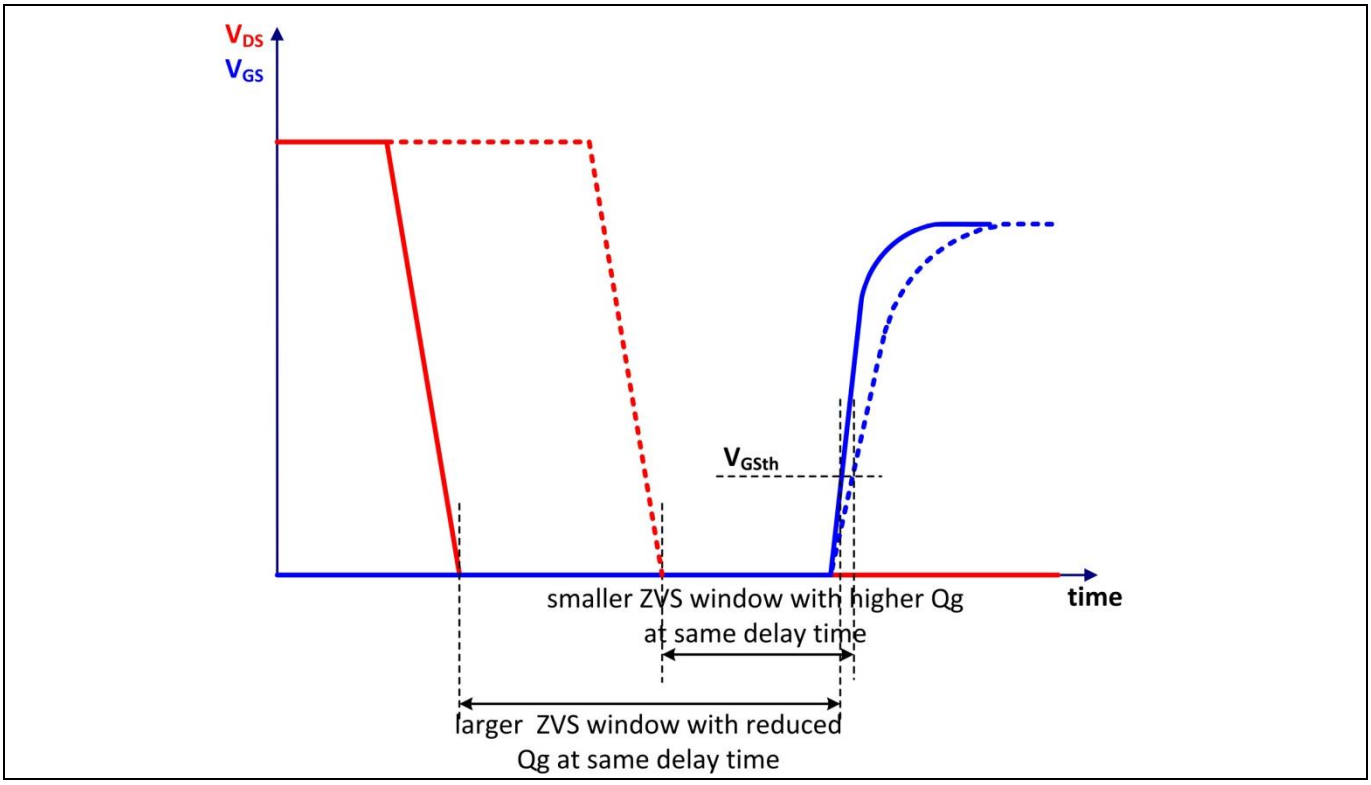

Figure 20 Simplified ZVS window (switch ON), depending on Q_g at same delay time

Figure 20 illustrates that with a lower Q_g a larger ZVS window is given with the same delay time at turning OFF. Due to this behaviour it is also possible to decrease the delay time which also gives the benefit of a shortening of the conduction time of the body diode. For example, in a phase shifted full bridge this allows to use a higher duty cycle and therefore an efficiency improvement.

3 Circuit design and layout recommendations for CFDA

As the CFDA CoolMOS™ family is based on the C6 technology, it also shows a stable and self-limiting switching behaviour and is easy to design in, even in layouts that are not perfectly optimized with respect to their parasitic environment. Although the CFDA switching behaviour is helping for a design in when compared to the CPA CoolMOS™ family, it is recommended that some layout considerations are regarded ensuring a proper functionality.
There are a number of recommendations to make with regards to circuit design and layout practices which will assure a combination of high performance and reliability. They can be recommended as if “in order of importance”, but realistically all are important, both in contribution toward circuit stability and reliability as well as overall efficiency and performance. They are not that dissimilar to recommendations made for the introduction of MOSFETs compared to bipolar transistors, or CoolMOS™ compared with standard MOSFETs; it is a matter of the degree of care.

3.1 Control dv/dt and di/dt by proper selection of external gate resistor $R_{g,ext}$

In order to exert full R_g control on the device maximum turn-off dv/dt we recommend the following procedure:

1. Check for highest peak current in the application
2. Choose external $R_{g,ext}$ accordingly not to exceed 50 V/ns
3. At normal operation condition quasi ZVS condition can be expected, which gives best efficiency results

For the CFDA CoolMOS™ family, detailed information for the switching characteristics of the CFDA family can be found in chapter 2.3, Internal gate resistor $R_{g,int}$, selflimiting di/dt and dv/dt.
There are listed diagrams which are representing the CFDA CoolMOS™ related switching behaviour:

- di/dt and dv/dt , for turn ON slopes, and
- di/dt and dv/dt , for turn OFF slopes ,

All with different external gate resistors $R_{g,ext}$[25] , see Figure 6 in Chapter 2.3.

Table 4 CFDA CoolMOS™ Internal Gate Resistor $R_{g,int}$ (all values = total sum of all internal gate resistor parts)

CoolMOS™ Type	$R_{G,int}$ (typ.)
IPx65R190CFDA	1.5 Ω
IPx65R150CFDA	1.5 Ω
IPx65R110CFDA	1.3 Ω
IPx65R080CFDA	0.75 Ω
IPx65R048CFDA	0.6 Ω
IPx65R660CFDA	6.5 Ω
IPx65R310CFDA	4.5 Ω
IPx65R420CFDA	4.0 Ω

Internal gate resistors have the advantage to be a low inductive type and lead to self limiting di/dt and dv/dt. The listed internal gate resistor $R_{g,int}$ in Table 4 above, is the sum of all internal gate resistor parts (build-in resistor, bond wire, bond finger and solder resistance). In the application the additional external gate resistor $R_{g,ext}$ allows to control the final dv/dt.

3.2 Minimize parasitic gate-drain board capacitance

Particular care must be spent on the coupling capacitances between gate and drain traces on the PCB. As fast switching MOSFETs are capable to reach extremely high dv/dt values any coupling of the voltage rise at the drain into the gate circuit may disturb proper device control via the gate electrode. As the CoolMOS™ CFDA series reaches low values of the internal C_{GD} capacitance (C_{rss} in datasheet), we recommend keeping layout coupling capacitances below the internal capacitance of the device to exert full device control via the gate circuit. Figure 21 shows a good example, where the gate and drain traces are either perpendicular to each other or go into different directions with virtually no overlap or paralleling to each other. A “bad” layout example is shown as reference to the good layout in Figure 23.

If possible, use source foils or ground-plane to shield the gate from the drain connection.

3.3 Use gate ferrite beads

We recommend the use of ferrite beads in the gate as close as possible to the gate electrode to suppress any spikes, which may enter from drain dv/dt into the gate circuit. As the ferrite bead sees a peak pulse current determined by external R_g and gate drive, it should be chosen for this pulse current. Choose the ferrite bead small enough in order not to slow down normal gate waveforms but with enough attenuation to suppress potential spikes at peak load current conditions. A suitable example is Murata BLM41PG600SN1, in an 1806 SMD package. It is rated for 6 A current and a DCR of 10 mΩ, with about 50-60 Ω effective attenuation above 100 MHz.

3.4 Locate gate drivers and gate turn-off components as close as possible to the gate

Always locate the gate drive as close as possible to the driven MOSFET and the gate resistor in close proximity of the gate pin (as an example, see R1 in Figure 21). This prevents it acting as an antenna for capacitive coupled signals. The controller/IC driver should be capable of providing a strong “low” level drive with voltage as near to ground as possible - MOS or bipolar/MOS composite output stages work well in that regard, due to low output saturation voltages. While some drivers may be deemed to have sufficient margin under static or “DC” conditions, with ground bounce, source inductance drop, etc., the operating margin to assure “OFF” mode can quickly disappear.

3.5 Use symmetrical layout for paralleling MOSFETs, and good isolation of gate drive between FETs

We recommend the use of multi-channel gate drivers in order to have separate channels for each MOSFET. Physical layout should be as symmetrical as possible, with the low impedance driver located as close as possible to the MOSFETs and on a symmetric axis.

3.6 How to make best use of the high performance of CoolMOS™ CFDA

To summarize, below recommendations are important when designing in CoolMOS™ CFDA to reach highest efficiency with clean waveforms and low EMI stress.

- Control dv/dt and di/dt by proper selection of external gate resistor
- Minimize parasitic gate-drain capacitance on board
- Use gate ferrite beads
- Locate gate drivers and gate turn-off components as close as possible to the gate
- Use symmetrical layout for paralleling

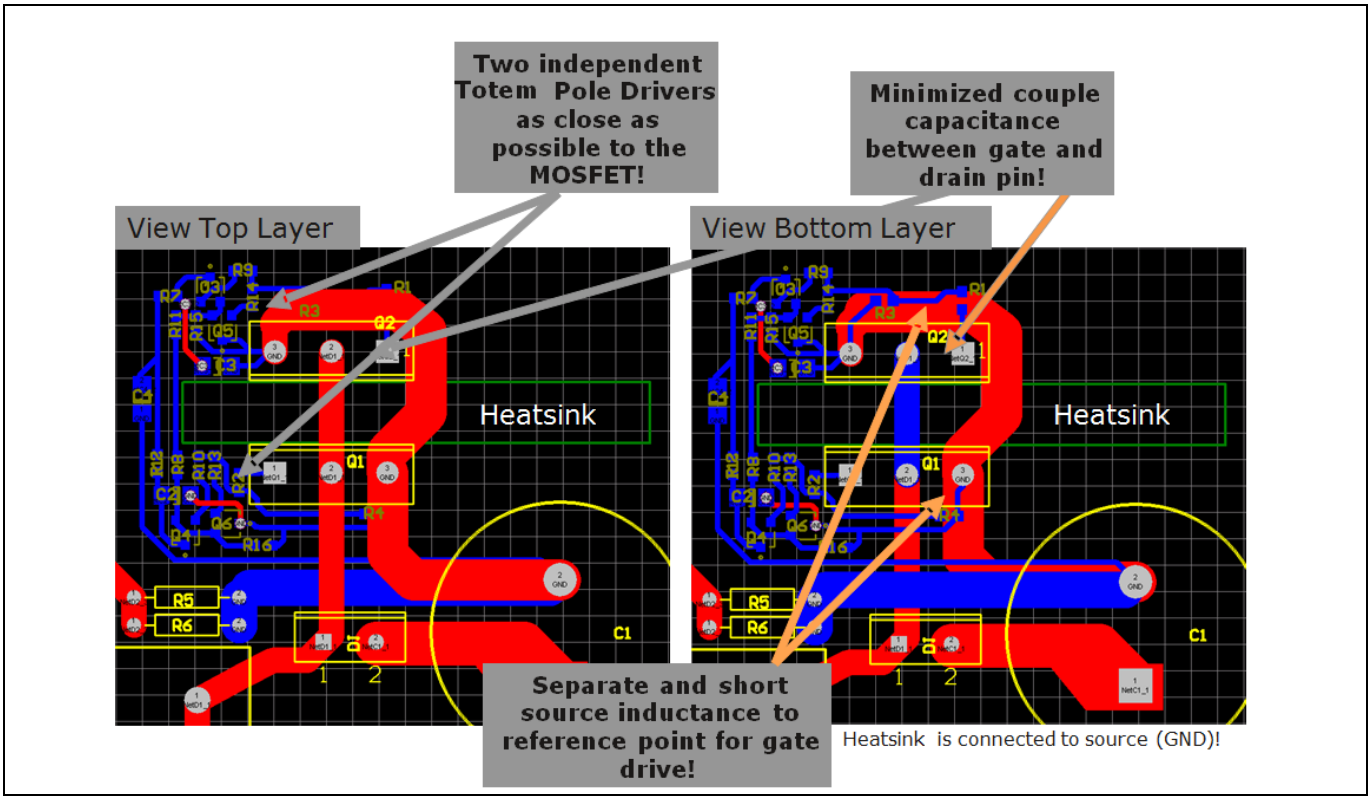

Figure 21 Good layout example ensuring clean waveforms when designing in CoolMOS™ CFDA

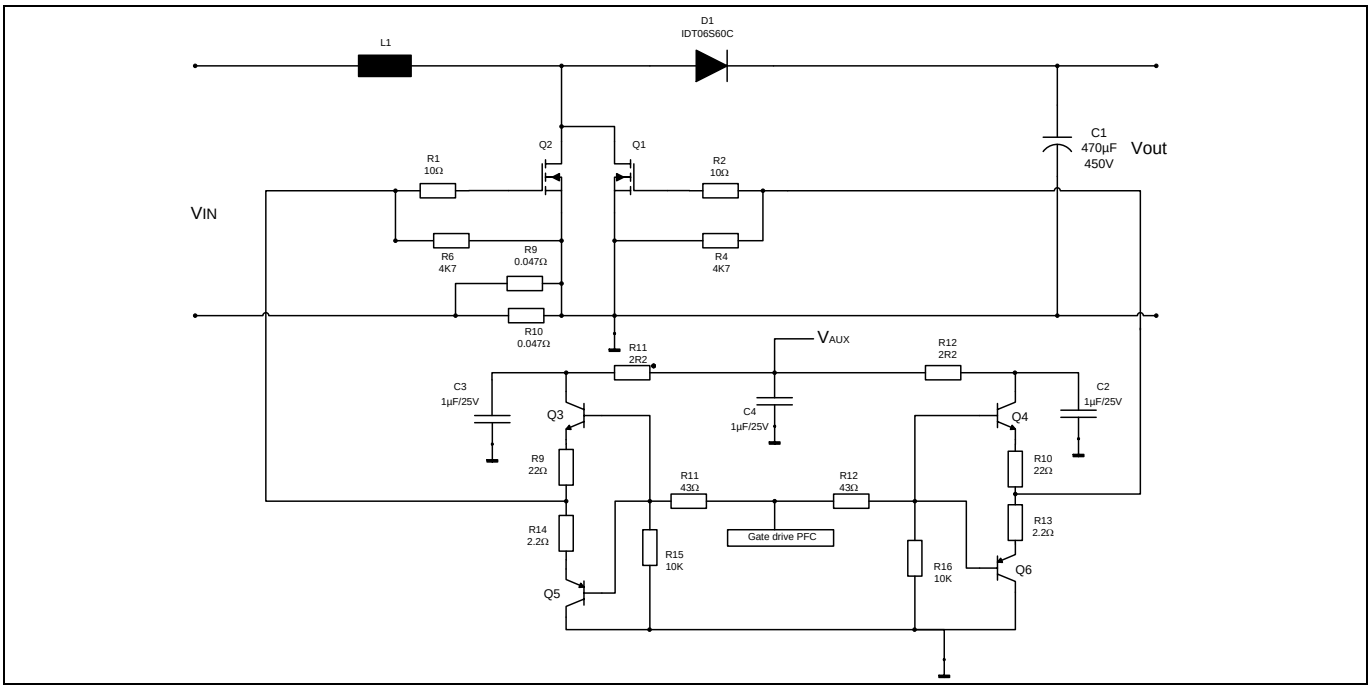

Figure 22 Good layout example showing schematic for PCB layout in Figure 21

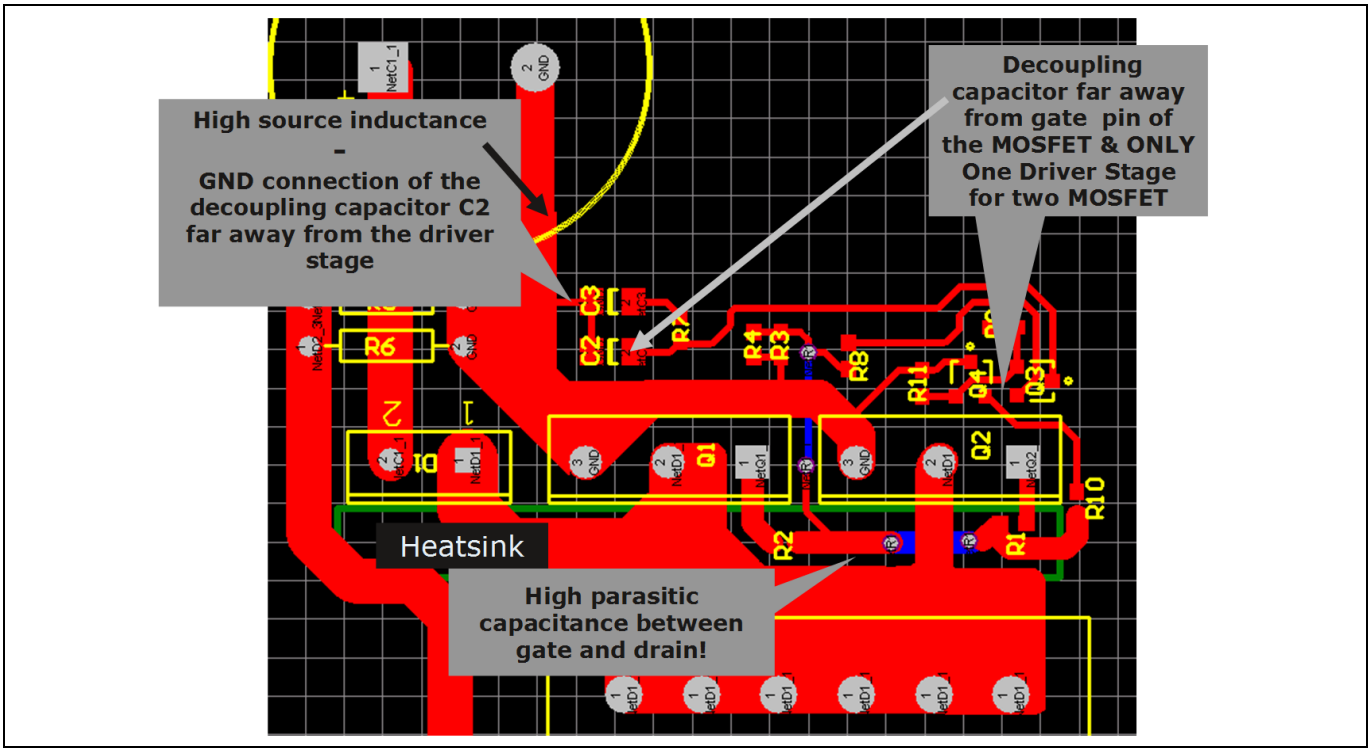

Figure 23 Bad layout example

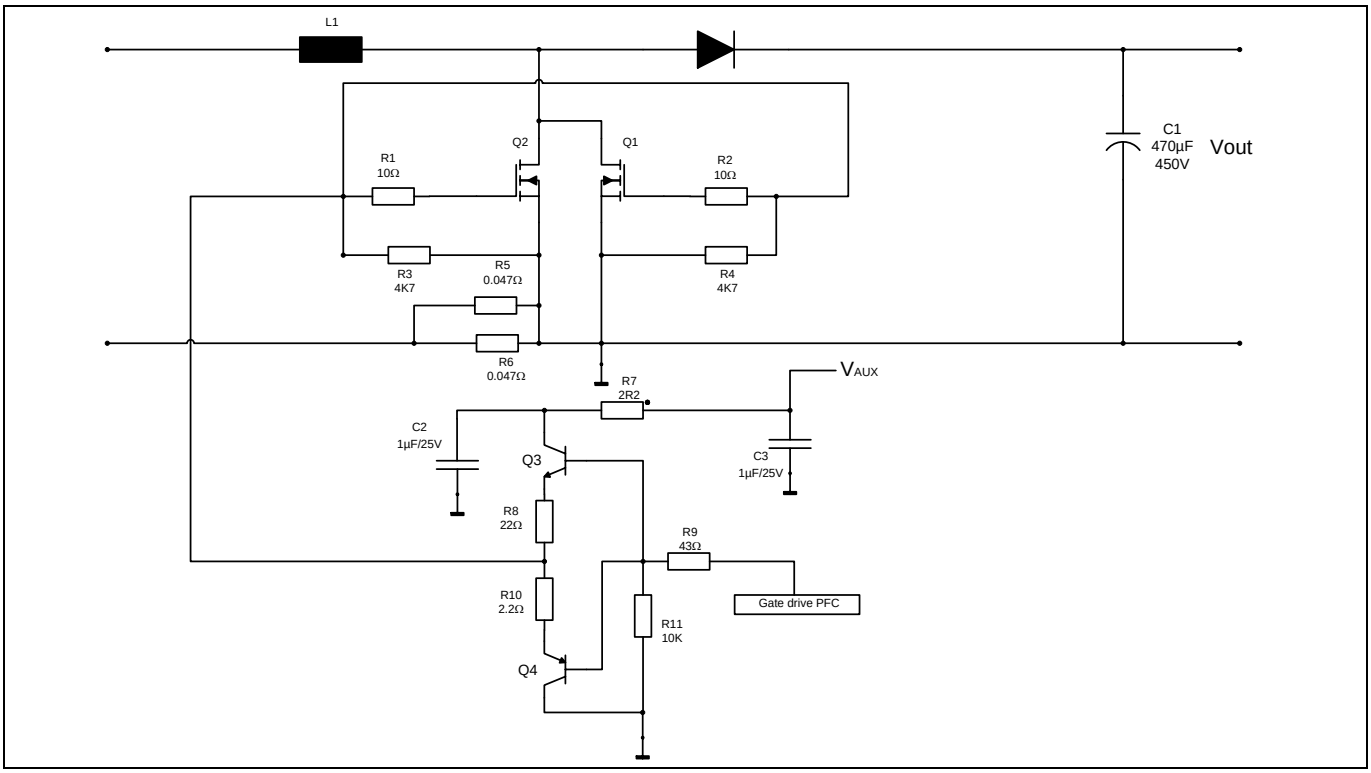

Figure 24 Schematic for bad layout example in Figure 23

4 Specific target applications

4.1 HID lighting bridge

The following schematic Figure 25 represents a typical HID[7] lamp ballast circuit, like in XENON lamp automotive.

Due to the non-optimized performance of the body diode of standard MOSFETs, D2 and D3 are used to override the body diodes of MOSFET T2 and T3 in the half bridge. For the current commutation it is now obligatory to implement fast or ultra fast diodes parallel to T2 and T3 because their trr is directly involved in the efficiency calculation. One of the main benefits of the lowered Q_{rr} of CFDA is that it is possible to remove these four diodes and use the implemented body diode with even higher efficiency in the same setup. The main benefit is therefore the reduction of needed components, with advantages in term of cost and space available on the PCB[21].

The following table visualizes the three measured efficiency values of the represented circuit.

Table 5 Efficiency comparison HID lamp ballast

T_1, T_2 half bridge MOSFETs	D_2, D_3, D_4, D_5 Diodes	Efficiency ŋ [%]
SPD07N60C3	all Diodes assembled	91,81
SPD07N60C3	not assembled (only body diode)	89,72
IPD65R660CFDA	not assembled (only fast body diode)	92,81

Note: The listed industrial type SPD07N60C3 in the table is a non automotive qualified device in former C3 technology and is used in this target application as a comparison reference device.

Another very important behaviour in an HID application is the long conduction phase of up to 2 ms of the body diode of the MOSFET which lowers the losses with a lower Q_{rr}.

Details and wave forms of the three different circuit constellations: We have compared the performance of the new devices with the commercial available SPD07N60C3 (a not automotive qualified type, used as comparison device) in a HID half bridge application. Using the new CoolMOS™ CFDA devices, the diodes D2, D3, D4 and D5 can be eliminated and allow reduced system costs Figure 25.

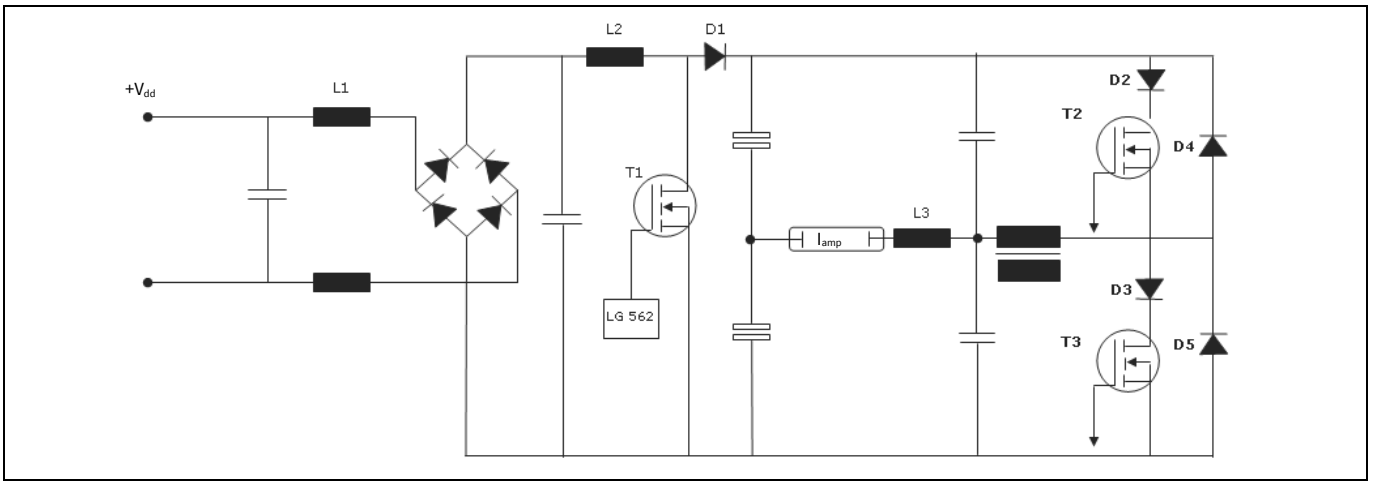

Figure 25 Typical HID half bridge circuit. By replacing the transistors T2 and T3 with the new CoolMOS™ 650 V CFDA device, the diodes D2 to D5 can be eliminated

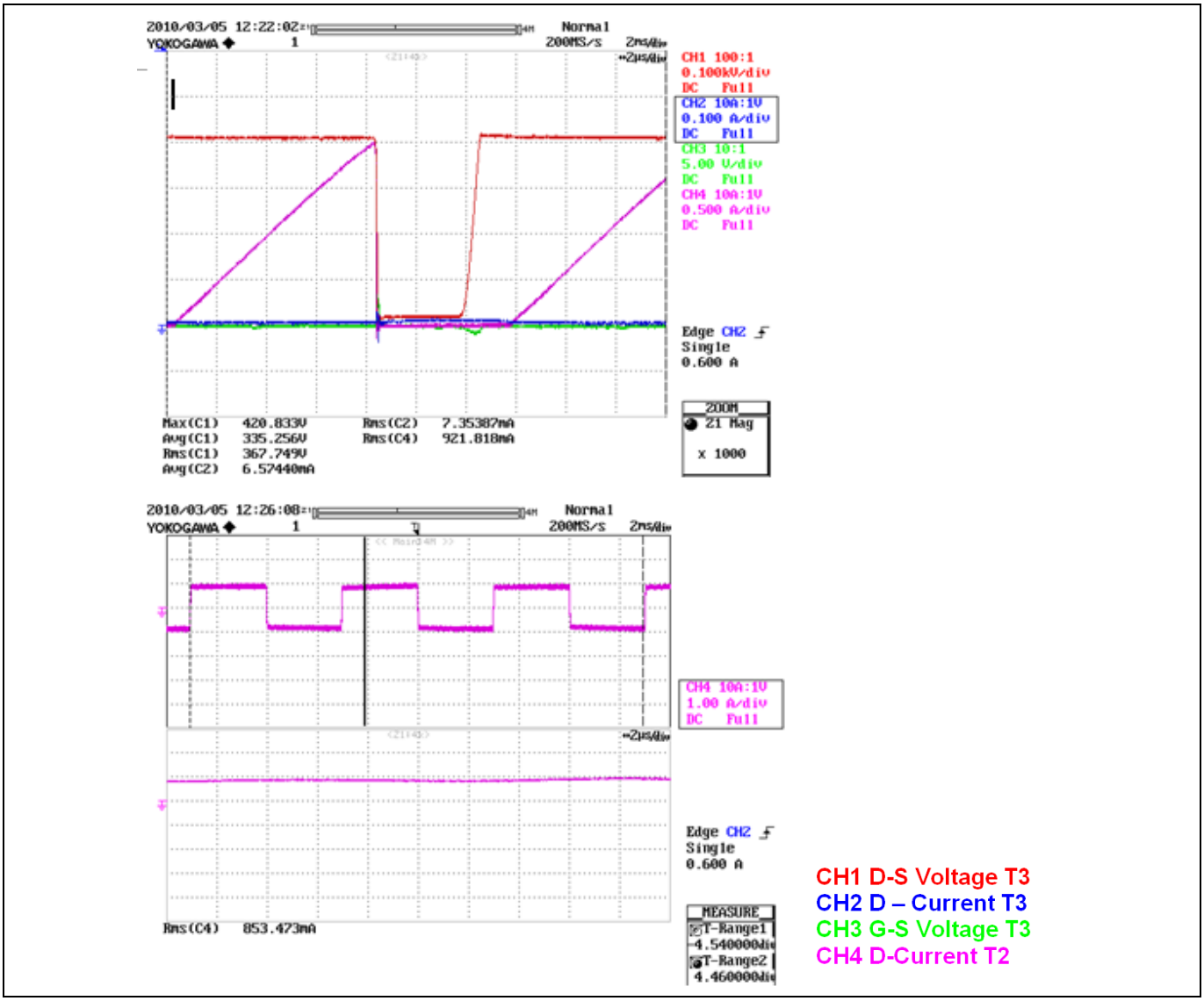

Figure 26 Circuit wave forms during the turn-off phase of transistor T3 with SPD07N60C3 as switch and with diodes D2 – D5. An efficiency of 91,81% is achieved.

For reference Figure 26 shows, the wave forms obtained by using the SPD07N60C3 device as transistors T2 and T3 and additionally the diodes D2, D3, D4 and D5. With this setup, we achieved an efficiency of 91,81%.

By removing the diodes in series to the transistors, the additional voltage drop in forward operation is eliminated. This solution requires, however, an even superior performance of the internal body diode of the MOSFET once the switching losses increase due to the reverse recovery charge stored in the MOSFET. This situation is depicted in Figure 27.

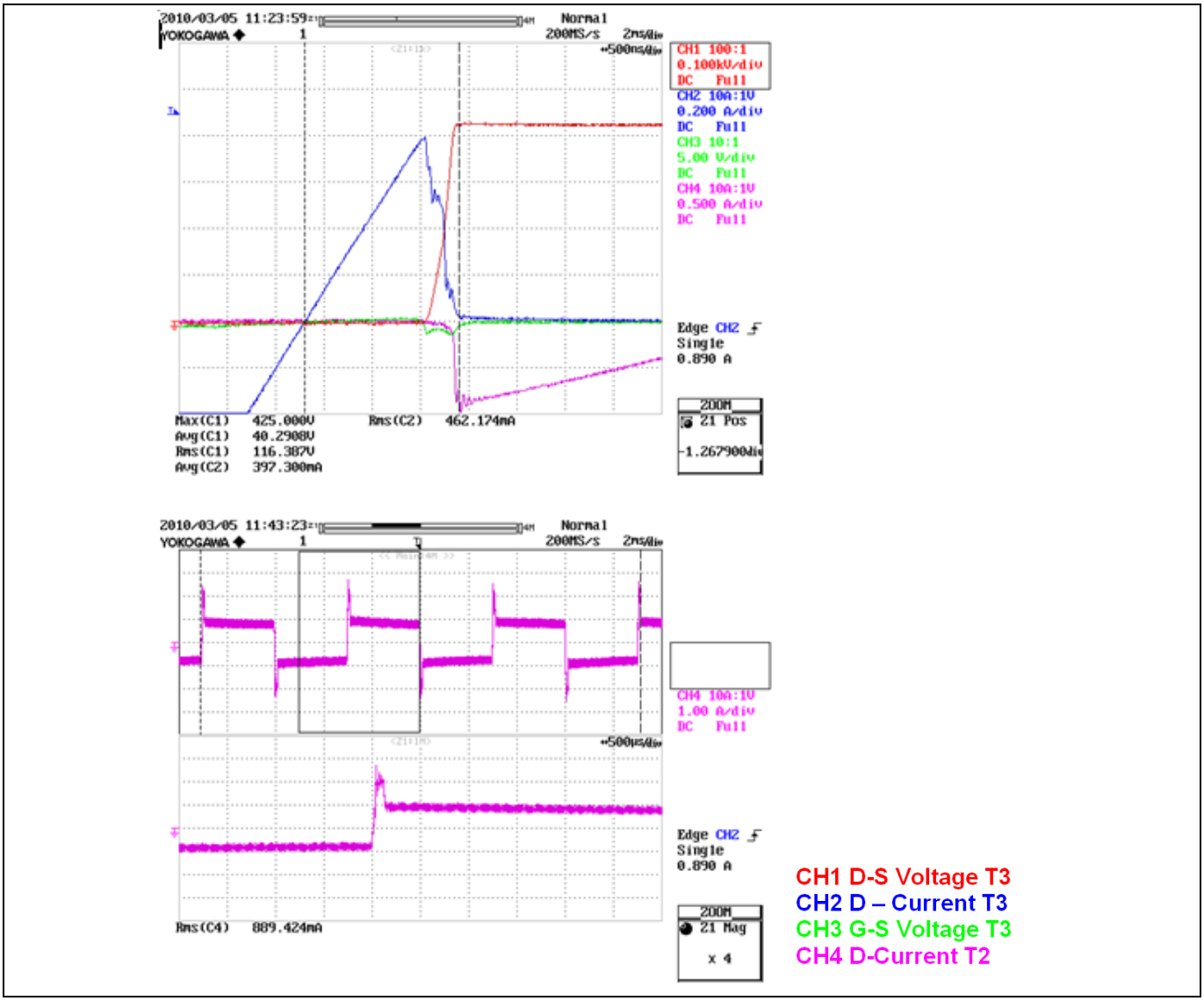

Figure 27 Circuit wave forms during the turn-off phase of transistor T3 with SPD07N60C3 without the diodes D2–D5. An efficiency of 89,72% is achieved.

In addition to increased switching losses, this setup also has the disadvantage that the MOSFET's could be destroyed due to the high reverse recovery current.

A superior solution is achieved by using the new IPD65R660CFDA device. Due to the superior performance of the internal body diode of the MOSFET, it is possible to implement a solution without the diodes D2-D5 and obtain at the same time a considerably better efficiency.

This is shown in Figure 28. The optimized construction of the internal body diode of the new IPD65R660CFDA device combined with a very low reverse recovery charge also enable reliable device operation.

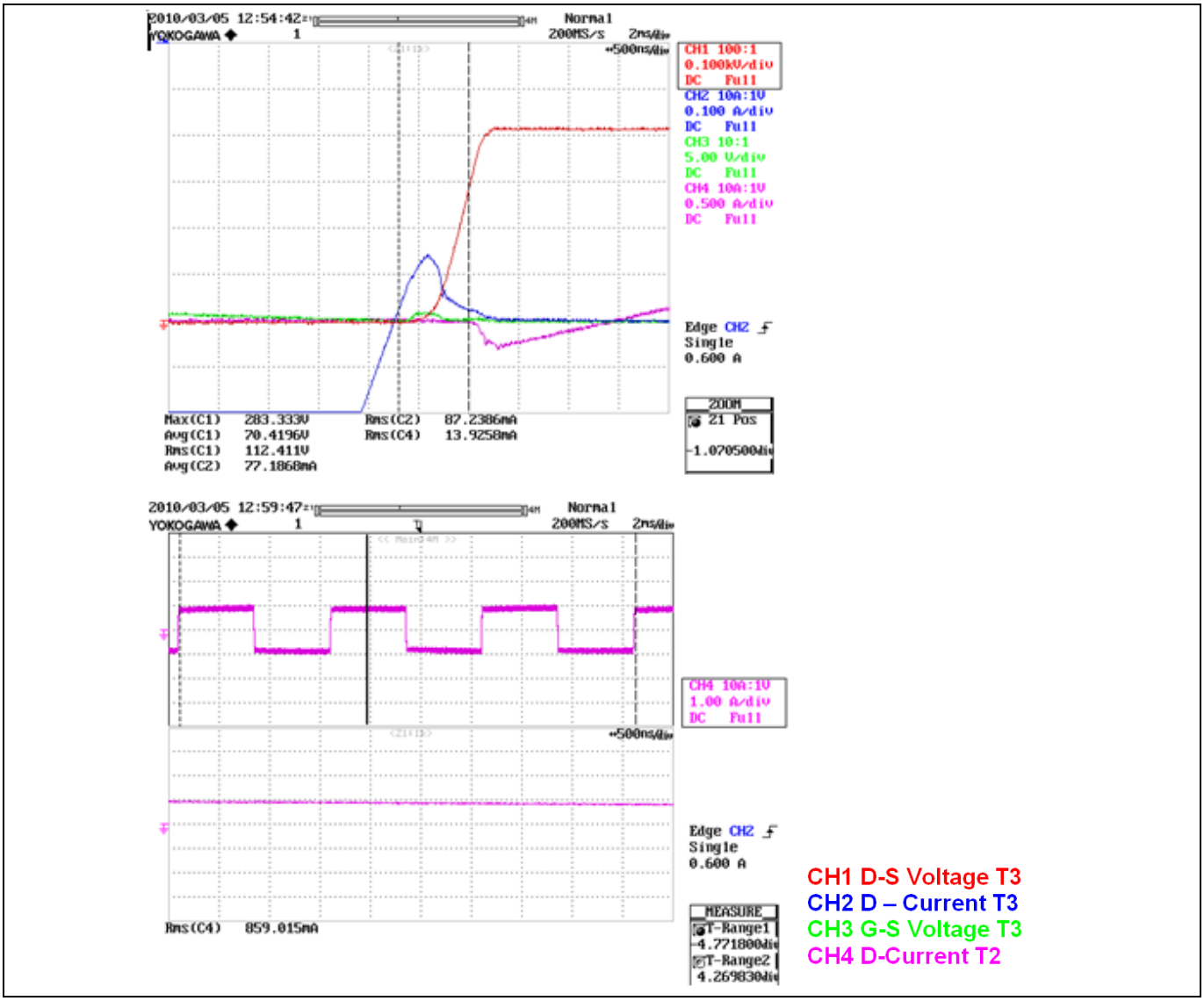

Figure 28 **Circuit wave forms during the turn-off phase of transistor T3 with IPD65R660CFDA without the diodes D2–D5. An efficiency of 92,81% is achieved.**

As a conclusion, the solution using CFDA devices for T2 / T3 (without Diodes D2 – D5) leads to a efficiency performance improvement of η = +3.09% (using C3 devices, without Diodes D2 – D5); and η = +1.0% (using C3 devices, with Diodes D2 – D5). Finally the superior solution using CFDA devices is much more robust and has a lower BOM compared to the other solutions.

4.2 DC-DC Converter (ZVS phase shifted full bridge)

The ZVS exploits the parasitic circuit elements to guarantee zero voltage across the switching device before turn ON, eliminating hence any power losses due to the simultaneous overlap of switch current and voltage at each transition, see also [9]. This chapter will describe the principal operation of the ZVS phase shifted full bridge and compare efficiency and transition time of the automotive qualified CFDA type versus the industrial CFD type.

Note: The listed industrial CFD type in this target application is a non automotive qualified device based on modified C3 technology and is used in this target application as a comparison reference device.

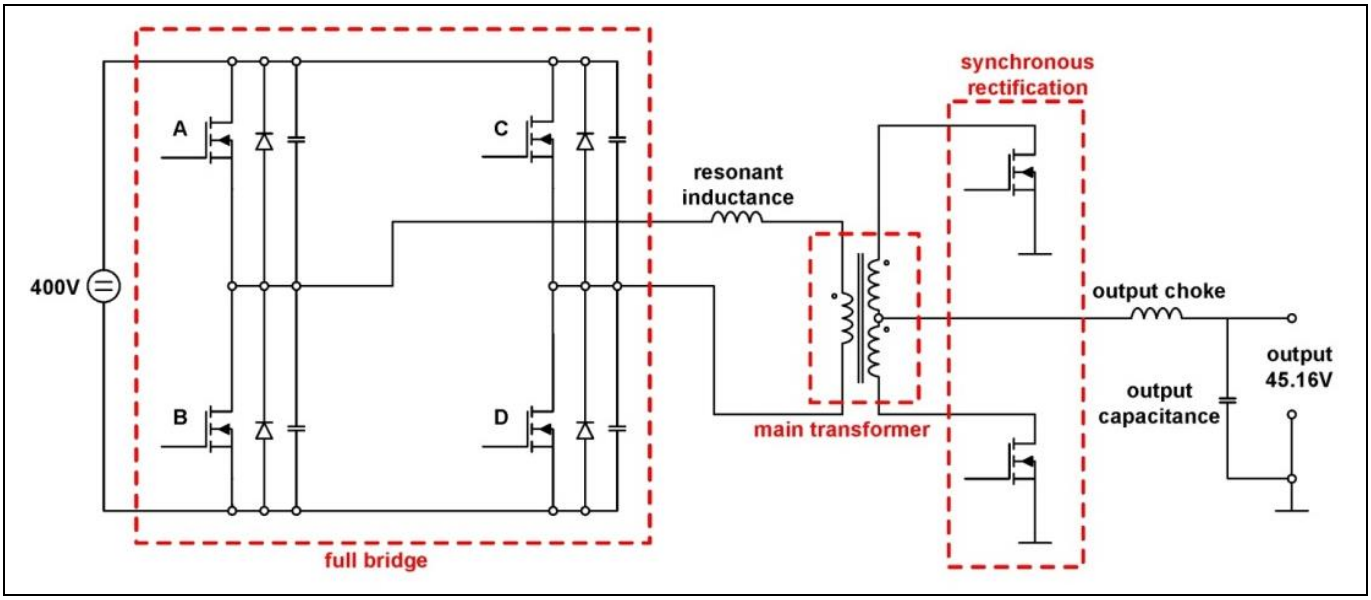

Figure 29 Simplified circuit of the ZVS phase shifted full bridge

Figure 29 shows the main parts of the ZVS phase shifted full bridge. The primary side including the full bridge (MOSFET A, B, C, D) in which the usage of CFDA will be analyzed. Furthermore, the resonant inductance which is necessary to have enough energy stored in the system to reach zero voltage switching and the primary windings of the main transformer. In the used setup the main transformer has a winding partitioning of 18 turns on the primary side and 3 plus 3 turns with a center tap on the secondary side. The synchronous rectification is done with two paralleled 200 V MOSFETs from the OptiMOS™ product line. The output choke has a value of about L = 10 mH inductance. This stage is a DC-DC converter from 400 V to 45 V which is minimum output voltage in a typical application for telecom servers. All the measurements and comparisons are done with the IPW65R080CFDA and SPW47N60CFD in the full bridge (MOSFET A, B, C, D).

First the overall efficiency of the whole converter will be analyzed. As visible in Figure 30 it is possible to reach efficiency values up to about 94.6% at 45 V output when the synchronous rectification is not activated. The efficiency measurements have been performed in this way in order to be independent from the delay time control between the primary and secondary switches, which strictly depends on the characteristics of primary devices used in each test. So, in order to see only the difference on the efficiency due to the different parts used in primary full bridge, it was obligatory only to use the body diodes for rectification.

This system efficiency has currently the highest value which can be achieved with the CFDA. Two ways are possible to improve the efficiency: using a new transformer with better primary-secondary coupling, which will reduce the peak on synchronous rectification MOSFETs, allowing the use of 150 V rating for them, with reduced $R_{DS(on)}$ losses. Additionally the output choke with about L = 10 mH inductance can be decreased (this choke is now a little bit over dimensioned to decrease the current ripple to a minimum) to reduce the copper losses and the output capacitance is represented.

The resonant inductance is dimensioned in order to achieve the best compromise between reaching ZVS at light load and copper losses impacting on the high load efficiency.

The comparative tests have been performed on a platform with V_{OUT}[26] = 45.16 V and P_{OUT}[27] = 1400 W.

Further efficiency increase can be realized by increasing the output voltage, increasing the windings of the main transformer to 22 on the primary and 4 plus 4 on the secondary side is a way to achieve a higher duty cycle window available for the regulation.

Nevertheless, current test platform is anyway valid to make a comparative analysis and show main differences between the technologies.

Figure 30 below represents the efficiency of the whole system. The measurement was done in the following way:

1. Set the delay times for A/B (Figure 29) and C/D (Figure 29) to optimize efficiency for CFD and measure efficiency
4. Plug in CFDA in the CFD optimized setup
2. Readjust delay times to optimize setup for CFDA
3. Implement the synchronous rectification in the CFDA optimized setup

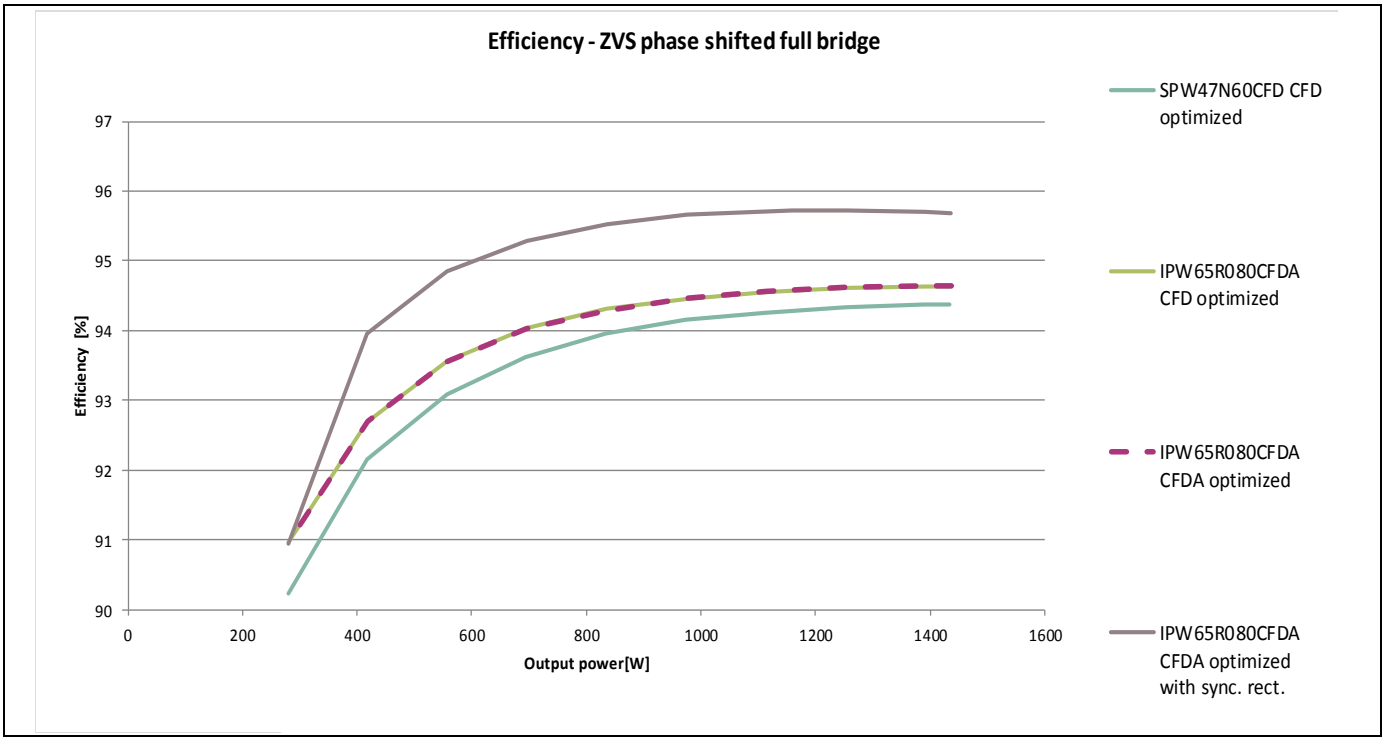

Figure 30 Efficiency comparison CFDA vs. CFD in ZVS phase shifted full bridge (Figure 29)

The main difference in the efficiency is given by the lower Q_g of CFDA which was mentioned in Chapter 2.6 (Input gate charge (Q_g)). The overall efficiency improvement is mainly due to the fact that, at $V_{DRIVER34}$[28] = 12 V, CFD needs about 32.5 mA more current from the gate drive for each MOSFET of the full bridge, that means 130 mA for the full bridge. At V_{DRIVER} = 12 V, this brings 1.56 W more losses over the whole operation area.

This result can be also theoretically achieved by calculating the driving losses as function of Q_g by:

$$P_{DRIVING}{}^{(29)} = 2 \cdot Q_g \cdot V_{DRIVER} \cdot f_{sw}{}^{(30)}$$

Where Q_G = 168 nC for CFDA and 322 nC for CFD (these values correspond to the parameters directly measured on characterized parts), so
$P_{DRIVING}$ = 1.6128 W for CFDA and 3.0912 W for CFD, from this calculation the difference in driving losses is 1.4784 W.

The next figure describes the V_{DS} transition time at 7.47 A and 1.05 A primary current which correspond to the time difference between 90% and 10% of V_{DS}.

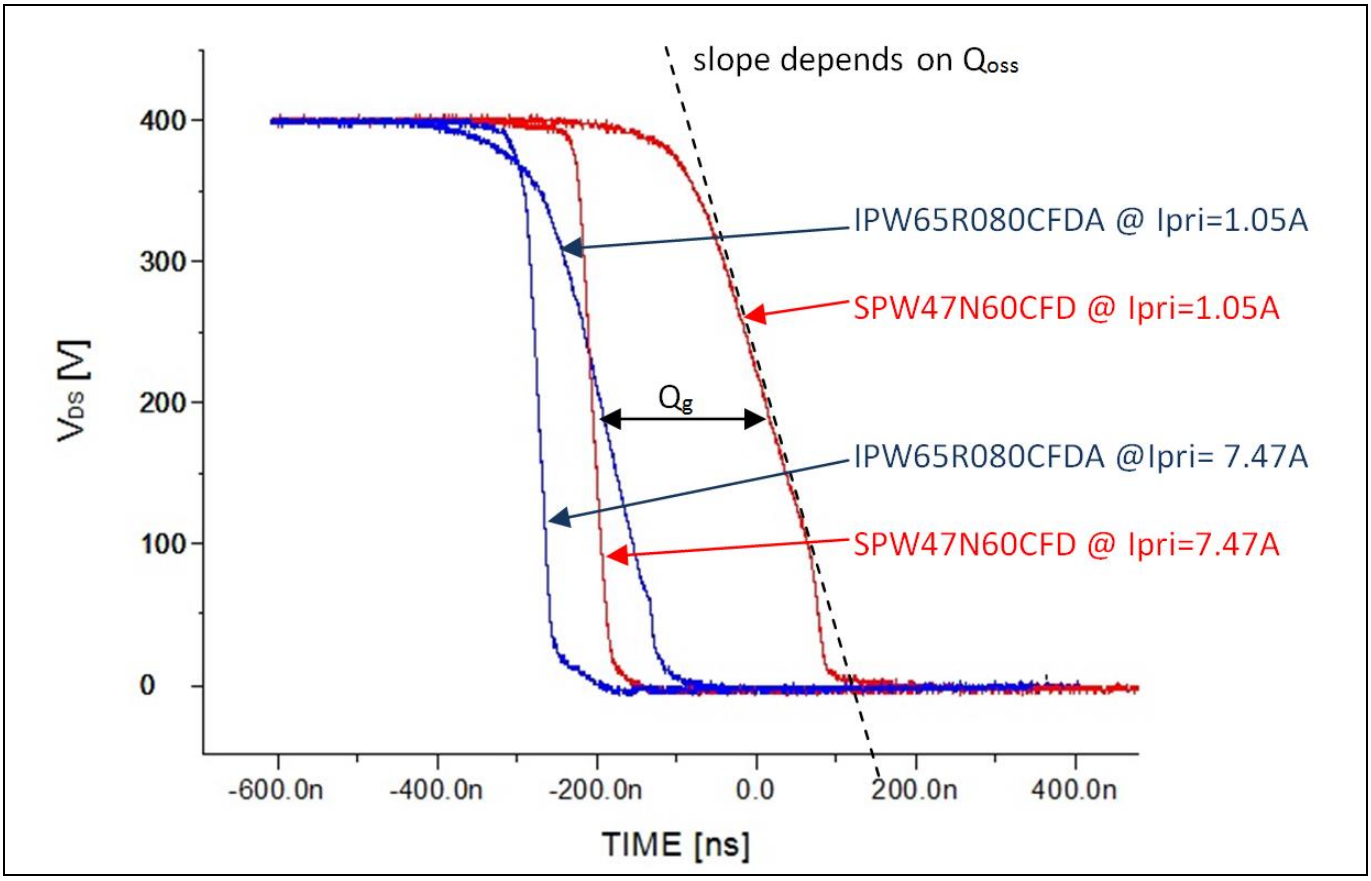

Figure 31 V_{DS} transition time of the low side MOSFET (D) on the primary side of the ZVS phase shifted full bridge (Figure 29). Comparison IPW65R080CFDA (blue) vs. SPW47N60CFD (red) at different loads

For all technologies, the V_{DS} transition time is independent on R_g and mainly depends on the Q_{oss}(31). Therefore, it is decreasing with increasing load.

In our case, the V_{DS} transition time is a little bit lower for CFD. This is due to the lower Q_{oss} of CFD compared to CFDA. This lower Q_{oss} can be negligible because firstly there is only a slight influence at low loads (when there is enough energy in the system the advantage of faster removing the charge of the output capacitance of the MOSFET does not exist anymore), secondly the impact of the driving losses is much higher. On the other hand, for all technologies, t_{d_off}[32] increases with increasing $R_{g\_turn\text{-}off}$[33]) and decreases with increasing load. In fact, at very light load, the contribution of V_{DS} transition (from 10% to 90%) is predominant rather than R_g. As soon as the load is increasing, the contribution of R_g becomes more important. So at light load, the turn-off time duration is also influenced by Q_g, in fact it is lower for CFDA compared to CFD, giving benefit in ZVS design at light load.

Furthermore with the CFDA it is visible that the time window between high load and light load is much more narrow than with the CFD.

5 Detailed explanations

5.1 Cosmic radiation impact

The cosmic radiation impact is depending on the following paramters

- V_{DS} voltage
- Junction temperature
- Altitude
- Device silicon area

as a profile versus time.

For the impact of the cosmic radiation please regard the explanation in the datasheet [10] in Chapter “Electrical characteristics, static characteristics, drain-source breakdown voltage”

5.2 Operation in linear mode

We do not recommend to operate our automotive MOSFET’s in linear mode. For the constraints of operating automotive MOSFETS in this mode and the related thermal instability under special circumstances we refer to the related Infineon application note:

http://www.infineon.com/dgdl/AutomotiveMOSFETsinLinearApplication-ThermalInstability.pdf

5.3 Parallel operation of power MOSFETS

For the parallel operation of power MOSFETS we refer to the related Infineon application note:

http://www.infineon.com/dgdl/Parallel_Operation_of_Power_MOSFET_.pdf

5.4 Recommendations for electrical safety and isolation in high voltage applications

For a proper functionality of discrete components according to electrical safety and isolation in HV applications, we refer to the related Infineon application note:

http://www.infineon.com/dgdl/Safety_and_isolation_high_voltage_discrete.pdf

5.5 Further datasheet explanation automotive MOSFETS

For a further detailed explanation of Datasheet topics, we refer to the related Infineon application note:

http://www.infineon.com/dgdl/20140428_appnote_MOSFET_Datasheet_explanation.pdf

5.6 General recommendations for assembly of Infineon packages

According to general recommendations for assembly Infineon packages, we refer to the related Infineon application note:

http://www.infineon.com/dgdl/General%20Recommendations%20for%20Assembly%20of%20Infineon%20Packages.pdf

6 Conclusion

Infineon's new CoolMOS™ CFDA device, offers the lowest $R_{DS(on)}$ combined with a high blocking voltage of 650 V. This new device features also a very low reverse recovery charge combined with a robust integral body diode. A specification of the max-values of the Q_{rr} and t_{rr} will be available in the datasheet. We have also evaluated the performance of this new device in a typical HID half bridge circuit, leaving out four diodes and getting superior efficiency. A second evaluation showed the performance improvement in a DC-DC converter with zero voltage switching (ZVS phase shifted full bridge). Due to the breakdown voltage of 650 V and the robust construction of the integral body diode, this new device offers additional safety against destruction during hard commutation of the MOSFET.

7 Product portfolio and naming system

650 V CoolMOS™ C6 CFDA series follows the same naming guidelines as already established with the former series e.g. IPW65R080CFDA:

650 V CoolMOS™ CFDA ACTIVE & PREFERRED

Product type	$R_{DS(on)}$ @ T_J = 25°C V_{GS} = 10 V [mΩ]	$I_{D,max.}$ @ T_J = 25°C [A]	$I_{D\_puls,max}$ [A]	$V_{GS(th),min-max}$ [V]	$Q_{G,typ.}$ [nC]	$R_{thJC,max.}$ [K/W]	Package
IPD65R420CFDA	420	8.7	27	3.5...4.5	32	1.5	TO-252
IPD65R660CFDA	660	6	17	3.5...4.5	20	2	TO-252
IPB65R110CFDA	110	31.2	99.6	3.5...4.5	11	0.45	TO-263
IPB65R150CFDA	150	22.4	72	3.5...4.5	86	0.64	TO-263
IPB65R190CFDA	190	17.5	57.2	3.5...4.5	68	0.83	TO-263
IPB65R310CFDA	310	11.4	34.4	3.5...4.5	41	1.2	TO-263
IPB65R660CFDA	660	6	17	3.5...4.5	20	2	TO-263
IPP65R110CFDA	110	31.2	99.6	3.5...4.5	11	0.45	TO-220
IPP65R150CFDA	150	22.4	72	3.5...4.5	86	0.64	TO-220
IPP65R190CFDA	190	17.5	57.2	3.5...4.5	68	0.83	TO-220
IPP65R310CFDA	310	11.4	34.4	3.5...4.5	41	1.2	TO-220
IPP65R660CFDA	660	6	17	3.5...4.5	20	2	TO-220
IPW65R048CFDA	48	63.3	228	3.5...4.5	27	0.25	TO-247
IPW65R080CFDA	80	43.3	127	3.5...4.5	16	0.32	TO-247
IPW65R110CFDA	110	31.2	99.6	3.5...4.5	11	0.45	TO-247
IPW65R150CFDA	150	22.4	72	3.5...4.5	86	0.64	TO-247
IPW65R190CFDA	190	17.5	57.2	3.5...4.5	68	0.83	TO-247

Figure 32 Product portfolio

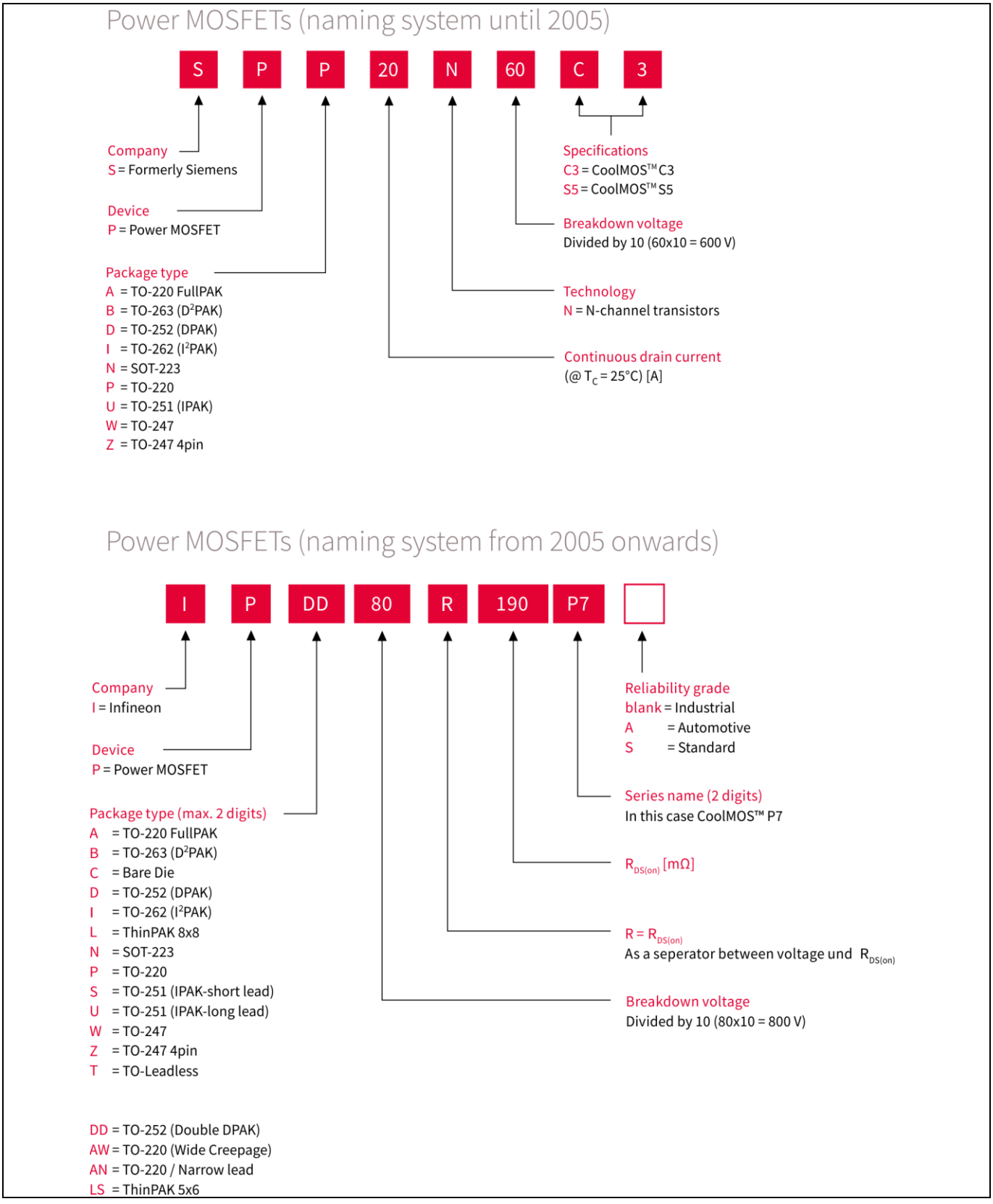

Figure 33 Naming system

8 LIST OF ABBREVIATIONS

[1]	…	CFDA	CoolMOS™ Fast Diode Automotive	Page 4
[2]	…	MOSFET	Metal Oxide Semiconductor Field Effect Transistor	Page 4
[3]	…	Q_G	Gate charge [10]	Page 4
[4]	…	$t_{rr,max}$	maximum reverse recovery time [10]	Page 4
[5]	…	$Q_{rr,max}$	maximum reverse recovery charge [10]	Page 4
[6]	…	ZVS	Zero Voltage Switching	Page 4
[7]	…	HID	High Intensity Discharge	Page 4
[8]	…	LED	Light Emitting Diode	Page 4
[9]	…	Q_{rr}	Reverse recovery charge [10]	Page 5
[10]	…	$T_{junction}$	Junction temperature of a MOSFET [10]	Page 5
[11]	…	C3	CoolMOS™ technology	Page 5
[12]	…	C6	CoolMOS™ technology	Page 5
[13]	…	$V_{(BR)DSS}$	Drain-Source-substrate breakdown voltage [10]	Page 8
[14]	…	C_{GS}	Internal gate source capacitance $C_{GS} = C_{iss}(34)-C_{rss}$	Page 20
[15]	…	C_{GD}	Internal gate drain capacitance $C_{GD} = C_{rss}$	Page 20
[16]	…	V_{GS}	Gate source voltage	Page 20
[17]	…	V_{DS}	Drain source voltage	Page 20
[18]	…	$R_{DS(on)}$	Drain-source on-state resistance [10]	Page 7
[19]	…	t_{rr}	Reverse recovery time [10]	Page 12
[20]	…	I_{rrm}	Maximum reverse recovery current [10]	Page 12
[21]	…	PCB	Printed Circuit Board	Page 28
[22]	…	$V_{DS,max}$	Maximum measured drain source voltage	Page 17
[23]	…	$R_{g,int}$	Internal gate resistor	Page 9
[24]	…	C_{rss}	MOSFET reverse transfer capacitance $C_{rss} = C_{GD}$ [10]	Page 10
[25]	…	$R_{g,ext}$	External gate resistor	Page 10
[26]	…	V_{OUT}	Output voltage	Page 32
[27]	…	P_{OUT}	Output power	Page 32
[28]	…	V_{DRIVER}	Gate drive voltage	Page 33
[29]	…	$P_{DRIVING}$	Gate drive power	Page 33
[30]	…	f_{sw}	Switching frequency	Page 33

Table of contents

9 REFERENCES

The referenced application notes can be found at http://www.infineon.com

Direct link to the CoolMOS™ automotive site:

http://www.infineon.com/cms/en/product/power/automotive

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Revision History

Major changes since the last revision

Page or Reference	Description of change
Revision 0.4	First Release
Revision 0.5	Update of Figure 32; Update Look & Feel
Revision 0.6	MCOM style check

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