C7 Gold

CoolMOS™ C7 Gold + TOLL = A Perfect Combination

About this document

Scope and purpose

This document is intended to describe Infineon's new TOLL (TO-Leadless) SMD package for high-voltage applications, fitted with the high performance 650 V CoolMOS™ C7 Gold Superjunction (SJ) MOSFET technology.

The major advantages for high voltage and high power, hard switching applications such as PFC and TTF will be discussed in detail. The document will focus on applying 650 V C7 Gold SJ MOSFET technology in the high voltage TOLL SMD package in order to increase power density and optimize switching performance.

Intended audience

This document is intended for design engineers who want to improve their high voltage power conversion applications by moving from through hole packages to SMD devices.

We listen to your comments

Is there any information within this document that you feel is wrong, unclear or missing? Your feedback will help us to continuously improve the quality of this document. Please send your comments or suggestions (including a reference to this document) to: support@infineon.com.

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1 Introduction

The last decade of SMPS (switched mode power supply) development was dominated by the trend towards higher power density and cost optimization.

Ever-faster switching speeds, ever-lower losses, optimization of board space and minimized total cost of ownership (TCO) are among the critical challenges facing today's power supply designers. By driving down on-state resistance while providing 'GaN-like' switching losses, the latest super junction (SJ) MOSFET technologies hold the key to addressing these challenges in modern hard- and soft-switching applications.

One can see this evolution of the silicon whereby the packages predominantly remained the well-established THD (through hole devices), such as TO-220 or TO-247 with their derivates. There became a trend for using more SMD packaged devices in order to support fast switching silicon and also to reduce the parasitic inductance associated with the long leads on many THD packages. Despite all the advantages of the available SMD devices they still have a significant challenge in respect of cooling. This remains one of the major challenges for high power PFC (power factor correction) circuits and is the main reason that TO-220 and TO-247 are still the main package types used for this application.

TOLL in combination with the C7 Gold technology offers the possibility to move away from through hole packages in high Power PFC circuits towards SMD solutions for the first time. This is a very important enabler for power density improvements and cost savings.

1.1 C7 Gold performance

The C7 Gold silicon technology is based on the well-known 650 V CoolMOS™ C7 that was introduced in early 2013. Since then, continued development has further improved the technology. One of the major evolutions of the C7 technology is the reduction of E_{oss} as is seen in Figure 1. For hard switching applications this energy is always lost because it is converted into heat once the device is turned on the next time with a positive gate signal. All the improvements offered by the C7 Gold technology result in reduced switching losses and, very importantly, also in reduction of the thermal resistance (R_{th}) of the device.

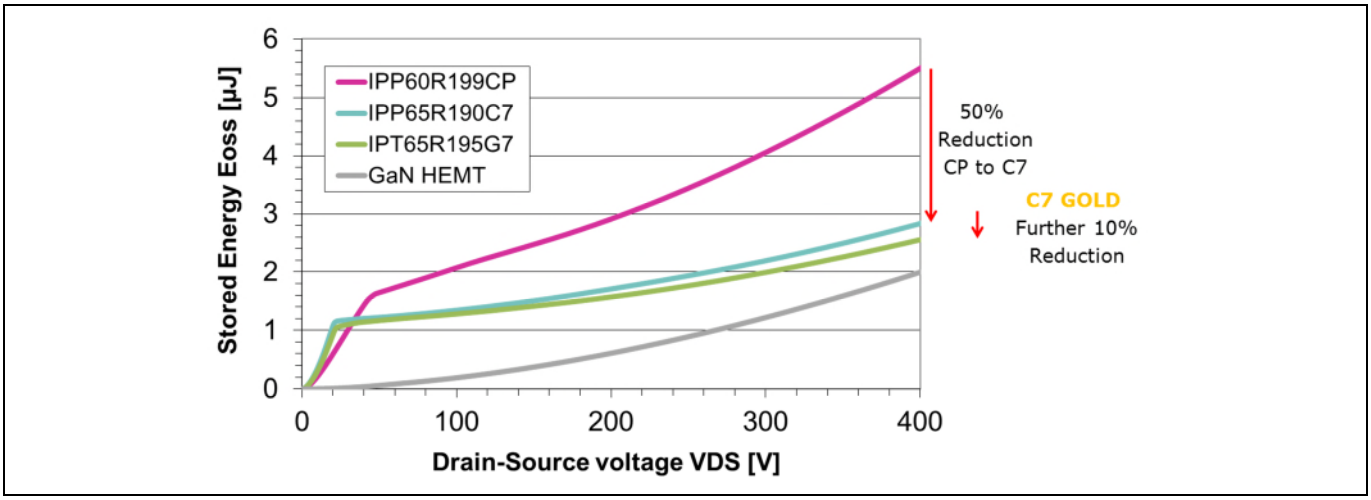


Figure 1 Stored E_{oss} in the output capacitance for different technologies

The new C7 Gold will be available with $R_{DS(on)}$ from 33 mOhm up to 195 mOhm. The 33 mOhm devices offer the lowest available $R_{DS(on)}$ for any 650 V SMD device worldwide. It is the perfect use case for high power hard switching PFC as well as for low switching and conduction loss dominated bridge rectifier replacement.

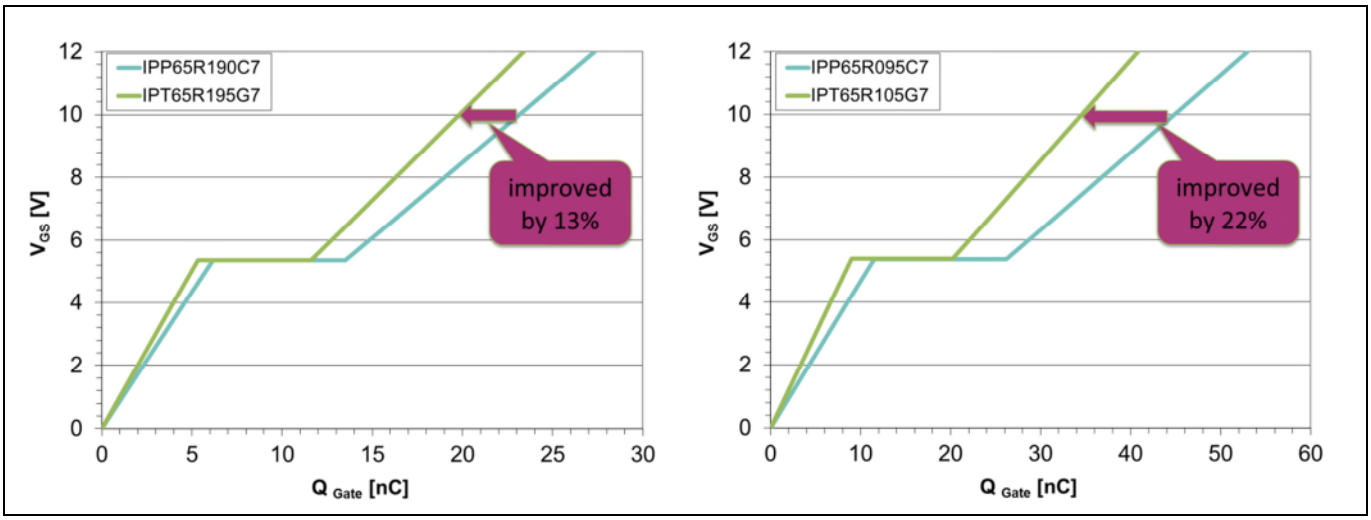


Figure 2 Gate charge comparison for 195 and 105 mOhm

Although lower Q_G means lower gate driving losses, Q_{GD} is a significant parameter related to switching transition times and losses. Figure 2 shows the gate charge comparison between 650 V CoolMOS™ C7 and the 650 V CoolMOS™ C7 Gold based on the 195 mOhm and 105 mOhm devices. One can see that the C7 Gold offers approximately 15-20% lower gate charge and will therefore switch much faster with much lower switching losses.

Note: There is no $R_{DS(on)}$ comparable device from any technology available until now, to allow a comparison with the 33 mOhm CoolMOS™ C7 Gold. Therefore Figure 2 and Figure 3 focus on the 195 mOhm and 105 mOhm devices only because in this range there are devices with compareable R_{DSon} available.

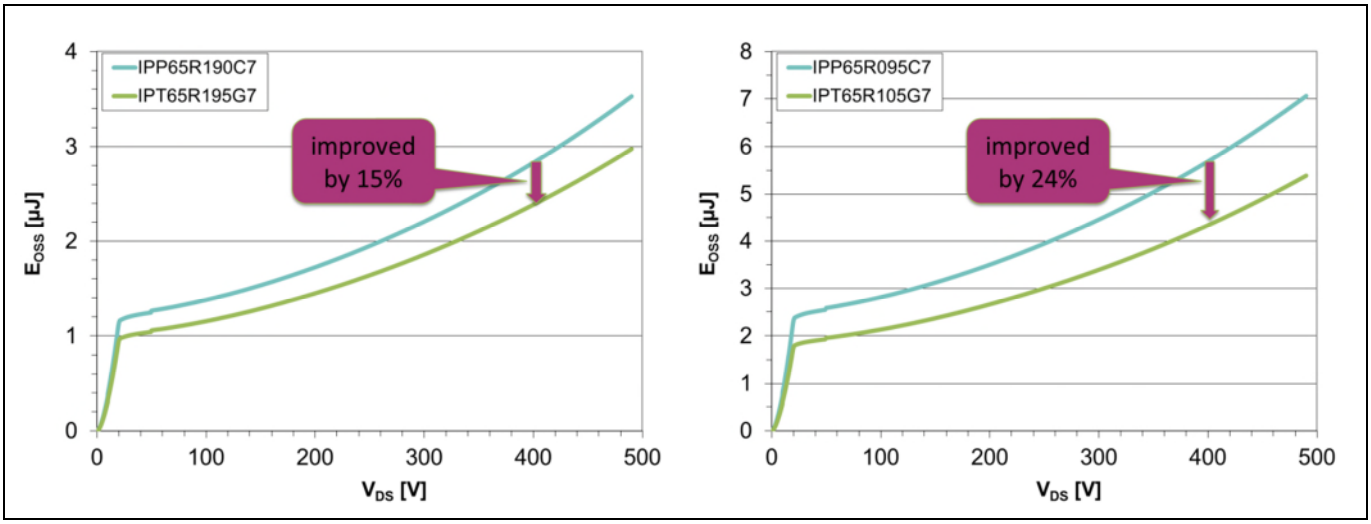


Figure 3 E_{oss} comparison for 195 and 105 mOhm

The E_{oss} reduction has a very high impact on the performance of conventional PFC topologies where the hard switching of the MOSFET is dominant. For this application the E_{oss} energy will become power losses during the turn on phase of the switch. The higher the switching frequency the more impact this performance improvement will have on overall energy efficiency.

In fact, the switching losses of the CoolMOS™ C7 Gold are reduced similar to the $R_{DS(on)}$ step within the 650 V CoolMOS™ C7 technology. This means that the 105 mOhm C7 Gold device exhibits the same switching losses as

the 125 mOhm C7 device. It is now possible to use (for the same power range) on step lower $R_{DS(on)}$ in order to reduce the overall power losses but retain the same light load efficiency.

1.2 TOLL (TO-Leadless) SMD package

The TOLL (P/PG-HSOF-8-2) package is a recently developed SMD package optimized for high power, high voltage and high reliability applications. It is based on the TOLL for low and medium voltage version (P/PG-HSOF-8-1) which is successfully used in industrial and automotive applications.

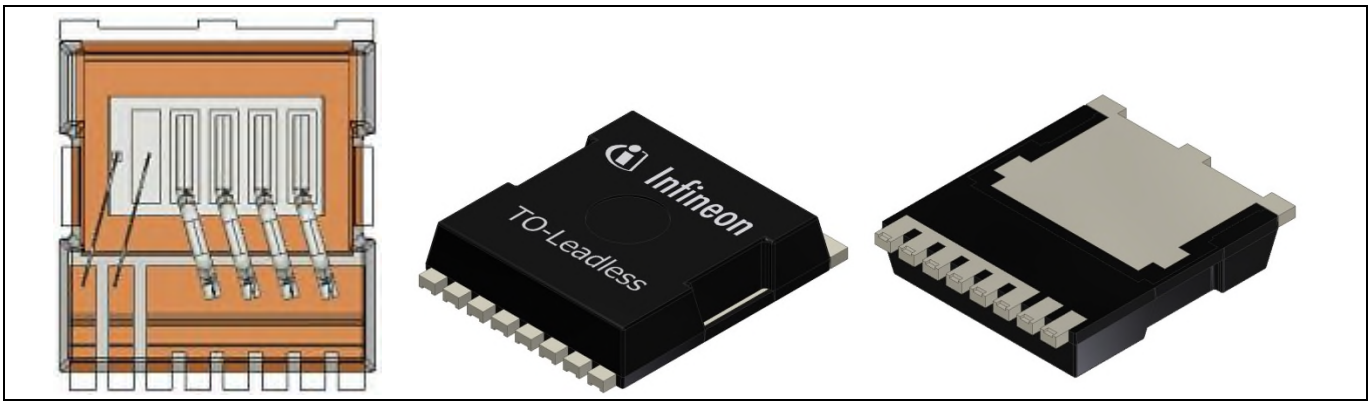


Figure 4 TOLL drawing from inside, top and bottom view

The small mechanical dimensions allow compact designs to be realized. The high current capability combined with the low thermal resistance (R_{thJC}) results in lower chip temperatures and therefore enables the designer to achieve higher power density and higher reliability.

One of the best quality aspects of the TOLL package is the TCOB (thermal cycling on board) reliability - especially when focused on FR4 PCB assembling. Please refer to the separate section in this document for more information about TCOB.

All mechanical details shown in the following chapters and a general recommendation for how to handle Infineon´s SMD devices can be found at www.infineon.com/packages.

Detailed mechanical information about the TOLL (P/PG-HSOF-8-2) is also available at http://www.infineon.com/cms/en/product/package.html?package=/packages/SMD_-_Surface_Mounted_Devices/P-PG-HSOF/.

Note: The TOLL package will be one of the packages of choice for Infineon's future CoolGaN™ portfolio.

2 The combination of C7 Gold and TOLL

The combination of the 650 V CoolMOS™ C7 Gold with the TOLL package is a very powerful combination.

The improved silicon C7 Gold technology offers better switching performance which reduces the switching losses when compared with devices of the same $R_{DS(on)}$. Due to the very low switching losses the technology is predominantly used to increase the switching frequency in order to reduce the size of the magnetic components, which offers significant cost reduction and increased power density.

The TOLL SMD package accepts an increased size silicon chip inside and offers 4-pin functionality in order to optimize the switching behavior. The lowest $R_{DS(on)}$ offered in the TOLL package is 33 mOhm compared to 45 mOhm in the TO-220 or D²PAK.

2.1 R_{thJC} improvement

The thermal resistance (R_{thJC}) of the device is a very important measure for the cooling performance of the device. The R_{thJC} improvement of C7 Gold is shown in Figure 5. For the same $R_{DS(on)}$, there is a 20% improvement achieved.

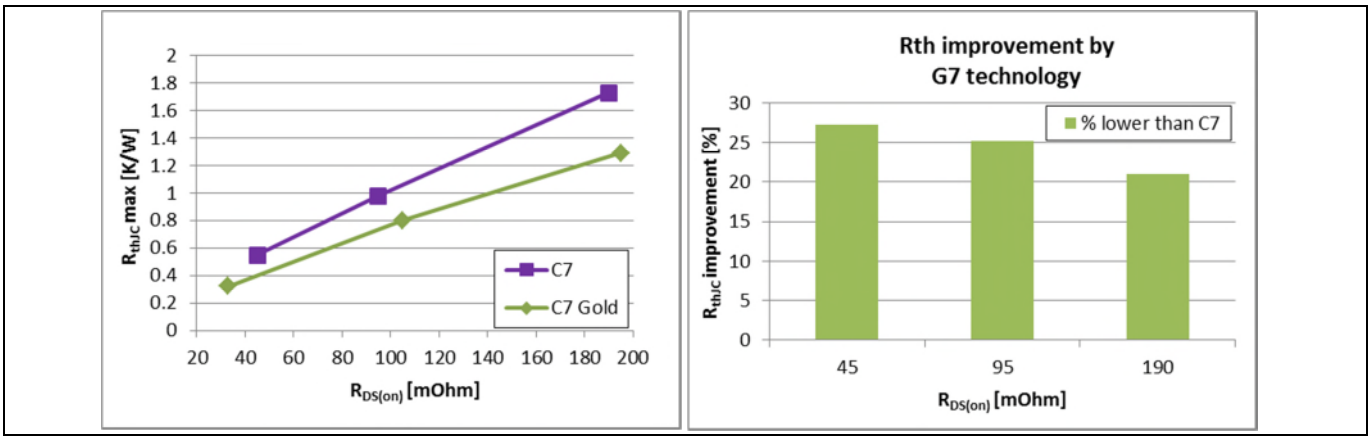


Figure 5 R_{thJC} vs $R_{DS(on)}$ comparison between C7 Gold in TOLL and C7 in D²PAK package

The R_{thJC} improvement shown in Figure 5 results (according the equation shown in Figure 6) in lower silicon temperatures for same level of heat transfer or power losses. The chart on the right shows the normalized improvement as a percentage based on interpolated $R_{DS(on)}$ for the C7 Gold devices against the $R_{DS(on)}$ the C7 technology offers. It can be seen that this will result in lower $R_{DS(on)}$ as the $R_{DS(on)}$ significantly increases with the temperature of the device.

$$R_{thJC} = \frac{\Delta_T}{P_v} \gg \Delta T = R_{thJC} \times P_v$$

Figure 6 R_{th} impact on temperature difference

Knowing the lower temperature of the device it is possible to either reduce the cooling effort or to increase the power range for a given configuration. Alternatively, a designer might consider increasing the reliability by maintaining a lower temperature within the system.

2.2 4pin functionality

The TOLL package offers 6 source connections for the drain current and one source sense connection for the gate reference potential. This source sense connection is designed for the gate charging power and should not

be used to carry the main drain current as it does not have the current handling capability of the other 6 power source connections. It is possible to connect all the source (power and sense) connections together without using the 4pin functionality of the package.

The most important reason to use a separate source sense pin for controlling the gate is to improve the efficiency by reducing switching losses and therefore minimizing heat generation. Reducing switching time is a well-understood method for improving efficiency – the faster a switch turns on and off, the shorter the time period during which a voltage exists across it and a current is flowing through it. Voltage multiplied by current is equal to power (loss), hence a switch that spends less time dissipating power is by definition a more efficient switch.

As well as this important advantage of the 4pin functionality, the gate waveforms will be much cleaner by using the sources sense connection as the means of driving the gate as the induced voltage peaks on the power source inductance will not feedback into the driving circuit as would happen in the standard configuration with only a single source connection to the MOSFET.

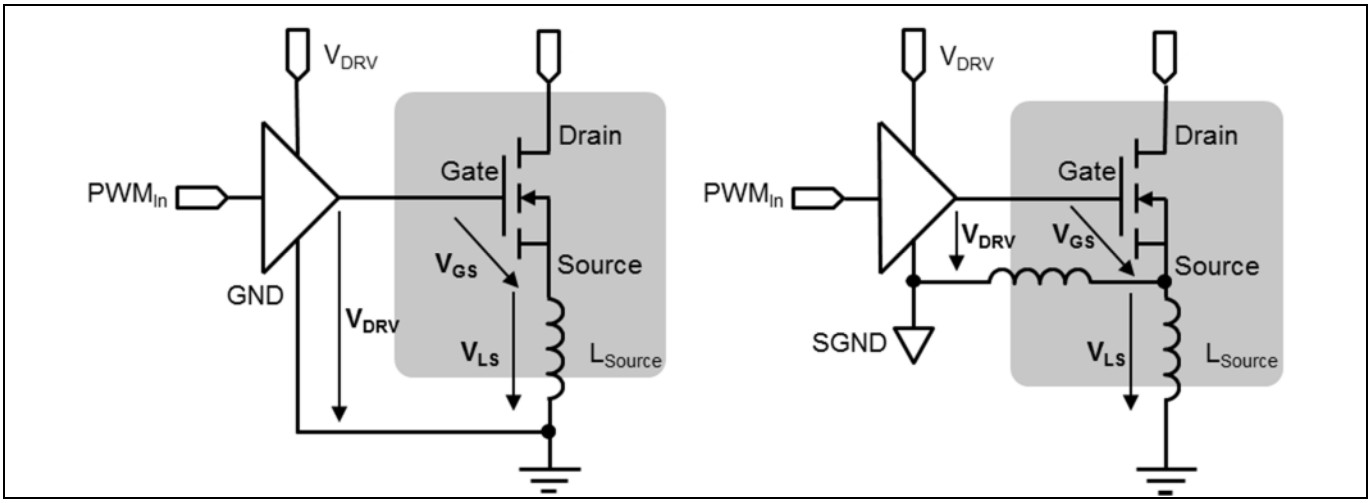


Figure 7 Driving scheme comparison for standard and 4pin setup

Due to the low pin inductance of the TOLL package (approximately 1 nH) the bouncing of the signal ground is at a much lower level when compared to the TO-247 4pin package, where the source inductance is approximately 15 nH which causes higher voltage peak at the turn on and turn of the transition. There is more detailed information about the 4pin features and application considerations in various 4pin application notes on *www.infineon.com.* This application note will focus on the C7 Gold technology.

2.3 Improved switching performance has impact to $R_{DS(on)}$ selection

As discussed in the earlier sections of this document, the C7 Gold has reduced switching loses for comparable $R_{DS(on)}$. This has an important impact on the selection of the optimized $R_{DS(on)}$ for a given power class in a certain topology.

There is a very important phenomenon driving overall losses to a optimum when the switching losses are equal to the conduction losses, as shown in Figure 8. Both types of loss depend on the chip area. As the chip size increases, $R_{DS(on)}$ will decrease with a square function and switching losses will increase linearly.

For hard switching topologies the switching losses are a combination of turn on and turn off losses. For the turn off losses, C_{OSS} is the root cause for E_{OSS} which is needed to charge the output capacitance. This capacitance will be shorted by the MOSFET when the device is turned on again and converted into heat. In order to reduce complexity and to minimize the impact of the gate resistor for the switching losses, the calculation for Figure 8

uses only E_{OSS} and ignores other switching losses as they are also determined by the current and the gate resistor. This means that the final switching losses will be higher than the capacitive switching losses shown in this chart.

Out of this loss comparison designers can conclude that for technologies with improved switching losses the optimum $R_{DS(on)}$ for a certain power range will be found at lower $R_{DS(on)}$ provided the switching frequency is not increased. This can be clearly seen in Figure 8 where the crossing point between the C_{OSS} related capacitive losses and the $R_{DS(on)}$ related conduction losses lies at a lower $R_{DS(on)}$ value for the C7 Gold technology due to its improved switching losses.

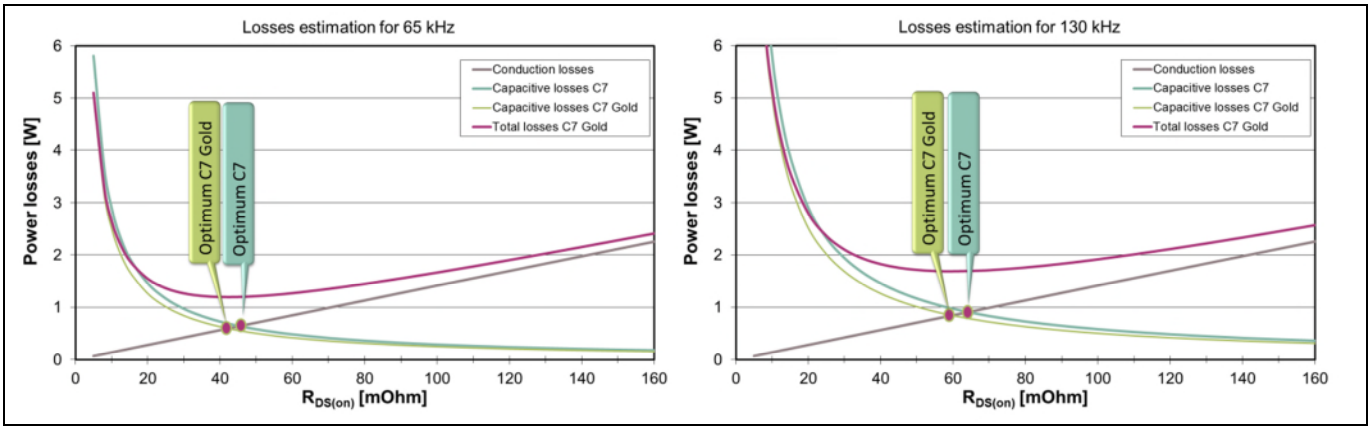


Figure 8 C_{oss} and $R_{DS(on)}$ based losses calculation for 65 kHz and 130 kHz

It can also be seen in Figure 8 that for higher switching frequencies the optimum $R_{DS(on)}$ is also higher. In order to increase the switching frequency in a given application without losing efficiency it is very important to use MOSFET technologies that offer lower switching losses for the same $R_{DS(on)}$. The new C7 Gold technology follows ecactly this strategy.

The new C7 Gold technology supports this by introducing nominal $R_{DS(on)}$ ranges as can be seen in Figure 9.

R_{DSON} Max mΩ	TO-LeadLess (TOLL)
195 mΩ	IPT65R195G7
105 mΩ	IPT65R105G7
33 mΩ	IPT65R033G7

Figure 9 Portfolio of C7 Gold products

Having the 33 mOhm device in the portfolio allows SMD devices to be used for higher power ranges in applications which were dominated by trough hole devises in the past (i.e. 3 kW in a standard CCM PFC). By the combination of lower $R_{DS(on)}$ and improved switching losses, the C7 Gold has lower overall power losses and, therefore, the cooling of the devices is much simpler. This is described in the following sections in more detail.

3 PCB assembly considerations for TOLL

The assembly process for SMD devices offers advantages in mass production. Firstly, SMD devices save space on the board and secondly the placement can be automated while most THD are inserted by manually which increases cost and reduces quality.

The PCB design and construction are key factors for achieving highly reliable solder joints. For example, TOLL packages should not be placed in the same location on opposite sides of the PCB (if double-sided mounting is used), because this results in a stiffening of the assembly which can lead to earlier solder joint failure when compared to a design where the component locations are offset. Furthermore, it is known that board stiffness has a significant influence on the reliability (temperature cycling) of the solder joint, if the system is used in fluctuating temperature conditions.

The outline of the TOLL devices is shown in Figure 10. More detailed information about the physical dimensions is available on the relevant datasheet(s) available on the Infineon website.

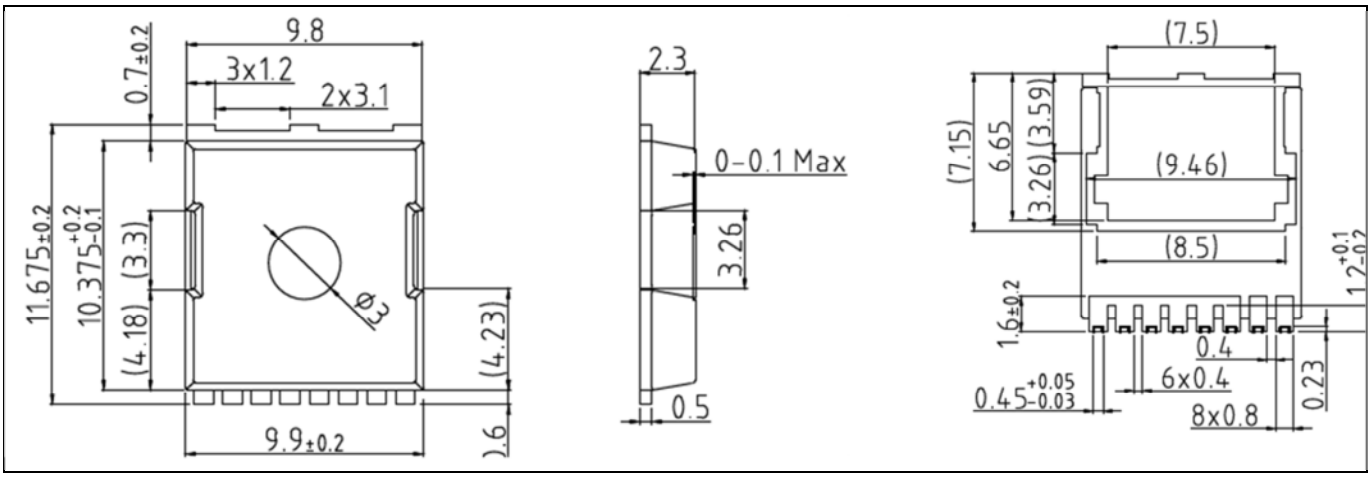


Figure 10 Outline Drawing of the TOLL (HSOF-8-2)

Figure 11 below shows the recommended PCB pad designs (including appropriate dimensions) for TOLL. This design is also used for thermal cycling on bord (TCOB) testing according to IPC9701A standard at Infineon.

Please note that the recommendations can only give dimensions for the solder-mask openings. Generally the copper dimensions depend on the capability of the board manufacturer. For high current applications, the copper dimensions for drain and source pads should be as large as possible to increase the conductor cross-sectional area.

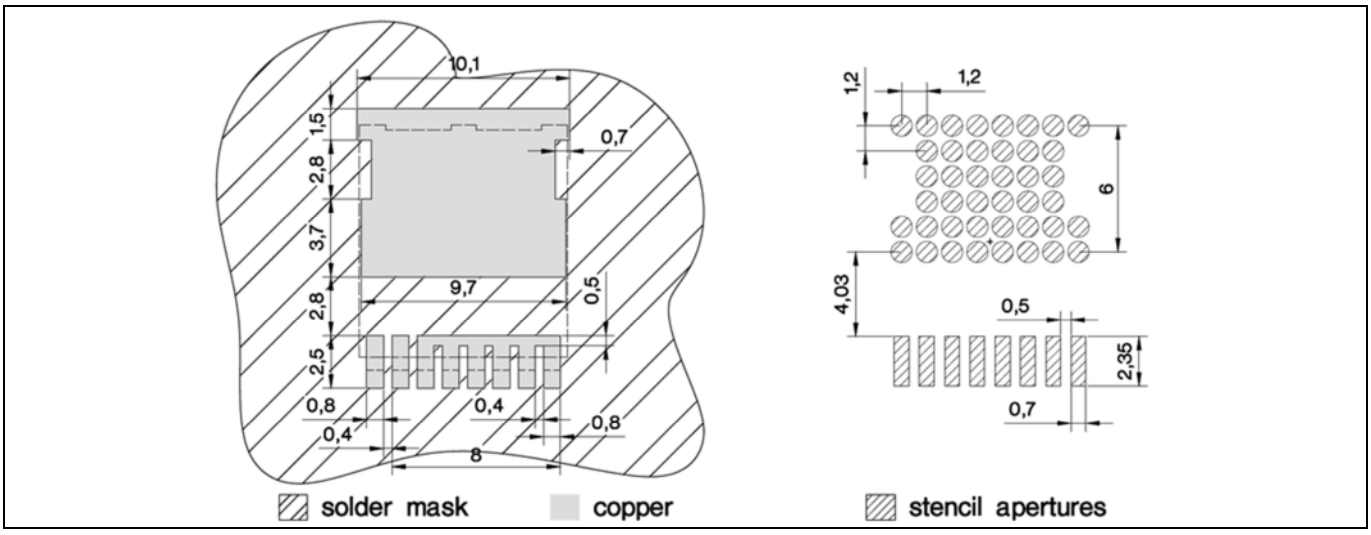


Figure 11 Footprint & stencil recommendation for PCB assembling

To connect the drain pad directly (thermally and electrically) to inner and/or bottom copper planes of the board, plated-through vias can be used. These vias help to distribute the heat into the board area, which spreads from the chip directly through the drain contact. Locating vias too near to (or within) the open solder mask can lead to solder wicking and could result in soldering issues and/or reduced reliability.

Thermal and electrical analysis and/or testing are recommended to determine the optimum number of vias needed for a specific application.

3.1 Lead design for manufacturing support

Conventional leadless packages such as CanPAK™ or SuperSO8 are not compatible with automatic optical inspection (AOI) because the solder joints are (partially) hidden under the package.

The connections of the TOLL package feature special grooves (as shown in Figure 12), located on the bottom side of the gate and source pins. The trapezoidal grooves lead to a visible solder joint, avoiding the necessity of an expensive X-ray inspection. The grooves also increase the wetting of the solder and therefore enhance the performance of the solder joint.

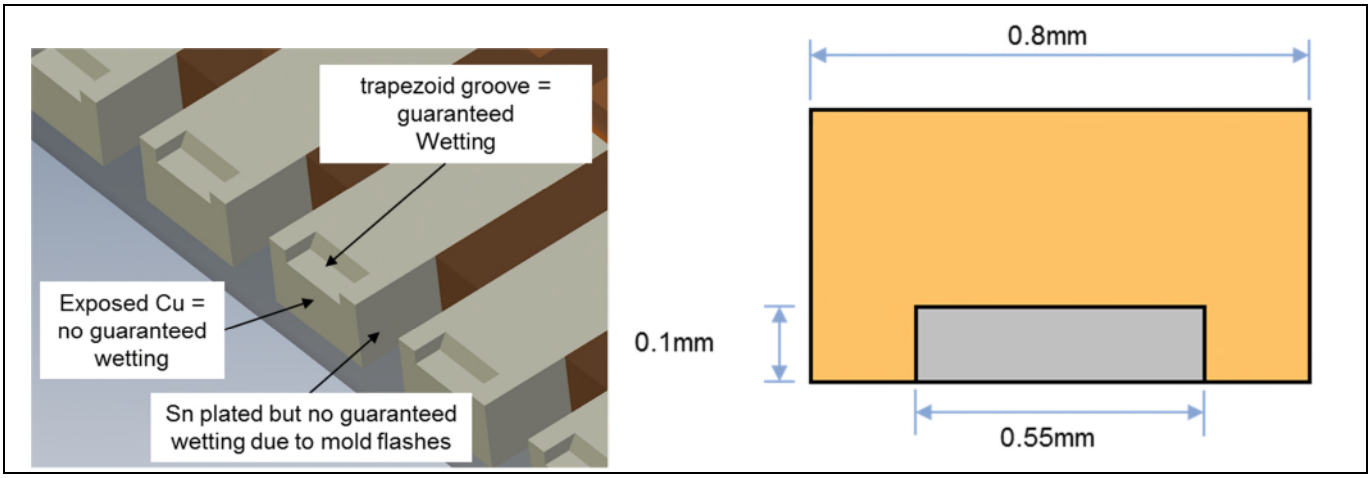


Figure 12 Grooves in the pins enhance better soldering

After soldering it is easy to identify a good solder joint using standard AOI. In Figure 13 a typical result of soldering is highlighted. Cutting through a source connection shows the solder (light yellow). The groove is completely filled and additionally a solder meniscus is visible on the left, allowing an assessment of the solder connection.

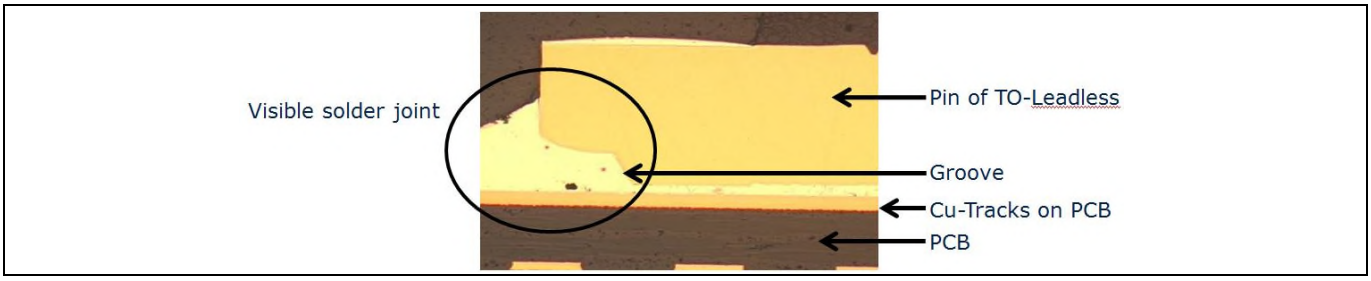


Figure 13 Visible solder meniscus allows a simple AOI inspection

3.2 TCOB reliability of the TOLL package

IPC9701 defines thermal cycling test at the PCB level. The TCOB test is designed to detect failure modes, which are due to the thermo-mechanical mismatch between devices and printed circuit board (PCB). These are mainly solder joint fatigue, but also potential internal package defects from the stress related to the CTE (coefficient of thermal expansion) mismatch to the PCB (e.g. delaminations, cracks or anything else).

A standard failure criteria during in-situ-monitoring is a resistance increase of the daisy chain (contact resistance monitoring between two contacts) of more than 20% (according to IPC9701A). In the case of very small daisy-chain resistances, a higher resistance threshold is used and documented within the test report.

Topic	Description		Comment
	Value	Unit	
Test Vehicle			
PG-HSOF-8-2	10 x 12	mm²	
Chip	25	mm²	MOSFET
Stress Boards			
Board material	a) high T_g FR4 b) IMS	-	a) Std. TCoB test board PMM b) For high power application
Board thickness/ layer	a) 1.6 mm/ 4-layer b) 3.2 mm IMS	-	
Finishing	Chem. Sn	-	
Solder material	SAC305	-	
Stencil thickness	120	µm	
Stress Condition			
Temperature range	-40° C ... 125° C	° C	1 cycle/ hour according to IPC 9701
Monitoring	Electrical readout & Cross sectioning	-	Online readout

Figure 14 TCOB Test Setup for TOLL

In Figure 14 the setup for the TCOB test is shown. The tests were performed for 4-layer PCB and IMS (isolated metal substrate).

Reviewing the test results of the TCOB based on the table in Figure 14:

- For the PCB version: no electrical failure and no optical objection detected up to 6000 cycles.
- For the IMS version: no electrical failure and no optical objection detected up to 896 cycles.

Due to higher thermo-mechanical mismatch, lifetime of the IMS assembly is reduced significantly with respect to assembly on FR4 PCB.

3.3 Creepage and clearance

According to UL/EN60950 the minimum distance between electrical connections for SMPS is defined as follows

- Creepage: The distance upon the surface between two electrical conductive areas is called creepage. The minimum creepage distances depend on the real RMS working voltages.
- Clearance: The clearance is defined as the shortest direct distance between two electrically conductive areas without any other material in between. Minimum clearance distances depend on peak working voltages.

Distances between electrically conductive areas shall be so dimensioned that overvoltages, including transients, which may enter the equipment, and peak voltages which may be generated within the equipment, do not break down the function or safety of the device for a given pollution degree.

Comparing the minimum distances between drain and other connections of the device one can see in Figure 15 that the TOLL with its 2.7 mm is offering more safety margin than even the very popular TO-247 package with 2.54 mm clearance. Therefore the TOLL package is perfectly suitable for replacement of any TO-247 device.

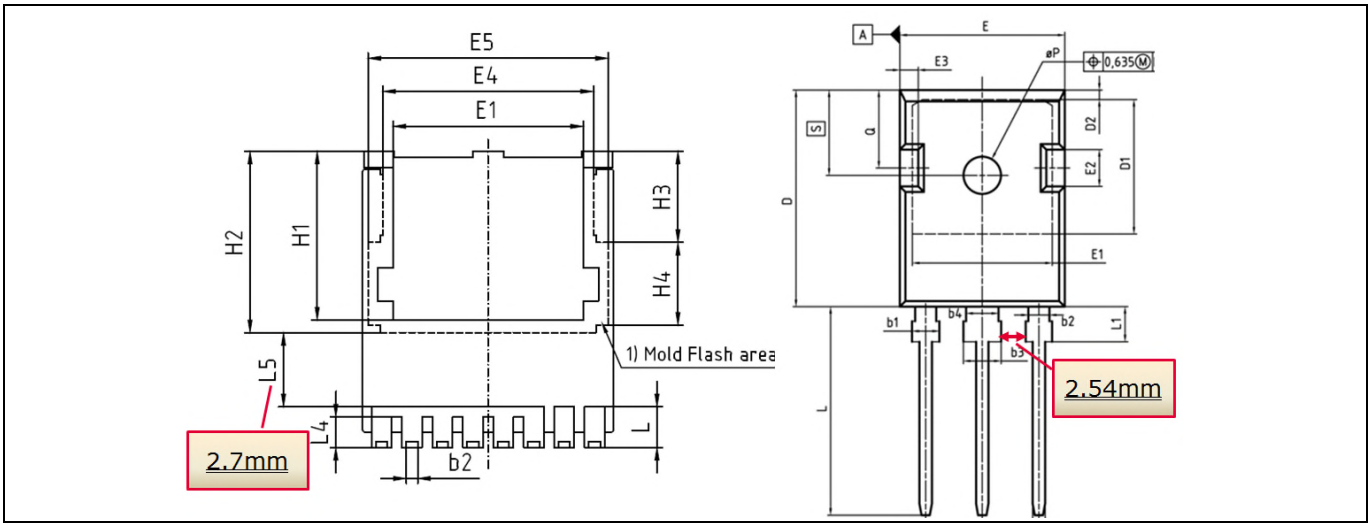


Figure 15 Comparison of TOLL and TO-247 clearances

3.4 Storage and transportation conditions

Improper transportation and unsuitable storage of components can lead to a number of issues during subsequent processing, including poor solderability, delamination, and package cracking effects.

The following standards should be taken into account:

- IEC 60721-3-0 Classification of environmental conditions: Part 3: Classification of groups of environmental parameters and their severities; introduction.
- IEC 60721-3-1 Classification of environmental conditions: Part 3: Classification of groups of environmental parameters and their severities; Section 1: Storage

- IEC 60721-3-2 Classification of environmental conditions: Part 3: Classification of groups of environmental parameters and their severities; Section 2: Transportation
- IEC 61760-2 Surface mounting technology – Part 2: Transportation and storage conditions of surface mounting devices (SMD) – Application guide.
- IEC 62258-3 Semiconductor Die Products – Part 3: Recommendations for good practice in handling, packing and storage
- ISO 14644-1 Clean rooms and associated controlled environments Part 1: Classification of airborne particulates

Maximum storage time: The conditions to be complied with in order to ensure issue-free processing of active and passive components are described in IEC 61760-2.

3.5 Moisture sensitivity level (MSL)

For moisture-sensitive packages, it is necessary to control the moisture content of the components. Penetration of moisture into the package molding compound is generally caused by exposure to ambient air. In many cases, moisture absorption leads to moisture concentrations in the component that are high enough to damage the package during the reflow process. Thus, it is necessary to dry moisture-sensitive components, seal them in a moisture-resistant bag, and only remove them immediately prior to assembly to the PCB. The permissible time (from opening the moisture barrier bag until the final soldering process) that a component can remain outside the moisture barrier bag is a measure of the sensitivity of the component to ambient humidity (Moisture Sensitivity Level, MSL). The most commonly applied standard IPC/JEDEC J-STD-033* defines eight different MSLs (see Figure 16). Please refer to the “Moisture Sensitivity Caution Label” on the packing material, which contains information about the moisture sensitivity level of our products. IPC/JEDEC-J-STD-20 specifies the maximum reflow temperature that shall not be exceeded during board assembly.

Level	Floor Life (out of bag)	
	Time	Conditions
1	Unlimited	≤30°C/85% RH
2	1 year	≤30°C/60% RH
2a	4 weeks	≤30°C/60% RH
3	168 hours	≤30°C/60% RH
4	72 hours	≤30°C/60% RH
5	48 hours	≤30°C/60% RH
5a	24 hours	≤30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤30°C/60% RH

Figure 16 Moisture sensitivity levels (acc. to IPC/JEDEC J-STD-033, RH=relative humidity)

If moisture-sensitive components have been exposed to ambient air for longer than the permitted time according to their MSLs, or the humidity indicator card indicates too much moisture after opening a Moisture Barrier Bag (MBB), the components have to be baked prior to the assembly process. Please refer to IPC/JEDEC J-STD-033* for details. Baking a package too often can cause solderability issues due to oxidation and/or intermetallic growth upon the open contact areas. In addition, packing material (e.g. trays, tubes, reels, tapes etc.) may not withstand higher baking temperatures. Please refer to imprints/labels on the packing to determine the maximum allowable temperature.

For Pb-free components, two MSLs can be given: One for a lower reflow peak temperature (Pb-containing process) and one for a higher reflow peak temperature (Pb-free). Each one is valid for the respective application.

The new C7 Gold technology supports highest Moisture sensitivity Level MSL1. Therefore it can be shelfed in this respect for unlimited time.

4 Thermal handling

Working with SMD devices can be very challenging if they are used for high power applications where high power losses are expected. Naturally, the power losses will convert into heat. For SMD devices it is necessary to extract this heat by cooling through the PCB as the package itself is mostly isolated on the top side of the PCB.

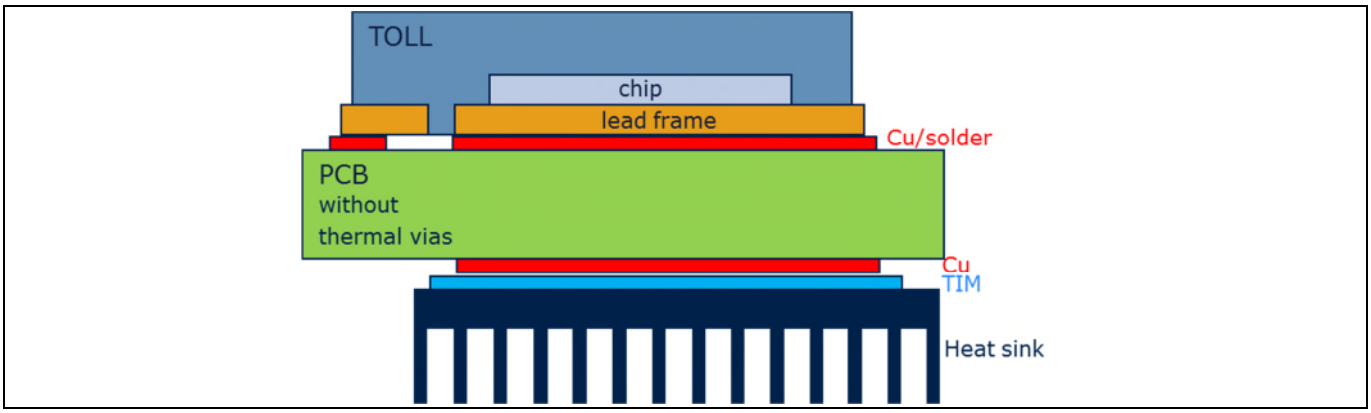


Figure 17 Schematic PCB assembly for TOLL on 2 layer FR4 board

In normal cases such as the one shown in Figure 17, the additional thermal resistance of the PCB will dominate the overall R_{th} of the cooling path and therefore limit the maximum power range for using SMD devices. Therefore, it is important to have a closer look to the thermal system of the application. In order to get a more clear idea of the thermal system, Table 1 shows also the thermal resistance break down for the single layers of the whole stack.

To understand the bottleneck for the thermal resistance of the whole system, one can consider the size of the soldering area of the SMD device for the cooling path. In case of TOLL this area is shown in Figure 11 and is approximately 80 mm² (8mm x 10mm).

Table 1 R_{th} break down for IPT65R033G7 assembly based on Figure 17

Layer	λ [W/(m*K)]	Thickness [mm]	R_{th} [K/W]
IPT65R033G7	na	2.2	0.32
Solder (Sn/Ag –mixture)	50	0.05	0.038
80 mm² Copper (Cu)	400	0.07	0.0022
PCB (FR4)	0.3	1.6	66.67
80 mm² Copper (Cu)	400	0.07	0.0022
Isolation Foil TIM (K10)	0.8	0.15	2.38
Heat sink (SK 566)	300	na	5
Total system	**na**	**na**	**74.41**

From Table 1, the total thermal resistance is 74.41 K/W and is dominated by the thermal resistance of the PCB. According the equation shown in Figure 18, the R_{th} of the thermal system will be improved linearly by reducing the PCB thickness linearly. Such a reduction of the PCB thickness is limited by the desired mechanical stability of the system. To minimize this stability issue the use of daughter boards can be considered for high power devices.

A well established technique to increase the area of the thermal path through the PCB is to apply copper planes on both sides of the PCB in order to spread the heat transfer to a larger area.

$$R_{th} = \frac{\mathrm{d}}{\lambda \times A}$$

Figure 18 Thermal resistance for heat dissipation

Where:-

d is the thickness of plain [m]

λ is the specific thermal conductivity [W/mK]

A is the area of heat flow [m^2]

There are some challenges to consider when increasing the area for the heat transport though the PCB such as parasitic capacitance due to the coupling of the heatsink as well as power density limitations.

4.1 Reducing the thermal resistance of the PCB by vias and copper planes

In order to reduce the thermal resistance of the system the use of thermal vias and copper planes for heat spreading is a well established technique for SMD assemblies.

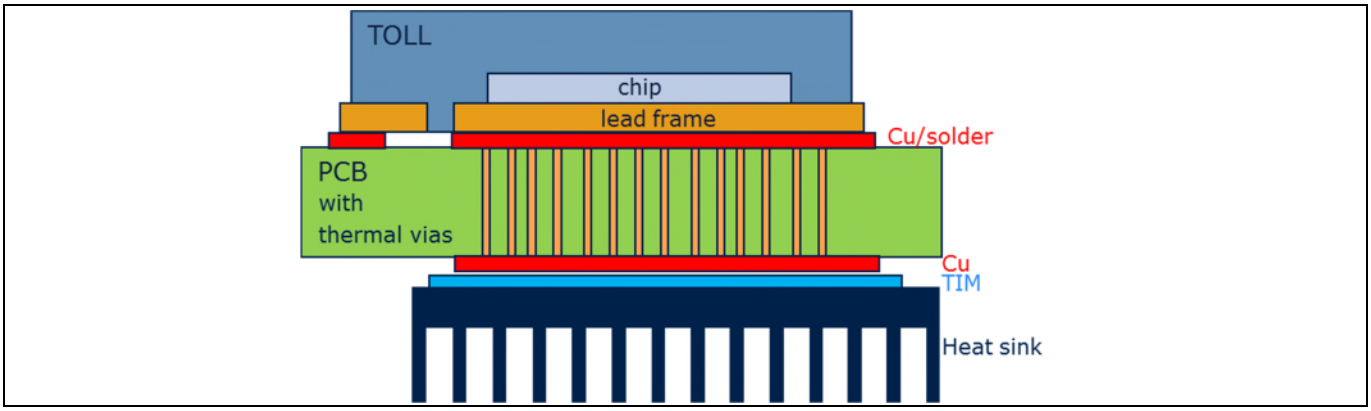
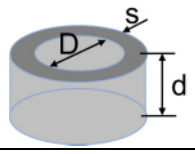


Figure 19 Schematic PCB assembly for TOLL with thermal vias on FR4 board

The dimension of the thermal vias offers a lot of opportunities for the designer. In our experience the optimum diameter of the vias is in the range of 0.3 mm to 0.5 mm as this size does not add additional cost to the PCB manufacture as it would for smaller diameters. In parallel, this allows use of spot masks for the soldering process. It is important to not allow solder to reach the opposite copper plane as it must remain flat for applying the heat sink. The thermal interface material has limited capability to level any surface roughness.

For the distance between the vias there is a sweet spot in the range of 0.5 mm to 1 mm. The calculation in Table 2 is based on vias with 0.3 mm diameter and a stepping of 1mm. Additionally, there is a overlay of a matrix shifted by half the stepping distance which defines a final diagonal distance between each via of 0.7 mm. With this arrangement a total of 160 vias are recommended for the 80 mm^2 soldering area of the TOLL.

The thermal resistance of one single via is calculated as shown in Figure 20. For the calculation in Table 2 the R_{th} of a single via results in a value of 108.6 K/W.



$$R_{th,via} = \frac{d}{\lambda \pi s(D+s)}$$

Figure 20 R_{th} of thermal vias

Where :-

d is the thickness of PCB [m]

λ is the specific thermal conductivity [W/mK]

s is the thickness of the side wall coating [m]

D is the diameter of the via [m]

Table 2 R_{th} break down for IPT65R033G7 assembly based on Figure 19

Layer	λ [W/(m*K)]	Thickness [mm]	R_{th} [K/W]
IPT65R033G7	na	2.2	0.32
Solder (Sn/Ag –mixture)	50	0.05	0.038
80mm² Copper (Cu)	400	0.07	0.0022
PCB (FR4 including 160 thermal vias with 0.3 mm)	na	1.6	0.68
80 mm² Copper (Cu)	400	0.07	0.0022
Isolation Foil TIM (K10)	0.8	0.15	2.38
Heat sink (SK 566)	300	na	5
Total system	**na**	**na**	**8.46**

In Table 2 the improvement from introducing thermal vias is demonstrated as compared to Table 1. The total R_{th} of the system is reduced to 8.46 K/W from the previous 65.9 K/W. This is a significant improvement by 87.2% or in other words only 12.8% of the R_{th} without thermal vias!

4.2 Silicon instead of heat sink

Previous chapters described how the power losses affect the cooling. Now, we can consider reducing the losses by the selection of a lower $R_{DS(on)}$ in order to decrease the thermal complexity.

$$P_V = I^2 * R_{DSon}$$

Figure 21 Conduction losses calculation for MOSFET

The correct $R_{DS(on)}$ selection allows the designer to reduce the conduction losses of the MOSFET according the equation shown in Figure 21. The higher the power of the application, the higher the current will be. This current increases the conduction losses by a square function. Therefore, it is very important to reduce the R_{DSon} as much as possible within the limitations shown in Figure 8.

In the application comparison (which will be discussed in following sections), this technique has been used in the comparison of the 650 V 45 mOhm C7 devices with the 33 mOhm C7 Gold ones.

Reducing the $R_{DS(on)}$ of the MOSFET means increasing its size. If the $R_{DS(on)}$ reduction leads to reduced overall losses, the size of the heat sink can also be reduced which leads to the so-called silicon replacement of the heatsink.

4.3 Thermal management of PCB by means of HSP (Heat Sink Paste) and TIP (Thermal Interface Paste)

The need to dissipate the heat generated from the component can be satisfied in different ways. For those applications where the amount of heat does not require a mechanical heat sink (with its additional costs and space requirements), but the FR4 substrate is not sufficiently dissipative in itself, the application of a specific thermo-dissipative paste is a viable solution. The dissipative paste distributes and transfers the heat to the surrounding environment. The paste is applied by screen printing during the construction of the bare PCB, and will partially fill the thermal vias, thus improving their performances.

Thermo-dissipative paste is also resistant to reflow and wave soldering, allowing a considerable time and cost saving for the assembly process when compared to thermo-dissipative preformed interface solutions applied after soldering.

As well as its thermal properties (thermal conductivity equal to 2 W / m° K) the paste also has good electrical insulation (30 kV / mm) properties

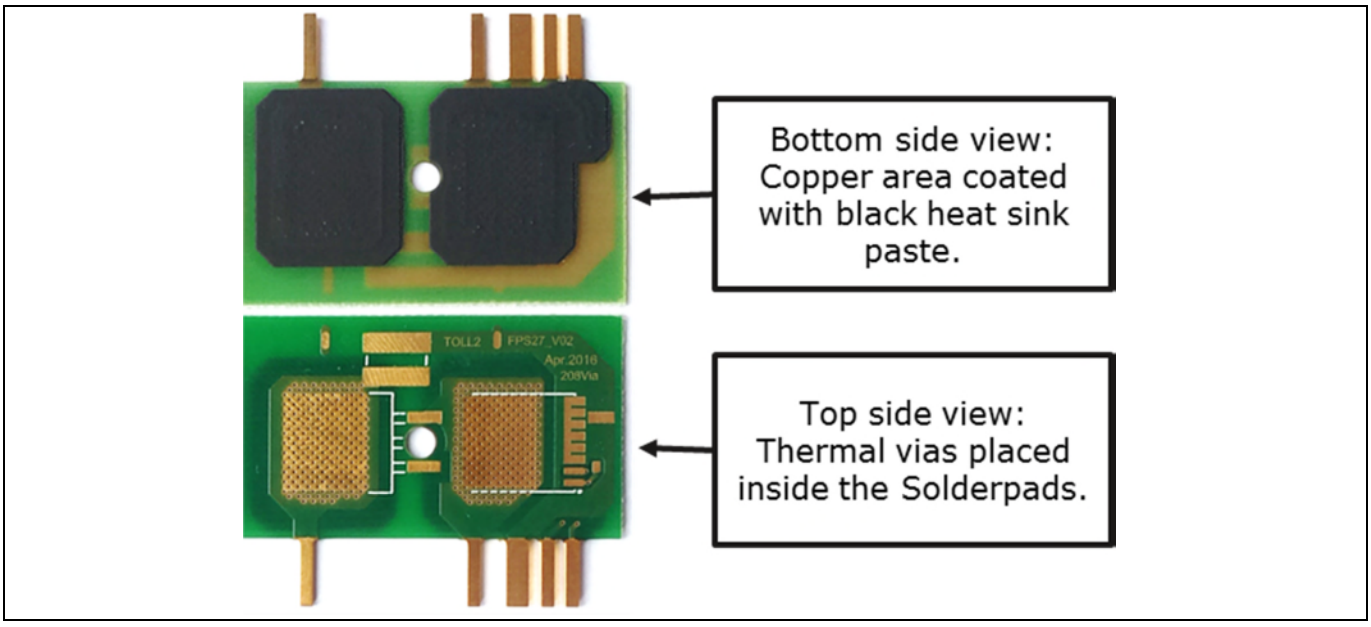


Figure 22 Daughter PCB with heat sink paste (pcb made in Italy by Serigroup Srl www.serigroup.it)

For applications where the amount of heat requires a mechanical heat sink, the thermal coupling can be improved by the use of a thermal interface paste as shown in Figure 23.

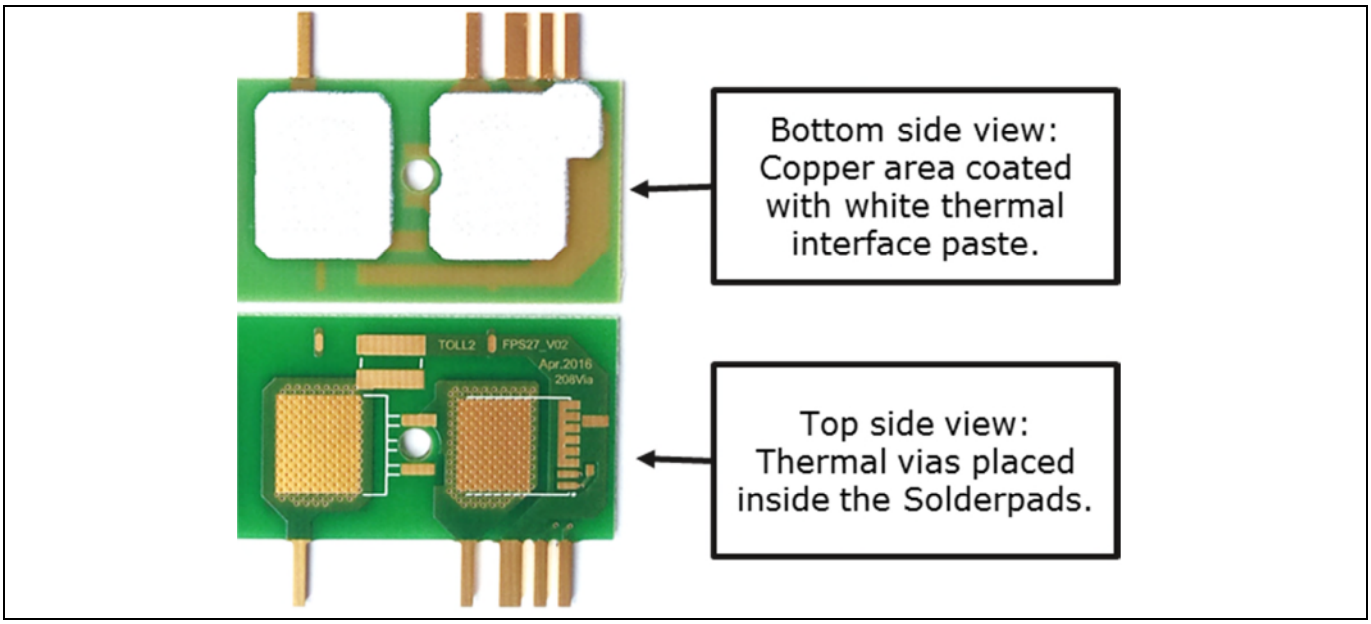


Figure 23 Daugther PCB with thermal interface paste (pcb made in Italy by Serigroup Srl www.serigroup.it)

The conductive thermal interface paste is electrically insulating and reflow / wave soldering resistant.

It is normally applied to the PCB before soldering, as the last process in the manufacture of the bare PCB.

Its high conformability feature eliminates gaps between the heat sink and copper on the bottom side of the PCB, ensuring optimum heat transfer from the substrate to the heatsink.

As well as the thermal properties (thermal conductivity equal to 2.2 W / m ° K) typical thermal interface paste has good electrical insulation properties (60 kV / mm).

5 Application results

The application testing for the C7 Gold devices shown in this document is performed by adding a daughter board to the 2.5 kW PFC evaluation board – including the Infineon CCM PFC controller (ICE3PCS01G) as shown in Figure 24.

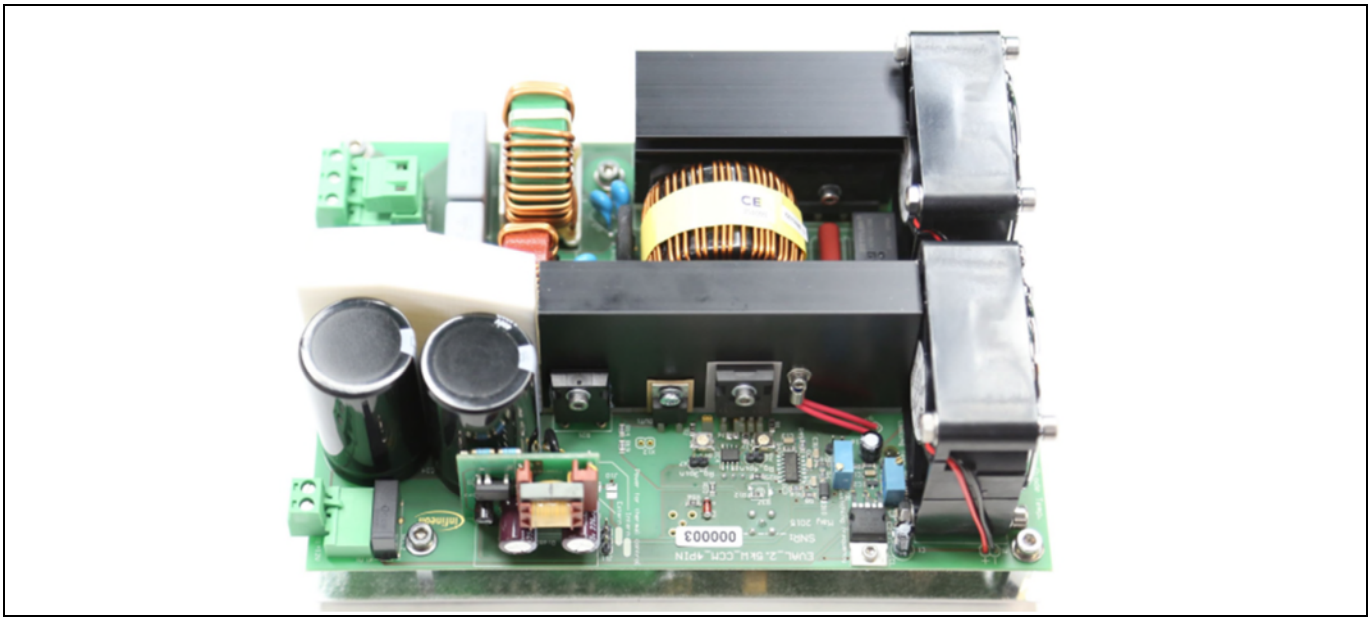


Figure 24 EVAL_2.5kW_CCM_4PIN evaluation board

The 2.5 kW evaluation board is an excellent example of a complete Infineon solution, and includes a PFC Controller, MOSFET Driver and Silicon Carbide (SiC) Diode allowing evaluation of the 4pin functionality and its advantages for efficiency and signal quality. The layout of the board is intended to allow easy access to the different devices and to add measurement probes to areas of interest. The evaluation board is fitted with double connectors for the power line input and 400 V output in order to allow sense techniques for precise efficiency measurements.

For more detailed information about the evaluation board please review www.infineon.com/C7-600V.

The original desing of this evaluation board is fitted with TO247 MOSFET. In order to use the TOLL C7 Gold devices in this evaluation board, some modification with daughter boards is required, as shown in Figure 25. The special daughter board shown in Figure 26 is designed to fit into the pin arrangement of the main PFC evaluation board.

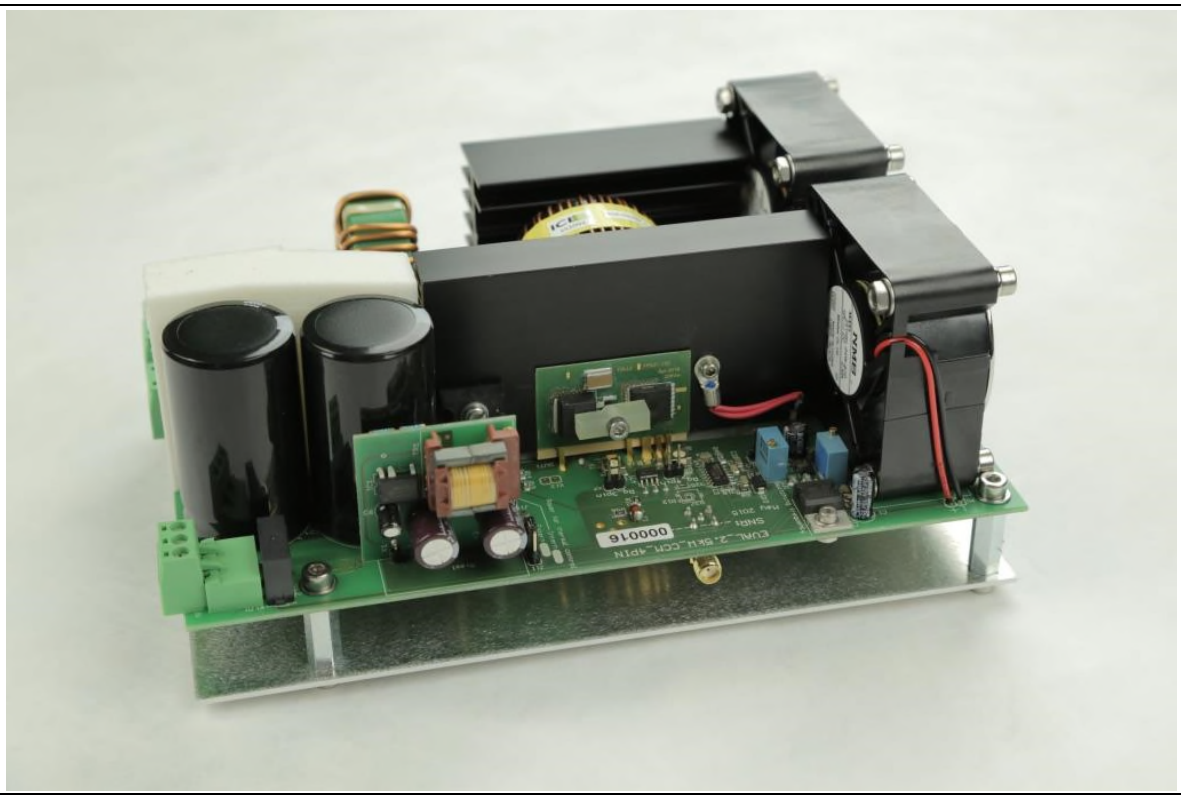


Figure 25 EVAL_2.5kW_CCM_4PIN evaluation board after modification for TOLL packages

The daughter boards have been designed as shown in Figures 26 & 27. This board contains the power MOSFET, the boost diode and the ceramic high frequency boost capacitor in order to minimize the parasitic loop inductance of the circuit. The pin layout aligns with the main PCB of the evaluation board. Thus, it is possible to remove the TO-220 diode and the TO-247-4pin MOSFET and replace them directly with the daughter board. It will be necessary to create a mechanical fixing to thermally connect the daughter board to the heat sink.

The mechanical fixing of the daughter board is possible with conventional springs or by screwing through the drilled hole in the middle of the PCB.

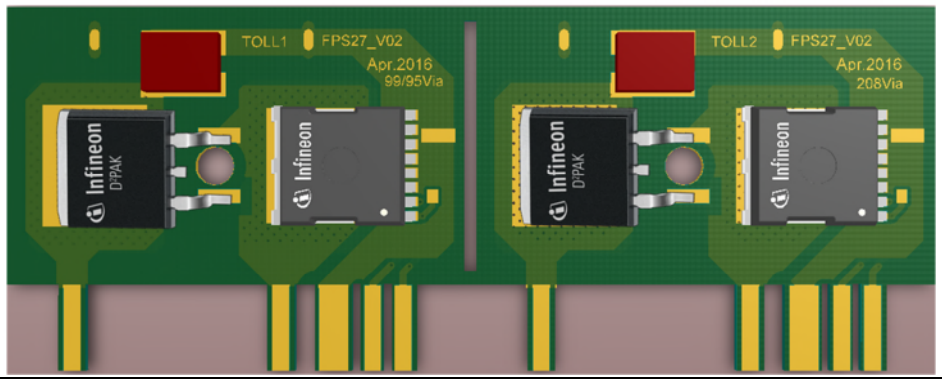


Figure 26 Top view of the TOLL daughter board for PFC circuit

The daughter board offers two different via layouts. The right one shown in Figure 27 does not have any vias in the soldering area of the SDM device - only around it. This version is suitable for any reflow soldering process, as there is no protection needed for preventing solder getting to the backside of the PCB. The left variant is made for best thermal performance and the whole area underneath the device contains thermal vias. It is understood that the variant with the high via density is the better choice for high power applications while the one with no vias in the solder area might be a better choice for lower power ranges if solder protection is not easy to implement into the production process.

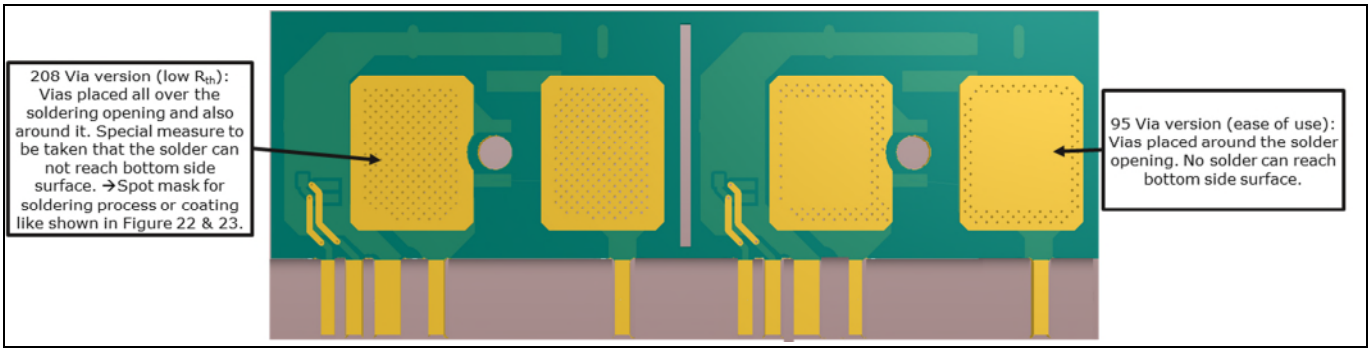


Figure 27 Bottom view of the TOLL daughter board

In order to not suck the solder through the vias during soldering process special measures are required. The best solution will vary with the choice of assembly process as is described in section 4.3.

The daughter boards with vias in the solder area have a coating added to the bottom side during the PCB manufacturing process. The coating acts as a protection during the soldering process and is suitable for a reflow or wave soldering process. It is not necessary to remove this coating after the soldering as the coating on this daughter PCB has good electrical isolation and good thermal conductivity similar to a thermal interface layer. Therefore, this daughter board can be assembled directly to the heatsink without any additional isolation layer or thermal interface.

5.1 Clean waveforms by low parasitic

For high power applications, parasitic inductances are a well-known issue for the designer. They not only cause oscillations but also voltage spikes. One way to limit this is to increase the gate resistance in order to slow down the switching speed but this has the drawback of reducing efficiency. The other way is to minimize the paracitic inductances of the leads by moving away from THD towards SMD, such as TOLL, which offers extremely low lead inductances.

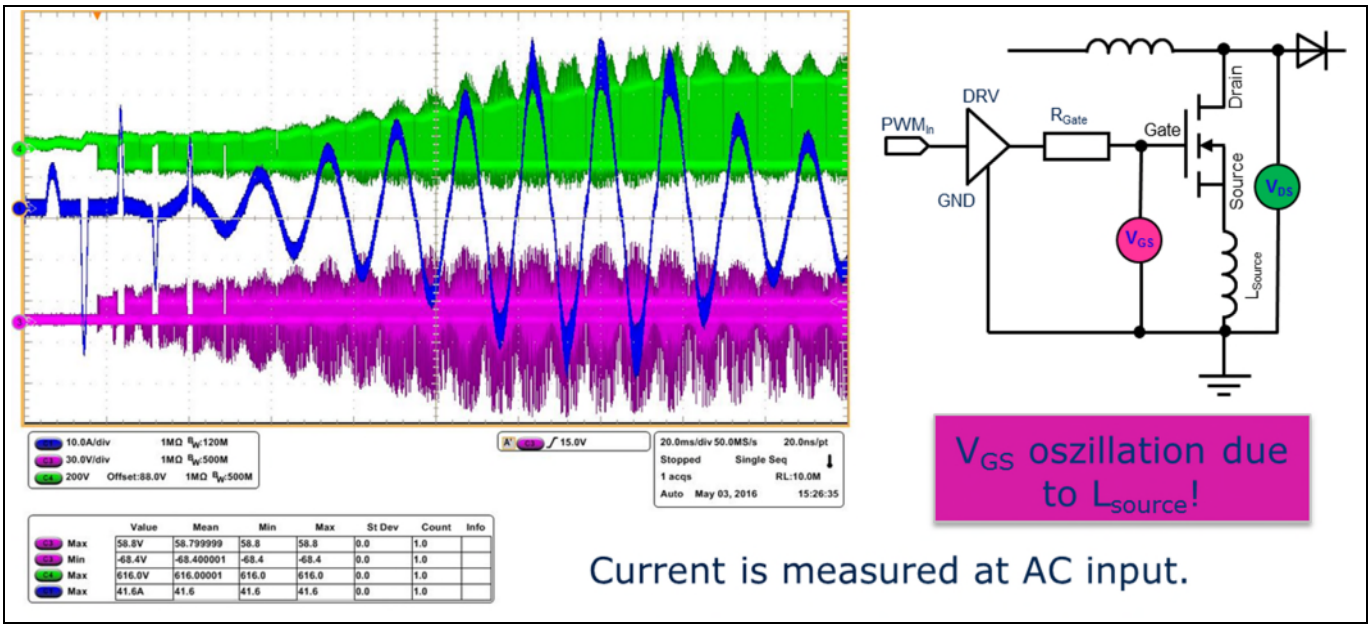


Figure 28 Startup at 90 V_{AC} with 1 kW load for IPW65R045C7 (TO247)

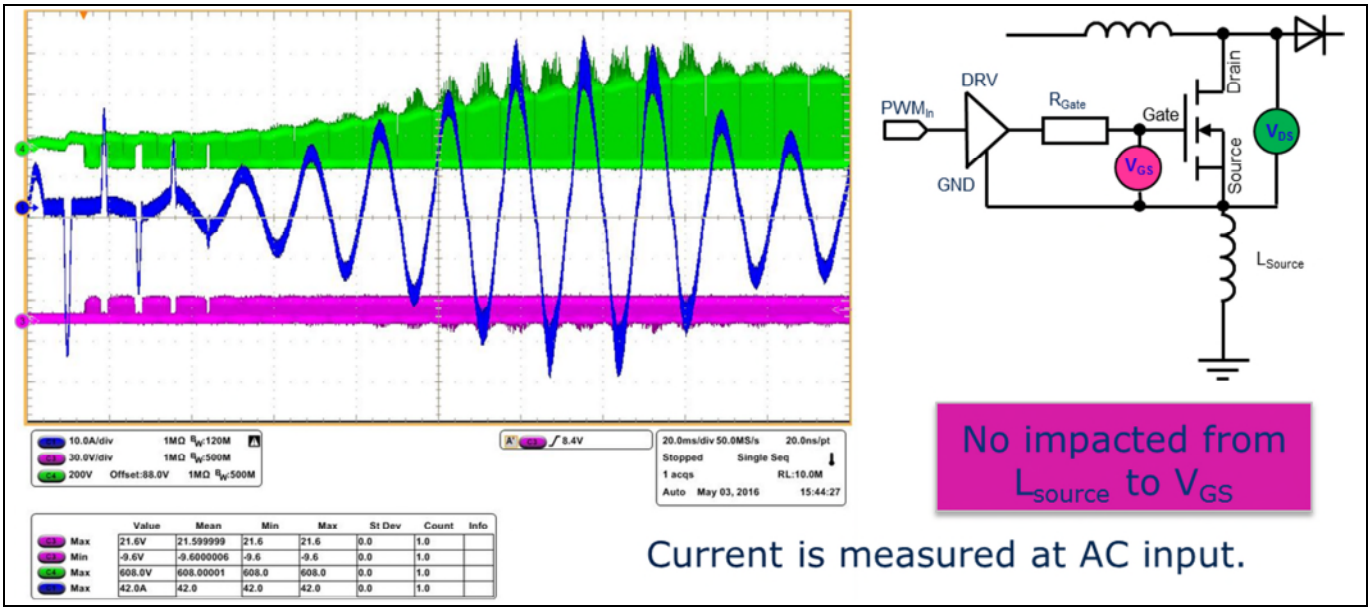


Figure 29 Startup at 90 V_{AC} with 1 kW load for IPT65R033C7 (TOLL)

In Figures 28 & 29, the startup of the PFC-Evaluation board is documented to allow a TO-247 4-pin and TOLL comparison. The blue line (channel 1) shows the AC input current, the magenta line (channel 3) shows the gate to power souce voltage and the green line (channel 4) shows the drain to source voltage. The comparison between Figures 28 & 29 shows the signal quality advantage for TOLL very clearly. Not only do the voltage spikes on the gate remain below 22 V, the Drain-Source voltage is also much more stable than for the TO-247, which is one important requirement for fast and efficient switching.

5.2 Efficiency impact

One of the most important aspects of the application testing is the monitoring of the device efficiency impact. For the C7 Gold technology offered in the TOLL package there have been several positive impacts discussed which all contribute to the overall efficiency of the whole PFC circuit.

The comparison shown in Figure 30 is based on a switching frequency of 65 kHz and a heat sink temperature of 60°C. The gate resistor used for both of the devices is set to 3 Ohm. For the TOLL the daughter PCB with the vias underneath the whole package area was used as the power range is up to 3kW. This PCB is fitted with 208 vias for each of the SMD (MOSFET and Diode) in order to minimize the additional thermal resistance of the PCB.

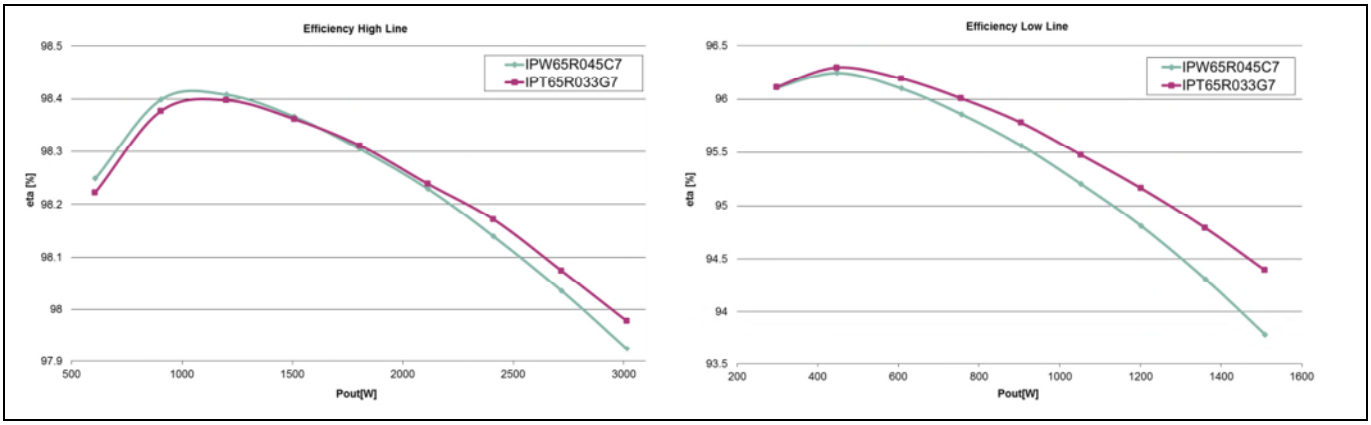


Figure 30 Efficiency for high line (230 V_{AC}) and low line (90 V_{AC}) input voltage

The comparison show the operation up to 3 kW in high line mode and 1.5 kW in low line operation. In both cases the efficiency with the IPT65R033G7 is higher in the high load region due to better switching performance and lower $R_{DS(on)}$. This effect is more pronounced in the low line testing as the contribution from the MOSFET is stronger than in the high line example. Looking to the high line measurement at light load, one can see that due to the very low switching losses increase by using 33mOhm device instead of 45mOhm, the light load efficiency is still very similar which is very unique for the C7 Gold technology as any other technology would show in this case much more disadvantage in the light load efficiency. This proves the simulation results shown in Figure 8.

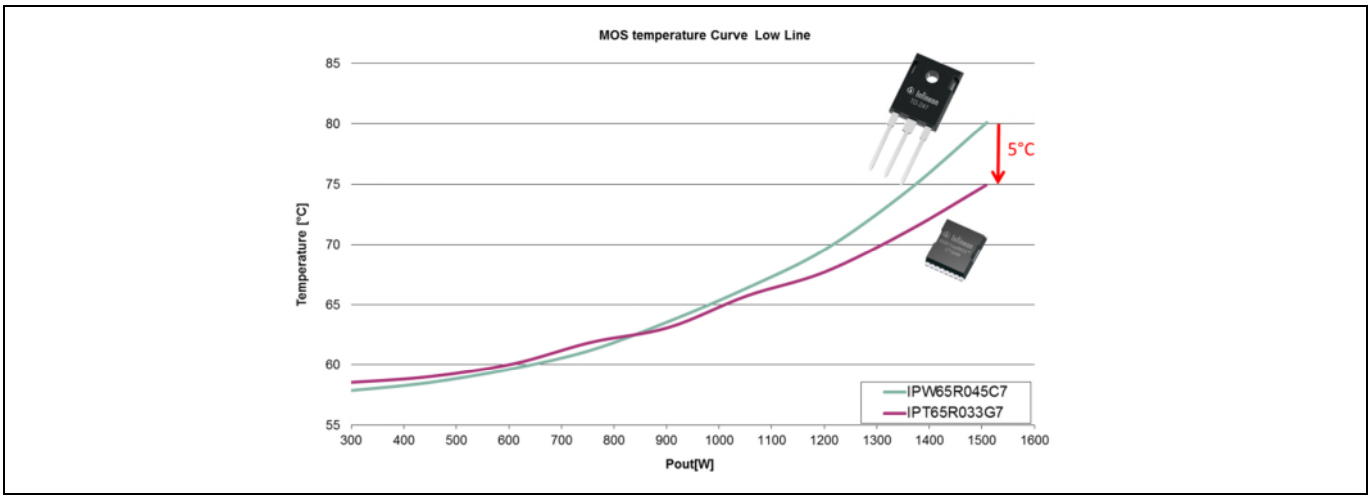


Figure 31 Temperature monitoring for 90 V_{AC} input voltage

As a result of the significantly increased efficiency for the thermally very critical, low line, high load area, the temperature of the TOLL MOSFET stay very coole as shown in Figure 31. At 1500 W the IPT65R033G7 remains about 5°C cooler than the equivalent TO-247 C7 device - although the cooling path for the TOLL also includes the additional R_{th} of the PCB as discussed in Table 2 compared to the conventional method with TO247 assembling.

5.3 Application conclusion

The application testing highlights the advantage of the C7 Gold TOLL SMD compared to the conventional TO-247 package. C7 Gold technology with improved switching performance enables use of a lower $R_{DS(on)}$ for a given power range. This offers a totally new optimization point for the applications that improves the high load range while not impacting the light load efficiency. Having better full load efficiency is an excellent starting point for reducing the cooling effort, thus supporting the drive towards increasing power density.

It has been shown that the C7 Gold technology enables first time the use of SMD devices for single stage standard PFC up to 3kW for high line operation which has been the clear domain for TO 247 in the past.

Therefore the portfolio will be further enlaged to a 600V technology which is also optimiced for soft switching applications like LLC for example.

Revision history

Major changes since the last revision

Page or reference	Description of change
Page 1 to 24	Format and wording update.
Figure 22, 23, 27, 28, 29	Picture update

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