55 W Flyback converter design using the IRS2982S controller
IRXLED04

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About this document

Scope and purpose
The purpose of this document is to provide a comprehensive functional description and guide to using the IRS2982S control IC for LED and general purpose switch mode power supply (SMPS). The scope applies to all technical aspects that should be considered in the design process, including calculation of external component values, MOSFET selection, PCB layout optimization as well as additional circuitry that may be added if needed in certain cases.

Intended audience
Power supply design engineers, applications engineers, students.

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1 Introduction

The IRS2982S is a versatile SMPS controller IC primarily intended for LED drivers in the 5 to 100 W power ranges suitable for Buck, Buck-Boost and Flyback converters operating in critical conduction mode (CrCM) and discontinuous mode (DCM) at light loads. Flyback converters will be covered in this application note focusing on an isolated voltage regulated design with PFC.

All of the control and protection required for the converter is integrated in the IRS2982S as well as a high voltage start-up cell to enable rapid illumination at switch on over a wide line input voltage range. The IRS2982S is also able to provide power factor correction in a single stage Flyback converter able to meet class C (lighting) line current harmonic limits of the EN61000-3-2 standard.

A 55W isolated voltage regulated PFC Flyback evaluation board based on the IRS2982S controller is described in detail in this application note and detailed test results are presented.

Figure 1  IRXLED04 55 W Flyback evaluation board
2 IRS2982S functional overview

The IRS2982S is comprised of the following functional blocks:

1. **High voltage start-up cell**
   The IC internal functional blocks remain disabled in low power mode until VCC first rises above the 
   $V_{CCUV+}$ under-voltage lock out (UVLO) threshold, continuing to operate while VCC remains above 
   $V_{CCUV}$. VCC is initially supplied through the integrated high-voltage start-up cell, which supplies a 
   controlled current from the HV input provided a voltage greater than $V_{HVSMIN}$, is present. The current 
   supplied is limited to $I_{HV\_CHARGE}$ reducing to less than $I_{HV\_OFF}$ when VCC reaches the cut-off threshold 
   $V_{HV\_OFF1}$. The HV start-up cell switches over from start-up mode to support mode after the feedback 
   input at FB has exceeded $V_{REG}$ for the first time. In this mode the cut-off threshold becomes $V_{HV\_OFF2}$.
   During steady state operation under all line-load conditions VCC is supplied through an auxiliary 
   winding on the Flyback transformer with VCC high enough so that the HV start-up in does not supply 
   current. If the auxiliary supply were unable to maintain VCC, the HV start-up cell operating in 
   support mode would supply current to assist.

2. **PWM controller**
   The SMPS control section operates in voltage mode where the gate drive output on time is 
   proportional to the error amplifier output voltage appearing at the compensation output COMP. An 
   external capacitor $CCOMP$ (shown in figure 4) connected to 0 V (ground) acts with the trans-
   conductance characteristic of the error amplifier to provide loop compensation and stability. 
   Minimum on time is reached when $V_{COMP}$ falls to $V_{COMP\_OFF}$ below which the gate drive is disabled. 
   Under very light load conditions $V_{COMP}$ transitions above and below $V_{COMP\_OFF}$ to produce burst mode 
   operation. Off time is determined by the demagnetization signal received at the ZX input, which is 
   derived from the auxiliary transformer winding that supplies VCC through a resistor divider. Internal 
   logic limits the minimum off time to $t_{OFFMIN}$, therefore the system transitions from CrCM to DCM at 
   light loads. If the ZX input signal fails to provide triggering the next cycle will start automatically 
   after a re-start period of $t_{WD}$.

3. **Protection**
   The IRS2982S includes cycle by cycle primary over-current protection, which causes the gate drive 
   to switch off if the voltage detected at the CS exceeds the threshold $V_{CSTH}$. This prevents the 
   possibility of transformer saturation at low line under heavy load but does not protect against output 
   overload or short circuit.

Over-voltage protection is also provided through the ZX input, which provides a voltage proportional to the 
output voltage. This disables the gate drive output and pulls the COMP voltage below the $V_{COMP\_OFF}$ threshold. 
The error amplifier then starts to charge $CCOMP$ until the gate drive starts up again at minimum on time. 
Under an open circuit output condition the over voltage protection causes the converter to operate in burst 
mode preventing the output voltage from rising too high.
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55 W Flyback converter design using the IRS2982S controller
IRS2982S functional overview

The IRS2982S uses an SO-8 package as shown below:

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>HV</td>
<td>High Voltage Start-up Input</td>
</tr>
<tr>
<td>2</td>
<td>FB</td>
<td>Feedback Input</td>
</tr>
<tr>
<td>3</td>
<td>COMP</td>
<td>Compensation and averaging capacitor input</td>
</tr>
<tr>
<td>4</td>
<td>ZX</td>
<td>Zero-Crossing &amp; Over-Voltage Detection input</td>
</tr>
<tr>
<td>5</td>
<td>CS</td>
<td>Current Sensing Input</td>
</tr>
<tr>
<td>6</td>
<td>COM</td>
<td>IC Power &amp; Signal Ground</td>
</tr>
<tr>
<td>7</td>
<td>OUT</td>
<td>Gate Driver Output</td>
</tr>
<tr>
<td>8</td>
<td>VCC</td>
<td>Logic &amp; Low-Side Gate Driver Supply</td>
</tr>
</tbody>
</table>

Figure 2   IRS2982S pin assignments

Figure 3   IRXLED04 Wiring Diagram
3 Flyback converter

3.1 Flyback converter types

There are several configurations of Flyback converter that may be used with the IRS2982S depending on the application. These can be classified according to isolation and regulation requirements as follows:

1. Isolated or non-isolated,
2. Current or voltage regulation,
   In the case of voltage regulation current limiting is needed for protection against overload or short circuit and in the case of current regulation over-voltage protection is necessary for an open-circuit.

The IRS2982S can operate in any of the four combinations of (1) and (2). Extremely accurate current or voltage regulation is achieved in non-isolated converters since direct feedback to the FB input is possible. Isolation is however required in the majority of Flyback converters. For isolated constant current regulation an opto-isolator is necessary; for isolated constant voltage regulation feedback may be taken from the auxiliary winding as shown in figure 4 with a small loss of line and load regulation accuracy. An opto-isolator is also necessary for highly accurate voltage regulation.

The basic circuit in figure 4 shows the main elements of the IRS2982S based PFC Flyback converter. This can be used as a stand-alone power supply or as a front end stage with a current regulating Buck regulator as the back end stage in a dimmable (or non-dimmable) off line LED driver. This front end stage is able to provide a regulated output voltage over a wide range of line and load with sufficient accuracy for the majority of applications.

![Diagram of isolated voltage regulated Flyback converter based on the IRS2982S](image)

**Figure 4** Isolated voltage regulated Flyback converter based on the IRS2982S

A 55 W PFC Flyback voltage regulated design as implemented in the IRXLED04 evaluation board will be discussed in detail in the following sections.
Flyback converter design using the IRS2982S controller

3.2 Eval board specifications

Input and output at normal operation:
- AC Input voltage 100 VAC up to 265 VAC (45 to 65 Hz)
- Output voltage 55 VDC
- Maximum output voltage ripple +/-3 V @ full load
- The tolerance of the nominal output voltage is +/-5% in the power range from 10% up to 100% of the rated output power.
- Maximum output continuous power 55 W
- PF >0.95 @50 W load and 230 VAC input voltage
- THD <10% @50% up to 100% load and < 20% @ 20% load with 230 VAC input voltage
- Efficiency >89% at 80% load and >88% at 100% load @ 230 VAC input voltage.
- Startup time to reach the secondary nominal output voltage of 55 VDC during full load condition and 230 VAC input voltage must be <300 ms.

Protection features
- Primary output over-voltage protection @ VOUT <= 60 VDC
- Cycle by cycle primary over-current protection

WARNING!
Output short circuit and overload protection are not provided on this evaluation board. This board can be damaged by sustained over loading or short circuiting the output!

No load operation
- Burst mode during no load condition.
- Max power losses during no load condition must be <500mW @230VAC input voltage

Max component temperature
During worst case scenario (ambient temperature 60 °C) the max allowed component temperature is:
- Resistor < 105 °C
- Ceramic capacity, film capacity and electrolyte capacity <85 °C
- Flyback Transformer and chokes <105 °C
- MOSFET, transistor and diodes <105 °C
- IC <100 °C

Dimension of evaluation board
- Max width 2.2” (55.9 mm), max length 4.4” (111.8 mm).

Safety Requirements
The single stage Flyback converter should cover the safety requirement regarding EN61347-2-13 and SELV max output voltage 60 VDC. This part of IEC 61347 specifies particular safety requirements for electronic control gear for use in DC supplies up to 250 V and AC supplies up to 1000 V at 50 Hz or 60 Hz and at an output frequency which can deviate from the supply frequency, associated with LED modules.

Note
This evaluation board is designed as a front end stage for a two stage power supply such as an LED driver where the back end stage is a current regulating Buck regulator. The Flyback converter uses primary voltage regulation with no secondary current feedback and is therefore not designed to withstand a sustained overload or short circuit condition. Additional circuitry may be added if such protection is required.
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55 W Flyback converter design using the IRS2982S controller

Schematic

4  Schematic

Figure 5  IRXLED04 55 W PFC Flyback schematic
5 Dimensioning

The IRXLED04 eval board is populated for basic voltage regulation from the transformer auxiliary winding as shown in figures 4 and 5. The Flyback converter is designed for power factor correction with low AC line current total harmonic distortion (iTHD). The MOSFET used is an IPA80R650CE 800 V rated CoolMOS device with 650 mΩ on resistance, 45 nC gate charge and low parasitic capacitances in a TO-220 FullPAK. This device is able to withstand high voltage ringing at switch off with minimal added snubber components and has low conduction and switching losses as well low gate drive current.

The output diode has less than 50 ns reverse recovery and a forward voltage drop less than 900m V at maximum rated current of 10 A at 25 °C temperature, reducing to 700 mV at 150 °C. The blocking voltage is 300 V, necessary to withstand the output voltage under open circuit condition at high line input added to the transformer secondary reflected voltage. The parameters of the MOSFET and output diode contribute to the overall high efficiency of the converter.

The Flyback transformer (more accurately described as a coupled inductor) consists of three windings; the primary for energy storage during the on time, the secondary for energy transfer to the output during the off time and the auxiliary, which supplies VCC and provides the required de-magnetization and voltage feedback signals. The IRS2982S (IC1) VCC supply is derived from the transformer auxiliary winding through DVCC1 initially charging CVB then CVCC1 and 2 through RVCC and DVCC2 with DZ to clamp the voltage to protect IC1. Voltage feedback is provided through a divider comprised of RFB1 and RFB2, which sets the output voltage. The auxiliary winding voltage is proportional to the output voltage so that:

\[
V_{\text{aux}} = V_{\text{ref}} \cdot \frac{R_{\text{FB1}} + R_{\text{FB2}}}{R_{\text{FB2}}} = V_{\text{out}} \cdot \frac{N_A}{N_S} \quad [\text{V}] \quad [1]
\]

Switching cycle peak current limiting is set by parallel shunt resistors RCS1 to 4, which give a combined resistance of 450 mΩ, setting the peak current to 2.67 A according to the threshold VCSTH of 1.2 V. This limits the inrush current during start-up and also protects against damage under over load or short circuit conditions. The eval board is not designed to withstand a sustained output overload or short circuit. The maximum peak current at low line and full load, assuming DMAX is 0.58 is calculated as:

\[
I_{\text{Pmax}} = \frac{2\sqrt{2} P_{\text{out}}}{D_{\text{MAX}} V_{\text{AC min}} \eta} = \frac{2\sqrt{2} \times 20}{0.58 \times 100 \times 0.9} = 2.71 \quad [\text{A}] \quad [2]
\]

The transformer turns-ratio is calculated as follows:

\[
N = \frac{N_P}{N_S} = \frac{\sqrt{2} V_{\text{AC min}}}{V_{\text{out}} + V_{F}} \cdot \frac{D_{\text{MAX}}}{1 - D_{\text{MAX}}} = \frac{\sqrt{2} \times 100}{55 + 1} \cdot \frac{0.58}{1 - 0.58} = 3.49 \quad [3]
\]

The primary to auxiliary winding turns-ratio is calculated to provide an auxiliary supply voltage of 20 V:

\[
\frac{N_P}{N_A} = \frac{\sqrt{2} V_{\text{AC min}}}{V_{\text{aux}} + V_{F(\text{aux})}} \cdot \frac{D_{\text{MAX}}}{1 - D_{\text{MAX}}} = \frac{\sqrt{2} \times 100}{20 + 1} \cdot \frac{0.58}{1 - 0.58} = 9.3 \quad [4]
\]

The transformer primary inductance is calculated according to the formula:

\[
L_{\text{PRI}} = \frac{V_{\text{AC min}}^2 \cdot \eta \cdot D_{\text{MAX}}^2}{2 \cdot P_{\text{out}} \cdot f_{\text{MIN}}} \quad [\text{H}] \quad [5]
\]
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55 W Flyback converter design using the IRS2982S controller

Dimensioning

\[
\frac{100^2 \cdot 0.9 \cdot 0.58^2}{2 \cdot 50 \cdot 40000} = 757 \cdot 10^{-6} \text{ H} = 757 \quad [\mu \text{H}]
\]

Where, \( \eta \) is the efficiency assumed to be 0.9 and minimum frequency set to 40 kHz to occur at the peak of the line input voltage at 100 Vrms.

The resistor divider comprising RFB1 and RFB2 sets the output voltage according to:

\[
V_{\text{OUT}} = \frac{N_P}{N_A} \cdot \frac{1}{N} \cdot V_{\text{REF}} \cdot \frac{R_{\text{FB1}} + R_{\text{FB2}}}{R_{\text{FB2}}} \quad [\text{V}] \quad [6]
\]

In this design, \( R_{\text{FB2}} = 20 \) k and \( R_{\text{FB1}} = 1 \) M. VREF is 400 mV specified in the IRS2982S datasheet therefore:

\[
9.3 \times \frac{1}{3.49} \cdot 0.4 \cdot \frac{20k + 1000k}{20k} = 54.4 \quad [\text{V}]
\]

The threshold for over voltage protection through the ZX input is given by the resistor divider consisting of RZX1 and RZX2, where \( R_{\text{ZX1}} = 47 \) k and \( R_{\text{ZX2}} = 14 \) k and \( V_{\text{OVTH}} \) is 5.1 V:

\[
V_{\text{OUTOV}} = \frac{N_P}{N_A} \cdot \frac{1}{N} \cdot V_{\text{OVTH}} \cdot \frac{R_{\text{ZX1}} + R_{\text{ZX2}}}{R_{\text{ZX2}}} \quad [\text{V}] \quad [7]
\]

\[
9.3 \times \frac{1}{3.49} \cdot 5.1 \cdot \frac{47k + 14k}{14k} = 59.2 \quad [\text{V}]
\]

The maximum reflected voltage appearing at the MOSFET drain is then calculated as follows based on the highest AC line input voltage of 265 Vac:

\[
V_{\text{DMAX}} = \sqrt{2} \cdot V_{\text{ACMAX}} + (V_{\text{OUT(MAX)}} + V_F) \cdot N \quad [\text{V}] \quad [8]
\]

\[
\sqrt{2} \cdot 265 + (60 + 1) \cdot 3.49 = 588 \quad [\text{V}]
\]

It is recommended to allow 30% headroom on top of the reflected voltage to accommodate the switch off transient and high voltage ringing. This requires a MOSFET with a minimum drain-source maximum rating of 765 V and therefore an 800 V part has been selected.

Four parallel 470 \( \mu \text{F} \) output capacitors (COUT1 to 4) have been used with a total capacitance of 1880 \( \mu \text{F} \), combined ripple current rating of 8 A and impedance of 7 mΩ at 100 kHz. The maximum low frequency output ripple can be calculated as follows:

\[
V_{\text{ripp}} = \frac{l_{\text{OUT}}}{2 \cdot \pi \cdot f_{\text{AC(min)}} \cdot C_{\text{OUT}}} \quad [\text{Vpp}] \quad [9]
\]

\[
\frac{1}{2 \cdot \pi \cdot 45 \cdot 1880 \cdot 10^{-6}} = 1.88 \quad [\text{Vpp}]
\]

\[
C_{\text{OUT}} = \frac{l_{\text{OUT}}}{2 \cdot \pi \cdot f_{\text{AC(min)}} \cdot V_{\text{ripp}}} \quad [\text{F}] \quad [10]
\]
6 Control loop

The voltage mode Flyback converter operating in critical conduction mode has a basic error amplifier to output voltage (VCOMP) transfer characteristic with a single pole of the form:

\[
\frac{V_{\text{OUT}}(s)}{V_{\text{COMP}}(s)} \approx \frac{k f_s}{D} \cdot \frac{1}{1 + \omega_p \omega_0}
\]  

[11]

Where,

\[
\omega_p \omega_0 = \frac{2 \omega_p}{R_{\text{LOAD}} \cdot C_{\text{OUT}}}, \quad R_{\text{LOAD}} = \frac{V_{\text{OUT}}}{I_{\text{OUT}}}
\]

And 'k' is a constant of approximately \(2.5 \times 10^{-6}\) defined by the IRS2982S.

To prevent over-shoot of the output voltage at start up while maintaining good regulation, power factor and line current THD a type 2 compensation network is used at the COMP pin, which is the output of the IRS2982S internal OTA error amplifier. The loop gain needs to cross 0 dB below the minimum line frequency with sufficient margin to achieve good PF/iTHD performance.

![Figure 6 Type 2 OTA compensation](image)

The transfer function has a zero at low frequency formed by R (RCMP) and CZ (CCMP2) and a pole at higher frequency formed by R and CP (CCMP1). The OTA \(g_m\) is approximately \(100 \mu \Omega^{-1}\) as specified in the data sheet.

The error amplifier transfer function is as follows:

\[
\frac{V_{\text{COMP}}(s)}{V_{\text{IN}}(s)} \approx \frac{R_{\text{LOWER}} g_m R}{R_{\text{LOWER}} + R_{\text{UPPER}}} \cdot \frac{1 + \frac{1}{SRC_p}}{1 + sRC_p}
\]  

[12]

The mid-band gain is given by:

\[
G_o = \frac{R_{\text{LOWER}} g_m R}{R_{\text{LOWER}} + R_{\text{UPPER}}}
\]  

[13]
Control loop

The zero is given by:

\[ \omega_z = \frac{1}{R.C_z} \]  \[14\]

The pole is given by:

\[ \omega_p = \frac{1}{R.C_p} \]  \[15\]

Figure 7  Bode plot showing gain and phase with type 2 compensation at full load, low line

The red lines show the converter plant transfer function from \( V_{\text{COMP}} \) to \( V_{\text{OUT}} \) and the blue lines show the feedback network and error amplifier transfer function. These are added together to give the loop transfer function \( T(s) \) shown by the dotted line.

It can be seen that at maximum load the gain crosses zero dB at approximately 20 Hz and the phase margin is 87 \(^\circ\), which provides a stable system. Bode plots at different line and load conditions indicate that the system will always be stable.
## Bill of materials

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Designator</th>
<th>Manufacturer</th>
<th>Part Number</th>
<th>Value/Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>BR1</td>
<td>Vishay</td>
<td>GBUA4-E3/51</td>
<td>600 V/4 A</td>
</tr>
<tr>
<td>1</td>
<td>CCF</td>
<td>TDK</td>
<td>C2012X7R2E102K085AA</td>
<td>1 nF/250 V/0805/10%</td>
</tr>
<tr>
<td>1</td>
<td>CCOM1</td>
<td>TDK</td>
<td>C2012X7R1E224K125AB</td>
<td>0.22 µF/25 V/0805/10%</td>
</tr>
<tr>
<td>1</td>
<td>CDC</td>
<td>Epcos</td>
<td>R32922C104M</td>
<td>0.1 µF/305 VAC/X2</td>
</tr>
<tr>
<td>1</td>
<td>CFB</td>
<td>TDK</td>
<td>C3216CH1H103K085AA</td>
<td>10 nF/50 V/1206/10%</td>
</tr>
<tr>
<td>1</td>
<td>COM1</td>
<td>Keystone</td>
<td>S001</td>
<td>0.04&quot; dia black</td>
</tr>
<tr>
<td>1</td>
<td>COM2</td>
<td>Keystone</td>
<td>S001</td>
<td>0.04&quot; dia black</td>
</tr>
<tr>
<td>1</td>
<td>COMP</td>
<td>Keystone</td>
<td>S004</td>
<td>0.04&quot; dia yellow</td>
</tr>
<tr>
<td>1</td>
<td>COUT1</td>
<td>Panasonic</td>
<td>EEU-FR1J471B</td>
<td>470 µF/63 V/20%</td>
</tr>
<tr>
<td>1</td>
<td>COUT2</td>
<td>Panasonic</td>
<td>EEU-FR1J471B</td>
<td>470 µF/63 V/20%</td>
</tr>
<tr>
<td>1</td>
<td>COUT3</td>
<td>Panasonic</td>
<td>EEU-FR1J471B</td>
<td>470 µF/63 V/20%</td>
</tr>
<tr>
<td>1</td>
<td>COUT4</td>
<td>Panasonic</td>
<td>EEU-FR1J471B</td>
<td>470 µF/63 V/20%</td>
</tr>
<tr>
<td>1</td>
<td>CSNB</td>
<td>TDK</td>
<td>C4532X7R3A102M200KA</td>
<td>1 nF/1 kV/20%/1812/X7R</td>
</tr>
<tr>
<td>1</td>
<td>CVB</td>
<td>TDK</td>
<td>C3216X5R1H106K160AB</td>
<td>10 µF/50 V/1206/10%</td>
</tr>
<tr>
<td>1</td>
<td>CVCC1</td>
<td>TDK</td>
<td>C3216C0G1H1049160AA</td>
<td>0.1 µF/50 V/1206/5%</td>
</tr>
<tr>
<td>1</td>
<td>CVCC2</td>
<td>Panasonic</td>
<td>EEU-EB1H220S</td>
<td>10 µF/50 V/1206/10%</td>
</tr>
<tr>
<td>1</td>
<td>CX1</td>
<td>Epcos</td>
<td>R32922C3104M</td>
<td>0.1 µF/305 VAC/X2</td>
</tr>
<tr>
<td>1</td>
<td>CX2</td>
<td>Epcos</td>
<td>R32922C3224M</td>
<td>0.22 µF/305 VAC/X2</td>
</tr>
<tr>
<td>1</td>
<td>CY1</td>
<td>Vishay</td>
<td>VY2102M29YSU63V7</td>
<td>1 nF/300 VAC/Y</td>
</tr>
<tr>
<td>1</td>
<td>CY2</td>
<td>Vishay</td>
<td>VY2102M29YSUG63V7</td>
<td>1 nF/300 VAC/Y</td>
</tr>
<tr>
<td>1</td>
<td>CY3</td>
<td>Vishay</td>
<td>VY2102M29YSU63V7</td>
<td>1 nF/300 VAC/Y</td>
</tr>
<tr>
<td>1</td>
<td>CZX</td>
<td>Kemet</td>
<td>C0805C220J5ACTU</td>
<td>22 µF/50 V/0805/5%</td>
</tr>
<tr>
<td>1</td>
<td>DOUT</td>
<td>Diodes Inc</td>
<td>SBR20A300CT</td>
<td>300 V/10 A/TO-220AB</td>
</tr>
<tr>
<td>1</td>
<td>DSNB</td>
<td>Diodes Inc</td>
<td>RS1MB-13-F</td>
<td>100 V/1 A/SMB</td>
</tr>
<tr>
<td>1</td>
<td>DVCC1</td>
<td>Diodes Inc</td>
<td>LL4148-13</td>
<td>75 V/0.15 A/MINIMELF</td>
</tr>
<tr>
<td>1</td>
<td>DVCC2</td>
<td>Diodes Inc</td>
<td>LL4148-13</td>
<td>75 V/0.15 A/MINIMELF</td>
</tr>
<tr>
<td>1</td>
<td>DZ</td>
<td>Micro Commercial Co</td>
<td>RZV55C18-TP</td>
<td>18 V/0.5 W/MINIMELF</td>
</tr>
<tr>
<td>1</td>
<td>F1</td>
<td>Bussman</td>
<td>SS-5H-1.6A-APH</td>
<td>T1.6 A/300 VAC/4-8.5</td>
</tr>
<tr>
<td>1</td>
<td>IC1</td>
<td>Infineon</td>
<td>IRS2982S</td>
<td>SMS Controller</td>
</tr>
<tr>
<td>1</td>
<td>IFB</td>
<td>Keystone</td>
<td>S003</td>
<td>0.04&quot; dia orange</td>
</tr>
<tr>
<td>1</td>
<td>L1</td>
<td>Kemet</td>
<td>SS24H-R05600-CH</td>
<td>2x60 mH Common Mode</td>
</tr>
<tr>
<td>1</td>
<td>MFB</td>
<td>Infineon</td>
<td>IPA80R650CE</td>
<td>800 V/4.5 A/TO-220</td>
</tr>
<tr>
<td>1</td>
<td>P1</td>
<td>Phoenix Contact</td>
<td>1985205</td>
<td>3 Position 3.5mm Green</td>
</tr>
<tr>
<td>1</td>
<td>P2</td>
<td>Phoenix Contact</td>
<td>1985195</td>
<td>2 Position 3.5mm Green</td>
</tr>
<tr>
<td>1</td>
<td>PFC</td>
<td>Keystone</td>
<td>S002</td>
<td>0.04&quot; dia white</td>
</tr>
<tr>
<td>1</td>
<td>RCF</td>
<td>Panasonic</td>
<td>ERJ-6GEYJ471V</td>
<td>470/0.125 W/0805/5%</td>
</tr>
<tr>
<td>1</td>
<td>RCMP</td>
<td>Panasonic</td>
<td>ERJ-6GEYJ334V</td>
<td>330 k/0.125 W/0805/5%</td>
</tr>
<tr>
<td>1</td>
<td>RCS1</td>
<td>Panasonic</td>
<td>ERJ-8GEYJ4R7V</td>
<td>4.7/0.25 W/1206/5%</td>
</tr>
<tr>
<td>1</td>
<td>RCS2</td>
<td>Panasonic</td>
<td>ERJ-8GEYJ1R5V</td>
<td>1.5/0.25 W/1206/5%</td>
</tr>
<tr>
<td>1</td>
<td>RCS3</td>
<td>Panasonic</td>
<td>ERJ-8GEYJ1R5V</td>
<td>1.5/0.25 W/1206/5%</td>
</tr>
<tr>
<td>1</td>
<td>RCS4</td>
<td>Panasonic</td>
<td>ERJ-8GEYJ1R5V</td>
<td>1.5/0.25 W/1206/5%</td>
</tr>
<tr>
<td>1</td>
<td>RFB1</td>
<td>Panasonic</td>
<td>ERJ-8GEYJ105V</td>
<td>1 M/0.25 W/1206/5%</td>
</tr>
<tr>
<td>1</td>
<td>RFB2</td>
<td>Panasonic</td>
<td>ERJ-8GEYJ203V</td>
<td>20 k/0.25 W/1206/5%</td>
</tr>
<tr>
<td>1</td>
<td>RG1</td>
<td>Panasonic</td>
<td>ERJ-8GEYJ4R7V</td>
<td>4.7/0.25 W/1206/5%</td>
</tr>
<tr>
<td>1</td>
<td>RG2</td>
<td>Panasonic</td>
<td>ERJ-8GEYJ103V</td>
<td>10 k/0.25 W/1206/5%</td>
</tr>
<tr>
<td>1</td>
<td>RHV</td>
<td>Yageo</td>
<td>CFR-50FB52-10K</td>
<td>10 k/0.5 W/5%</td>
</tr>
<tr>
<td>1</td>
<td>ROUT</td>
<td>Panasonic</td>
<td>ERJ-8GEYJ153V</td>
<td>15 k/0.25 W/1206/5%</td>
</tr>
<tr>
<td>1</td>
<td>RSNB1</td>
<td>Panasonic</td>
<td>ERJ-8GEYJ474V</td>
<td>470 k/0.25 W/1206/5%</td>
</tr>
</tbody>
</table>
## IRXLED04

55 W Flyback converter design using the IRS2982S controller

### Bill of materials

<p>| | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RSNB2</td>
<td>Panasonic</td>
<td>ERJ-8GEYJ474V</td>
<td>470 k/0.25 W/1206/5%</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>RSNB3</td>
<td>Panasonic</td>
<td>ERJ-8GEYJ474V</td>
<td>470 k/0.25 W/1206/5%</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>RVCC1</td>
<td>Panasonic</td>
<td>ERJ-8GEYJ100V</td>
<td>10 k/0.25 W/1206/5%</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>RVCC2</td>
<td>Panasonic</td>
<td>ERJ-8GEYJ511V</td>
<td>510 k/0.25 W/1206/5%</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>RZX1</td>
<td>Panasonic</td>
<td>ERJ-8GEYJ473V</td>
<td>47 k/0.25 W/1206/5%</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>RZX2</td>
<td>Panasonic</td>
<td>ERJ-8ENF1402V</td>
<td>14 k/0.125 W/0805/1%</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>T1</td>
<td>Wurth Finepower</td>
<td>750316066 Rev 00 TPT-PQ2627-001A</td>
<td>Flyback Transformer</td>
<td>800 µH 64:18:7</td>
</tr>
<tr>
<td>1</td>
<td>VCC</td>
<td>Keystone</td>
<td>5000</td>
<td>0.04” dia red</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>VCS</td>
<td>Keystone</td>
<td>5003</td>
<td>0.04” dia orange</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>VD(HV)</td>
<td>Keystone</td>
<td>5000</td>
<td>0.04” dia red</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>VOUT+</td>
<td>Keystone</td>
<td>5000</td>
<td>0.04” dia red</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>VOUT-</td>
<td>Keystone</td>
<td>5001</td>
<td>0.04” dia black</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>VR1</td>
<td>Epcos</td>
<td>S10K320E2K1</td>
<td>510 V/3.5 kA/10 mm</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Z1</td>
<td>Keystone</td>
<td>1902F</td>
<td>Standoff, Hex 0.65” L 4-40THR Nylon</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Z2</td>
<td>B &amp; F Fastner</td>
<td>NY PMS 440 0025 PH</td>
<td>Screw, Philips 4-40 x 1/4 Nylon</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Z3</td>
<td>Heatsink (for MFB)</td>
<td>577102B04000G</td>
<td>HEATSINK TO-220 W/TAB 5/7”</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Z4</td>
<td>Screw</td>
<td>9900</td>
<td>MACHINE SCREW PAN PHILLIPS 4-40</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Z5</td>
<td>Nut</td>
<td>4694</td>
<td>HEX NUT 3/16” STEEL 4-40</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Z6</td>
<td>Washer</td>
<td>4693</td>
<td>WASHER SPLIT LOCK #4 STEEL</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Z7</td>
<td>Heatsink (for DOUT)</td>
<td>Aavid Thermalloy</td>
<td>591202B00000G</td>
<td></td>
</tr>
</tbody>
</table>
Transformer specification

Core type and material: Wurth 150-2239 PQ2625, PC44
Bobbin: THT, Vertical, Wurth p/n: 070-5649
Primary inductance and leakage inductance:
Lp = 795µH (±5%), measured between pin1 and pin3, leakage inductance ≤ 10µH

<table>
<thead>
<tr>
<th>Start</th>
<th>End</th>
<th>No. of Turns</th>
<th>Wire Size</th>
<th>Layers</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>2</td>
<td>31</td>
<td>1 x φ0.4mm</td>
<td>½ Primary</td>
</tr>
<tr>
<td>11,12</td>
<td>9,10</td>
<td>9</td>
<td>2 x triple φ0.45mm</td>
<td>½ Secondary</td>
</tr>
<tr>
<td>5</td>
<td>4</td>
<td>7</td>
<td>1 x φ0.32mm</td>
<td>Flyback Auxiliary</td>
</tr>
<tr>
<td>9,10</td>
<td>7,8</td>
<td>9</td>
<td>2 x triple φ0.45mm</td>
<td>½ Secondary</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>33</td>
<td>1 x φ0.4mm</td>
<td>½ Primary</td>
</tr>
</tbody>
</table>

Figure 8  Flyback transformer specification
IRXLED04
55 W Flyback converter design using the IRS2982S controller

PCB Layout

9 PCB Layout

Figure 9  PCB top side components and traces

Figure 10  PCB bottom side components and traces
9.1 PCB layout guidelines for system optimization

The left side of the above figure shows the primary and secondary high frequency current loops surrounded by a black outline in each case. The primary loop on the left side of the board originates from CDC connecting first to the transformer (T1) primary (pin 1). The other side of the primary winding (pin 3) is connected to the drain of the MOSFET (MFB). To minimize EMI this trace should be kept as short as possible, however in this board due to the shape and the alternative DPAK footprint that has also been included, MFB could not be located directly next to T1. A ground plane has been placed on the other side of the PCB to absorb some of the EMI. The current sense resistors (RC1-4) are located such that the connection to the high frequency 0V bus return of CDC is extremely short with the other end connected to the source of MFC through another short trace. A pad connected to CDC 0V is provided so that a grounded heatsink may be used, provided the MOSFET is in an insulated TO-220 FullPAK. This also absorbs some of the EMI originating from the drain.

The secondary high frequency current loop originates from T1 pins 11 and 12 connecting through a short trace to DOUT, which then connects through another very short trace to COUT1. The negative side of COUT1 returns directly back to T1 pins 7 and 8 again through another short trace providing the tightest possible HF current loop. Parallel output capacitors COUT2-4 are connected to COUT1 through very heavy Copper traces to provide minimum impedance and best possible HF ripple current sharing between the capacitors. A grounding pad is also provided for the DOUT heat sink. The diode must also be in a TO-220 FullPAK to use a grounded heatsink.

The primary-secondary 0V Y capacitor (CY3) is connected directly to each 0V HF point with the shorted possible traces.

The layout techniques described minimize EMI emitted by the converter as much as possible.

Aside from EMI considerations, it is essential to design the PCB so that the IRS2982 is able to operate correctly without suffering from potential interference caused by noise or incorrect grounding. The picture on the right of the above figure shows the area around IC1. Pin 6 is the 0V (ground) connection, which is returned to the 0V side of CDC through a direct connection. It is also essential that decoupling capacitor CVCC1 be located directly next to IC1 with direct connections to the VCC and COM/0V pins.

As in all switching power supplies, the signal and power grounds must be kept separate and join together only at the star point, which is at the negative side of the high frequency capacitor (CDC).

Components associated with IC1 such as CCF, CZX CMP1 and RCMP are connected to the signal ground with the shortest traces possible back to pin 6.
Additionally, clearance distances between high voltage traces and other parts of the circuit are kept as large as possible to comply with safety requirements. For this reason the middle leads of MFB and DOUT are bent forward to connect to a pad located further from the other two pads.
10. Test results

10.1 Operation at maximum load

The following measurements were made with IPA80R650CE MOSFET fitted as MFB.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>VAC</td>
<td>Vrms</td>
<td>100 120 230 265</td>
</tr>
<tr>
<td>Vdrain(ref)</td>
<td>V</td>
<td>326 349 510 550</td>
</tr>
<tr>
<td>VCSpk</td>
<td>V</td>
<td>1.19 1.06 0.73 0.69</td>
</tr>
<tr>
<td>ICSpk</td>
<td>A</td>
<td>2.63 2.35 1.62 1.53</td>
</tr>
<tr>
<td>Ton</td>
<td>µs</td>
<td>16.00 12.03 4.39 3.68</td>
</tr>
<tr>
<td>Toff</td>
<td>µs</td>
<td>12.16 10.87 8.22 7.76</td>
</tr>
<tr>
<td>D</td>
<td></td>
<td>0.57 0.53 0.35 0.32</td>
</tr>
<tr>
<td>Fs</td>
<td>kHz</td>
<td>35.51 43.67 79.30 87.41</td>
</tr>
<tr>
<td>ZXmax</td>
<td>V</td>
<td>4.7 4.7 4.7 4.7</td>
</tr>
</tbody>
</table>

Table 1 Test result summary

10.2 Test measurements under different line and load conditions

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>100%</td>
<td>51.98</td>
<td>51.98</td>
<td>1.00</td>
<td>57.79</td>
<td>89.95%</td>
<td>0.993</td>
<td>5.60%</td>
<td>1.50</td>
</tr>
<tr>
<td>50%</td>
<td>26.39</td>
<td>52.77</td>
<td>0.50</td>
<td>28.94</td>
<td>91.17%</td>
<td>0.994</td>
<td>6.10%</td>
<td>0.75</td>
</tr>
<tr>
<td>20%</td>
<td>10.80</td>
<td>54.02</td>
<td>0.20</td>
<td>12.10</td>
<td>89.29%</td>
<td>0.981</td>
<td>8.70%</td>
<td>0.30</td>
</tr>
<tr>
<td>0.50%</td>
<td>2.80</td>
<td>56.09</td>
<td>0.05</td>
<td>3.67</td>
<td>76.42%</td>
<td>0.855</td>
<td>n/a</td>
<td>0.08</td>
</tr>
<tr>
<td>0</td>
<td>0.00</td>
<td>59.30</td>
<td>0.00</td>
<td>0.68</td>
<td>0.00%</td>
<td>n/a</td>
<td>n/a</td>
<td>0.02</td>
</tr>
</tbody>
</table>

Table 2 Input 100 VAC

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>100%</td>
<td>52.02</td>
<td>52.02</td>
<td>1.00</td>
<td>57.01</td>
<td>91.25%</td>
<td>0.994</td>
<td>5.60%</td>
<td>1.50</td>
</tr>
<tr>
<td>50%</td>
<td>26.43</td>
<td>52.85</td>
<td>0.50</td>
<td>28.81</td>
<td>91.72%</td>
<td>0.992</td>
<td>6.10%</td>
<td>0.75</td>
</tr>
<tr>
<td>20%</td>
<td>10.82</td>
<td>54.12</td>
<td>0.20</td>
<td>12.14</td>
<td>89.16%</td>
<td>0.971</td>
<td>8.50%</td>
<td>0.30</td>
</tr>
<tr>
<td>0.50%</td>
<td>2.82</td>
<td>56.38</td>
<td>0.05</td>
<td>3.81</td>
<td>73.99%</td>
<td>0.802</td>
<td>n/a</td>
<td>0.08</td>
</tr>
<tr>
<td>0</td>
<td>0.00</td>
<td>59.20</td>
<td>0.00</td>
<td>0.63</td>
<td>0.00%</td>
<td>n/a</td>
<td>n/a</td>
<td>0.02</td>
</tr>
</tbody>
</table>

Table 3 Input 120 VAC
IRXLED04
55 W Flyback converter design using the IRS2982S controller

Test results

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>100%</td>
<td>52.19</td>
<td>52.19</td>
<td>1.00</td>
<td>56.09</td>
<td>93.05%</td>
<td>0.983</td>
<td>9.10%</td>
<td>1.50</td>
</tr>
<tr>
<td>50%</td>
<td>26.51</td>
<td>53.01</td>
<td>0.50</td>
<td>28.89</td>
<td>91.74%</td>
<td>0.954</td>
<td>8.80%</td>
<td>0.75</td>
</tr>
<tr>
<td>20%</td>
<td>10.83</td>
<td>54.17</td>
<td>0.20</td>
<td>12.51</td>
<td>86.60%</td>
<td>0.825</td>
<td>15.40%</td>
<td>0.30</td>
</tr>
<tr>
<td>0.50%</td>
<td>2.79</td>
<td>55.83</td>
<td>0.05</td>
<td>3.76</td>
<td>74.24%</td>
<td>0.360</td>
<td>50.00%</td>
<td>0.08</td>
</tr>
<tr>
<td>0</td>
<td>0.00</td>
<td>56.00</td>
<td>0.00</td>
<td>0.33</td>
<td>0.00%</td>
<td>n/a</td>
<td>n/a</td>
<td>0.02</td>
</tr>
</tbody>
</table>

Table 4  Input 230 VAC

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>100%</td>
<td>52.22</td>
<td>52.22</td>
<td>1.00</td>
<td>56.12</td>
<td>93.05%</td>
<td>0.975</td>
<td>9.90%</td>
<td>1.50</td>
</tr>
<tr>
<td>50%</td>
<td>26.52</td>
<td>53.04</td>
<td>0.50</td>
<td>29.00</td>
<td>91.45%</td>
<td>0.929</td>
<td>9.90%</td>
<td>0.75</td>
</tr>
<tr>
<td>20%</td>
<td>10.82</td>
<td>54.09</td>
<td>0.20</td>
<td>12.69</td>
<td>85.25%</td>
<td>0.755</td>
<td>16.70%</td>
<td>0.30</td>
</tr>
<tr>
<td>0.50%</td>
<td>2.78</td>
<td>55.53</td>
<td>0.05</td>
<td>3.61</td>
<td>76.91%</td>
<td>0.267</td>
<td>50.00%</td>
<td>0.08</td>
</tr>
<tr>
<td>0</td>
<td>0.00</td>
<td>55.70</td>
<td>0.00</td>
<td>0.31</td>
<td>0.00%</td>
<td>n/a</td>
<td>n/a</td>
<td>0.02</td>
</tr>
</tbody>
</table>

Table 5  Input 265 VAC
IRXLED04
55 W Flyback converter design using the IRS2982S controller

Test results

**Figure 4**  Line regulation at different loads

**Figure 5**  Load regulation at different AC input voltage values
Test results

Figure 6  Power factor vs load

Figure 7  THDi vs load
Figure 8  Efficiency vs load
IRXLED04
55 W Flyback converter design using the IRS2982S controller

Test results

10.3 Start and steady state operation at maximum load

Figure 9  100 VAC steady state operation at 100% load
Input current (yellow), CS (blue), VCC (red), VOUT ripple (green)

Figure 10  100 VAC start-up at 100% load
Input current (yellow), CS (blue), VCC (red), VOUT (green)
IRXLED04
55 W Flyback converter design using the IRS2982S controller

Test results

Figure 11  230 VAC steady state operation at 100% load
Input current (yellow), CS (blue), VCC (red), VOUT ripple (green)

Figure 20  230 VAC start-up at 100% load
Input current (yellow), CS (blue), VCC (red), VOUT (green)

At both 120VAC and 230VAC with full load the output voltage rises within the specified time with minimal or no over-shoot. Cycle by cycle current limit operates for the first few AC line half-cycles limiting inrush current.
10.4 Start-up under different line and load conditions

Figure 12  100 VAC start-up at 100% load
Output voltage (yellow), VCOMP (red), VFB (green)

Figure 13  120 VAC start-up at 100% load
Output voltage (yellow), VCOMP (red), VFB (green)
Test results

Figure 14  230 VAC start-up at 100% load
Output voltage (yellow), VCOMP (red), VFB (green)

Figure 15  265 VAC start-up at 100% load
Output voltage (yellow), VCOMP (red), VFB (green)
IRXLED04
55 W Flyback converter design using the IRS2982S controller

Test results

Figure 16 120 VAC start-up at 50% load
Output voltage (yellow), VCOMP (red), VFB (green)

Figure 17 120 VAC start-up at 20% load
Output voltage (yellow), VCOMP (red), VFB (green)
IRXLED04
55 W Flyback converter design using the IRS2982S controller

Test results

Figure 18  230 VAC start-up at 50% load
Output voltage (yellow), VCOMP (red), VFB (green)

Figure 19  230 VAC start-up at 20% load
Output voltage (yellow), VCOMP (red), VFB (green)
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55 W Flyback converter design using the IRS2982S controller

Test results

Figure 20  120 VAC start-up at 0% load
Output voltage (yellow), VCOMP (red), VFB (green)

Figure 30  265 VAC start-up at 0% load
Output voltage (yellow), VCOMP (red), VFB (green)
10.5 Operation at line peak and zero crossing

Figure 21 120 VAC at 100% load, AC line peak
Gate drive (yellow), CS (blue), VZX (red), Vdrain (green)

Figure 22 120 VAC at 100% load line zero-crossing
Gate drive (yellow), CS (blue), VZX (red), Vdrain (green)
Test results

Figure 23  230 VAC at 100% load line peak
Gate drive (yellow), CS (blue), VZX (red), Vdrain (green)

Figure 24  230 VAC at 100% load line zero-crossing
Gate drive (yellow), CS (blue), VZX (red), Vdrain (green)

Close to the line zero-crossing the amplitude of VZX is below the VZX+ threshold of 1.54 V so the next
switching cycle is not started until the restart interval timeout period $t_{WD}$. This does not significantly impact
power factor and THD.
10.6  Burst mode operation at zero load

Figure 25  120 VAC start-up at 0% load burst mode operation
Gate drive (yellow), VCOMP (blue), VZX (red)

Figure 26  230 VAC start-up at 0% load burst mode operation
Gate drive (yellow), VCOMP (blue), VZX (red)
10.7 Light load DCM operation

![Figure 27](image)

**Figure 27** 100 VAC start-up at zero load
Gate drive (yellow), VCOMP (blue), VZX (red), Vdrain (green)

10.8 Over-voltage protection through ZX

![Figure 28](image)

**Figure 28** 265 VAC load step from 100% to 0%
VOUT (yellow), Gate drive (blue), VCOMP (red), VZX (green)
10.9 High voltage start-up operation

The high voltage start-up (HV pin) input current is measured with a 10 k resistor (RHV) connected from HV to the bus so that the oscilloscope traces in the following figures display approximately 1 mA/div:

Figure 29 100 VAC start-up at 100% load
HV start-up current (yellow), VFB (blue), VCC (red), Gate drive (green)

Figure 40 265 VAC start-up at 100% load
HV start-up current (yellow), VFB (blue), VCC (red), Gate drive (green)
10.10 High voltage start-up cell operation during zero load burst mode

Figure 30  120 VAC start-up at 0% load
HV start-up current (yellow), VFB (blue), VCC (red), Gate drive (green)

Figure 31  230 VAC start-up at 0% load
HV start-up current (yellow), VFB (blue), VCC (red), Gate drive (green)

These waveforms show that in burst mode the auxiliary winding is able to supply VCC therefore the HV start-up cell support mode does not come into operation.
10.11 Thermal Performance under normal operating conditions

Figure 32  100 VAC at 100% load (board top and bottom sides)

Figure 33  265 VAC at 100% load (board top and bottom sides)
10.12 Thermal Performance under abnormal operating conditions

10.12.1 Open feedback loop (RFB1 removed), VCC supply connected

The IRS2982S (IC1) reaches maximum case temperature at high line, 20% load. Temperature is measured in ambient of 25 °C.

Figure 34  265 VAC at 20% load (IHV is 1mA/div)
VCC (yellow), VCOMP (blue), IHV (red), VOUT (green)

Figure 35  265 VAC at 20% load, IRS2982S case temperature
10.12.2 VCC supply removed (DVCC2 removed), feedback loop connected

The IRS2982S (IC1) reaches maximum case temperature at high line, 20% load. Temperature is measured in ambient of 25 °C.

![Graph showing VCC supply removed, feedback loop connected](image1)

**Figure 36** 265 VAC at 20% load (IHV is 1mA/div)
VCC (yellow), VCOMP (blue), IHV (red), VOUT (green)

![Temperature graph of IRS2982S](image2)

**Figure 37** 265 VAC at 20% load, IRS2982S case temperature
10.12.3 Reduced VCC supply (Support mode)

The IRS2982S (IC1) reaches maximum case temperature at high line, 20% load. Temperature is measured in ambient of 25 °C. VCC is supplied from an external supply maintained just above the UVLO threshold.

Figure 38 265VAC at 20% load (IHV is 1mA/div)
VCC (yellow), VCOMP (blue), IHV (red), VOUT (green)

Figure 50 265 VAC at 100% load, IRS2982S case temperature
10.13 Line current harmonics according to EN61000-3-2

<table>
<thead>
<tr>
<th>Requirements</th>
<th>Harmonics Limits Class C according EN 61000-3-2 for System Power &gt; 25W</th>
</tr>
</thead>
<tbody>
<tr>
<td>Harmonics Order</td>
<td>Maximum value expressed as a percentage of the fundamental input current</td>
</tr>
<tr>
<td>2</td>
<td>≤2%</td>
</tr>
<tr>
<td>3</td>
<td>&lt;30 λ%</td>
</tr>
<tr>
<td>5</td>
<td>10%</td>
</tr>
<tr>
<td>7</td>
<td>≤7%</td>
</tr>
<tr>
<td>9</td>
<td>≤5%</td>
</tr>
<tr>
<td>11 ≤ n ≤ 39</td>
<td>≤3%</td>
</tr>
</tbody>
</table>

λ = power factor

Table 6 EN61000-3-2 Class C limits for system power >25 W

![Figure 39](harmonic_test_results_100_load.png)  
Figure 39 Harmonic test results at 120 VAC and 100% load

![Figure 40](harmonic_test_results_50_load.png)  
Figure 40 Harmonic test results at 120 VAC and 50% load
IRXLED04
55 W Flyback converter design using the IRS2982S controller

Test results

Figure 41  Harmonic test results at 230 VAC and 100% load

Figure 42  Harmonic test results at 230 VAC and 50% load

Class C limits are met at 50% and 100% loads at 120 VAC and 230 VAC.
10.13.1 EMI Conducted Emissions (tested to CISPR22 limits)

Figure 43 Conducted emissions at 120 VAC and 100% load

Figure 44 Conducted emissions at 230 VAC and 100% load

The red limit line shows the limit for the quasi-peak measurement, for which the frequency sweep trace is also shown in red. To pass the red trace must to remain below the red limit line and the pink average measurement trace must remain below the yellow average limit line. The orange peak trace may be disregarded.

EMI emissions are very dependent on the board layout, please refer to section 9.1.

Note

Infineon Technologies does not guarantee compliance with any EMI standard.
11 Conclusion

The specifications as listed in section 3.2 are met with efficiency exceeding 90% across the full line input voltage range from 50% to 100% load. Power factor remains above 0.95 at 120 VAC and 230 VAC nominal inputs from 50% load to 100%. The input current total harmonic distortion (iTHD) remains below 10% from 20% to 100% load over at 120 VAC input and from 70% to 100% load at 230 VAC, remaining below 20% down to 20% load from 100 to 265 VAC. At lighter loads power factor falls and iTHD increases, however output voltage regulation remains tight. Output voltage ripple at twice the AC line frequency remains 1.6 Vpp at full load at 60 Hz independent of the input voltage, which matches the calculated value from equation (10). Type 2 compensation of the operational trans-conductance error amplifier (OTA) provides tight load regulation from 10% to 100% load with a small increase below 10%. The output voltage rises to its operating level in less than 300 ms with no overshoot from 100 VAC to 265 VAC with only minimal overshoot at 100 VAC over the full load range. Performance indicates an over-damped control loop corresponding to the phase margin determined in section 6. The type 2 control loop compensation network successfully controls the startup and settling response while providing high power factor and low iTHD over a wide line/load range, which is able to meet EN61000-3-2 class C requirements for lighting apparatus. Over voltage protection as detected through the ZX input operates correctly to limit the output voltage under open and very light load conditions. Operation in DCM and burst mode are also seen to maintain output voltage regulation where necessary. Cycle by cycle primary over current protection operates correctly at start-up to limit inductor current and stress of the MOSFET. Operating waveforms confirm the calculated peak current value from section 5.

Thermal performance under normal operating conditions (measured in open air at 25 degrees C ambient) as shown in section 10.11, indicates a temperature rise of 45°C at the transformer windings, however the cores remain at a lower temperature. The input bridge (BR1) operates component at low line with a rise of 33°C with a greatly reduced temperature rise at high line of 23°C. The MOSFET (MFB) has a 37°C rise at low line and a 24°C rise at high line due to higher primary peak current at low line for the IPA80R650CE measured with no heatsink attached.

Under all normal conditions the high voltage start-up cell is deactivated as the feedback loop closes and it switches over from start-up mode to support mode. The HV cell allows the power supply to start up rapidly at any line input voltage, meeting the maximum specification of 300 ms from switch on to reaching nominal output voltage.

Standby power is composed of the power dissipated in the output resistor ROUT and the power consumed by the controller IC VCC supplying the MOSFET gate drive during burst mode operation as shown in figures 35 and 36. The power dissipated in ROUT is 240mW in this design, which can be reduced by increasing the resistor value although this could cause the output to sightly exceed 60V under an open load condition. This would not be an issue in designs with lower output voltages. Figure 36 shows that the burst duration at 230VAC is much shorter than that at 120VAC as shown in figure 35, which explains why the standby power is higher at low line.
Conclusion

Under fault conditions as shown in section 10.12, the start-up cell continues to operate in support mode in the following cases:

1. The feedback loop is open because the IRS2982S never switches to support mode. In this case there is no output voltage regulation however the output voltage is limited by continuous operation of the over-voltage protection. The IRS2982S draws between 1 and 2 mA under this condition causing the case temperature to rise 50°C at maximum line input 265 VAC. The IC would therefore remain within its recommended operating range at an ambient temperature up to 75°C.

2. VCC is not supplied through the auxiliary transformer winding but the feedback loop is still connected. In this case the HV start-up cell operating in support mode supplies all of the current to VCC. At maximum line input with 20% load, which is the worst case, the IRS2982S case temperature rises nearly 80°C. At a high ambient temperature there is a risk that the IC could exceed its maximum recommended operating temperature of 125°C. This situation should be avoided by ensuring that VCC receives current from the auxiliary winding during initial testing of the board.

3. VCC is not sufficiently supplied through the auxiliary transformer winding so that the HV start-up cell continues to supply current in support mode. For this test the auxiliary VCC supply was adjusted to maintain VCC just above the under-voltage lock-out threshold where the HV start-up cell continues to supply a little over 1 mA during normal operation. In this case at maximum line input the IRS2982S case temperature rise measured was 40°C.

Quasi-peak and average conducted emission sweeps fall within limits over the frequency spectrum from 150 kHz to 30 MHz. It should be noted that these measurements were not made by a certified test lab and are intended only as an indication of performance.

In conclusion, the IRS2982S based Flyback converter design provides excellent performance and robustness with tight control and reliable protection. This design is well suited as a front end section in a two stage LED driver, where the back end section would typically be a constant current regulated Buck stage. Since there is no output over-load or short circuit protection the output current can reach several Amps, therefore the converter could become damaged under prolonged operation in these conditions.

References


Attention:

Revision History

Major changes since the last revision

<table>
<thead>
<tr>
<th>Page or Reference</th>
<th>Description of change</th>
</tr>
</thead>
<tbody>
<tr>
<td>First Release</td>
<td></td>
</tr>
<tr>
<td>Rev 1.1</td>
<td>Added heat sinks and fasteners to the BOM</td>
</tr>
<tr>
<td>Rev 1.2</td>
<td>Correction to equation (5) and calculation. Added wiring diagram.</td>
</tr>
</tbody>
</table>
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