600 V CoolMOS™ P6
SJ MOSFET for Server, Telecom, PC Power and Consumer

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Application Note

About this document

Scope and purpose
This Application Note describes the characteristics of CoolMOS™ P6, the seventh technology platform of Infineon’s high voltage power MOSFETs designed according to the revolutionary Superjunction (SJ) principle. CoolMOS™ P6 will be described in reference to the existing CoolMOS™ generations both from a technology viewpoint and application performance. Design guidelines will be given to enable CoolMOS™ P6 optimized performance.

Intended audience
This document is intended for design engineers who want to improve their high voltage power conversion applications.

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Introduction

The new 600 V CoolMOS™ P6 is the seventh technology platform of Infineon’s high voltage power MOSFETs designed according to the revolutionary Superjunction (SJ) principle. After launching the 600 V C6 in 2009, 600 V E6 in 2010 the new P6 implements a combination of ultra-low $R_{\text{DS(on)}}$, high ruggedness, fast and well controlled switching speed, not sacrificing ease of use in combination with efficiency improvement. CoolMOS™ P6 series is designed for particularly applications, where the focus is not only in high efficiency and power density, but also provides ease-of-use as key requirements. The experimental measured results show efficiency comparisons with C6 and E6 series. Also CoolMOS™ P6 gives a well controlled switching characteristic, especially in peak current conditions such as load steps, start-up, and AC cycle drop-out. For providing the maximum flexibility to control CoolMOS™ P6 switching speed from design engineers, CoolMOS™ P6 offers the reduced integrated gate resistor value according to the device $R_{\text{DS(on)}}$ range. In summary, the combination of 600 V CoolMOS™ C6, E6 and P6 series will fulfill a wide range of applications requirements whether it requests ease-of-use at driven side given by C6 or the efficiency focus offered by P6. CoolMOS™ P6 electrical characteristic provides all benefits of a fast switching Superjunction (SJ) MOSFET while keeping ease-of-use and efficiency improvement. As usual CoolMOS™ P6 MOSFETs achieves low conduction loss and switching losses. It leads the design engineers to their power converters with high efficiency, high power density, and cool thermal behavior. Furthermore CoolMOS™ P6 series MOSFETs are universal applicable, i.e., suitable for hard and soft switching topologies (e.g. PFC, LLC)

1.1 Features and Benefits

Table 1 represents the main features and the benefits of CoolMOS™ P6, which will be discussed in detail in this Application Note.

<table>
<thead>
<tr>
<th>Features</th>
<th>Benefits</th>
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<tbody>
<tr>
<td>Reduced gate charge ($Q_g$)</td>
<td>Improved efficiency especially in light load condition</td>
</tr>
<tr>
<td>Optimized gate threshold voltage ($V_{th}$) for soft switching</td>
<td>Lower gate drive capability required</td>
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<tr>
<td>Good body diode ruggedness</td>
<td>Better efficiency in soft switching applications</td>
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<tr>
<td>Optimized integrated $R_g$</td>
<td>Suitability for hard- &amp; soft-switching topologies</td>
</tr>
<tr>
<td>Improved $dv/dt$</td>
<td>Good controllability</td>
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<td></td>
<td>High robustness &amp; better efficiency</td>
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1.2 Target Applications

Table 2 represents the target applications and topologies for CoolMOS™ P6 series MOSFETs.

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<thead>
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<th>PWM</th>
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<td>Boost-Stage</td>
<td>LLC</td>
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<tr>
<td>Telecom</td>
<td>Boost-Stage</td>
<td>LLC</td>
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SJ MOSFET for Server, Telecom, PC Power and Consumer

Introduction

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<td>Consumer</td>
<td>Boost-Stage</td>
<td>LLC</td>
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All the features and benefits of 600 V P6 MOSFETs in connection with the target applications and topologies will be analyzed in section 3.

1.3 Superjunction (SJ) Principle

“All CoolMOS™ series are based on the Superjunction principle, which is a revolutionary technology for high voltage power MOSFETs [1,2], Infineon Technologies has been the first company worldwide to commercialize this idea into the market [4]. Where conventional power MOSFETs just command on one degree of freedom to master both on-state resistance and blocking voltage, the Superjunction principle allows two degrees of freedom for this task. Therefore conventional MOSFETs are stuck with the limit of silicon, a barrier which marks the optimum doping profile for a given voltage class. This limit line has been theoretically derived by Chen and Hu in the late 80ies [3]. No commercial product has an on-state resistance better than the limit line of silicon.” [5] Figure 1 represents the area-specific on-resistance versus breakdown voltage.

![Figure 1](image)

**Figure 1** Area-specific on-resistance versus breakdown voltage comparison of standard MOSFET and CoolMOS™ technology [6]

“In contrast to that the Superjunction principle allows to reduce the on-state resistance of a high voltage MOSFET virtually to zero, limited only by technology efforts and manufacturing capabilities.” [5]

“The basic idea is simple: instead of having electrons flowing through a relatively high resistive (high voltage blocking) n-area, we allow them to flow in a very rich doped n-area, which gives naturally a very low on-state resistance. The crucial point for the SJ technology is to make the device block its full voltage, which requires a careful balancing of the additional n-charge by adjacently positioned deep p-columns, which go all the way straight through the device close to the back side n+ contact. This is where manufacturing capability comes in, as the charges within the device need to be compensated precisely under the constraints of a mass market production line.” [5] Figure 2 shows the cross section of a standard MOSFET (left) comparing with a SJ MOSFET (right).
“The SJ principle gives us the opportunity to create Best-in-Class types, which have not been possible before such as a 100 mΩ/600 V part in a TO-220 package. Furthermore it allows making parts with very low capacitances for a given $R_{DS(on)}$ as the silicon chip is much smaller than for a conventional power MOSFET. Both input and high voltage level of the output capacitance scale directly with the chip size, whereas reverse capacitance and to some extent the low voltage level of the output capacitance is technology dependent. Characteristic of all Superjunction devices is a strong non-linearity of the output capacitance with high values at low voltage and low values at high voltage. This behavior can be easily understood if you take into account that the output capacitance is proportional to the area of the blocking pn-junction and inverse proportional to the width of the space charge layer (or the voltage sustaining area). At low voltage the p-columns are not depleted and form a very big surface, furthermore the width of the space charge layer is very narrow (the white area in” Figure 2). ” At high voltage however the p-columns are fully depleted and the space charge layer has reached its full extension of roughly 45μm for a 600 V device. Important is that the non-linearity of the output capacitance allows a quasi zero-voltage-switching (ZVS) turn-off of the device, lowering turn-off losses. Superjunction devices are by nature fast in switching. Very small capacitances together with a low gate charge make rise and fall times of a few nanoseconds a reality. ” [5] For more information on Superjunction devices please read the article “Mastering the Art of Slowness” which is available on www.infineon.com/coolmos.
2 Technology parameters

2.1 Gate charge ($Q_g$)

One of the most important improvements of CoolMOS™ P6 is in device gate charge ($Q_g$) reduction which brings benefits especially in light load conditions due to reduced driving losses. P6 will offer a 30% $Q_g$ reduction in comparison with E6 which mainly comes from the reduction of the plateau charge. It also allows a very fast switching for turn-on and turn-off. The driver circuit current capability for P6 will be reduced over the whole $R_{DS(on)}$ range. Figure shows $Q_g$ in nC of P6 against E6 over the whole $R_{DS(on),max}$ range of P6.

![Graph showing Gatecharge reduction $Q_g \times R_{DS(on),max}$ [nC*mΩ]](image)

Figure 3 $Q_g$ comparison 600 V P6 vs. E6

2.2 High Gate threshold voltage ($V_{th}$)

In resonant topologies like LLC and ZVS it is possible to eliminate the turn-on loss but the turn-off loss is still one of big portion in the total losses consideration. A high gate threshold voltage ($V_{th}$) enables to give early turn-off of the MOSFET which results in better efficiency. Figure shows the transconductance characteristic comparison between P6, E6, and CP under same $R_{DS(on),max}$ 190 mΩ.
Our CP and E6 technologies are defined with the typical $V_{th}$ at 3 V. On this characteristic you can see that the P6-technology will show an increased $V_{th}$ to typical 4 V. Regarding the switching speed, it could observe that the slope of P6 is much faster than that of E6 and pretty close to CP, which provides low switching losses and gives high power conversion efficiency.

2.3 Energy stored in output capacitance ($E_{oss}$)

Figure 5 shows $E_{oss}$ loss which is indirect proportion to the output capacitance as a function of drain to source voltage of the MOSFET. E6 and P6 will have the same $C_{oss}$ value, so there is no difference visible in $E_{oss}$ and $Q_{oss}$.

Figure 5 represents $E_{oss}$ comparison between 600 V P6, E6, and CP in the $R_{DS(on),\text{max}}$ range of 380 mΩ.
CoolMOS™ P6 comes with an integrated gate resistor \(R_g\) in order to achieve self-limiting di/dt and dv/dt characteristics. This integrated small \(R_g\) allows fast turn-on and turn-off at normal operating current conditions but limits di/dt and dv/dt in case of abnormal conditions. The values of integrated \(R_g\) scales inversely with the gate charge respectively device capacitances. Figure 6 shows the value of \(R_g\) are used in P6 to maximizing efficiency while not sacrificing ease of use and good controllability.
Figure 6   Internal gate resistor for CoolMOS™ C6, E6 and P6 series

2.5  \( \text{dv/dt at turn-off in a 300 W PC Silverbox} \)

In Figure 7 is the measured \( \text{dv/dt} \) comparison between E6, P6, and CP in the \( R_{\text{DS(on)\_max}} \) range of 190 mΩ. CP has a maximum \( \text{dv/dt} \) of 50 V/ns and a high slope. Compared to CP, P6 technology offers a smooth \( \text{dv/dt} \) and an improved level of control. Even under a minimum of \( R_{\text{g,ext}} \), \( \text{dv/dt} \) of P6 is still lower than 50 V/ns. P6 technology is a very robust technology to withstand over 50 V/ns without changes in the characteristics. Due to the improvement of \( \text{dv/dt} \), it is allowed that to reduce the external \( R_g \) results to gain the efficiency.
2.6 \( E_{\text{on}} \) and \( E_{\text{off}} \) P6 vs. E6 vs. CP

Figure 8 shows the result of \( E_{\text{on}} \) and \( E_{\text{off}} \) characterization measurements for E6, P6 and CP at 5 A and 15 A drain current load under \( V_{\text{GS}}=12 \text{ V} \) and \( V_{\text{DS}}=400 \text{ V} \) in the range of gate resistor (\( R_g \)) from 3.4 \( \Omega \) to 31.2 \( \Omega \). \( E_{\text{on}} \) and \( E_{\text{off}} \) losses of P6 are much lower and significantly improved than that of E6 and on the similar level with CP. This improvement of P6 is based on reducing \( C_{\text{rss}} \) and the total \( Q_g \) working together with high \( V_{\text{th}} \) for low turn-off losses. With 10 \( \Omega \) external \( R_g \) at 5 A, P6 has 15% lower switching losses than that of E6. For 10 \( \Omega \) external \( R_g \) at 15 A case, P6 has 30% lower switching losses than that of E6.

Due to the improved turn-off losses P6 fits well in discontinuous conduction mode PFC and soft switching topologies like LLC where the turn-off losses are dominant.
Figure 8  
$E_{on}$ and $E_{off}$ comparison IPP60R190P6 vs. IPP60R190E6 and IPP60R199CP at $I_{D}=5$ A and $I_{D}=15$ A and test ambient temperature (TC) of 25°C
Measurement results

In this section real application measurements will be showed to demonstrate the benefits CoolMOS™ P6 in hard- and soft-switching applications.

3.1 Efficiency measurement in a 300 W PC Silverbox in CCM PFC

In this measurement the 600 V P6 is compared to E6 and CP in the 190 mΩ $R_{\text{DS(on)}}$ range.

Setup parameters:
- $V_{\text{in}} = 90 \text{ V}_{\text{AC}}$
- $V_{\text{out}} = 400 \text{ V}_{\text{DC}}$
- $P_{\text{out}} = 0 \text{ W to 300 W}$
- Frequency = 65 kHz
- $R_{\text{g,ext}} = 10 \Omega$, in a plug and play scenario between 600 V P6, E6 and CP

![Efficiency Low Line graph](image_url)

Figure 9 600 V P6 vs. E6 vs. CP comparison in absolute efficiency
The plug and play measurement shows the benefit of CoolMOS P6 in comparison to CoolMOS™ E6 and CoolMOS™ CP. In this 300 W continuous conduction mode (CCM) PC Silverbox, CCM operates after output power until 70 W or higher otherwise it works in DCM. Even in this light load condition, which is not an apple to apple comparison, P6 has a slightly efficiency improvement. When the output power over 70 W, CCM is operated, the efficiency improvement of P6 is visible in the range of 0.2% till 0.3% in full-load, comparing with that of E6. This efficiency benefit results due to Q\textsubscript{g} reduction and relatively high V\textsubscript{th}.

### 3.2 Efficiency measurement in a 200 W PC Silverbox in LLC stage

In this measurement the 600 V P6 is compared to E6 and CP in the 280 mΩ R\text{DS(on)} range.

**Setup parameters:**
- PC Silverbox LLC stage 200 W
- V\textsubscript{in} = 90 V\textsubscript{AC}
- V\textsubscript{out} = 400 V\textsubscript{DC}
- P\textsubscript{out} = 0 W to 200 W
- Frequency = 65 kHz
- R\textsubscript{g,ext\_turn-on} = 27 Ω
- R\textsubscript{g,ext\_turn-off} = 10 Ω
- Plug and play scenario between 600 V P6, E6, and CP
Figure 11  600 V P6 vs. E6 vs. CP comparison in absolute efficiency (upper) and delta efficiency (lower)

In this LLC measurement, P6 shows an efficiency benefit against E6 over 0.8% in light load. This improvement is also based on $Q_g$ reduction of 30% comparing with E6. At the full load, P6 and E6 give similar efficiency measured results due to the same $R_{DS(on)}$ level which is the important parameter at full load.
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Measurement results

Figure 12  600 V E6 vs. P6 comparison in turn-off

Figure 12 show $V_{GS}$, $V_{DS}$, and $I_D$ switching waveforms of P6 and E6. The miller plateau of P6 is much shorter than that of E6 to provide fast turn off. This reduction in based on $Q_g$ reduction of 30%. Due to the high $V_{th}$, a earlier turn-off and reduced turn-off time, lower losses are observed and it help to improve the power conversion efficiency.

3.3  Ringing measurements

In Figure 13, gate ringing oscillations of P6 in comparison with E6 and CP are illustrated. $V_{gs}$ peak is measured in this case using a typical PFC stage exhibiting 7.2 pF capacitive coupling between gate and drain emulating the parasitic capacitance of the PCB. This layout parasitic capacitance can be a source of noise on the gate switching waveforms especially with increasing load current.

In the measurement, P6 shows very good gate switching waveform even with reduced $Q_g$ and internal $R_g$. P6 slight increase in magnitude of oscillations over E6 is expected due to its faster switching characteristic than that of E6. Nevertheless it is still acceptable and provides enough margin before hurting the ±30 V gate ringing specification limit.
Figure 13  600 V P6 vs. E6 vs. CP comparison in ringing tendency
Figure 14  600 V P6 vs. E6 vs. CP comparison in ringing tendency

Figure 14 shows typical switching waveform of IPP60R190P6 in a PFC. This test circuit configured with an additional external gate to drain capacitance exhibiting 7.2 pF for capacitive coupling between gate and drain emulating PCB parasitic capacitance. Designers should put extra care in the layout to minimize this parasitic capacitance to enable the highest performance of the MOSFET. In this measurement, 5 Ω external $R_g$ for 190mΩ device is used.

Switching waveforms are measured with $V_{DS}=400$ V (shown in green) and $V_{GS}=13$ V (shown in crimson). The current waveform shown in yellow is increasing every pulse up to saturation which is represented with an offset in $V_{DS}$ at the peak current level of 75 A. P6 with optimized $R_g$ shows a good switching waveform without hurting the $V_{GS}$ specification limit.

3.4 Brownout measurements

In SMPS, there are some applications which are designed shut down under a specified minimum input voltage. This requirement is normally implemented by using the protection function of the controller, so the MOSFET will be protected against input undervoltage (brownout) at low-line. One of the challenging during operation at brownout range is managing the temperature stability of the MOSFET while the power supply is delivering the output power. The combination of high conduction and switching losses due to high operating current gives high power dissipation in the MOSFET resulting to a high temperature rise in the device.
CoolMOS™ P6 offers reduced $Q_g$ and low integrated $R_g$ which enable fast switching. This provides low turn-on and turn-off losses. The switching losses contribution in the total power loss of the MOSFET is reduced in the case of P6 compared to C3 and E6 for the same $R_{DS(on)}$. Temperature rise due to high switching losses of C3 and E6 increases the device $R_{DS(on)}$ value that results to a high conduction loss as well. High total power dissipation results to a high temperature of the device. In the 300 W CCM PFC application test below, CoolMOS™ P6 case temperature shows 10°C lower than that of C3 and E6 at low line input voltage. CP with the lowest $Q_g$ and the fastest switching shows the lowest temperature rise.

![Figure 15](image_url)

600 V C3 vs. P6 vs. E6 vs. CP comparison during brownout test

### 3.5 Hard commutation on conducting body diode

Hard commutation on conducting body diode is required for soft switching applications and a tradeoff is required between high commutation ruggedness of body diode and fast switching. All properties of a fast switching device (high di/dt, low $Q_g$, low $R_g$) results into high voltage peak during hard commutation on a conducting body diode. Figure 16 shows the voltage peaks under hard commutation followed after 10 µs body diode conduction time (in normal operation conditions you will not find longer body diode conduction times than 400 ns).
Figure 15 shows the $V_{DS(max)}$ overshoot due to high $di/dt$ in a commutation. The device under test is same as the switch, both with an $R_{ext}$ of 10 $\Omega$. $V_{DS(max)}$ overshoot will be influenced by the parasitic components of the layout, the external $R_g$ and the switching speed of the switch. P6 has an improved commutation behavior against CP.

Figure 16  Hard commutation on conduction body diode comparison 600 V P6 vs. E6 vs. CP
4 Design Guideline for using 600 V CoolMOS™ P6

In the following sections we will give some guidelines how to use the CoolMOS™ P6 in the best way to enable an optimized performance.

4.1 Minimum external gate resistor ($R_{g,ext}$)

In well designed power supply we recommend to use a very low ohmic external resistor in the range of minimum 5 $\Omega$ for turn-on and zero ohm for turn-off. This efficiency driven $R_g$ selection could be taken due to an implementation of an $R_{g,int}$ and the very robust design of CoolMOS™ P6. However, the selection on external $R_g$ is always a function on the PCB parasitic components which generates an unexpected voltage- or current peak on the MOSFET due to voltage signal from L stray $\times \frac{di}{dt}$ and current signal from C parasitics $\times \frac{du}{dt}$. To prevent such peaks a reduction of the parasitic components or an increased $R_{g,ext}$ for the MOSFET is recommended.

4.2 Paralleling of 600 V P6

For paralleling 600 V P6 we generally recommend the use of ferrite beads on the gate or separated totem poles driving circuit.
5 Portfolio

CoolMOS™ P6 series follows the same naming guidelines as already established with the C6 series e.g. IPP60R190C6, where “I” stands for Infineon Technologies, “P” for power MOSFETs, “P” for the package TO-220, “60” for the voltage class (divided by 10), “R190” for the on-state resistance in Ohms and P6 for the name of the series. Table 3 shows the portfolio of CoolMOS™ P6.

Table 3 600 V CoolMOS™ P6 Series

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<th>TO-247</th>
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<th>ThinPAK 8x8</th>
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6 References

[5] G. Deboy, L. Lin, R. Wu: “CoolMOST C6 Mastering the Art of Slowness”, Application Note revision 1.0 2009-12-21, pp. 5-6
[6] IFX: “CoolMOSTM 900V – New 900V class for Superjunction devices – A new horizon for SMPS and renewable energy applications”, Application Note revision 1.0 2008-02, pp. 6, Figure 1

Revision History

<table>
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Useful Links and Material

- Webpage – 600 V CoolMOS™ P6
  http://www.infineon.com/P6

- Product Brief – 600 V CoolMOS™ P6 - English
  http://www.infineon.com/dgdl/Infineon-Product_Brief_600V_CoolMOS_P6-PB-v02_00-EN.pdf?fileId=db3a30433acf32c9013ad1967d312ad

- Product Brief – 600 V CoolMOS™ P6 - Japanese
  http://www.infineon.com/dgdl/Infineon-ProductBrief_PowerMOSFETs_CoolMOSP6_Japanese-PB-v01_00-JA.pdf?fileId=5546d4624bcaebcf014c0e4045e9467a

- Brochure – Latest Power Management Selection Guide
  http://www.infineon.com/powermanagement-selectionguide

- Evaluationboard: 300W CCM PFC
  http://www.infineon.com/300w-pfc-evaluationboard

- Evaluationboard: 600W LLC 12V Analog
  http://www.infineon.com/600w-llc-evaluationboard-a

- Evaluationboard: 600W LLC 12V Digital
  http://www.infineon.com/600w-llc-evaluationboard-d

- Application Note Introduction to Infineons Simulation Models for Power MOSFETs
  http://www.infineon.com/dgdl/Infineon+-Application+Note+-Introduction+to+Infineons+Simulation+Models+for+Power+MOSFETs.pdf?fileId=db3a30434921d30014496fae9027a02

- Application Note CoolMOS™ - Electrical Safety and Isolation in High Voltage Applications – English
  http://www.infineon.com/dgdl/Infineon+-Application+Note+-PowerMOSFETs+-CoolMOS%E2%84%A2+-Electrical+Safety+and+Isolation+in+High+Voltage+Applications.pdf?fileId=db3a30433d1d0bbe013d20e0cbf017f

- Application Note PFC CCM Boost Converter Design Guide
  http://www.infineon.com/dgdl/Infineon-ApplicationNote_PFCCMBoostConverterDesignGuide-AN-v02_00-EN.pdf?fileId=5546d4624a56ed8014a62c75a923b05

- Application Note CoolMOS™ Primary Side MOSFET Selection for LLC Topology
  http://www.infineon.com/dgdl/Infineon+-Application+Note+-Power+MOSFETs+-CoolMOS+-Primary+Side+MOSFET+Selection+for+LLCTopology.pdf?fileId=5546d46147a9c2e40147d3430e927e5d

- Application Note OptiMOS™ CoolMOS™ Optimal Solutions Suitable for DCDC Converter
  http://www.infineon.com/dgdl/Infineon-ApplicationNote_OptiMOS_CoolMOS_OptimalSolutionsSuitableforDCDCConverter-AN-v01_00-EN.pdf?fileId=5546d4624b0b249c014b3a76f2282d2b