DrBlade™ 2

DrBlade™ 2nd Generation

Selection of Boot Capacitor Value for DrBlade™ 2

TDA21320, TDA21321

Application Note

About this Document

Scope and purpose

With the DrBlade™ 2 Product family, Infineon has introduced a voltage check of the boot capacitor to protect the high-side (HS) switch against an insufficiently low driving voltage. This document provides guidelines for the choice of value for the boot capacitor depending on the operating conditions.

Intended audience

This document is intended for system design engineers using DrBlade™ 2 products.

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1 Introduction

A DrBlade™ 2 power stage integrates power MOSFETs and driver in a common package. It provides a variety of protection features to prevent damage to the device and the load, under almost every foreseeable scenario.

Part of that protection scheme is the surveillance of the voltage across the boot capacitor that drives the HS MOSFET. If this gate to source voltage is too low, the driver stops operating in order to protect the HS MOSFET, regardless of the state of the PWM input signal.

Restrictions on the HS MOSFET turn-on can result in delays in the converters response to load steps. This note discusses the design considerations necessary to ensure a proper transient response in DrBlade™ 2 applications at highly dynamic loads with long tri-state periods leading to charge depletion at the boot capacitor. This charge loss is compensated for by an integrated refresh operation. The choice of the boot capacitor value is an integral part of the design to prevent unwanted $UVLO_{BOOT}$ error states.

In case of an $UVLO_{BOOT}$ error the system controller can initiate shutdown if it discovers a missing phase, phase current mismatch, excessive temperature and/or overcurrent protection (OCP) events on other phases.

To maintain stable driving voltage for the HS MOSFET a larger boot capacitor is generally preferred. When also considering proper cooperation of protection and refresh features in dynamic load applications, as described above, selection of the boot capacitor value requires particular attention.

For other aspects of the DrBlade™ 2 products, refer to the respective datasheets.

2 Feature Description

2.1 Undervoltage Lockout for Boot Voltage ($UVLO_{BOOT}$) Protection Feature

This feature stops driver operation when the voltage across the boot capacitor is below a critical threshold. This prevents driving the HS MOSFET with an insufficiently low voltage.

Figure 1 depicts the application circuit of a DrBlade™ 2 device, showing the pin names for reference.

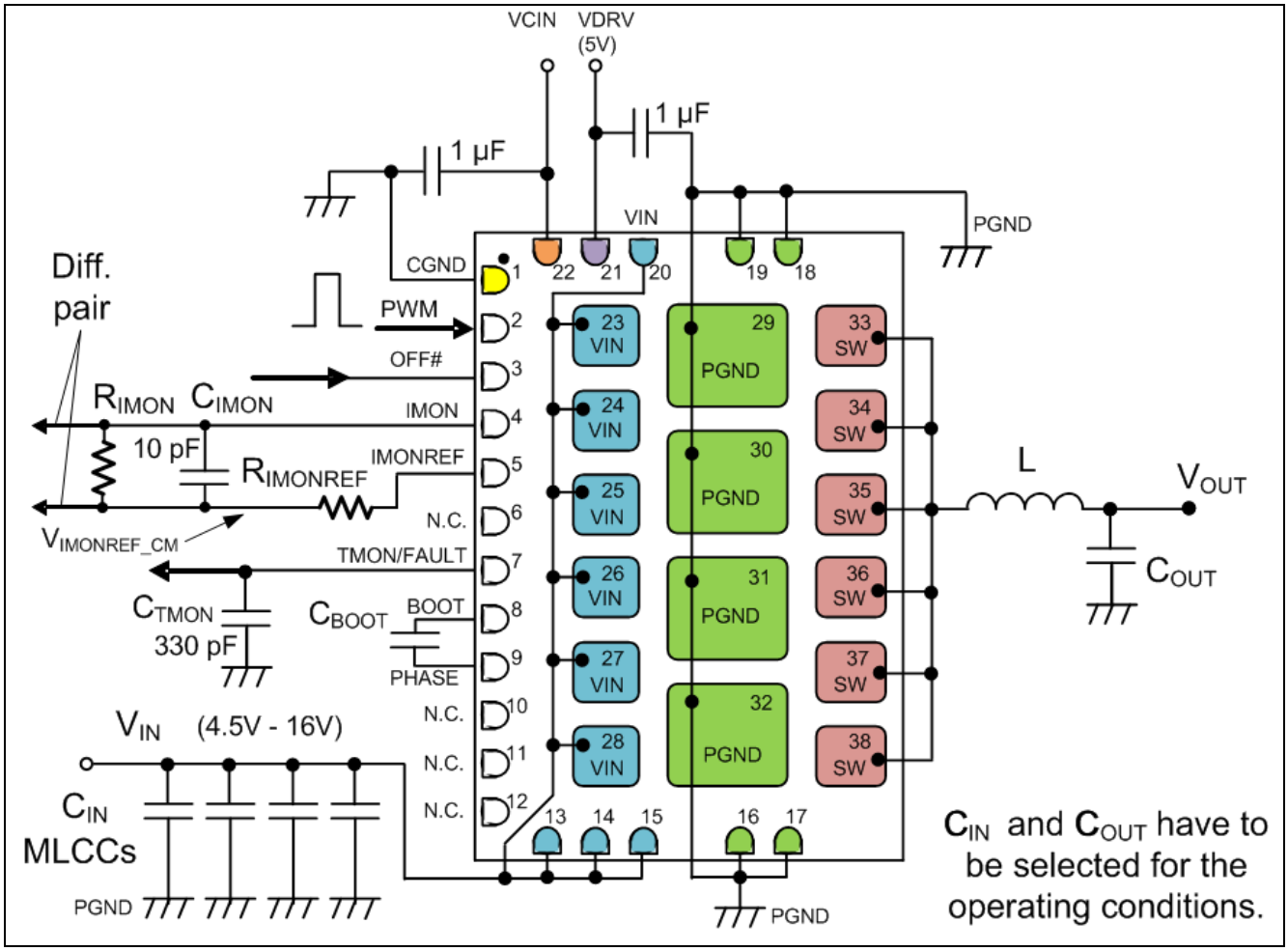

Figure 1 Basic Application Circuit as Example of Implementation

The voltage between the BOOT and SW pins is monitored after V_{CIN} and V_{DRV} have cleared their respective UVLO conditions. The SW pin is replicated as PHASE pin to connect C_{BOOT}. At startup, the low-side MOSFET (LS MOSFET) gate drive (driver output GL) is enabled to respond to the PWM signal when V_{DRV} is active. If the voltage across the boot capacitor is still below the $V_{UVLOboot\_R}$ threshold, the active LS MOSFET forces charge into the boot capacitor during the PWM 'L' state. Otherwise, when the boot capacitor voltage exceeds the rising threshold of the undervoltage lockout value of the boot voltage ($V_{UVLOboot\_R}$), the HS MOSFET gate drive (driver output GH) is enabled. This is shown at time t_1 in Figure 2.

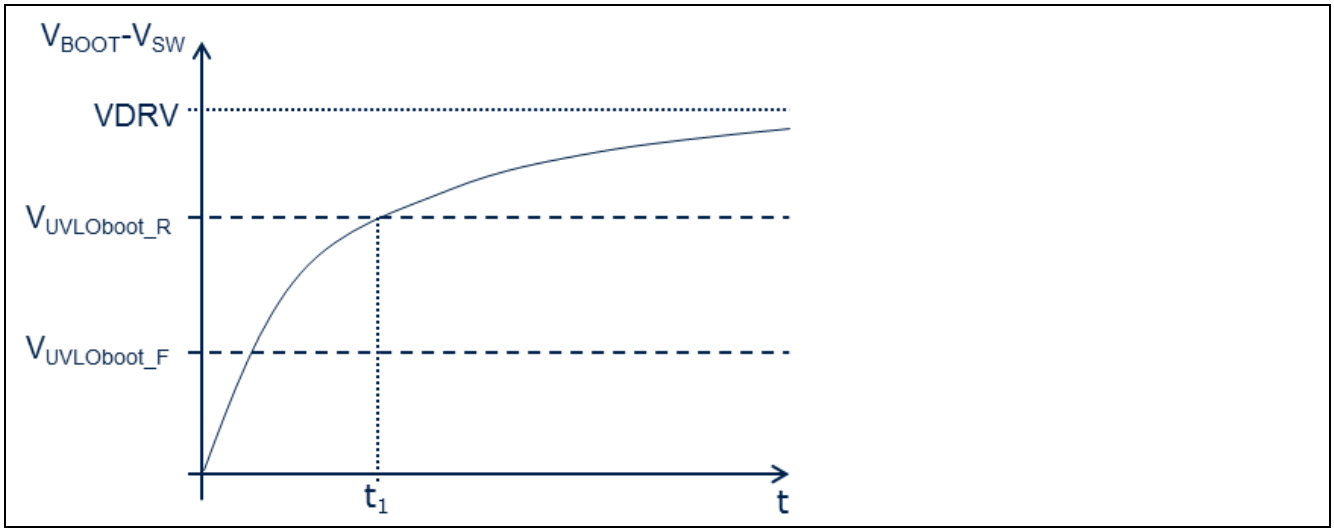

Figure 2 UVLO$_{BOOT}$ at Startup (GH is Enabled at t_1)

At startup and at any time when the boot voltage falls below the falling threshold of the undervoltage lockout value of the boot voltage ($V_{UVLOboot\_F}$) an internal boot-error flag is set. The boot-error flag is reset when the boot voltage exceeds the rising threshold of the undervoltage lockout value ($V_{UVLOboot\_R}$).

If, during the falling edge of the PWM signal (from 'H' to tri-state or from 'H' to 'L'), the UVLO$_{BOOT}$ error flag is set, an internal UVLO$_{BOOT}$ counter is incremented by one. This counter is reset to zero if, during a falling edge of PWM, the UVLO$_{BOOT}$ error flag is not set, and the counter value is less than three.

When the counter value reaches three, the driver outputs GH and GL remain disabled, and the power stage output is kept in tri-state, regardless of the PWM input.

To reset the driver and resume operation, the PWM input has to be held continuously in tri-state for 19 µs (typically). When this happens, the UVLO$_{BOOT}$ counter resets to zero and the driver performs the startup sequence described above in order to sufficiently charge the boot capacitor.

The driver will also be reset when VCIN and/or VDRV will be re-cycled.

2.2 Boot Refresh Circuit

When the converter operates in continuous conduction mode (CCM), switching never stops. This ensures that the boot capacitor is properly recharged during each cycle. Other modes of operation – for example, discontinuous conduction mode (DCM), or a disengaged phase in dynamic phase-shedding operation in multiphase buck converters – can lead to extended periods of tri-state operation during which both MOSFETs are kept in the off-state.

To prevent depletion of the boot capacitor during an extended period in tri-state, a boot refresh circuit is used. Lost charge is replenished from a constant current source connected to the VIN terminal of the device. To ensure full current capability of the current source the voltage difference (V_{IN} - V_{SW}) should be more than 4.8 V.

The boot refresh circuit is activated only after continuous tri-state has been established for at least 19 µs (typically), and the voltage across the boot capacitor has fallen below $V_{UVLOboot\_F}$. The circuit remains active until the voltage across the boot capacitor has reached $V_{UVLOboot\_R}$, or until the PWM input signal leaves the tri-state region.

3 Circuit Interactions

3.1 Scenario Showing Lacking Transient Support

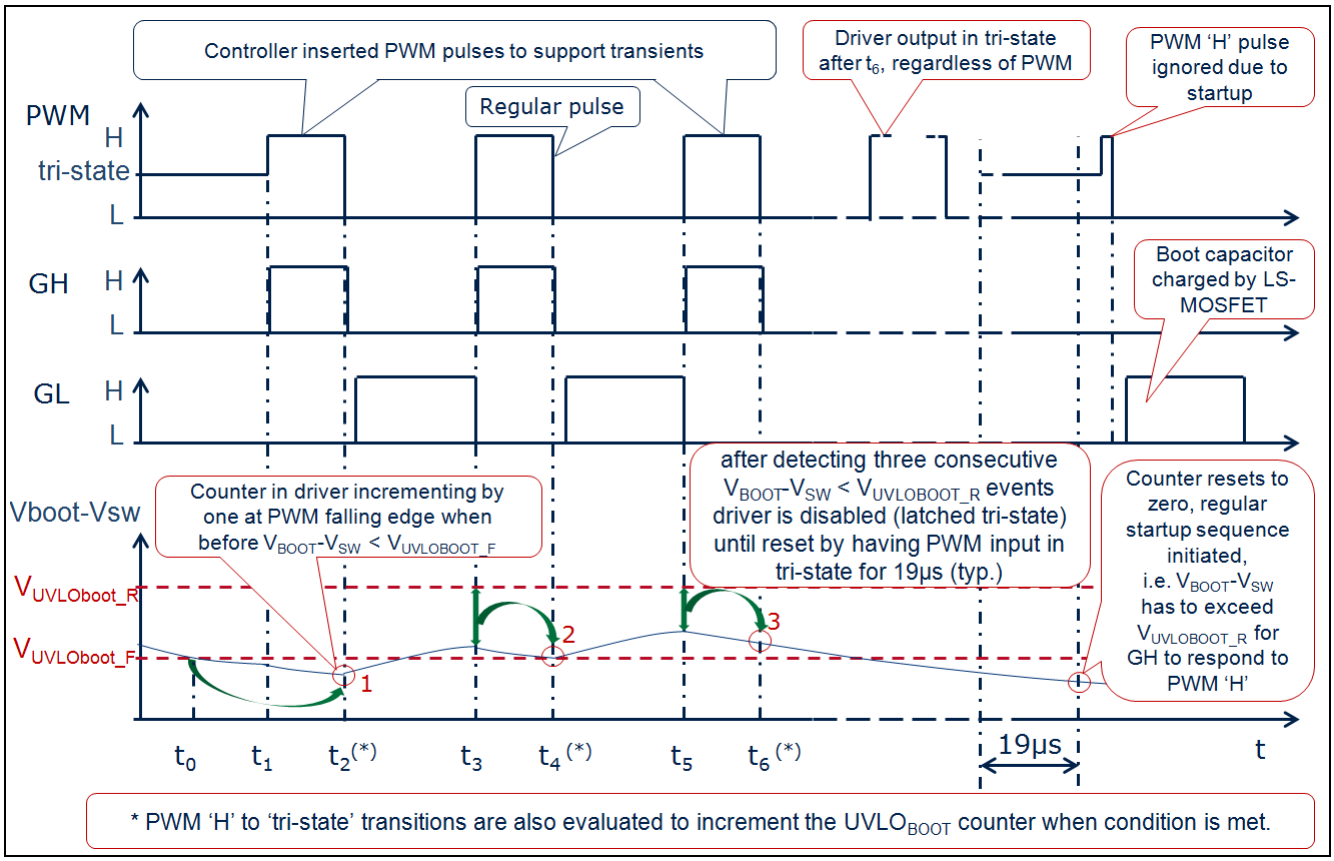

Figure 3 Transient Event Causes Trigger of $UVLO_{BOOT}$

Figure 3 shows an event that could trigger the $UVLO_{BOOT}$ protection circuit. Up to t_1, PWM is in the tri-state condition (e.g. disabled phase or end of DCM cycle). At t_0 the voltage across the boot capacitor falls below the lower detection threshold $V_{UVLOBOOT\_F}$. At t_1, a sudden load increase triggers the PWM to go 'H'. The refresh circuit does not engage. The HS MOSFET gate is driven from a voltage close to $V_{UVLOBOOT\_F}$. The gate charge for the HS MOSFET is taken from the boot capacitor. At the falling edge of the PWM (t_2), the gate voltage is below $V_{UVLOBOOT\_F}$ and the internal $UVLO_{BOOT}$ error flag is set. The $UVLO_{BOOT}$ counter value changes from '0' to '1'. The LS MOSFET now turns on and charge is added to the boot capacitor.

However, in a transient event as shown here, the first PWM 'H' pulse can be the result of the transient support feature, and can be closely followed by a regular pulse. Therefore, the LS MOSFET can be on for a short time only before the second pulse at t_3 turns the HS MOSFET on again. Here, charge is also taken from the boot capacitor. At t_4 (the falling edge of the second PWM 'H' pulse), the voltage across the boot capacitor is still well below $V_{UVLOBOOT\_R}$. The error flag remains set and the counter value changes from '1' to '2'. Subsequently, the LS MOSFET turns on again and charge is added to the boot capacitor. With the transient support feature still active, the third PWM 'H' pulse appears at t_5. The time between the PWM 'H' pulses is too short for the boot capacitor voltage to rise above $V_{UVLOBOOT\_R}$. At t_6 (the falling edge of the third PWM 'H' pulse), the error flag is still set and the counter value change from '2' to '3'. At this point, the driver disengages the gate drive of both MOSFETs and the output enters tri-state.

Circuit Interactions

To resume normal operation, a reset has to be done. This happens when the PWM input is in tri-state for long enough to activate the internal low power mode. After 19 µs (typically) the counter resets to zero and a regular startup sequence is initiated in which the boot capacitor voltage has to exceed $V_{UVLOBOOT\_R}$. This happens quickly when the LS MOSFET is turned on for regular periods. Only then will the HS MOSFET gate drive respond to PWM 'H' states and the $UVLO_{BOOT}$ protection feature is activated.

3.2 Prevention of Unwanted $UVLO_{BOOT}$ Events

3.2.1 Effect of $UVLO_{BOOT}$ Refresh Circuit

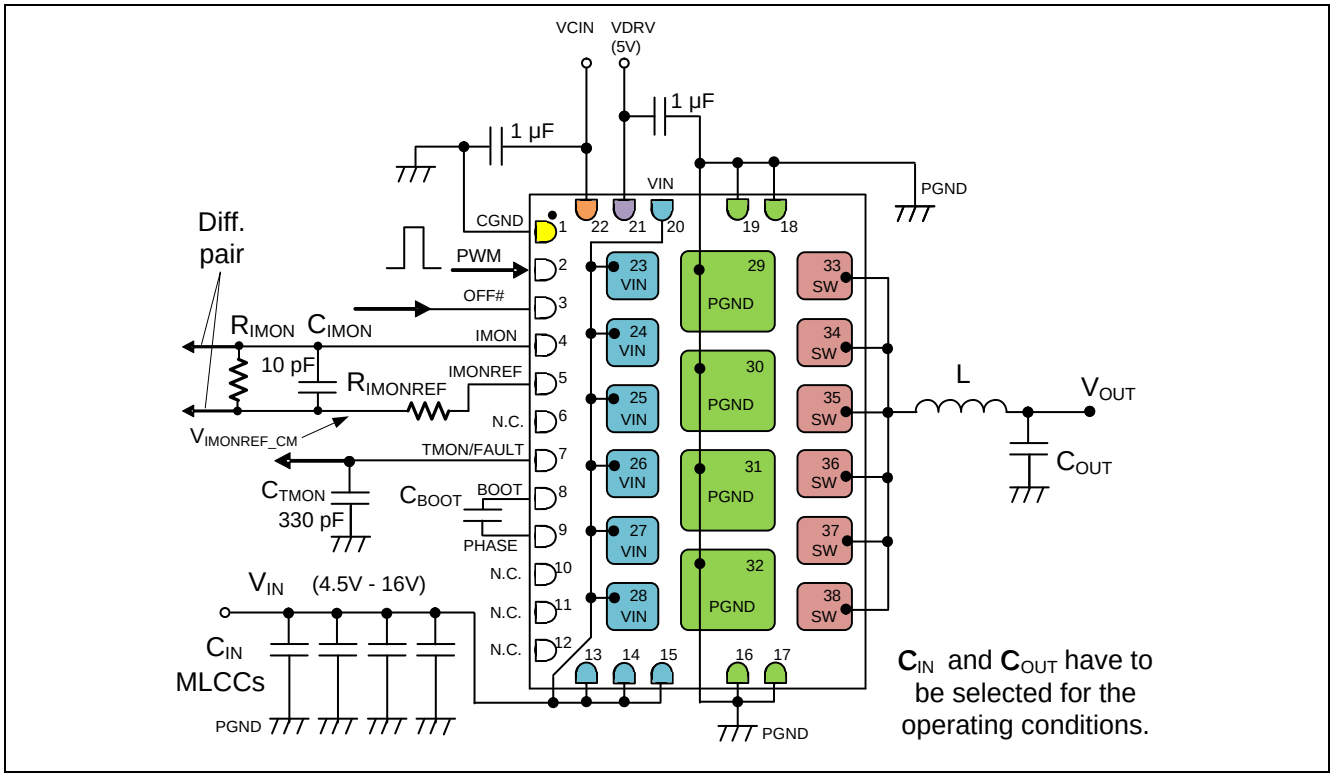

Figure 4 Basic Circuit Schematic (as Provided in Datasheet)

The refresh circuit typically provides 200 µA when driven with a voltage difference (V_{IN} - V_{SW}) of at least 4.8 V. The voltage difference between $V_{UVLOboot\_R}$ and $V_{UVLOboot\_F}$ is of not more than 480 mV.

Using these assumptions, the correlation between refresh time and boot capacitor value can be defined as:

$$\Delta Q_{BOOT} = C_{BOOT} \cdot \Delta V_{BOOT} \quad [1]$$

$$\Delta t_{BOOT} = C_{BOOT} \cdot \frac{\Delta V_{BOOT}}{I_{BOOT}} \quad [2]$$

$$\Delta t_{BOOT} = 2400V/A \cdot C_{BOOT} \quad [3]$$

Given a boot capacitor of 1 µF, the boot refresh circuit remains active for 2.4 ms, unless a PWM pulse causes the device to react. A boot capacitor of 100 nF still requires 240 µs to fully refresh to $V_{UVLOboot\_R}$.

Circuit Interactions

Therefore, the refresh circuit is only used to trickle charge the boot capacitor during extended tri-state periods. It does not play a role in the quick recharge of the boot capacitor to prevent an $UVLO_{BOOT}$ error.

3.2.2 Recharge During LS MOSFET On-Time

The boot capacitor C_{BOOT} is charged by V_{DRV} during the LS MOSFET on-time, via an integrated boot switch. V_{CBOOT} is the voltage across the boot capacitor.

$$V_{CBOOT}(t) = V_{DRV} \cdot (1 - e^{\frac{-t}{\tau}}) \quad [4]$$

$$\tau = C_{BOOT} \cdot R_{BOOT} \quad [5]$$

Since the boot switch consists of a MOSFET in parallel to its body diode, R_{BOOT} depends on the voltage across itself.

$$\tau = C_{BOOT} \cdot R_{BOOT}(V_{RBOOT}) \quad [6]$$

with

$$V_{RBOOT} = V_{DRV} - V_{CBOOT} \quad [7]$$

$$V_{CBOOT}(t) = V_{DRV} \cdot (1 - e^{\frac{-t}{C_{BOOT} \cdot R_{BOOT}(V_{CBOOT})}}) \quad [8]$$

This is an implicit equation and therefore not useful for obtaining the required LS MOSFET on-time.

A graphical approach is taken instead.

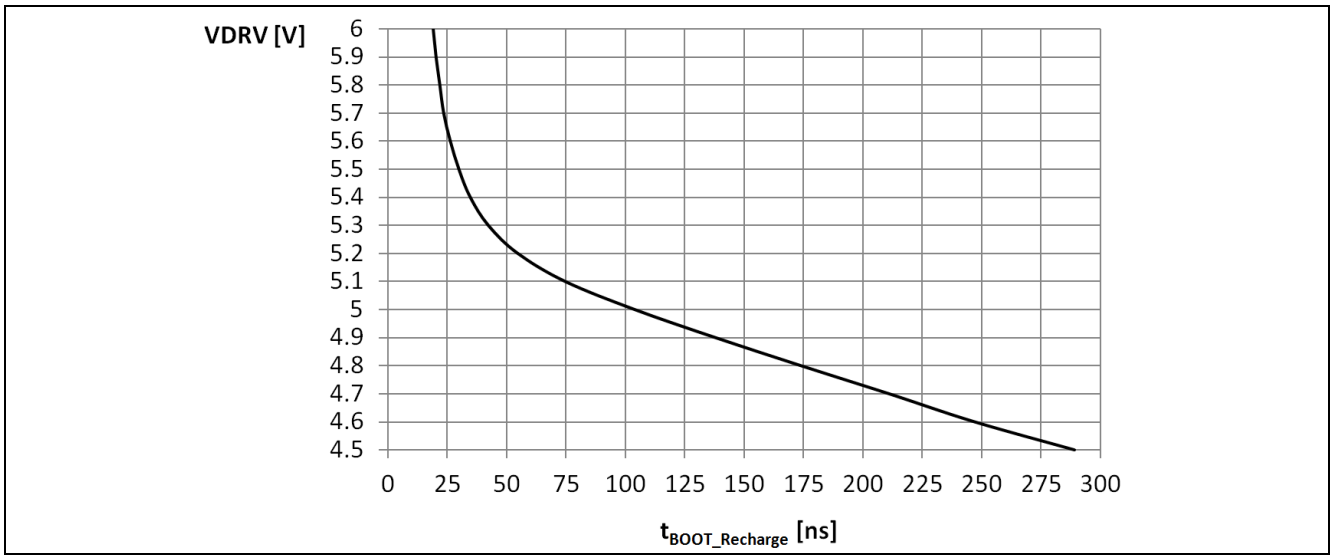

Figure 5 Typical Recharge Time with 47 nF Boot Capacitor as Function of Driving Voltage

Circuit Interactions

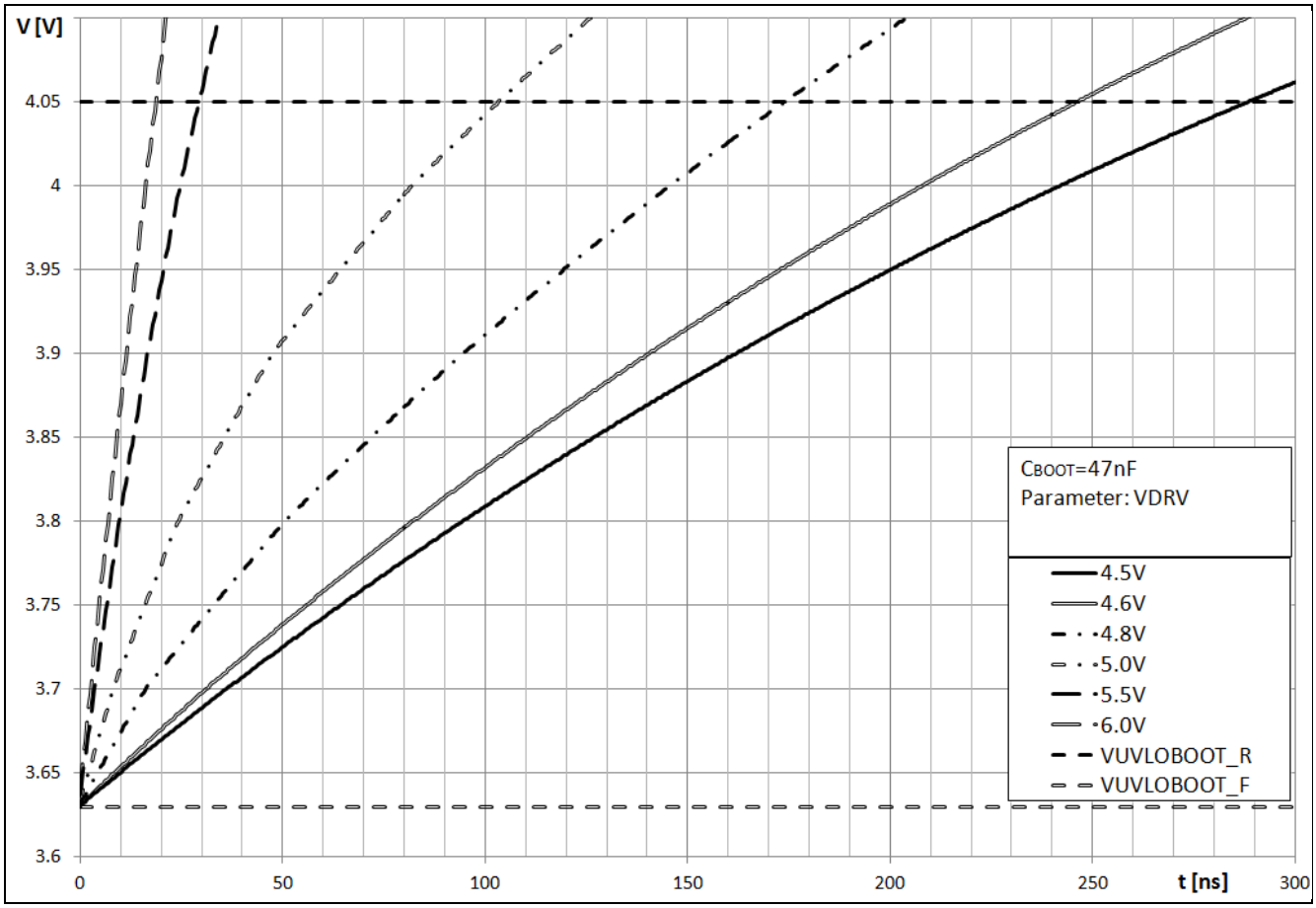

Figure 6 Typical Recharge Time Characteristic for a 47 nF Boot Capacitor

Different boot capacitor values scale the recharge time linearly.

$$t_{Boot\_Recharge} = t_{Boot\_Figure3} \cdot (C_{BOOT}/47nF) \quad [9]$$

The actual on-time of the LS MOSFET depends on the switching frequency, the maximum duty cycle setting and the setting of additional transient support pulses.

$$t_{off} = t_{on\_LS} = \left(1 - \left(D_{max} + D_{transient\_support}\right)\right)/f_{sw} \quad [10]$$

The application has to ensure that the actual on-time of the LS MOSFET (t_{on_LS}) is at least as long as the time required to recharge the boot capacitor to $V_{UVLOBOOT\_R}$.

$$t_{on\_LS} \geq t_{Boot\_Recharge} \quad [11]$$

As previously described in the $UVLO_{BOOT}$ circuit description, when the error conditions for the boot voltage apply, the third falling edge of the PWM signal triggers the fault.

For further considerations the following assumptions are made:

- high thresholds for the undervoltage lockout ($V_{UVLOBOOT\_F}$ = 3.7 V, $V_{UVLOBOOT\_R}$ = 4.2 V)
- V_{CBOOT} falls to $V_{UVLOBOOT\_F}$ when the HS MOSFET is turned on at t = 0
- nominal value for C_{BOOT}
- maximum gate charge for the HS MOSFET

Circuit Interactions

Turning on the HS MOSFET just before the boot capacitor voltage reaches $V_{UVLOBOOT\_R}$ is the worst case scenario for prolonging the $UVLO_{BOOT}$ condition.

Lastly, the charge taken from the boot capacitor during each HS MOSFET turn-on event before the 3rd pulse has to be considered:

$$Q_{HS\_total} = 2 \cdot Q_{G\_HS} \quad [12]$$

Additional charging time is required to compensate for the gate charge required.

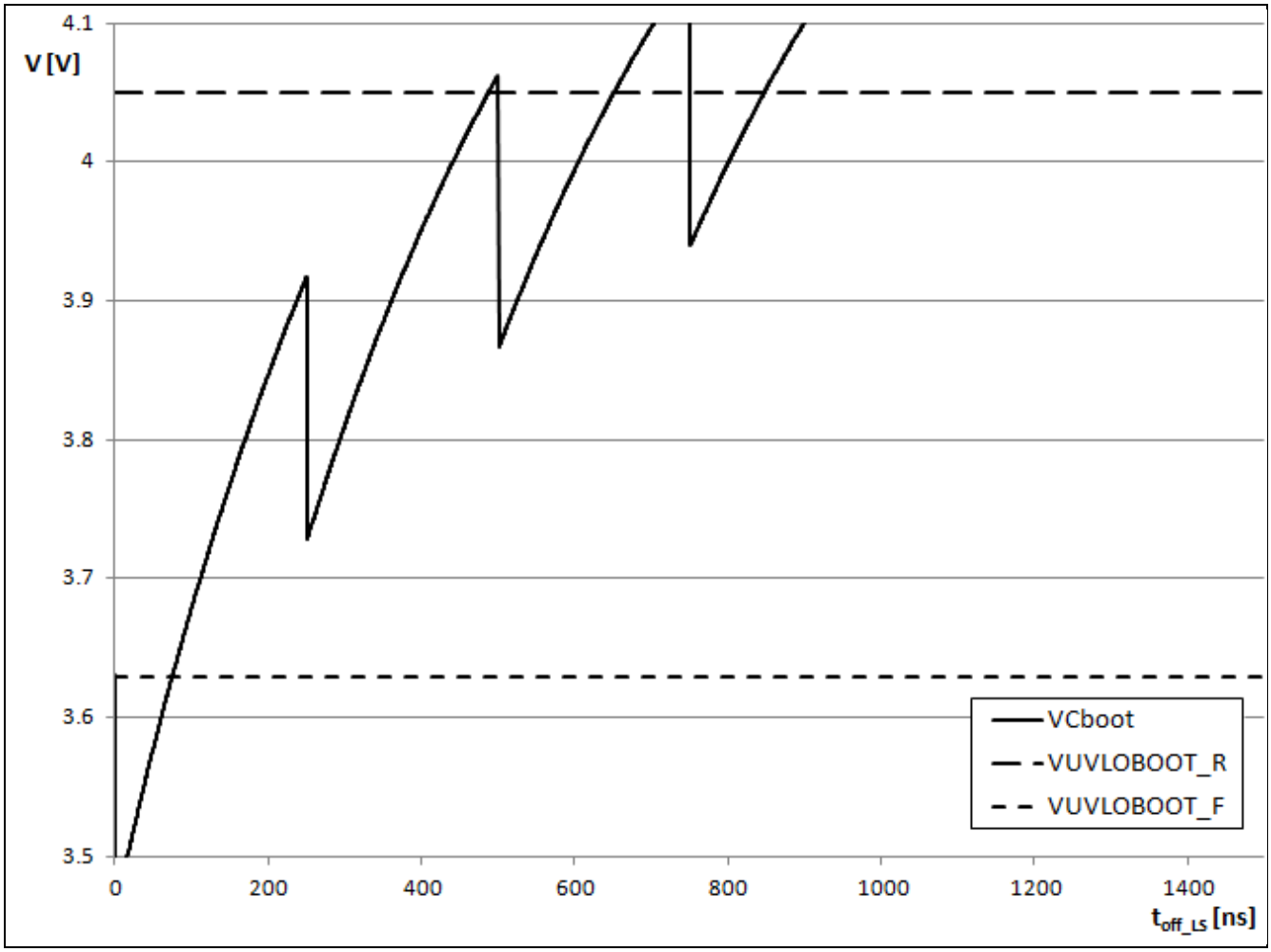

Figure 7 Typical Charging Curve of a 47 nF Boot Capacitor on TDA21320 at V_{DRV} = 4.5 V as a Function of Accumulated LS MOSFET On-Time

Figure 7 shows an example of aworst case event during the charging process of a 47 nF boot capacitor. At t = 0 charge is taken from the boot capacitor to turn-on the HS MOSFET. $V_{UVLOBOOT\_R}$ is exceeded before the third falling edge of the PWM signal. The event does not cause an $UVLO_{BOOT}$ error. A specific case of this scenario is a switching frequency of 500 kHz at s maximum regular duty cycle of 50 %, and one additional transient support pulse with a 25% duty cycle with respect to the switching period.

4 Boot Capacitor Selection Guide

Figure 8 to Figure 22 show the maximum duty cycle permitted against switching frequency depending on the choice of the boot capacitor for a given minimum gate drive voltage V_{DRVmin} (supplying the boot capacitor). These diagrams assume the highest gate charge for the respective device and the nominal value of the respective boot capacitor.

If the controller can introduce one additional pulse per switching cycle to support the transition, the switching frequency has to be read from '$f_{sw\_transient\_support}$'. If the controller simply enhances the duty cycle to support a transient, the switching frequency has to be read from '$f_{sw\_no\_added\_pulses}$'. This interprets the count of switching events in case of an $UVLO_{BOOT}$ error condition.

'D_{total}' is the maximum duty cycle per switching cycle resulting from the sum of the regular pulse (D_{max}) and any additional pulses ($D_{transient\_support}$) that may be introduced to support the transient.

The maximum boot capacitor value under consideration is 470 nF. When including tolerance, DC voltage bias and temperature dependency, the smallest recommended nominal value for C_{BOOT} is 47 nF.

The following figures assume 16 V rated boot capacitors with +/- 10 % accuracy. If the operating point is above the line of a specified capacitor, a lower value has to be selected.

4.1 Boot Capacitor Selection Guide for TDA21320

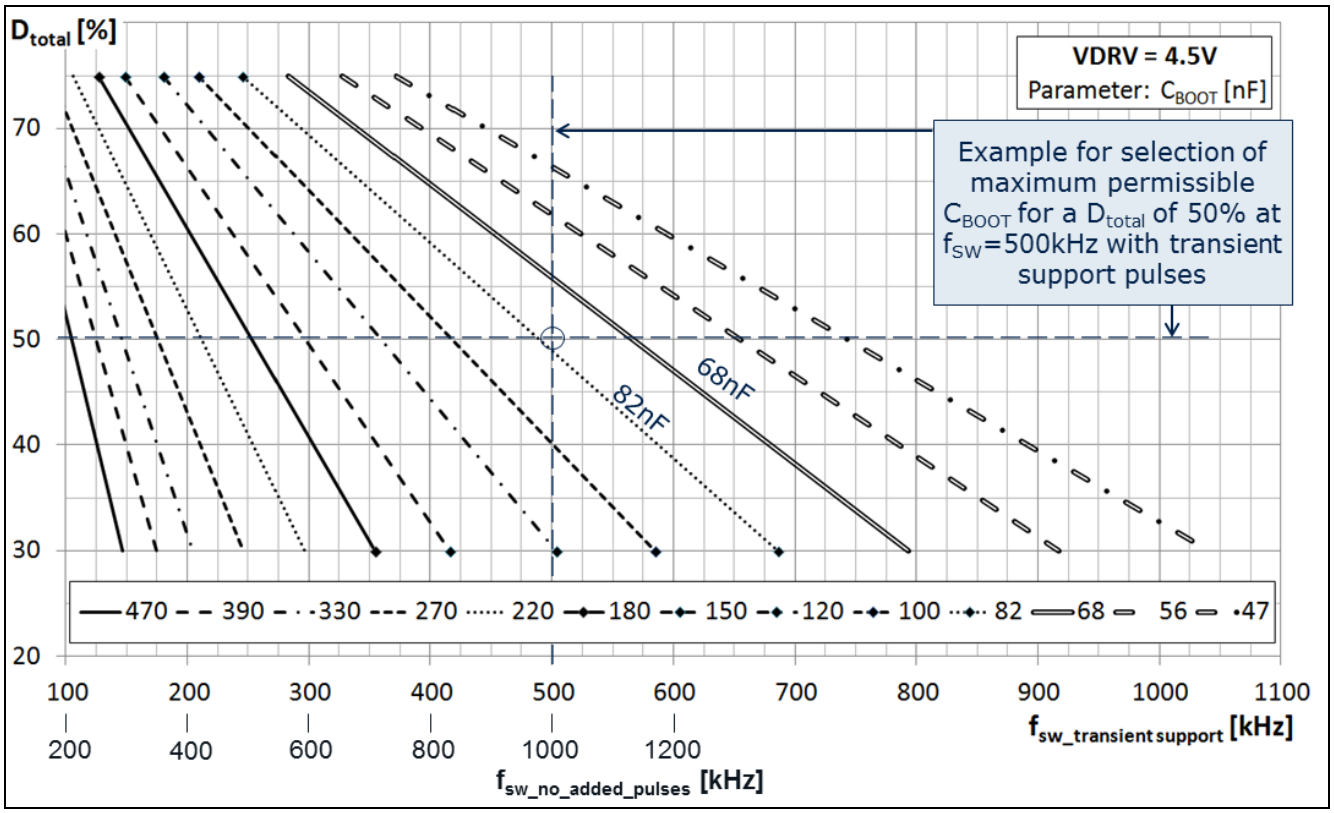

Figure 8 Maximum C_{BOOT} for V_{DRVmin} = 4.5 V, Note: $D_{total} = D_{max} + D_{transient\_support}$

In this example the 68 nF capacitor has to be chosen because the intersection is above the 82 nF line.

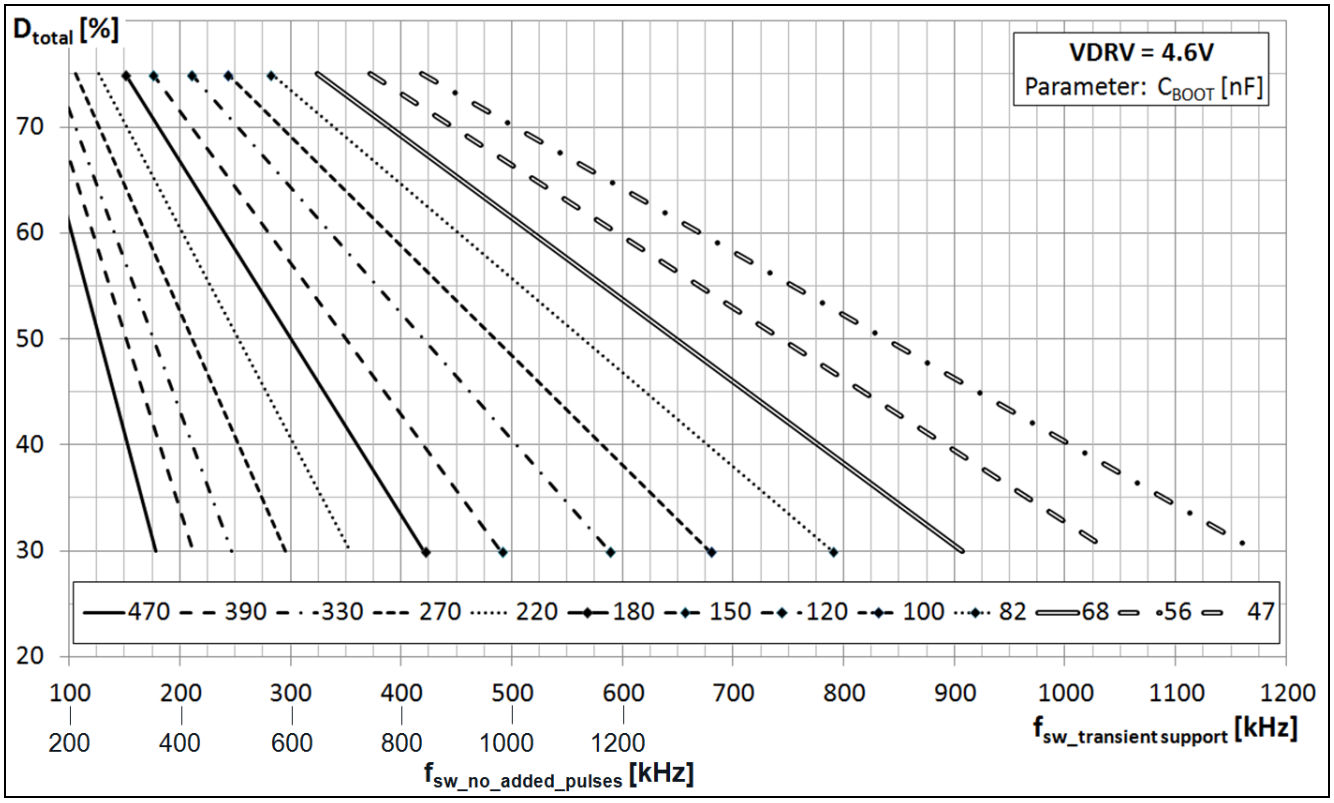

Figure 9 Maximum C_{BOOT} for V_{DRVmin} = 4.6 V, Note: $D_{total} = D_{max} + D_{transient\_support}$

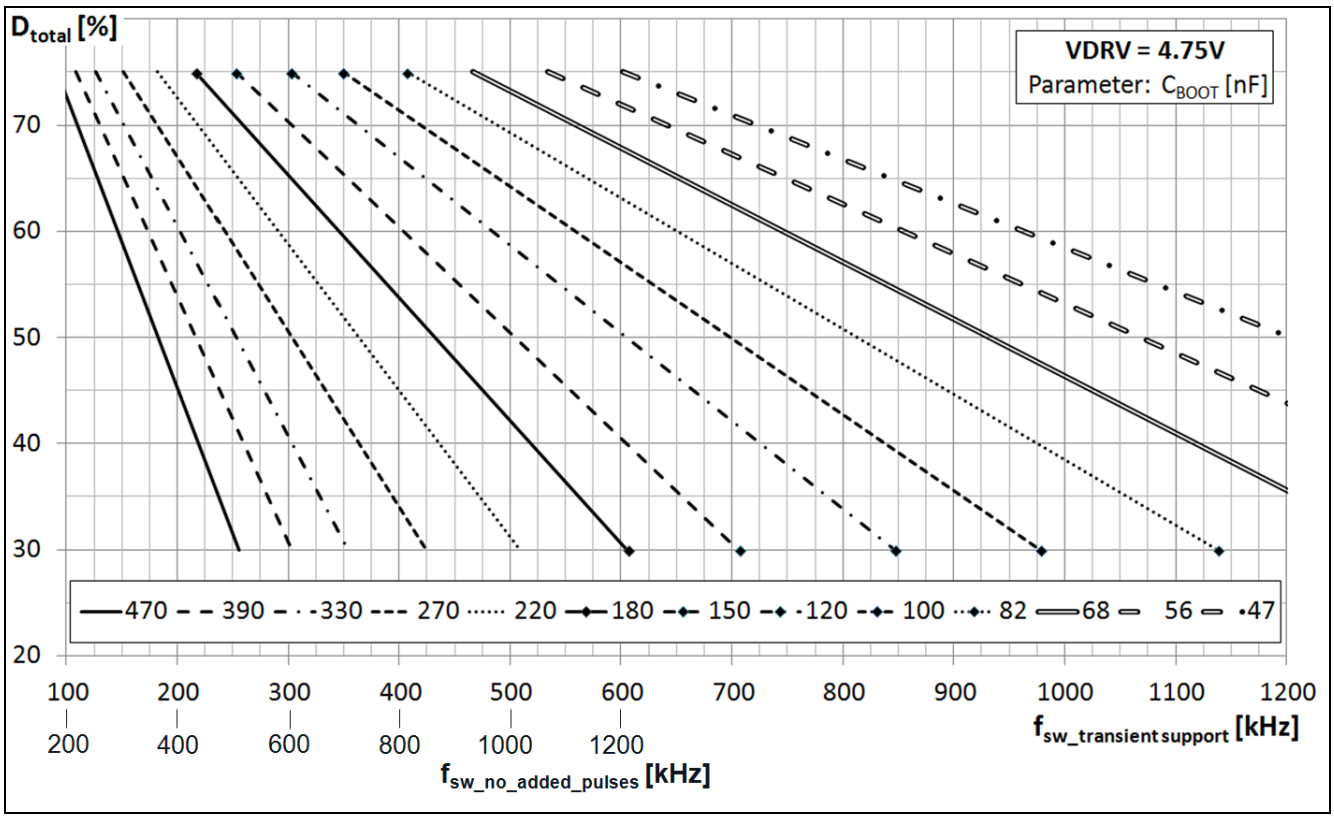

Figure 10 Maximum C_{BOOT} for V_{DRVmin} = 4.75 V, Note: $D_{total} = D_{max} + D_{transient\_support}$

Boot Capacitor Selection Guide

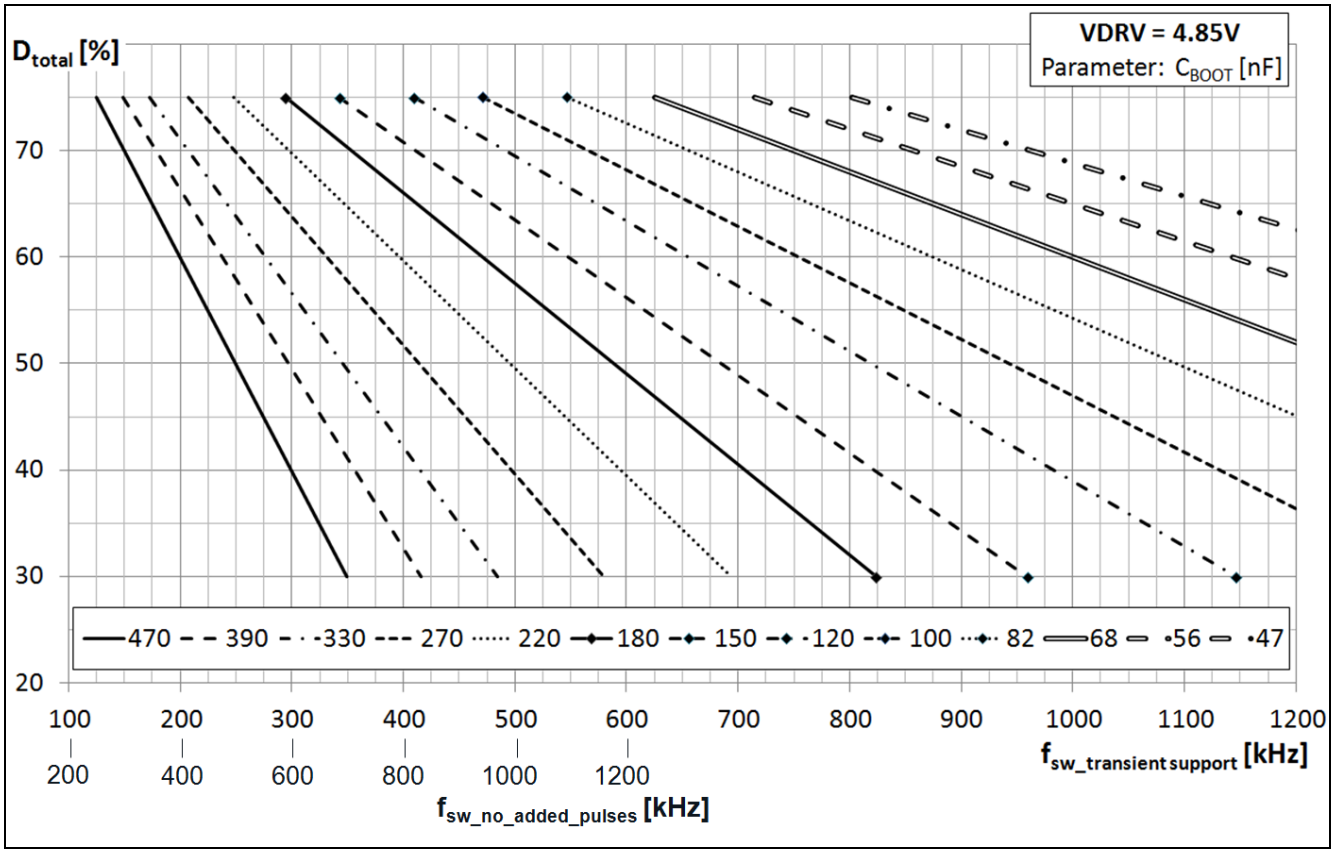

Figure 11 Maximum C_{BOOT} for V_{DRVmin} = 4.85 V, Note: $D_{total} = D_{max} + D_{transient\_support}$

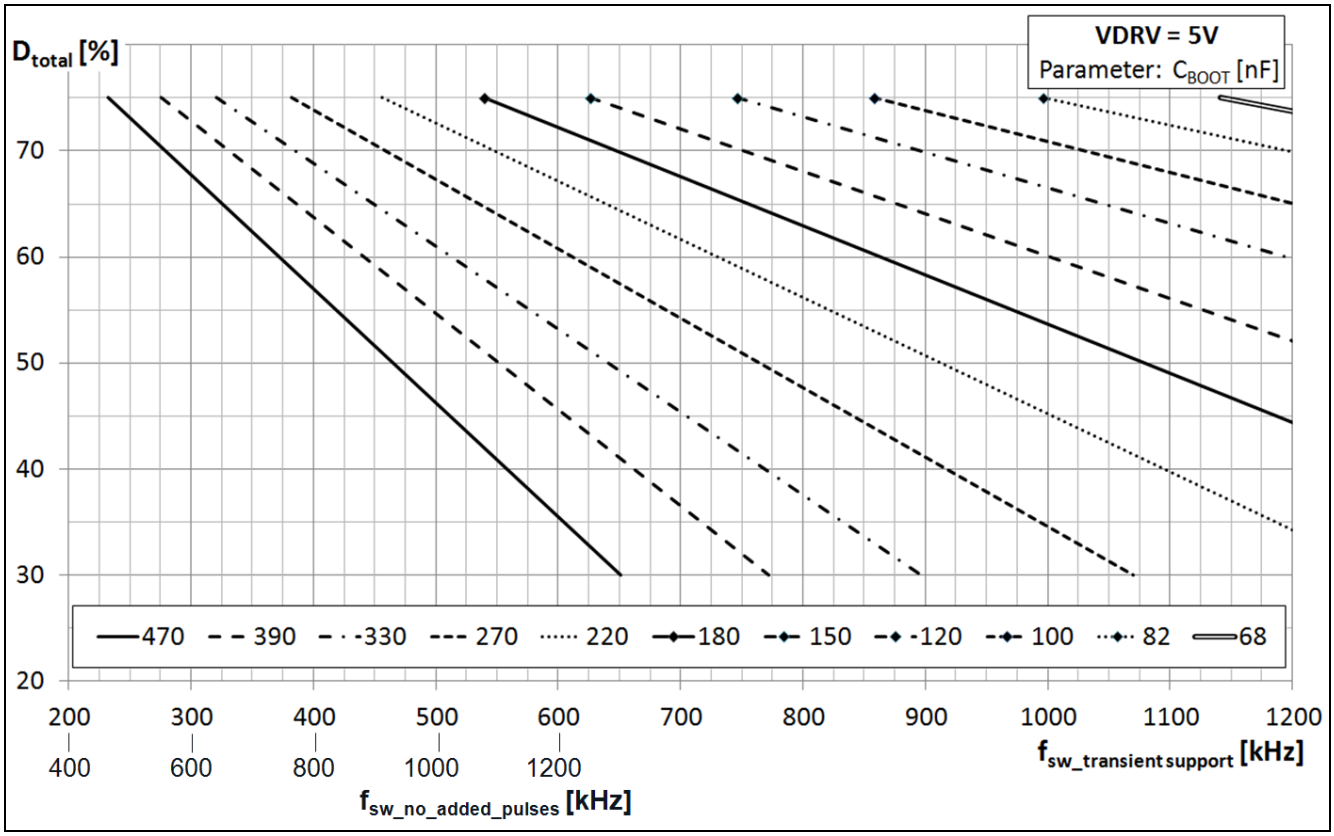

Figure 12 Maximum C_{BOOT} for V_{DRVmin} = 5 V, Note: $D_{total} = D_{max} + D_{transient\_support}$

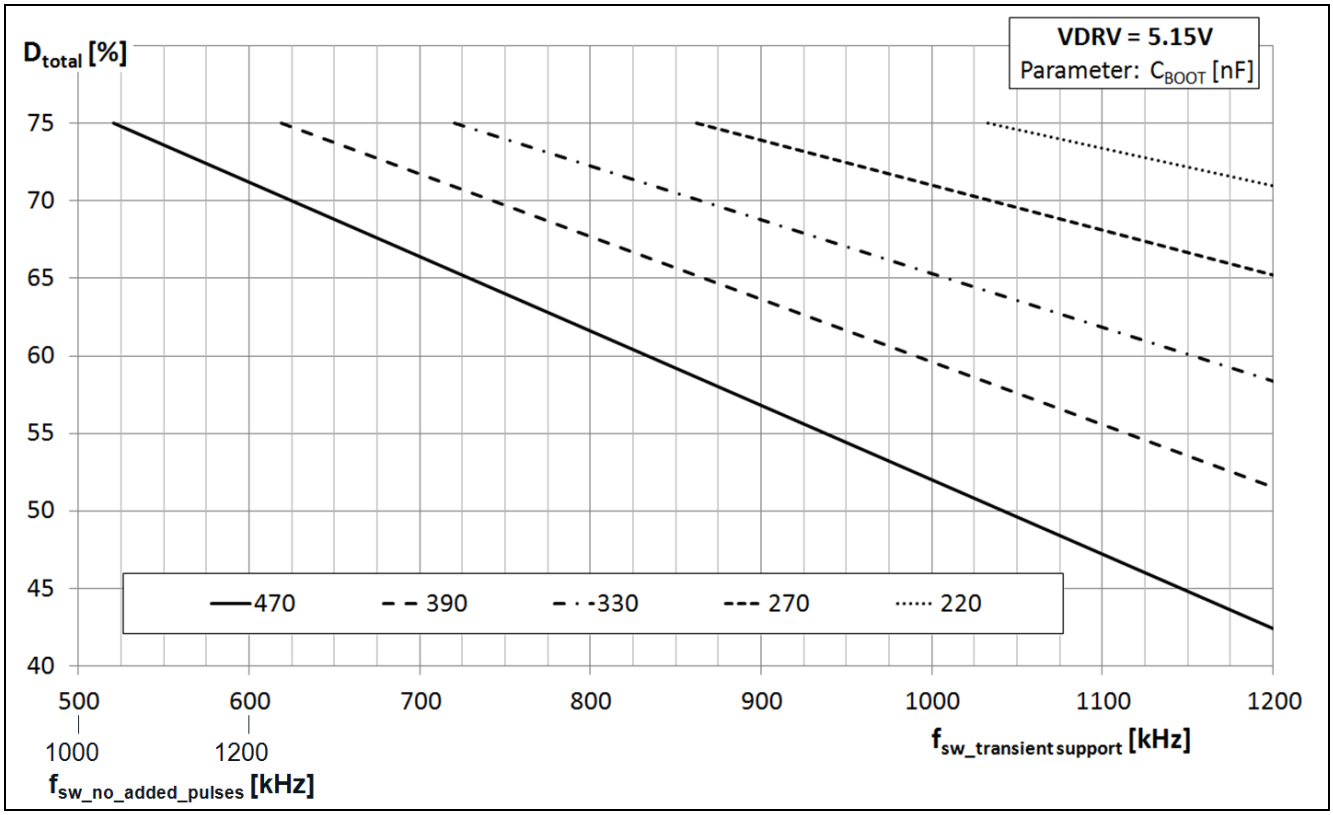

Figure 13 Maximum C_{BOOT} for V_{DRVmin} = 5.15 V, Note: $D_{total} = D_{max} + D_{transient\_support}$

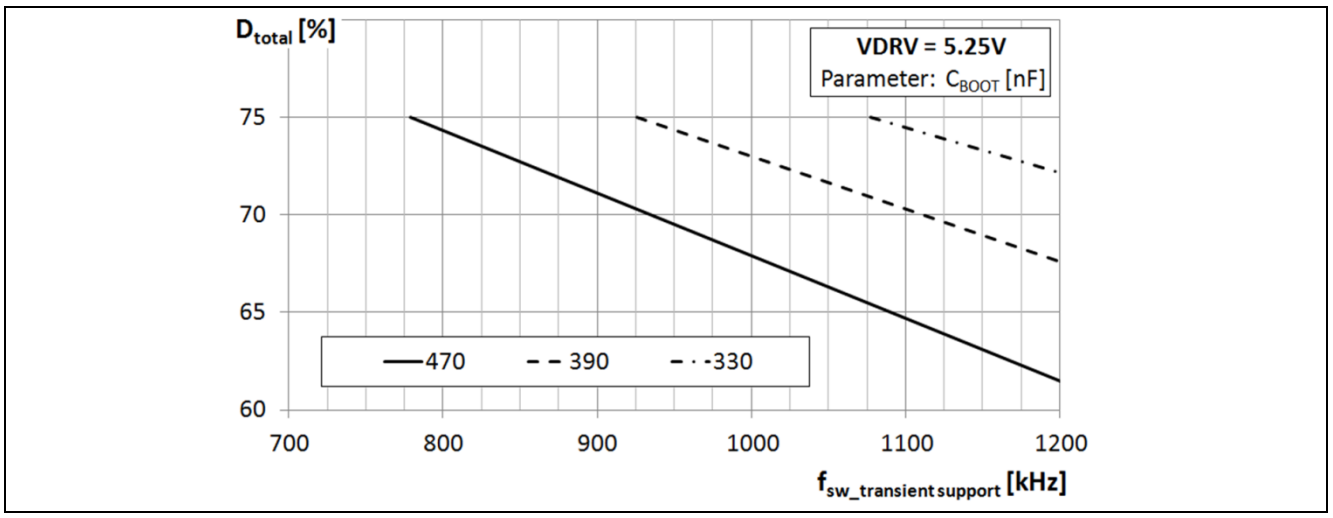

Figure 14 Maximum C_{BOOT} for V_{DRVmin} = 5.25 V, Note: $D_{total} = D_{max} + D_{transient\_support}$

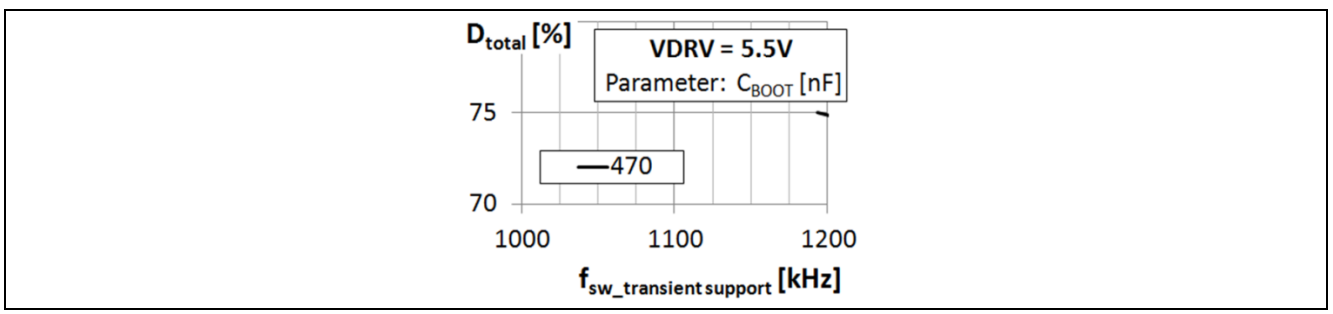

Figure 15 Maximum C_{BOOT} for V_{DRVmin} = 5.5 V, Note: $D_{total} = D_{max} + D_{transient\_support}$

For TDA21320, a boot capacitor of 470 nF can be used at D_{total} = 75 % and $f_{sw\_transient\_support}$ = 1200 kHz, when V_{DRVmin} = 5.51 V.

4.2 Boot Capacitor Selection Guide for TDA21321

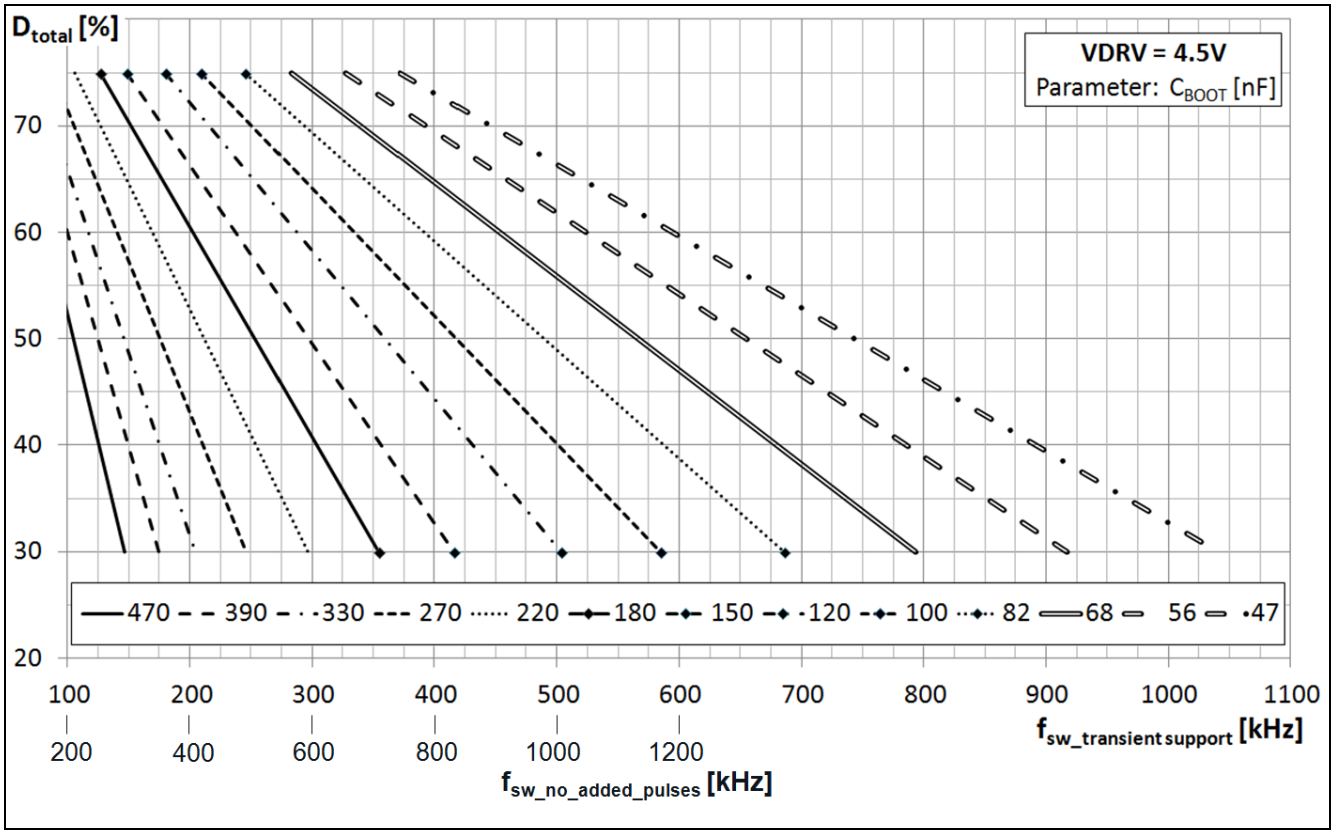

Figure 16 Maximum C_{BOOT} for V_{DRVmin} = 4.5 V, Note: $D_{total} = D_{max} + D_{transient\_support}$

Boot Capacitor Selection Guide

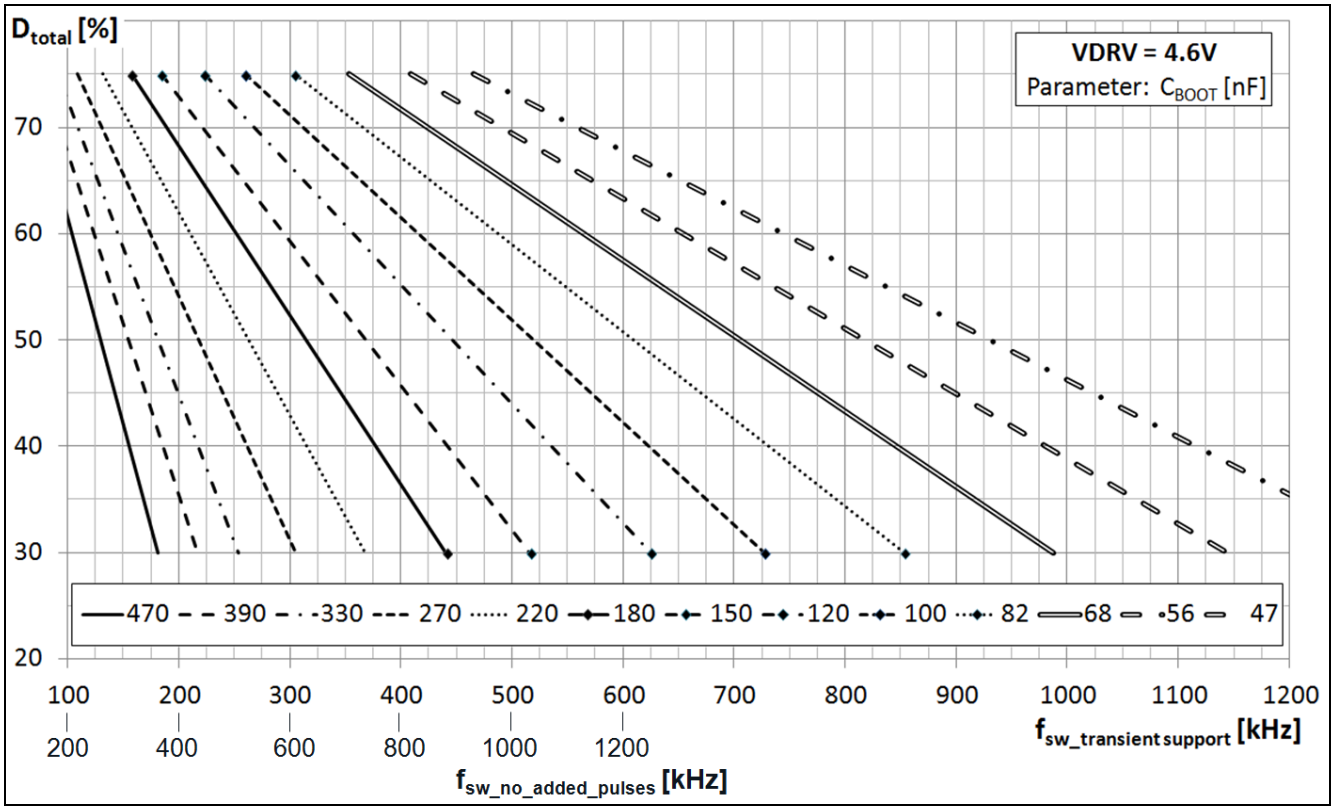

Figure 17 Maximum C_{BOOT} for V_{DRVmin} = 4.6 V, Note: $D_{total} = D_{max} + D_{transient\_support}$

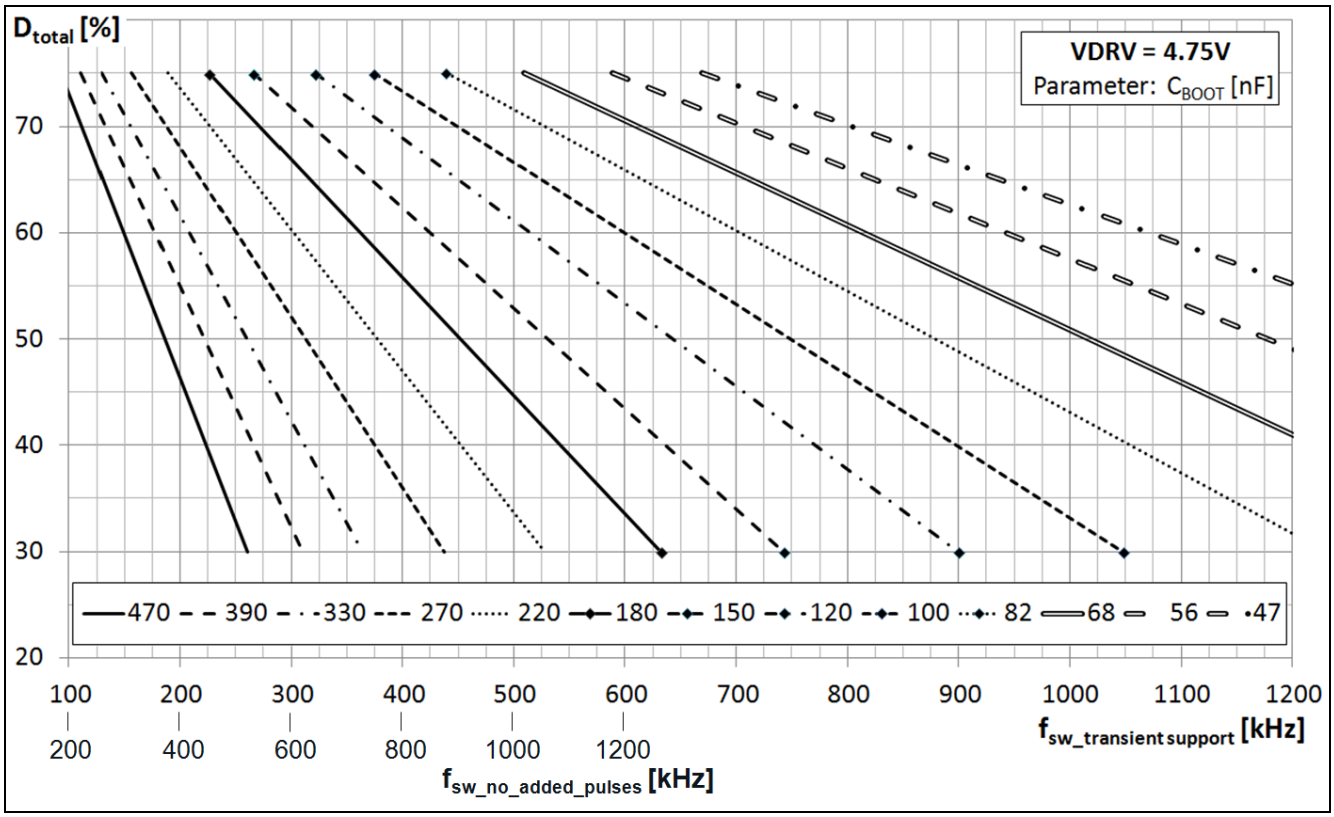

Figure 18 Maximum C_{BOOT} for V_{DRVmin} = 4.75 V, Note: $D_{total} = D_{max} + D_{transient\_support}$

Boot Capacitor Selection Guide

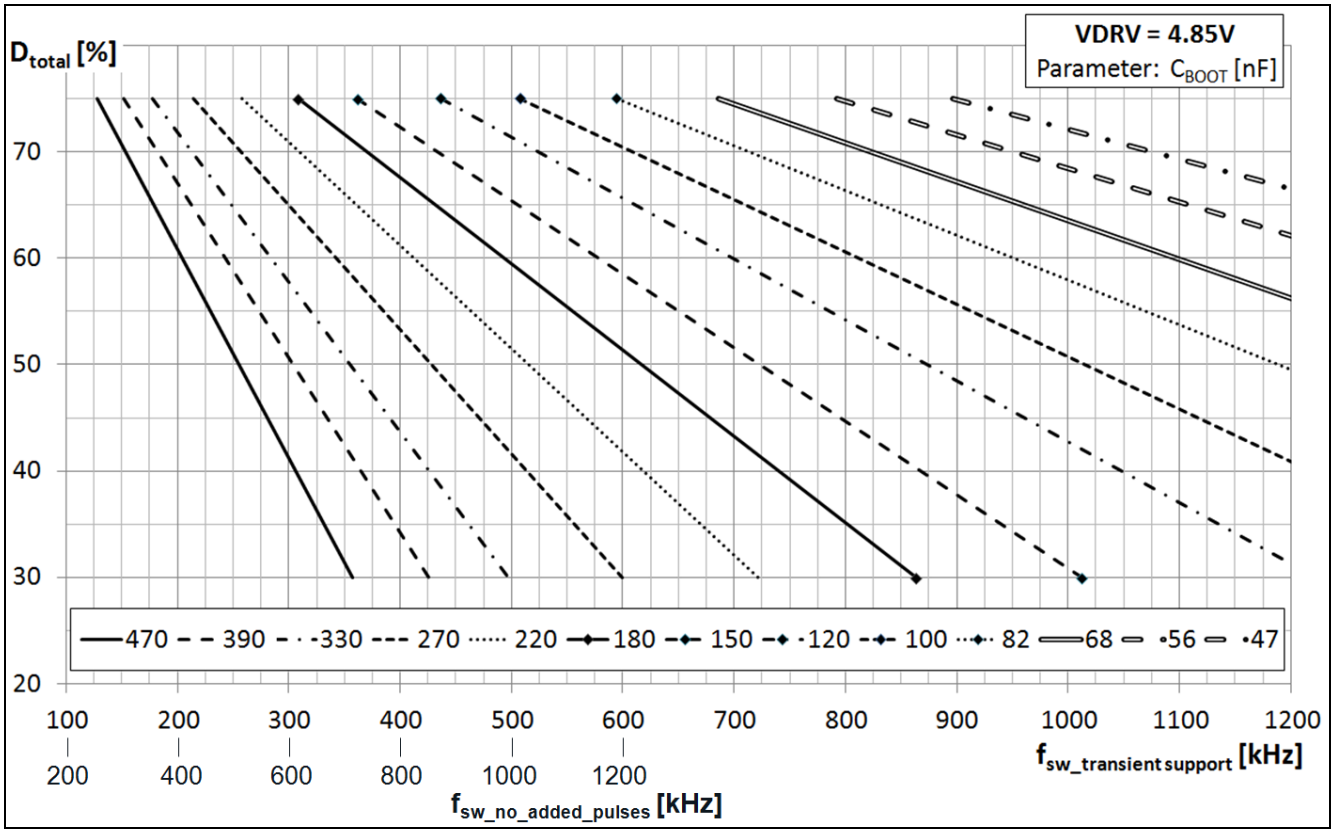

Figure 19 Maximum C_{BOOT} for V_{DRVmin} = 4.85 V, Note: $D_{total} = D_{max} + D_{transient\_support}$

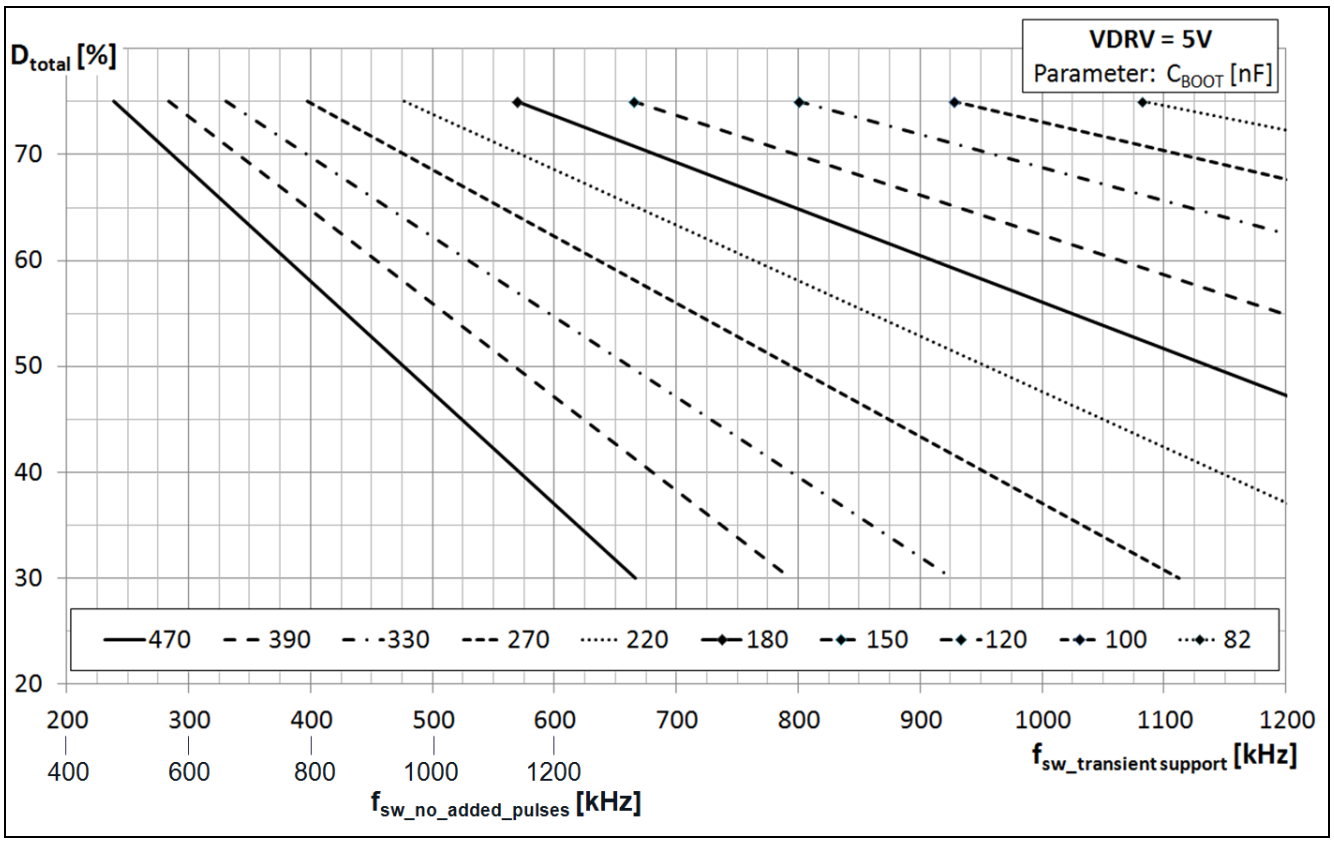

Figure 20 Maximum C_{BOOT} for V_{DRVmin} = 5 V, Note: $D_{total} = D_{max} + D_{transient\_support}$

Boot Capacitor Selection Guide

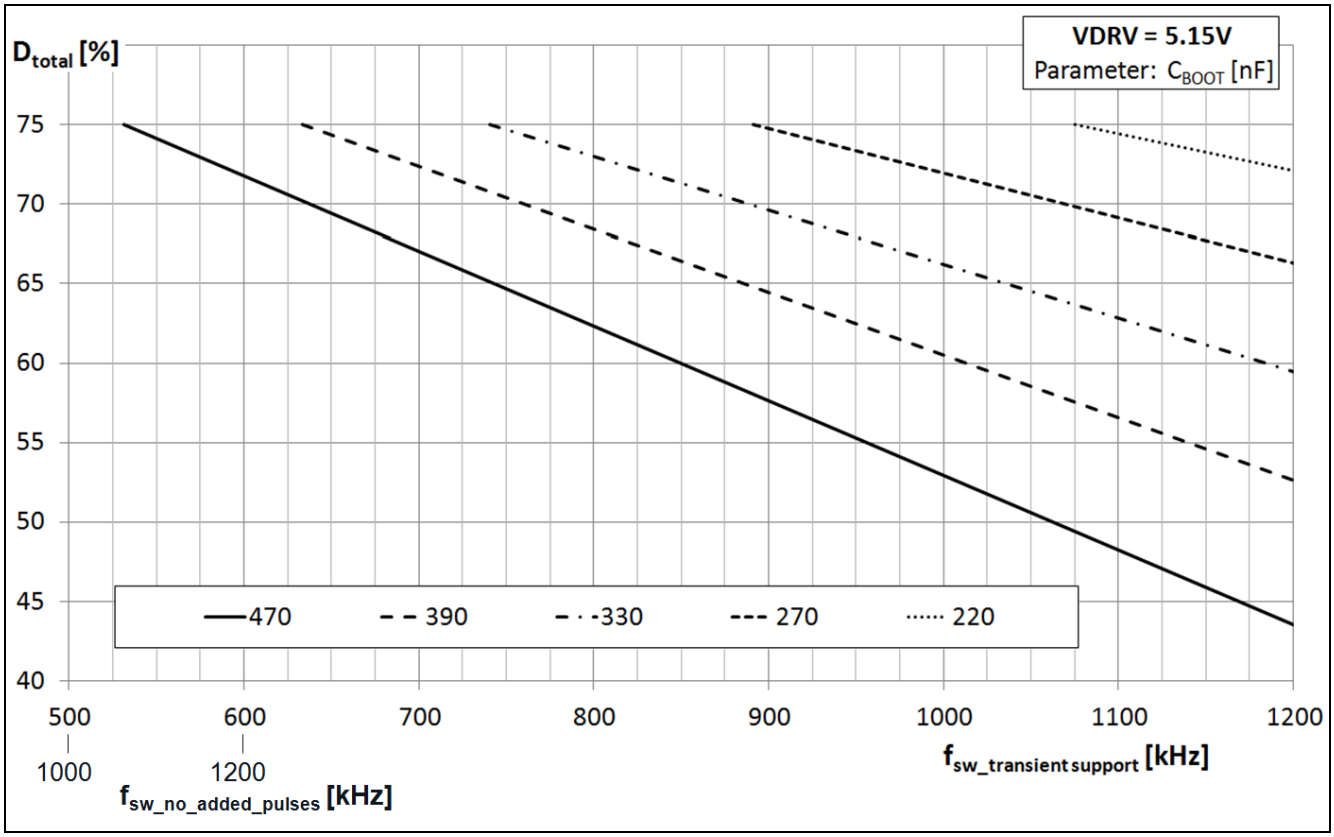

Figure 21 Maximum C_{BOOT} for V_{DRVmin} = 5.15 V, Note: $D_{total} = D_{max} + D_{transient\_support}$

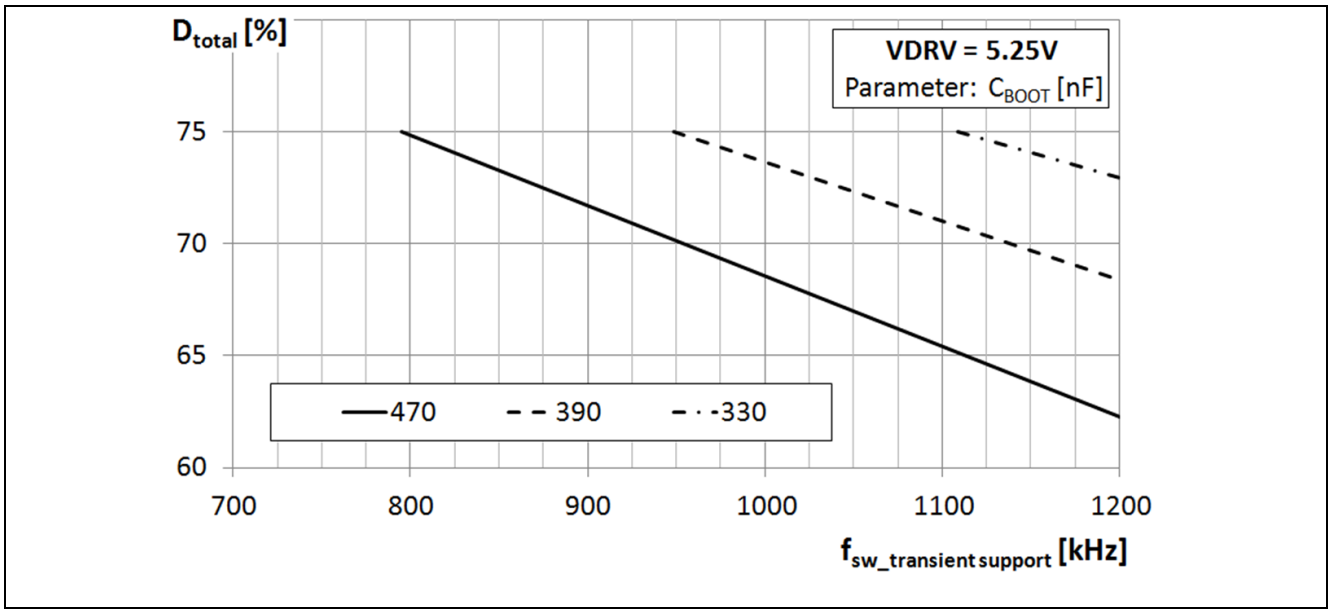

Figure 22 Maximum C_{BOOT} for V_{DRVmin} = 5.25 V, Note: $D_{total} = D_{max} + D_{transient\_support}$

For TDA21321, a boot capacitor of 470 nF can be used at D_{total} = 75 % and $f_{sw\_transient\_support}$ = 1200 kHz, when V_{DRVmin} = 5.49 V.

5 Conclusion

Viable boot capacitor values range from 47 nF to 470 nF, dependent on circuit conditions. To reliably support load transients, the value of the boot capacitor may not exceed the value obtained from the diagrams provided in this document. It is important to ensure that the operating mode during transients is fully understood, as this affects the countable events for the $UVLO_{BOOT}$ error output.

Primarion™ digital DC/DC controllers can support steep transients since they feature a variety of transient support functions. When using these functions, make sure that you understand the implications of the selection of the boot capacitor, and how this depends on pulse count and the total duty cycle at a given switching frequency and driver supply voltage.

Additional information can be found here:

- DrBlade™ 2 power stage and Digital VR Controller
- More Info: http://www.infineon.com/cms/en/product/promopages/DCDC-System-Solution/
- Power Management Selection Guide: http://www.infineon.com/powermanagement-selectionguide
- Where to Buy: www.infineon.com/wheretobuy
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Revision History

Major changes since the last revision

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