TLE9845QX P/N Application Note

Motor Drive with P/N-channel Power MOSFET Half Bridge Application

About this document

Scope and purpose

This application note describes the MOSFET drive functionalities of the TLE984xQX device family using the example of a half bridge application with one P-channel and one N-channel MOSFET. It further explains the special Drain-Source protection of the TLE9845QX, including configuration of the differential measurement unit. Code examples are added at the end of each chapter.

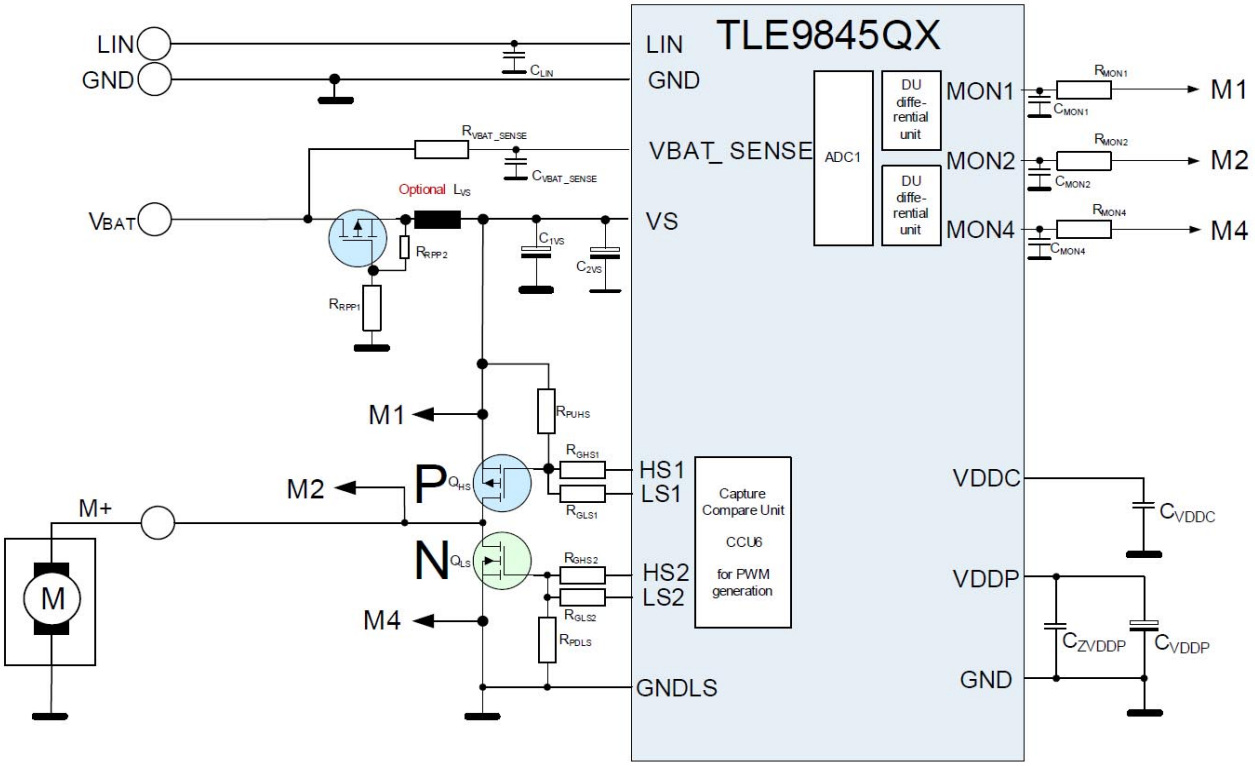

Figure 1 PN-MOSFET Application Diagram

Note: The Code examples, given in this document, have to be verified in the application.
It is recommended to use TLE9845QX_EVB_Rev1.4 or newer to evaluate given code examples.

Intended audience

This template is intended for Customer and FAE to explain MOSFET drive functionalities and functional safety features of the TLE9845QX device.

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1 MOSFET drive Introduction

This Chapter describes the device modules used for single MOSFET drive applications with TLE984xQX embedded Power ICs. The simplified application diagramm shown in Figure 1 is used as a reference in this chapter.

The integrated Highside and Lowside Switches are used as an inverter-stage, to drive an external connected P- or N-channel MOSFET. The needed PWM-Signals can be generated with the CCU6.

1.1 Capture Compare Unit 6 (CCU6)

The CCU6 is a high-resolution 16-bit capture and compare unit with application specific modes. For MOSFET-drive it is recommended to use the Timer T12 block.

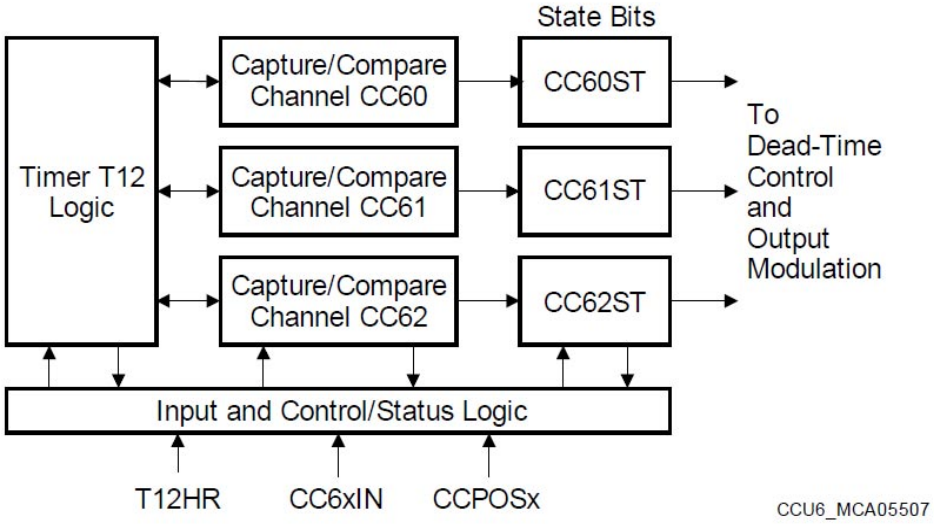

Figure 2 Overview Diagram of Timer12

The basic operating modes of T12 are, either Edge-Aligned mode or Center-Aligned mode. Edge-Aligned mode will be used for the example in Chapter 1.4.

Associated with Timer T12 are three individual capture/compare channels, that can perform compare or capture operations.

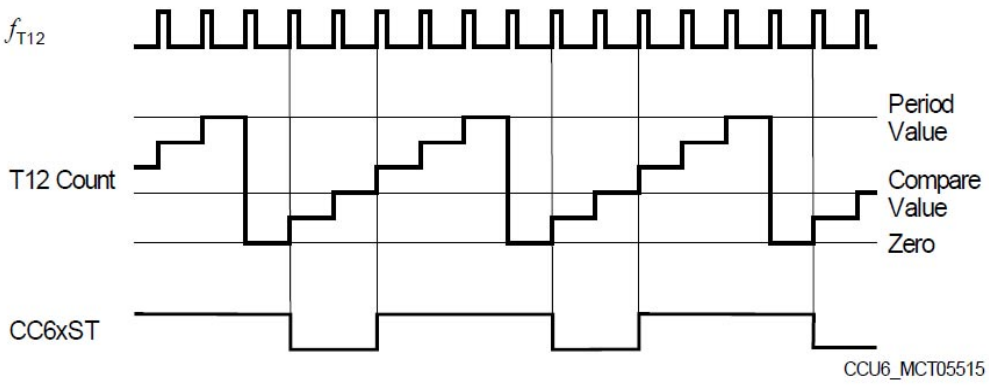

Figure 3 Compare Operation, Edge-Aligned mode

Figure 3 illustrates an example of a compare operation waveform. In this example, the compare values are changed while the timer is running. The changes are performed via a software preload of the Shadow Register,

CC6xSR. The value is transferred to the actual Compare Register CC6xR with the T12 Shadow Transfer signal, T12_ST, that is assumed to be enabled.

The generation of (complementary) signals for the Highside and the Lowside switches of one inverter-stage is based on the same compare channel. For example, if the High Side switch should be active while the T12 counter value is above the compare value (State Bit = 1), then the low-side switch should be active while the counter value is below the compare value (State Bit = 0).

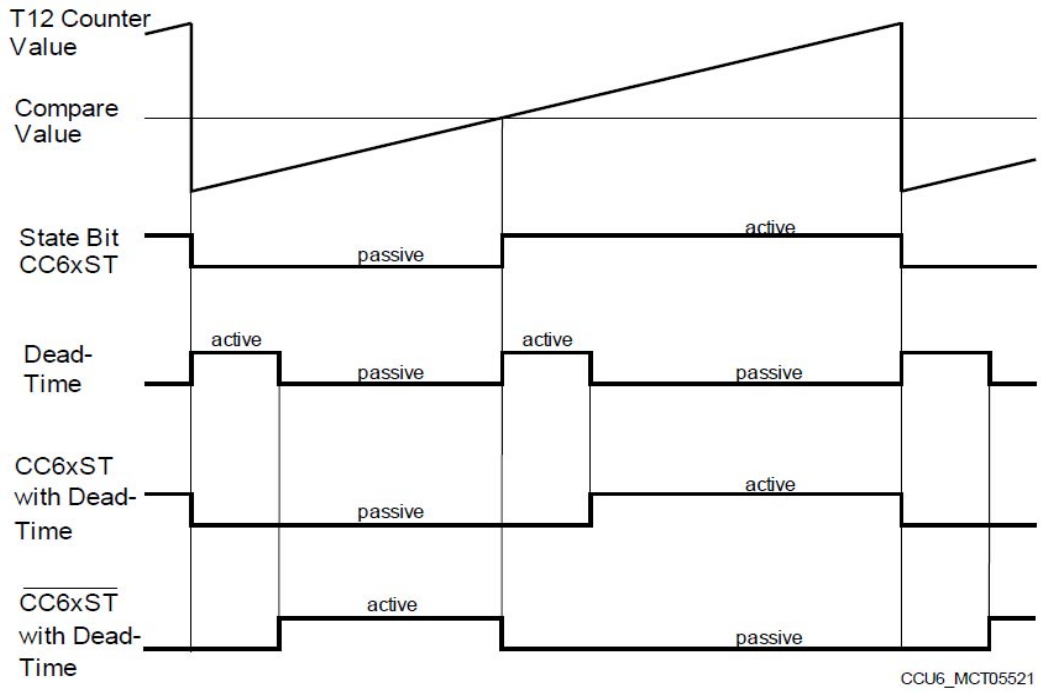

Figure 4 Dead-Time Generation Waveforms

To generate a delay between the complementary signals, the **CCU6** contains a Dead-Time generation block.

The state selection is based on the signals **CC6xST** and **CC6xST**, which are delivered by the dead-time generator (see Figure 4). Both signals are never active at the same time, but can be passive at the same time. This happens during the dead-time of each compare channel after a change of the corresponding state bit **CC6xST**.

The last block of the data path is the output modulation block. Here, all the modulation sources and the trap functionality are combined and control the actual level of the output pins. The configuration of this block is explained in the example codes and related to the application.

1.2 Low Side Switch Module Configuration (LS1/2)

The general purpose low-side switch is optimized to control an on-board relay. In this application example it will be used as an inverter-stage for MOSFET drive. The low-side switches provide embedded protection functions including overcurrent and overtemperature detection. The module is designed for on-board connection.

The low-side switches can be operated in PWM mode. To enable the PWM mode of the low-side switch, the corresponding bits **LSx_PWM** and **LSx_ON** in the control register **LSx_CTRL** have to be set.

The implemented combinatorial logic is shown in Figure 5.

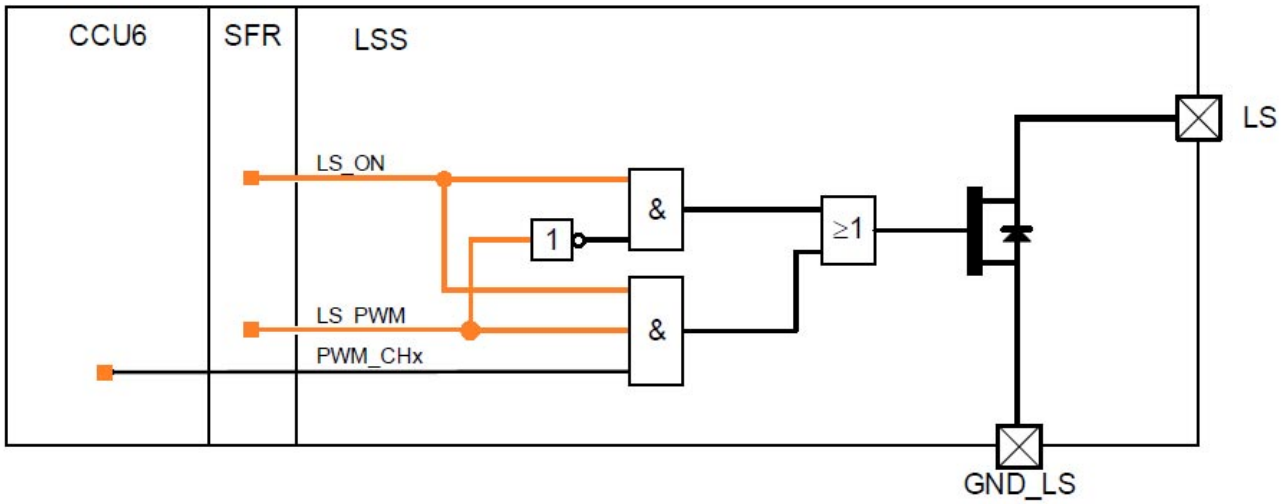

Figure 5 PWM usage of low side switch module

PWM_CHx can be configured to a **CCU6**-channel. This functionality is used for MOSFET-drive.

1.3 High Side Switch Module Configuration (HS1/2)

The high-side switch is optimized for driving resistive loads. Only small line inductance are allowed. Typical applications are single or multiple LEDs of a dashboard, switch illumination or other loads that require a high-side switch.

The PWM mode can also be enabled by a **HSx_CTRL - SFR** bit. The PWM configuration has to be done in the corresponding PWM module. All protection functions are also available in this mode. The maximum PWM frequency should not exceed 25 kHz (disabled slew rate control only). In PWM mode the high side switches have to be enabled first by the corresponding bits in the **HSx_CTRL** register.

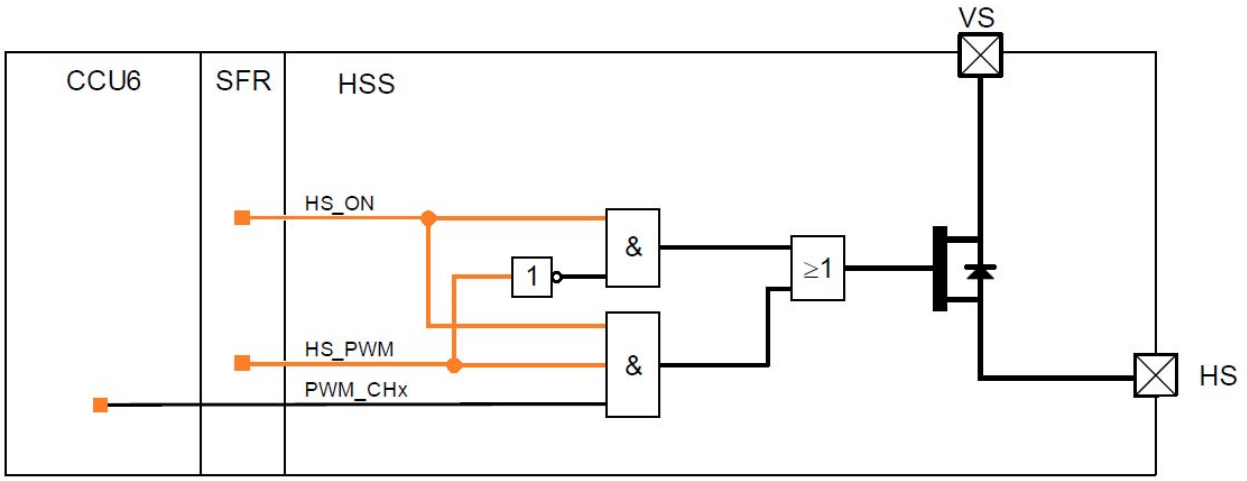

Figure 6 PWM usage of high side switch

To avoid any output glitches on the HSx outputs, the **HSx_PWM** bit should be set before the corresponding PWM unit is enabled (In this case Timer T12).

Note: For frequencies higher than 10 kHz, the slew rate setting has to be set to 30V/µs. Otherwise the internal power dissipation of the switch might damages the device.

In PWM mode all protection functions are available.

1.4 Single MOSFET Drive Code Examples

All Code Examples are implemented for the TLE9845QX_EVB_Rev1.4

Note: This code examples are only for single MOSFET drive. For PN-halfbridge CODE example see Chapter 2.2.

1.4.1 CCU6 configuration

In this code example the CCU6 is configured to generate two complementary 20kHz PWM Signals. The Dead-Time generator is used to set a 1µs Delay between HSx and LSx.

```
/* CCU6 configuration ********************************************************/
  CCU6->TCTR0.bit.CTM   = 0;          /* Edge-Aligned Mode                     */
  CCU6->T12PR.reg       = 2000;       /* 20kHz                                 */
  CCU6->T12DTC.bit.DTM  = 40;         /* Dead-Time = 1µs                       */
  CCU6->T12DTC.bit.DTE0 = 1;          /* Dead-Time Enable for channel 0        */
  CCU6->CC60SR.reg      = 1000;       /* Compare Value for 50% Dutycycle       */
  CCU6->T12MSEL.bit.MSEL60   = 3;     /* Compare output on pins COUT6n and CC6n. */
  CCU6->CMPSTAT.bit.CC60PS   = 0;     /* Passive State before Compare          */
  CCU6->CMPSTAT.bit.COUT60PS = 1;     /* Passive State after Compare           */
  CCU6->MODCTR.bit.T12MODEN |= 3;     /* Modulation enable for CC60 and COUT60 */
  CCU6->TCTR4.bit.T12STR = 1;         /* Shadow Transfer Request               */
```

After CCU6 is configured, the integrated low side and high side switches have to be set to PWM mode to drive the connected MOSFET.

In Chapter 1.4.2 LS2 and HS2 are configured to drive a N-channel MOSFET.

In Chapter 1.4.3 LS1 and HS1 are configured to drive a P-channel MOSFET.

For both cases, the CCU6 configuration form Chapter 1.4.1 is needed.

1.4.2 N-Channel MOSFET Drive

In this example HS2 and LS2 are configured to be used in PWM mode to drive a N-Channel MOSFET.

```
/* N-Channel MOSFET Inverter Initialisation **************************************/
  /*Low Side configuration                                                      */
  LS->CTRL.bit.LS2_EN  = 1;           /* LS2 Enable                            */
  LS->CTRL.bit.LS2_PWM = 1;           /* LS2 PWM Enable                        */
  LS->CTRL.bit.LS2_SRCTL_SEL    = 1; /* LS2 Fast Slew Rate selection           */
  LS->PWMSRCSEL.bit.LS2_SRC_SEL = 0; /* LS2 PWM Source Selection CC60          */
  /*High Side configuration                                                     */
  HS->CTRL.bit.HS2_EN  = 1;           /* HS2 Enable                            */
  HS->CTRL.bit.HS2_PWM = 1;           /* HS2 PWM Enable                        */
  HS->CTRL.bit.HS2_SRCTL_SEL    = 1; /* HS2 Fast Slew Rate selection 30V/µs     */
  HS->CTRL.bit.HS2_OC_SEL       = 3; /* HS2 Overcurrent Threshold set to 150mA  */
  HS->PWMSRCSEL.bit.HS2_SRC_SEL = 3; /* HS2 PWM Source Selection COUT60         */
```

After configuration is finished, Timer T12 can be startet:

```
 CCU6->TCTR4.bit.T12RS   = 1;     /* Run T12                                  */
```

1.4.3 P-Channel MOSFET Drive

In this example HS1 and LS1 are configured to be used in PWM mode to drive a P-Channel MOSFET

```
/* P-Channel MOSFET Inverter Initialisation ***********************************/
  /*Low Side configuration                                                     */
  LS->CTRL.bit.LS1_EN  = 1;          /* LS2 Enable                            */
  LS->CTRL.bit.LS1_PWM = 1;          /* LS2 PWM Enable                        */
  LS->CTRL.bit.LS1_SRCTL_SEL    = 1; /* LS2 Fast Slew Rate selection          */
  LS->PWMSRCSEL.bit.LS1_SRC_SEL = 0; /* LS2 PWM Source Selection CC60         */
  /*High Side configuration                                                    */
  HS->CTRL.bit.HS1_EN  = 1;          /* HS2 Enable                            */
  HS->CTRL.bit.HS1_PWM = 1;          /* HS2 PWM Enable                        */
  HS->CTRL.bit.HS1_SRCTL_SEL    = 1; /* HS2 Fast Slew Rate selection 30V/µs   */
  HS->CTRL.bit.HS1_OC_SEL       = 3; /* HS2 Overcurrent Threshold set to 150mA*/
  HS->PWMSRCSEL.bit.HS1_SRC_SEL = 3; /* HS2 PWM Source Selection COUT60       */
```

After configuration is finished, Timer T12 can be startet with:

```
 CCU6->TCTR4.bit.T12RS   = 1;       /* Run T12                                */
```

2 PN-MOSFET Drive

To drive a P-Channel MOSFET and a N-Channel MOSFET in a P/N-halfbridge configuration, all integrated HS and LS switches have to be used in PWM configuration. Chapter 2.1 describes the waveforms, generated by the CCU6, the applied Gate-voltages and the PN-Halfbridge phase node voltage.

2.1 PN-Halfbridge Switching behavoir

In PN-halfbridge mode, both MOSFETs are driven by the integrated HS- and LS-switches (see Figure 1).

To simplify deadtime behavior, the integrated HS-LS-pairs are switched without deadtime. They are protected against cross current conduction with gate pre-resistors. The Dead Time generator is used to realise the deadtime between the N-channel and P-channel MOSFET (waveforms see Figure 7)

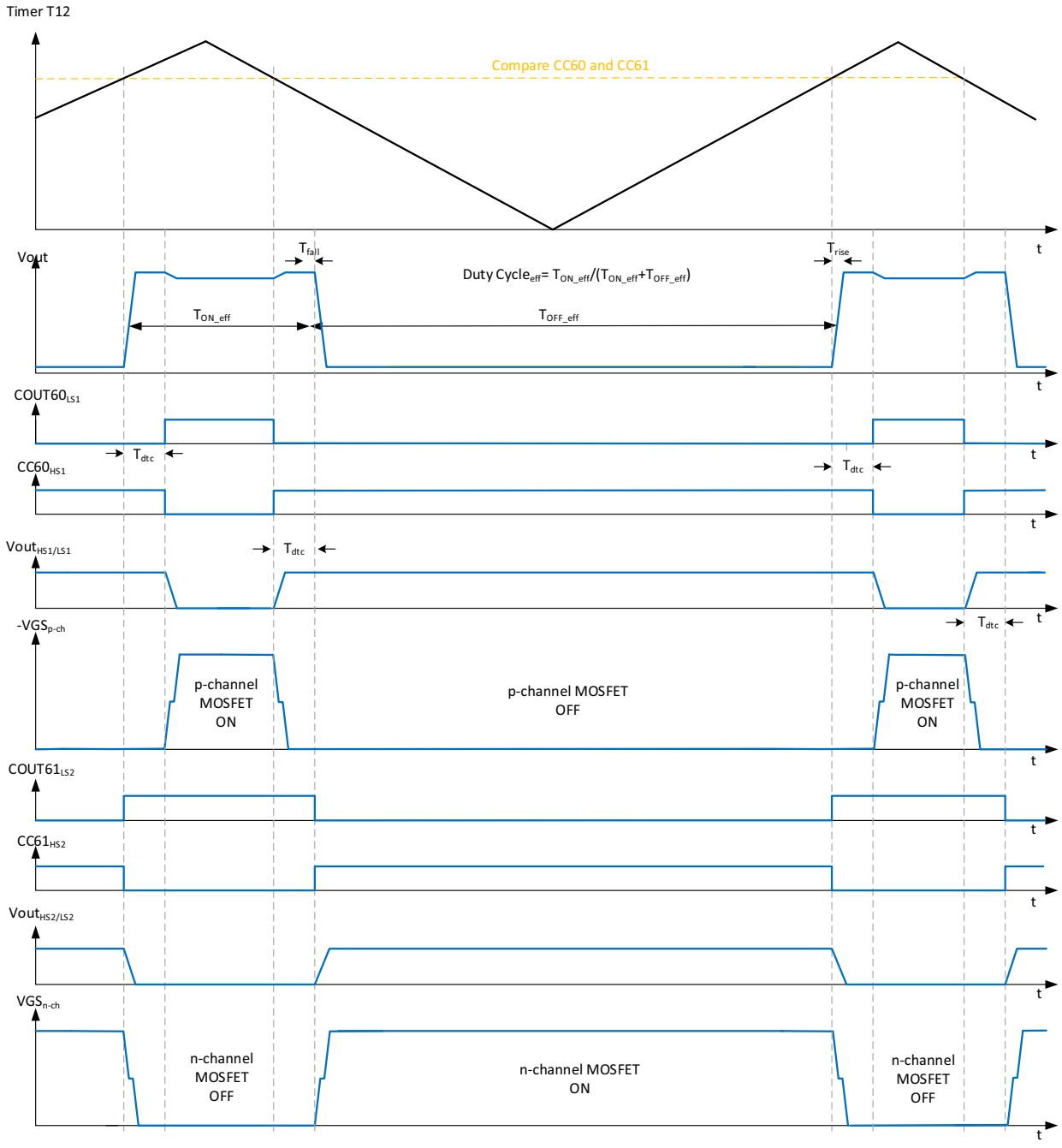

Figure 7 PN-Halfbridge Waveforms with CCU6 signals

The code implementation in Chapter 2.2 is based on the waveforms in Figure 7. In this example the difference is related to the deadtime. For a halfbridge configuration a deadtime generation between P-channel high side MOSFET and N-channel low side MOSFET is realised via CCU6 deadtime generator. For this operation mode two channels of the CCU6 Timer T12 are used with the same compare value, but complementary passive states. Timer T12 is running in Center-Aligned mode.

Note: Figure 7 is an example implementation and has to be verified in the application. It is recommended to use TLE9845QX_EVB_Rev1.4 or newer to evaluate this waveforms.

2.2 PN-MOSFET Drive CODE Example

In this chapter P-channel MOSFET and N-channel MOSFET are configured to switch alternating. The implementation is based on Figure 7. CCU6 is used to generate the needed PWM-pattern. Channel 0 of timer T12 drives the P-channel MOSFET (CC60/HS1, COUT60/LS1). Channel 1 of timer T12 drives the N-channel MOSFET(CC61/HS2, COUT61/LS2).

2.2.1 CCU6 Configuration for PN-Halfbridge

```
/* CCU6 configuration ***********************************************************/
  CCU6->TCTR0.bit.CTM   = 1;          /* Center-Aligned Mode                      */
  CCU6->T12PR.reg       = 1000;       /* 20kHz                                    */
  CCU6->T12DTC.bit.DTM  = 40;         /* Dead-Time = 1µs                          */
  CCU6->T12DTC.bit.DTE0 = 1;          /* Dead-Time Enable for channel 0           */
  CCU6->T12DTC.bit.DTE1 = 1;          /* Dead-Time Enable for channel 1           */
  CCU6->CC60SR.reg      = 500;        /* Compare Value for 50% Dutycycle          */
  CCU6->CC61SR.reg      = 500;        /* Compare Value for 50% Dutycycle          */
  CCU6->T12MSEL.bit.MSEL60   = 3;     /* Compare output on pins COUT60 and CC60. */
  CCU6->T12MSEL.bit.MSEL61   = 3;     /* Compare output on pins COUT61 and CC61. */
  CCU6->MODCTR.bit.T12MODEN |= 3;     /* Modulation enable for CC60 and COUT60    */
  CCU6->MODCTR.bit.T12MODEN |= 0xC;   /* Modulation enable for CC61 and COUT61    */

  /* PS before/after CMP:  CC60     CC61     COUT60   COUT61                     */
  CCU6->CMPSTAT.reg     = (0<<8) | (1<<10) | (0<<9) | (1<<11);
  /* passive level setup: COUT61    CC61     COUT60    CC60                      */
  CCU6->PSLR.bit.PSL    = (1<<3) | (0<<2)  | (0<<1) | (1<<0);

  CCU6->TCTR4.bit.T12STR     = 1;     /* Shadow Transfer Request                  */
```

2.2.2 HS1/2 and LS1/2 Configuration

The CODE example is splitted in P- and N-channel inverter initialisation

```
/* P-Channel MOSFET Inverter Initialisation *************************************/
  /* Low Side configuration                                                     */
  LS->CTRL.bit.LS1_EN           = 1; /* LS1 Enable                            */
  LS->CTRL.bit.LS1_PWM          = 1; /* LS1 PWM Enable                        */
  LS->CTRL.bit.LS1_SRCTL_SEL    = 1; /* LS1 Fast Slew Rate selection          */
  LS->PWMSRCSEL.bit.LS1_SRC_SEL = 3; /* LS1 PWM Source Selection COUT60       */
  /* High Side configuration                                                    */
  HS->CTRL.bit.HS1_EN           = 1; /* HS1 Enable                            */
  HS->CTRL.bit.HS1_PWM          = 1; /* HS1 PWM Enable                        */
  HS->CTRL.bit.HS1_SRCTL_SEL    = 1; /* HS1 Fast Slew Rate selection 30V/µs   */
  HS->CTRL.bit.HS1_OC_SEL       = 3; /* HS1 Overcurrent Threshold set to 150mA */
```

```
  HS->PWMSRCSEL.bit.HS1_SRC_SEL = 0; /* HS1 PWM Source Selection CC60           */
/* N-Channel MOSFET Inverter Initialisation ***********************************/
  /* Low Side configuration                                                    */
  LS->CTRL.bit.LS2_EN  = 1;          /* LS2 Enable                           */
  LS->CTRL.bit.LS2_PWM          = 1; /* LS2 PWM Enable                       */
  LS->CTRL.bit.LS2_SRCTL_SEL    = 1; /* LS2 Fast Slew Rate selection         */
  LS->PWMSRCSEL.bit.LS2_SRC_SEL = 4; /* LS2 PWM Source Selection COUT61      */
  /* High Side configuration                                                   */
  HS->CTRL.bit.HS2_EN  = 1;          /* HS2 Enable                           */
  HS->CTRL.bit.HS2_PWM = 1;          /* HS2 PWM Enable                       */
  HS->CTRL.bit.HS2_SRCTL_SEL    = 1; /* HS2 Fast Slew Rate selection 30V/µs  */
  HS->CTRL.bit.HS2_OC_SEL       = 3; /* HS2 Overcurrent Threshold set to 150mA */
  HS->PWMSRCSEL.bit.HS2_SRC_SEL = 1; /* HS2 PWM Source Selection CC61        */
```

2.2.3 Start Timer T12

After CCU6, LS1/2 and HS1/2 are configured the Timer T12 can be started

```
/* RUN TIMER T12 **************************************************************/
  CCU6->TCTR4.bit.T12RS   = 1;       /* Run T12                               */
```

2.2.4 Dutycycle configuration

Due to the simplification of the deadtime generator, the shadow registers for channel 0 and 1 contain the same value. After updating the shadow register, a shadow transfer request has to be performed.

```
/* SET_DUTYCYCLE **************************************************************/
void set_Dutycycle(uint16_t dc)
{
  CCU6->CC60SR.reg = dc;      /* Compare Value Channel 0                       */
  CCU6->CC61SR.reg = dc;      /* Compare Value Channel 1                       */
  CCU6->TCTR4.bit.T12STR = 1; /* Shadow Transfer Request                       */
}
```

Note: This is a simplified function and has to be verified in application. There is no exception handling for the range of “dc”. In this example, “dc” has to be between the value “1” and the period value in register CCU6_T12PR.

3 Differential Measurement Unit for V_{DS}-Monitoring

This chapter shows, how to configure the needed modules to realise a MOSFET protection. The CCU6 will switch off the MOSFETs in shortcircuit condition automatically without any CPU load.

The integrated Differential Unit can be used to realise a drain-source-monitoring function for a P/N halfbridge application. The MON pins have to be connected to the halfbridge as shown in Figure 8. ADC1 is used in sequencer mode to sample the signals at the monitor pins. Highside and lowside MOSFET have to be measured alternately. Therefore the enable signals have to be aligned to the CCU6-PWM pattern (see Figure 9).

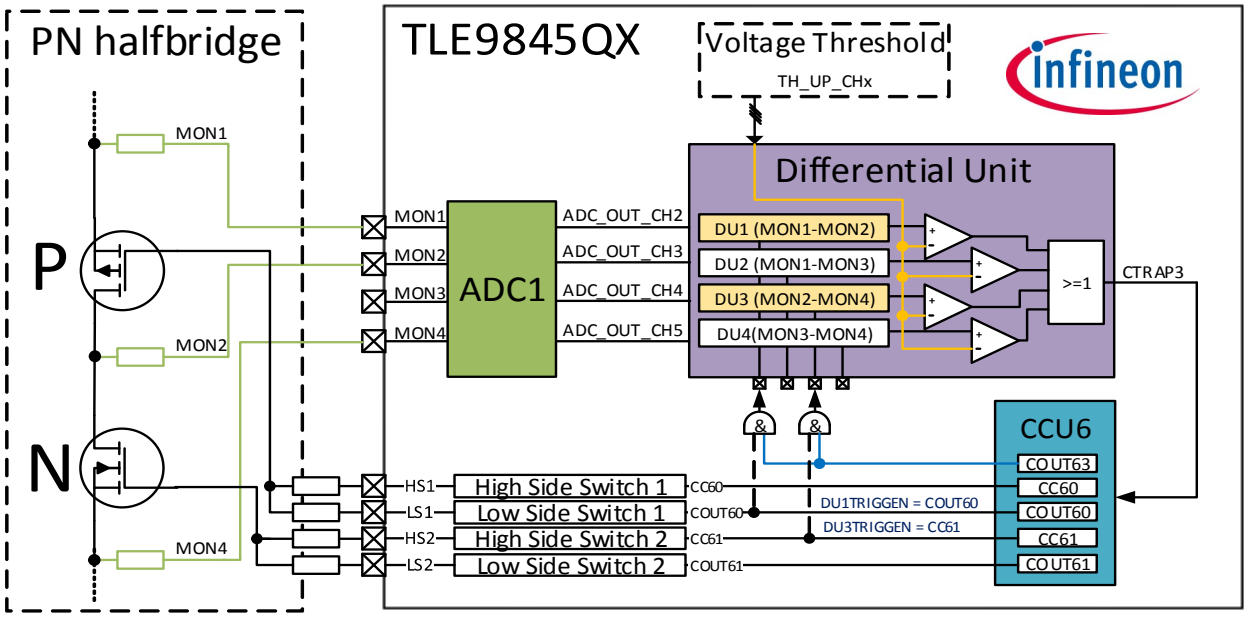

Figure 8 Drain-Source monitor concept with Differential Measurement Unit

The functional structure of the protection functionality is shown in Figure 8. To realize the protection, ADC1, the Differential Unit and the CCU6 have to be configured. ADC1 samples the monitor signals in sequencer mode during halfbridge operation. CCU6 generates the PWM signals for the halfbridge, which are also used to generate the Differential Unit trigger signal. To blank out the MOSFETs switching slope, timer T13 is used as a blank time generator. Caused by CCU6 signals COUT60 and CC61, the Differential Units 1 and 3 are hardware enabled. This causes an alternating enable signal for DU1 and DU3. These signals are compared with an upper threshold value, that can be configured. In case of exceeding the threshold, CTRAP3 signal is generated to switch the CCU6 to passive state. This causes a halfbridge shutdown to protect the MOSFETs.

3.1 Blank Time Generation with Timer T13

The drain-source voltage is measured during the low ohmic ON-Phase of the MOSFETs. The timer T12 channels enable the differential units directly. Timer T13 is used as a blank time generator, to disable the differential units during the MOSFET switching slope. Figure 8 shows the integrated AND gates. They provides the blank functionality with signal COUT63 for the differential unit enable signal DUxTRIGGEN. The trigger for timer T13 is generated via T12 channel capture compare signals COUT60 and CC61 (see Figure 9). Every enable signal for the differential units (DUxTRIGGEN, x = 1, 2, 3, 4) is AND gated with output signal COUT63 of timer T13.

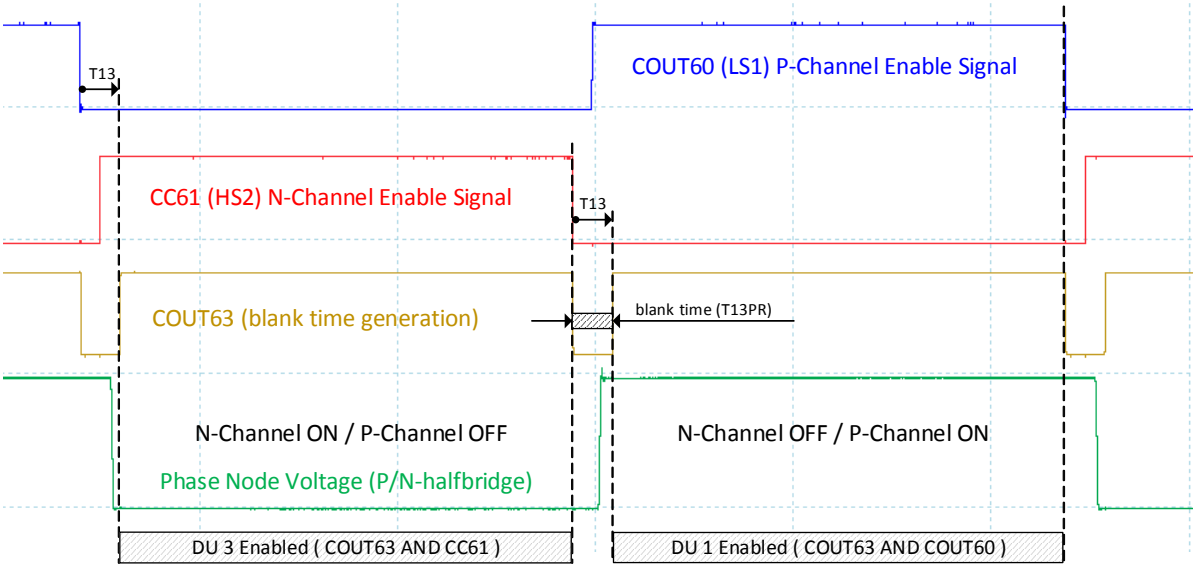

Figure 9 Differential Unit enable signals from CCU6

3.2 ADC1 Configuration

ADC1 operates in sequencer mode. It samples the sensed drain and source voltages ate the MON pins (MON1, MON2, MON4) as fast as possible. The single ended measured values are written in the ADC1_FILT_OUTx (x = 2 ,3 ,5) registers. These registers are directly used for the differential units. In the CODE example, the adc filters are deactivated and the sample time is set to the minimum value.

3.3 Differential Unit Measurement

The differential measurement unit is a sub-unit of the digital postprocessing. It calculates the difference between selectable monitoring channels. The data processing unit also offers a differential evaluation of the monitoring channels. This offers the possibility to build up a V_{DS} monitoring for P/N-halfbridge control.

3.4 CTRAP3 behavior of CCU6

The CTRAP functionality is a fast emergency stop without CPU load. In this case, the trigger signal is generated from the differential units (**CTRAP3**). The trap functionality permits the PWM outputs of CCU6 to react on the state of the input signal. This functionality can be used to switch off the power devices if the trap input becomes active (e.g. to perform an emergency stop). The trap handling and the effect on the output modulation are controlled by the bits in the trap control register **CCU6_TRPCTR**. When a trap condition is detected (**CTRAP** = 0) and the input is enabled (**TRPPEN** = 1), both, the trap flag **TRPF** and the trap state bit **TRPS**, are set to 1 (trap state active). The output of the trap state bit TRPS leads to the output modulation blocks (for T12 and for T13) and can there deactivate the outputs (set to passive state). In this case the CTRAP3 signal is generated. Figure 8 qualitatively shows the combinatorical logic for CTRAP3 generation.

3.5 V_{DS}-Monitoring CODE Example

The CODE example explains how to configure the required modules to realise a drain-source-monitoring and protection function. To generate the PWM-Signals, the CODE example from Chapter 2 is necessary. It is recommended to use TLE9845_EVB_Rev1.4 or newer to evaluate this implementation.

Note: This is an example implementation and has to be verified in the application. The drain-source protection function is exclusive for TLE9845QX.

3.5.1 T13 configuration (DU enable and blank time)

```
/* T13 used for blank time generation ****************************************/
  CCU6->T13PR.reg            = 80;  /* T13 Period used for blank time 2µs       */
  CCU6->TCTR2.bit.T13SSC     = 1;   /* SingleShot Control                       */
  CCU6->TCTR2.bit.T13TEC     = 4;   /* Trigger Event Control: Channel 0,1,2     */
  CCU6->TCTR2.bit.T13TED     = 3;   /* Trigger Event Direction: UP/DOWN         */
  CCU6->CMPSTAT.bit.COUT63PS = 0;   /* Passive State before Compare             */
  CCU6->CMPSTAT.bit.T13IM    = 1;   /* COUT63 Inverted Modulation               */
  CCU6->PSLR.bit.PSL63       = 1;   /* Passive State High                       */
  CCU6->MODCTR.bit.ECT13O    = 1;   /* Enable Compare T13 Output COUT63         */
  CCU6->TCTR4.bit.T13STR     = 1;   /* Shadow Transfer Request                  */
```

3.5.2 ADC1 configuration (sequencer initialisation)

```
/* ADC1 initialisation *******************************************************/
  ADC1->CTRL3.bit.MCM_PD_N = 1;     /* Measurement Core Module Enable           */
  ADC1->CTRL_STS.bit.PD_N  = 1;     /* ACTIVE ADC1 is switched on               */
  ADC1->CTRL3.bit.SW_MODE  = 0;     /* Enable Sequencer Mode                    */
  ADC1->SQ0_1.bit.SQ0      = 0x2C;  /* Sequence 0 Setup:  MON1, MON2, MON4      */
  ADC1->SQ0_1.bit.SQ1      = 0x2C;  /* Sequence 1 Setup:  MON1, MON2, MON4      */
  ADC1->SQ2_3.bit.SQ2      = 0x2C;  /* Sequence 2 Setup:  MON1, MON2, MON4      */
  ADC1->SQ2_3.bit.SQ3      = 0x2C;  /* Sequence 3 Setup:  MON1, MON2, MON4      */
  ADC1->FILT_UP_CTRL.reg   = 0x00;  /* filter disable                           */
  ADC1->FILT_LO_CTRL.reg   = 0x00;  /* filter disable                           */
  ADC1->CTRL3.bit.SAMPLE_TIME_HVCH = 0; /* minimum sample time                  */
  ADC1->CTRL3.bit.SAMPLE_TIME_LVCH = 0; /* minimum sample time                  */
```

3.5.3 Differential Unit configuration (CCU6 trigger adjustments)

```
/* Differential Unit initialisation ******************************************/
  /* DU1 = MON1 - MON2                                                        */
  SCU->MODPISEL4.bit.DU1TRIGGEN    = 0x03;  /* selection  for COUT60           */
  ADC1->DCHTH1_4_UPPER.bit.DCH1_UP = 8;     /* 8 * 30mV = 240mV                */
  ADC1->MMODE0_11.bit.MMODE_D1     = 0x02;  /* overvoltage/-limit measurement  */
  ADC1->DUIN_SEL.bit.DU1_EN        = 1;     /* DCH1 Enable                     */
  /* DU3 = MON2 - MON4                                                        */
  SCU->MODPISEL4.bit.DU3TRIGGEN    = 0x01;  /* selection for CC61              */
  ADC1->DCHTH1_4_UPPER.bit.DCH3_UP = 8;     /* 8 * 30mV = 240mV                */
  ADC1->MMODE0_11.bit.MMODE_D3     = 0x02;  /* overvoltage/-limit measurement  */
  ADC1->DUIN_SEL.bit.DU3_EN        = 1;     /* DCH3 Enable                     */
```

3.5.4 CTRAP configuration (CCU6 disable feature)

```
/* CTRAP3 function enable ****************************************************/
  CCU6->PISEL0.bit.ISTRP  = 0x03;  /* CTRAP_3 The input pin for CTRAP_3.       */
  CCU6->TRPCTR.bit.TRPEN  = (0xF); /* Bits Enabled (CC60, COUT60, CC61, COUT61) */
  CCU6->TRPCTR.bit.TRPM2  = 0x1;   /* Software Reset                           */
  CCU6->TRPCTR.bit.TRPPEN = 0x1;   /* Trap Pin Enable                          */
  CCU6->ISR.bit.RTRPF = 1;         /* Reset Trap Flag before Start T12         */
```

4 Revision History

Revision	Date	Changes
1.0	2016-06-15	Release state

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